HARRIS SEMICONDUCTOR

IRFP360, IRFP362

20A and 23A, 400V, 0.2 and 0.25 Ohm, N-Channel Power MOSFETs

January 1998

Features

- 20A and 23A, 400V
- $r_{DS(ON)}$ = 0.2Ω and 0.25Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFP360	TO-247	IRFP360
IRFP362	TO-247	IRFP362

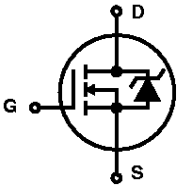
NOTE: When ordering, use the entire part number.

Description

These are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. They can be operated directly from integrated circuits.

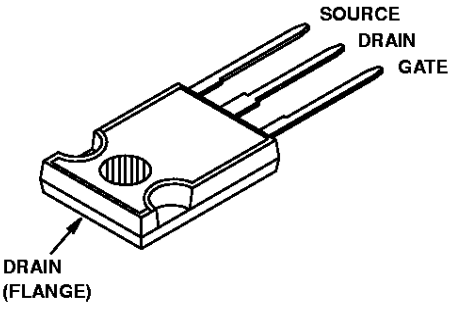
Formerly developmental type TA17464.

Symbol



Packaging

JEDEC STYLE TO-247



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2290.2**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		IRFP360	IRFP362	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	400	400	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	400	400	V
Continuous Drain Current	I_D	23	20	A
$T_C = 100^oC$	I_D	14	13	A
Pulsed Drain Current (Note 3)	I_{DM}	92	80	A
Gate to Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation	P_D	250	250	W
Linear Derating Factor		2	2	W/^{o}C
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	1200	1200	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	^{o}C
Maximum Temperature for Soldering				
Leads at 0.063in (1.6mm) from case for 10s	T_L	300	300	300
Package Body for 10s, see Techbrief 334	T_{pkg}	260	260	260

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

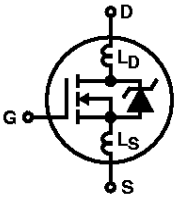
NOTE:

1. $T_J = 25^oC$ to 125^oC.

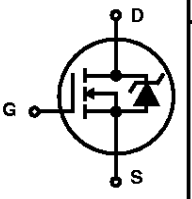
Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V, (Figure 10)	400	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$	-	-	250	μA
On-State Drain Current (Note 2) IRFP360	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V	23	-	-	A
IRFP362			20	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
On Resistance (Note 2) IRFP360	$r_{DS(ON)}$	I_D = 13A, V_{GS} = 10V, (Figures 8, 9)	-	0.18	0.20	Ω
IRFP362			-	0.20	0.25	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V$, $I_{DS} > 13A$, (Figure 12)	14	21	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, $I_D \approx 25A$, R_{GS} = 4.3Ω, V_{GS} = 10V, R_L = 7.5Ω, (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	22	33	ns
Rise Time	t_r		-	94	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	120	ns
Fall Time	t_f		-	66	99	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, I_D = 25A, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{G(REF)}$ = 1.5mA, (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	68	100	nC
Gate to Source Charge	Q_{gs}		-	17	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	24	-	nC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz, (Figure 11)		-	4000	-	pF
Output Capacitance	C_{OSS}			-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	97	-	pF
Internal Drain Inductance	L_D	Measured Between the Contact Screw on Header closer to Source and Gate Pins and Center of Die	Modified MOSFET Symbol Showing the Internal Device Inductances 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured From the Source Lead, 6mm (0.25in) from Header and Source Bonding Pad		-	13	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.50	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	30	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier		-	-	23	A
Pulse Source to Drain Current (Note 2)	I_{SDM}			-	-	92	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	T_J = 25°C, I_{SD} = 23A, V_{GS} = 0V, (Figure 13)		-	-	1.8	V
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_{SD} = 25A, dI_{SD}/dt = 100A/μs		200	460	1000	ns
Reverse Recovery Charge	Q_{RR}	T_J = 25°C, I_{SD} = 25A, dI_{SD}/dt = 100A/μs		3.1	7.1	16	μC

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. V_{DD} = 50V, starting T_J = 25°C, L = 4mH, R_G = 25Ω, Peak I_{AS} = 23A (Figures 15, 16).

Typical Performance Curves Unless Otherwise Specified

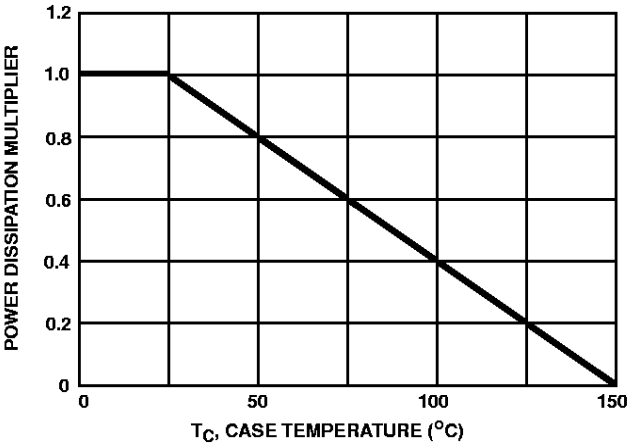


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

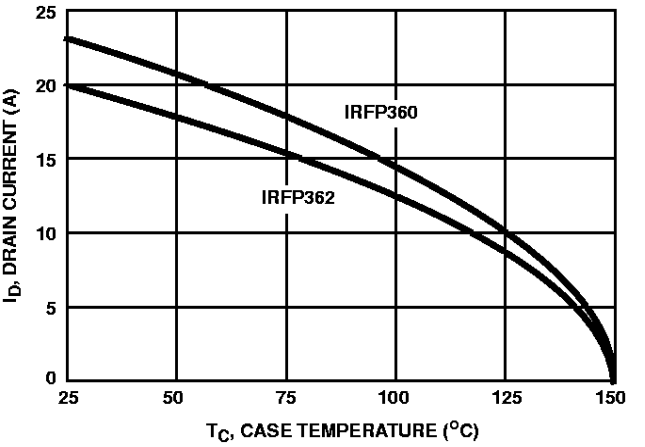


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

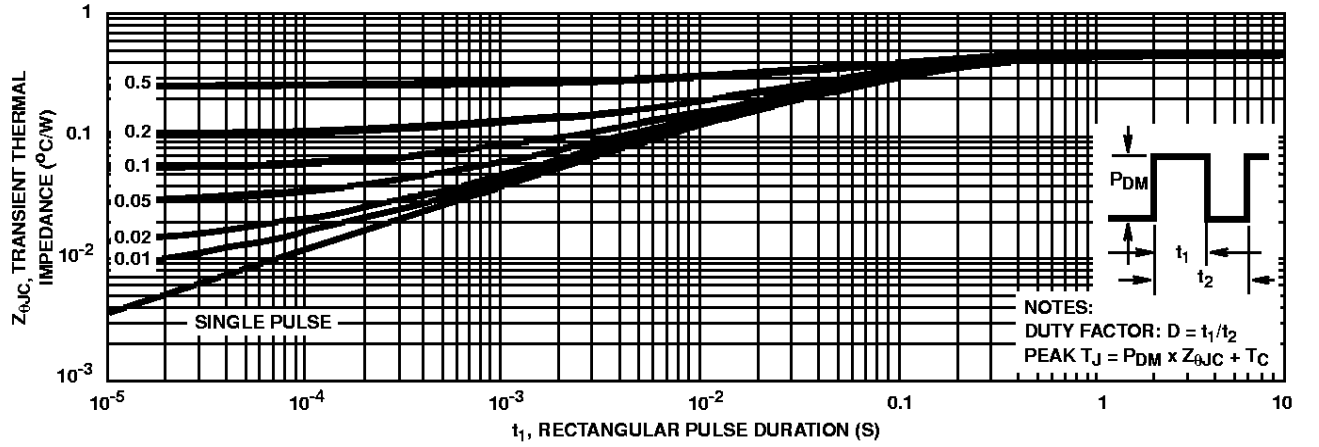


FIGURE 3. TRANSIENT THERMAL IMPEDANCE

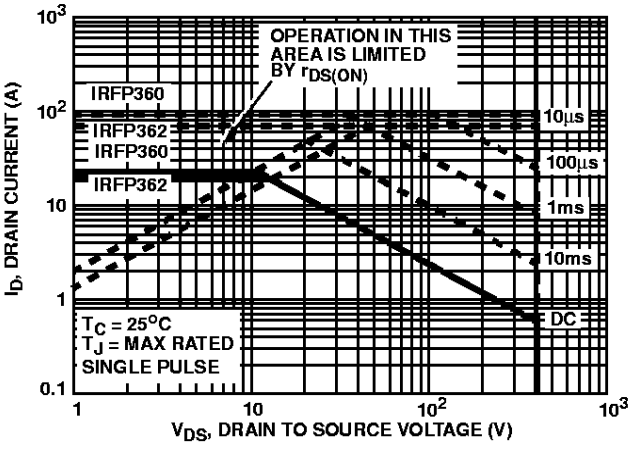


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

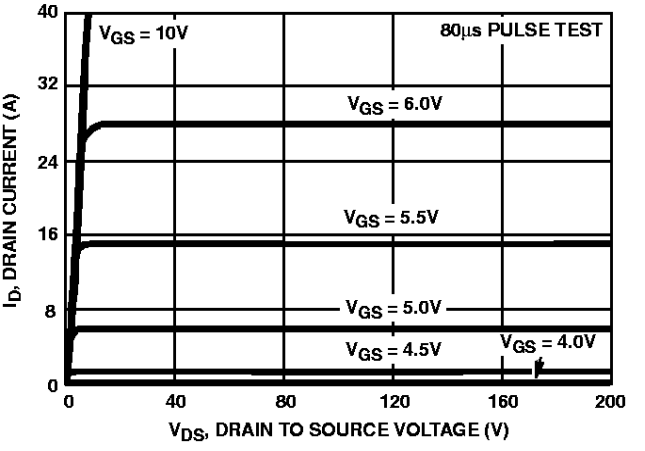


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

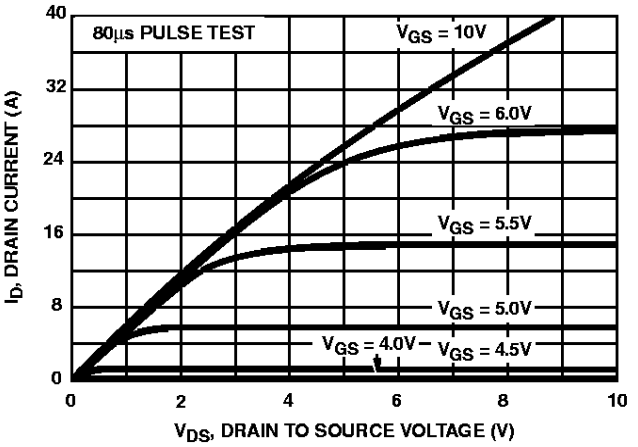


FIGURE 6. SATURATION CHARACTERISTICS

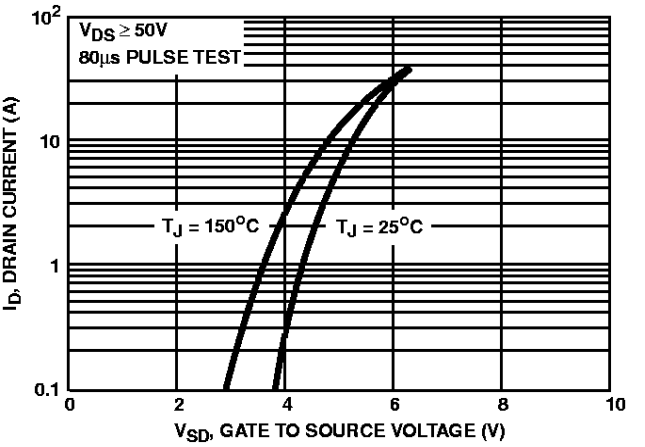


FIGURE 7. TRANSFER CHARACTERISTICS

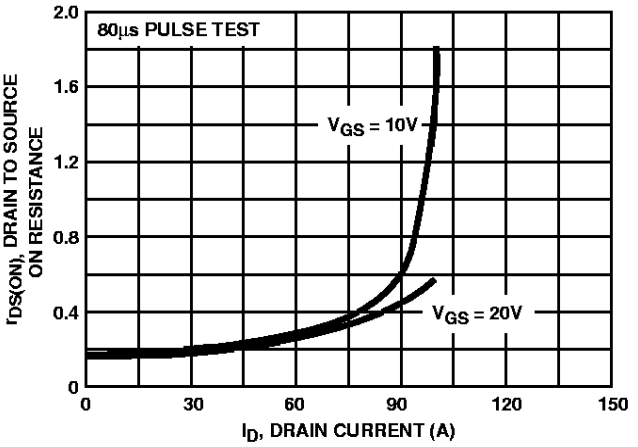


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

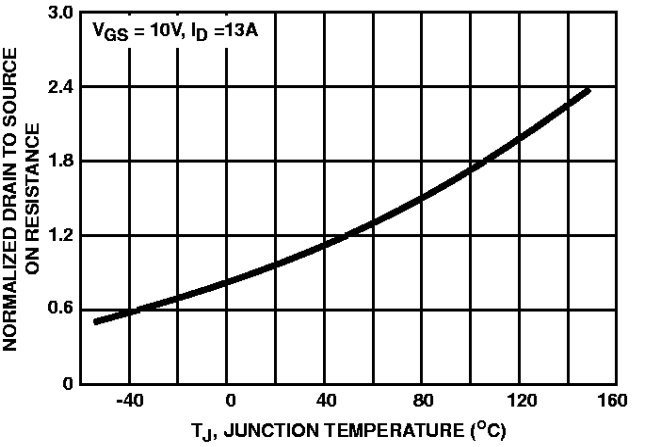


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

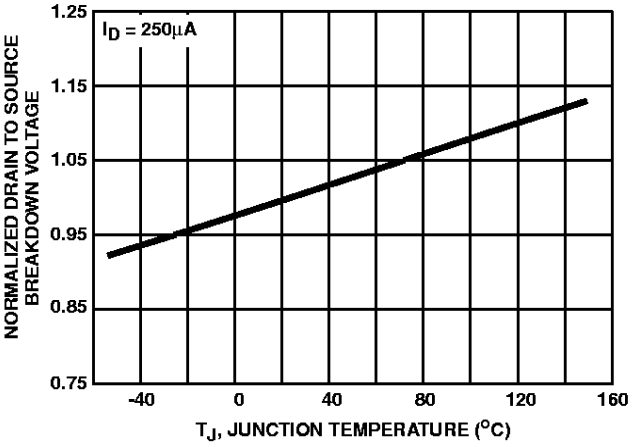


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

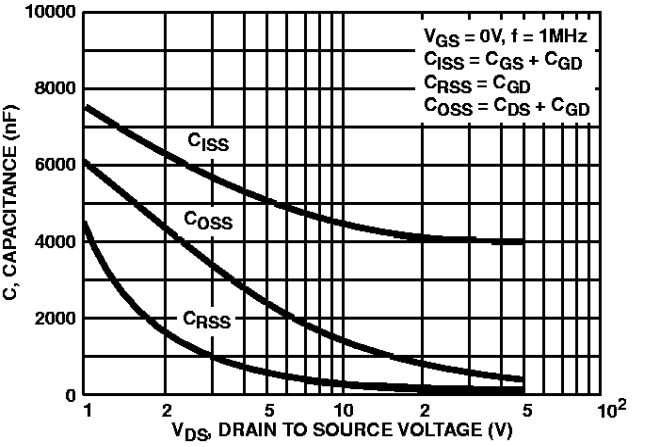


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

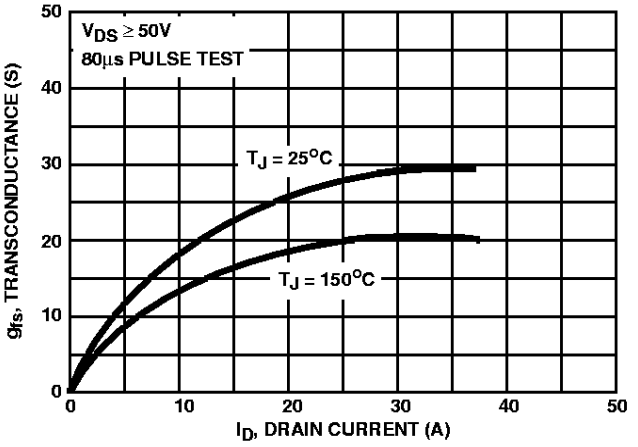


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

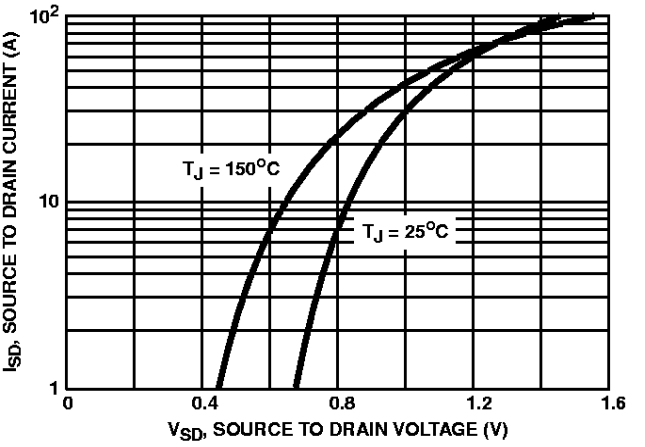


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

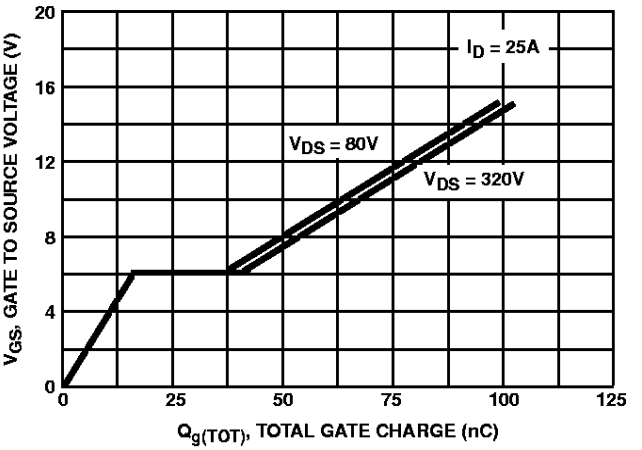


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

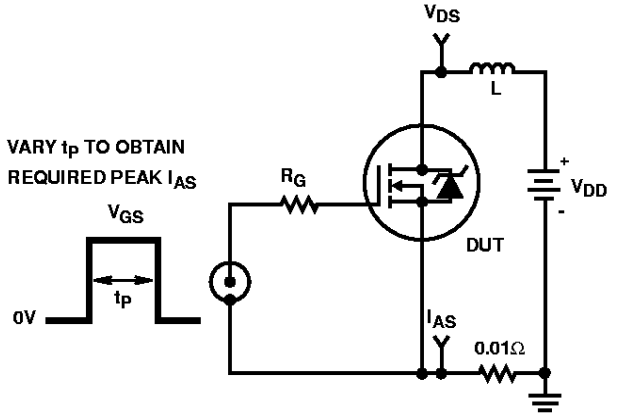


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

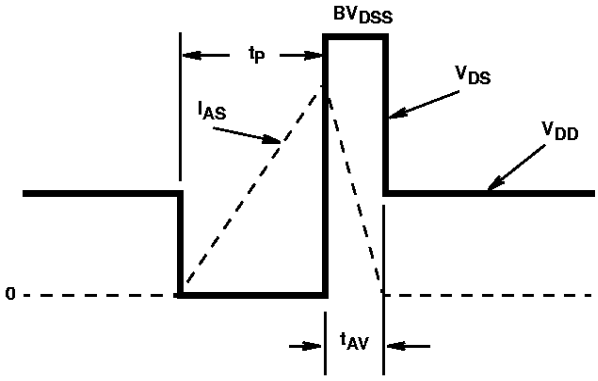


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

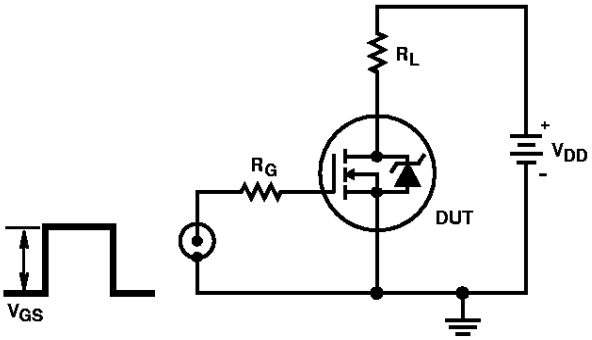


FIGURE 17. SWITCHING TIME TEST CIRCUIT

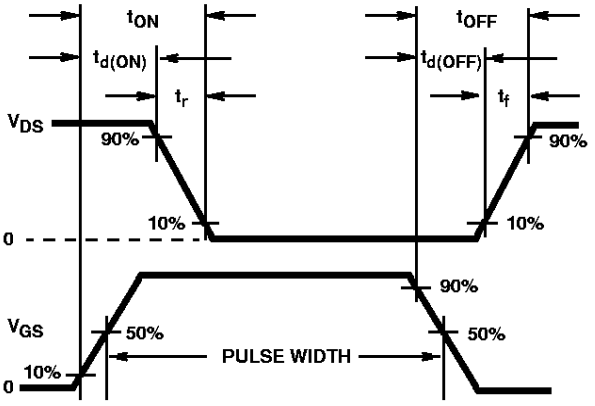


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

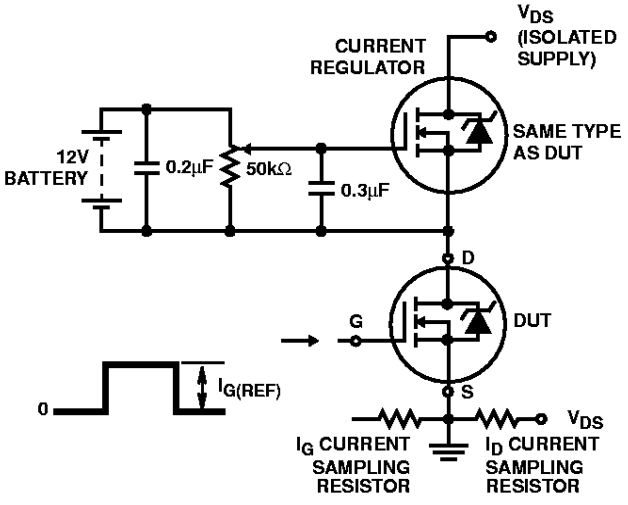


FIGURE 19. GATE CHARGE TEST CIRCUIT

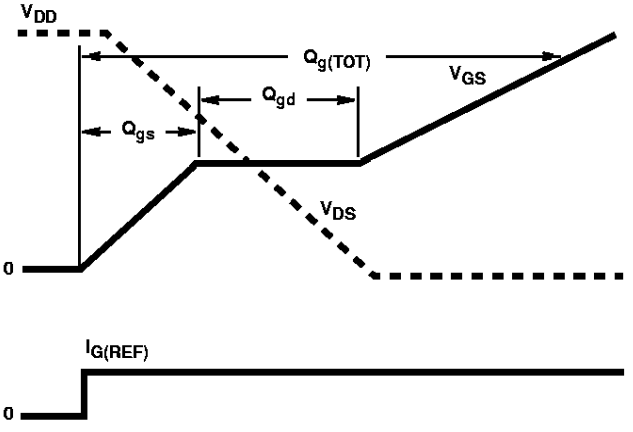


FIGURE 20. GATE CHARGE WAVEFORMS