CY90F922NC/F922NCS/922NCS
CY90F923NC/F923NCS/F924NC
CY90F924NCS/V920-101/102

F²MC-16LX CY90920 Series

The CY90920 series is a family of general-purpose Cypress 16-bit microcontrollers designed for applications such as vehicle instrument panel control.

The instruction set retains the AT architecture from the F²MC-8L and F²MC-16LX families, with further refinements including high-level language instructions, extended addressing modes, improved multiplication and division operations (signed), and bit processing. In addition, long word processing is made possible by the inclusion of a built-in 32-bit accumulator.

Features

■ Clock

Built-in PLL clock frequency multiplication circuit.
Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 8 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 32 MHz).
Operation by sub clock (up to 50 kHz: 100 kHz oscillation clock divided by two) is allowed.

■ 16-bit input capture (8 channels)

Detects rising, falling, or both edges.
16-bit capture register × 8
The value of a 16-bit free-run timer counter is latched upon detection of an edge input to pin and an interrupt request is generated.

■ 16-bit reload timer (4 channels)

16-bit reload timer operation (select toggle output or one-shot output)
Selectable event count function

■ Real time watch timer (main clock)

Operates directly from oscillator clock.
Interrupt can be generated by second/minute/hour/date counter overflow.

■ PPG timer (6 channels)

Output pins (3 channels), external trigger input pin (1 channel)
Operation clock frequencies: f_{CP}, $f_{CP}/2^2$, $f_{CP}/2^4$, $f_{CP}/2^6$

■ Delay interrupt

Generates interrupt for task switching.
Interrupts to CPU can be generated/cleared by software setting.

■ External interrupts (8 channels)

8-channel independent operation
Interrupt source setting available: “L” to “H” edge/ “H” to “L” edge/ “L” level/ “H” level.

■ 8/10-bit A/D converter (8 channels)

Conversion time: 3 μs (at f_{CP} = 32 MHz)
External trigger activation available (P50/INT0/ADTG)
Internal timer activation available (16-bit reload timer 1)

■ UART(LIN/SCI) (4 channels)

Equipped with full duplex double buffer
Clock-asynchronous or clock-synchronous serial transfer is available

■ CAN interface (4 channels: CAN0 and CAN2, and CAN1 and CAN3 share transmission and reception pins, and interrupt control registers).

Conforms to CAN specifications version 2.0 Part A and B.
Automatic resend in case of error.
Automatic transfer in response to remote frame.
16 prioritized message buffers for data and ID
Multiple message support
Flexible configuration for receive filter: Full bit compare/full bit mask/two partial bit masks
Supports up to 1 Mbps
CAN wakeup function (RX connected to INT0 internally)

■ LCD controller/driver (32 segment x 4 common)

Segment driver and command driver with direct LCD panel (display) drive capability

■ Reset on detection of low voltage/program loop

Automatic reset when low voltage is detected
Program looping detection function

■ Stepping motor controller (4 channels)

High current output for each channel × 4
Synchronized 8/10-bit PWM for each channel × 2

■ Sound generator (2 channels)

8-bit PWM signal mixed with tone frequency from 8-bit reload counter.
PWM frequencies: 125 kHz, 62.5 kHz, 31.2 kHz, 15.6 kHz (at f_{CP} = 32 MHz)
Tone frequencies: PWM frequency /2/ , divided by (reload frequency +1)

■ Input/output ports

General-purpose input/output port (CMOS output) 93 ports

■ Function for port input level selection

Automotive/CMOS-Schmitt

■ Flash memory security function

Protects the contents of Flash memory (Flash memory product only)

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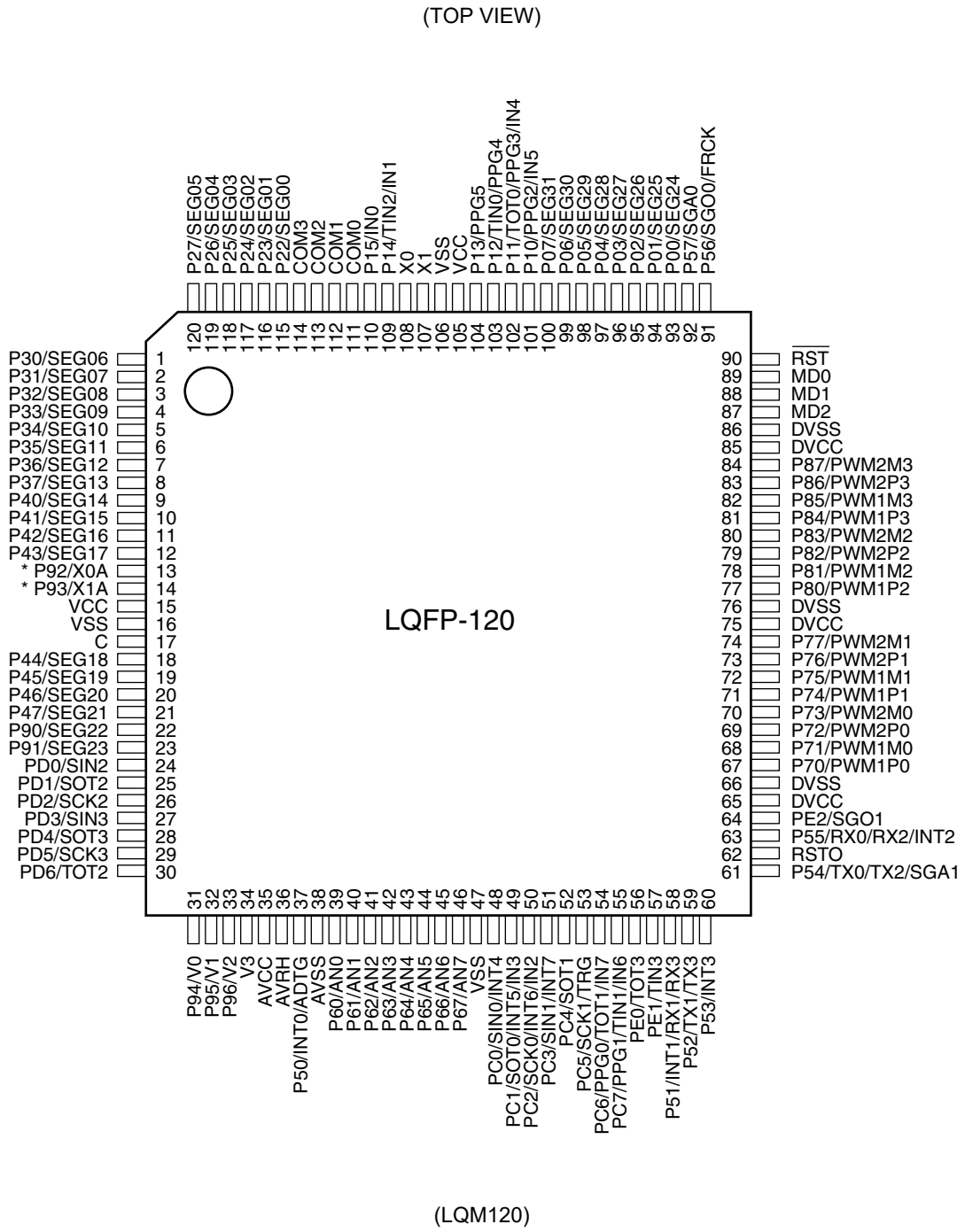
1. Product Lineup

Part number / Parameter	CY90 F922NC	CY90 F922NCS	CY90 F923NC	CY90 F923NCS	CY90 F924NC	CY90 F924NCS	CY90 922NCS	CY90 V920-101	CY90 V920-102
Type	Flash memory product						MASK ROM product	Evaluation product	
CPU	F^2MC-16LX CPU								
System clock	PLL clock multiplier circuit (× 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped) Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8)								
Sub clock pins (X0A, X1A)	Yes	No	Yes	No	Yes	No	No	No	Yes
ROM	Flash memory 256 Kbytes		Flash memory 384 Kbytes		Flash memory 512 Kbytes		256 Kbytes	External	
RAM	10 Kbytes		16 Kbytes		24 Kbytes		10 Kbytes	30 Kbytes	
I/O port	91 ports	93 ports	91 ports	93 ports	91 ports	93 ports	93 ports	93 ports	91 ports
LCD controller	32 segment × 4 common								
LIN-UART	UART (LIN/SCI) 4 channels								
CAN interface	4 channels								
16-bit input capture	8 channels								
16-bit reload timer	4 channels								
16-bit free-run timer	1 channel								
Real time watch timer	1 channel								
16-bit PPG timer	6 channels								
External interrupt	8 channels								
8/10-bit A/D converter	8 channels								
Low-voltage/CPU operating detection reset	Yes							No	
Stepping motor controller	4 channels								
Sound generator	2 channels								
Flash memory security	Yes						—		
Operating voltage	4.0 V to 5.5 V							4.5 V to 5.5 V	
Package	LQFP-120							PGA-299	

2. Pin Assignment



(LQM120)

*: CY90V920-101, CY90F922NCS,CY90F923NCS,CY90F924NCS,CY90922NCS: P92, P93
CY90V920-102, CY90F922NC,CY90F923NC,CY90F924NC: X0A, X1A

3. Pin Descriptions

Pin No.	Pin Name	I/O Circuit Type*1	Function
108	X0	A	High-speed oscillation input pin
107	X1		High-speed oscillation output pin
13	X0A	B	Low-speed oscillation input pin
	P92	I	General-purpose I/O port
14	X1A	B	Low-speed oscillation output pin
	P93	I	General-purpose I/O port
90	RST	C	Reset input pin
93	P00	F	General-purpose I/O port
	SEG24		LCD controller/driver segment output pin
94	P01	F	General-purpose I/O port
	SEG25		LCD controller/driver segment output pin
95	P02	F	General-purpose I/O port
	SEG26		LCD controller/driver segment output pin
96	P03	F	General-purpose I/O port
	SEG27		LCD controller/driver segment output pin
97	P04	F	General-purpose I/O port
	SEG28		LCD controller/driver segment output pin
98	P05	F	General-purpose I/O port
	SEG29		LCD controller/driver segment output pin
99	P06	F	General-purpose I/O port
	SEG30		LCD controller/driver segment output pin
100	P07	F	General-purpose I/O port
	SEG31		LCD controller/driver segment output pin
101	P10	I	General-purpose I/O port
	PPG2		16-bit PPG ch.2 output pin
	IN5		Input capture ch.5 trigger input pin
102	P11	I	General-purpose I/O port
	TOT0		16-bit reload timer ch.0 TOT output pin
	PPG3		16-bit PPG ch.3 output pin
	IN4		Input capture ch.4 trigger input pin
103	P12	I	General-purpose I/O port
	TIN0		16-bit reload timer ch.0 TIN input pin
	PPG4		16-bit PPG ch.4 output pin
104	P13	I	General-purpose I/O port
	PPG5		16-bit PPG ch.5 output pin
109	P14	I	General-purpose I/O port
	TIN2		16-bit reload timer ch.2 TIN input pin
	IN1		Input capture ch.1 trigger input pin

Pin No.	Pin Name	I/O Circuit Type*1	Function
110	P15	I	General-purpose I/O port
	IN0		Input capture ch.0 trigger input pin
111	COM0	P	LCD controller/driver common output pin
112	COM1	P	LCD controller/driver common output pin
113	COM2	P	LCD controller/driver common output pin
114	COM3	P	LCD controller/driver common output pin
115	P22	F	General-purpose I/O port
	SEG00		LCD controller/driver segment output pin
116	P23	F	General-purpose I/O port
	SEG01		LCD controller/driver segment output pin
117	P24	F	General-purpose I/O port
	SEG02		LCD controller/driver segment output pin
118	P25	F	General-purpose I/O port
	SEG03		LCD controller/driver segment output pin
119	P26	F	General-purpose I/O port
	SEG04		LCD controller/driver segment output pin
120	P27	F	General-purpose I/O port
	SEG05		LCD controller/driver segment output pin
1	P30	F	General-purpose I/O port
	SEG06		LCD controller/driver segment output pin
2	P31	F	General-purpose I/O port
	SEG07		LCD controller/driver segment output pin
3	P32	F	General-purpose I/O port
	SEG08		LCD controller/driver segment output pin
4	P33	F	General-purpose I/O port
	SEG09		LCD controller/driver segment output pin
5	P34	F	General-purpose I/O port
	SEG10		LCD controller/driver segment output pin
6	P35	F	General-purpose I/O port
	SEG11		LCD controller/driver segment output pin
7	P36	F	General-purpose I/O port
	SEG12		LCD controller/driver segment output pin
8	P37	F	General-purpose I/O port
	SEG13		LCD controller/driver segment output pin
9	P40	F	General-purpose I/O port
	SEG14		LCD controller/driver segment output pin
10	P41	F	General-purpose I/O port
	SEG15		LCD controller/driver segment output pin
11	P42	F	General-purpose I/O port
	SEG16		LCD controller/driver segment output pin

Pin No.	Pin Name	I/O Circuit Type*1	Function
12	P43	F	General-purpose I/O port
	SEG17		LCD controller/driver segment output pin
18	P44	F	General-purpose I/O port
	SEG18		LCD controller/driver segment output pin
19	P45	F	General-purpose I/O port
	SEG19		LCD controller/driver segment output pin
20	P46	F	General-purpose I/O port
	SEG20		LCD controller/driver segment output pin
21	P47	F	General-purpose I/O port
	SEG21		LCD controller/driver segment output pin
37	P50	I	General-purpose I/O port
	INT0		INT0 external interrupt input pin
	ADTG		A/D converter external trigger input pin
58	P51	I	General-purpose I/O port
	INT1		INT1 external interrupt input pin
	RX1		CAN interface 1 RX input pin
	RX3		CAN interface 3 RX input pin
59	P52	I	General-purpose I/O port
	TX1		CAN interface 1 TX output pin
	TX3		CAN interface 3 TX output pin
60	P53	I	General-purpose I/O port
	INT3		INT3 external interrupt input pin
61	P54	I	General-purpose I/O port
	TX0		CAN interface 0 TX output pin
	TX2		CAN interface 2 TX output pin
	SGA1		Sound generator ch.1 SGA output pin
63	P55	I	General-purpose I/O port
	RX0		CAN interface 0 RX input pin
	RX2		CAN interface 2 RX input pin
	INT2		INT2 external interrupt input pin
91	P56	I	General-purpose I/O port
	SGO0		Sound generator ch.0 SGO output pin
	FRCK		Free-run timer clock input pin
92	P57	I	General-purpose I/O port
	SGA0		Sound generator ch.0 SGA output pin
39	P60	H	General-purpose I/O port
	AN0		A/D converter input pin
40	P61	H	General-purpose I/O port
	AN1		A/D converter input pin

Pin No.	Pin Name	I/O Circuit Type*1	Function
41	P62	H	General-purpose I/O port
	AN2		A/D converter input pin
42	P63	H	General-purpose I/O port
	AN3		A/D converter input pin
43	P64	H	General-purpose I/O port
	AN4		A/D converter input pin
44	P65	H	General-purpose I/O port
	AN5		A/D converter input pin
45	P66	H	General-purpose I/O port
	AN6		A/D converter input pin
46	P67	H	General-purpose I/O port
	AN7		A/D converter input pin
67	P70	L	General-purpose output-only port
	PWM1P0		Stepping motor controller ch.0 output pin
68	P71	L	General-purpose output-only port
	PWM1M0		Stepping motor controller ch.0 output pin
69	P72	L	General-purpose output-only port
	PWM2P0		Stepping motor controller ch.0 output pin
70	P73	L	General-purpose output-only port
	PWM2M0		Stepping motor controller ch.0 output pin
71	P74	L	General-purpose output-only port
	PWM1P1		Stepping motor controller ch.1 output pin
72	P75	L	General-purpose output-only port
	PWM1M1		Stepping motor controller ch.1 output pin
73	P76	L	General-purpose output-only port
	PWM2P1		Stepping motor controller ch.1 output pin
74	P77	L	General-purpose output-only port
	PWM2M1		Stepping motor controller ch.1 output pin
77	P80	L	General-purpose output-only port
	PWM1P2		Stepping motor controller ch.2 output pin
78	P81	L	General-purpose output-only port
	PWM1M2		Stepping motor controller ch.2 output pin
79	P82	L	General-purpose output-only port
	PWM2P2		Stepping motor controller ch.2 output pin
80	P83	L	General-purpose output-only port
	PWM2M2		Stepping motor controller ch.2 output pin
81	P84	L	General-purpose output-only port
	PWM1P3		Stepping motor controller ch.3 output pin
82	P85	L	General-purpose output-only port
	PWM1M3		Stepping motor controller ch.3 output pin

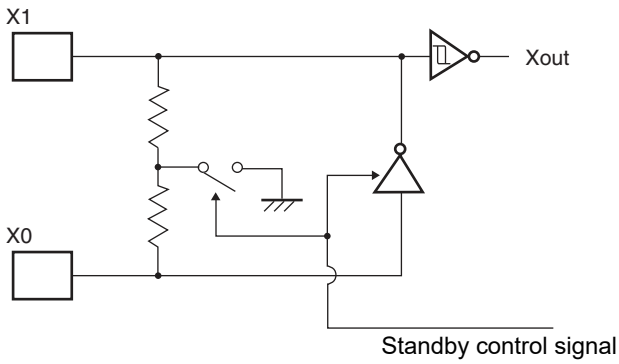
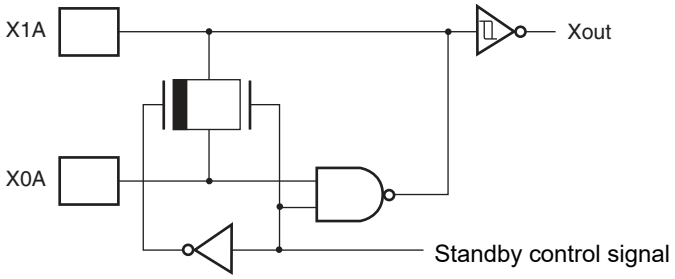
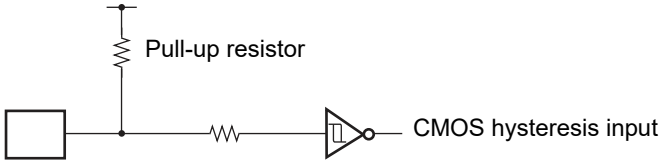
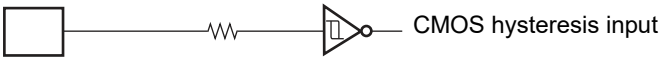
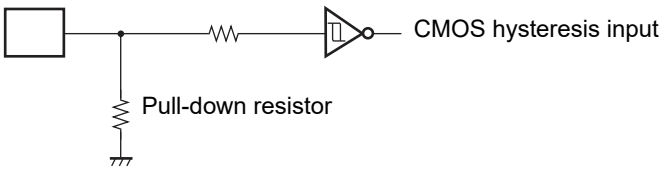
Pin No.	Pin Name	I/O Circuit Type*1	Function
83	P86	L	General-purpose output-only port
	PWM2P3		Stepping motor controller ch.3 output pin
84	P87	L	General-purpose output-only port
	PWM2M3		Stepping motor controller ch.3 output pin
22	P90	F	General-purpose I/O port
	SEG22		LCD controller/driver segment output pin
23	P91	F	General-purpose I/O port
	SEG23		LCD controller/driver segment output pin
31	P94	G	General-purpose I/O port
	V0		LCD controller/driver reference power supply pin
32	P95	G	General-purpose I/O port
	V1		LCD controller/driver reference power supply pin
33	P96	G	General-purpose I/O port
	V2		LCD controller/driver reference power supply pin
34	V3	—	LCD controller/driver reference power supply pin
48	PC0	J	General-purpose I/O port
	SIN0		UART ch.0 serial data input pin
	INT4		INT4 external interrupt input pin
49	PC1	I	General-purpose I/O port
	SOT0		UART ch.0 serial data output pin
	INT5		INT5 external interrupt input pin
	IN3		Input capture ch.3 trigger input pin
50	PC2	I	General-purpose I/O port
	SCK0		UART ch.0 serial clock I/O pin
	INT6		INT6 external interrupt input pin
	IN2		Input capture ch.2 trigger input pin
51	PC3	J	General-purpose I/O port
	SIN1		UART ch.1 serial data input pin
	INT7		INT7 external interrupt input pin
52	PC4	I	General-purpose I/O port
	SOT1		UART ch.1 serial data output pin
53	PC5	I	General-purpose I/O port
	SCK1		UART ch.1 serial clock I/O pin
	TRG		16-bit PPG ch.0 to ch.5 external trigger input pin
54	PC6	I	General-purpose I/O port
	PPG0		16-bit PPG ch.0 output pin
	TOT1		16-bit reload timer ch.1 TOT output pin
	IN7		Input capture ch.7 trigger input pin

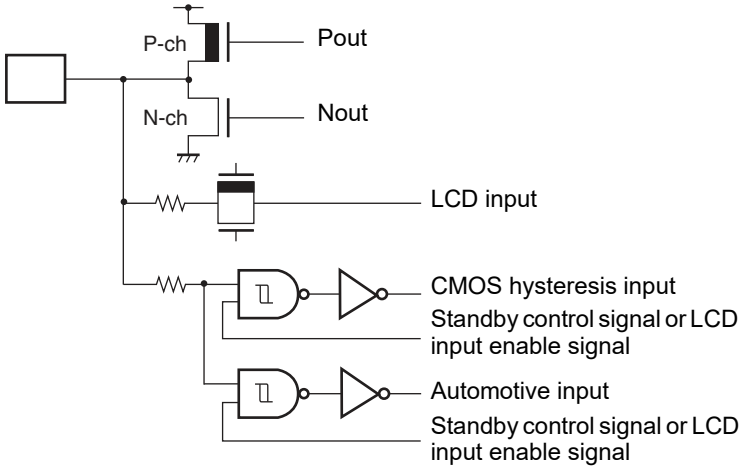
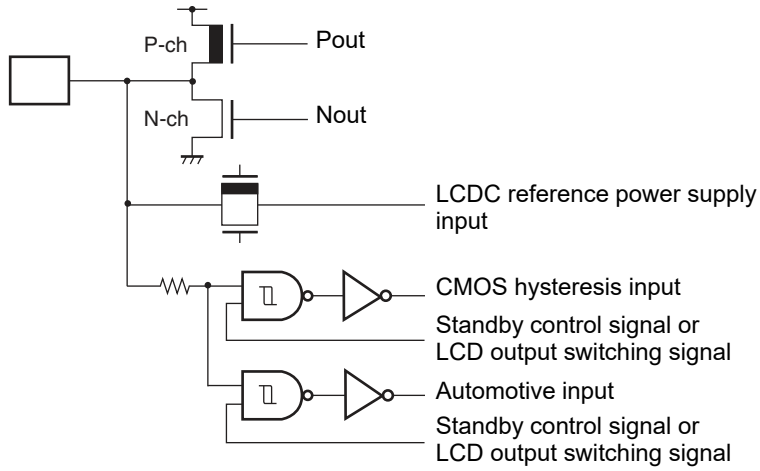
Pin No.	Pin Name	I/O Circuit Type*1	Function
55	PC7	I	General-purpose I/O port
	PPG1		16-bit PPG ch.1 output pin
	TIN1		16-bit reload timer ch.1 TIN input pin
	IN6		Input capture ch.6 trigger input pin
24	PD0	J	General-purpose I/O port
	SIN2		UART ch.2 serial data input pin
25	PD1	I	General-purpose I/O port
	SOT2		UART ch.2 serial data output pin
26	PD2	I	General-purpose I/O port
	SCK2		UART ch.2 serial clock I/O pin
27	PD3	J	General-purpose I/O port
	SIN3		UART ch.3 serial data input pin
28	PD4	I	General-purpose I/O port
	SOT3		UART ch.3 serial data output pin
29	PD5	I	General-purpose I/O port
	SCK3		UART ch.3 serial clock I/O pin
30	PD6	I	General-purpose I/O port
	TOT2		16-bit reload timer ch.2 TOT output pin
56	PE0	I	General-purpose I/O port
	TOT3		16-bit reload timer ch.3 TOT output pin
57	PE1	I	General-purpose I/O port
	TIN3		16-bit reload timer ch.3 TIN input pin
64	PE2	I	General-purpose I/O port
	SGO1		Sound generator ch.1 SGO output pin
62	RSTO	N	Internal reset signal output pin
65, 75, 85	DVCC	—	Power supply input pins dedicated for high current output buffer
66, 76, 86	DVSS	—	Power supply GND pins dedicated for high current output buffer
35	AVCC	—	A/D converter dedicated power supply input pin
38	AVSS	—	A/D converter dedicated power supply GND pin
36	AVRH	—	A/D converter Vref+ input pin. Vref- is fixed to AVSS.
89	MD0	D	Mode setting input pin. Connect to VCC pin.
88	MD1	D	Mode setting input pin. Connect to VCC pin.
87	MD2	D/E*2	Mode setting input pin. Connect to VSS pin.
17	C	—	External capacitor pin. Connect a 0.1 μF capacitor between this pin and the VSS pin.
15, 105	VCC	—	Power supply input pins
16, 47, 106	VSS	—	GND power supply pins

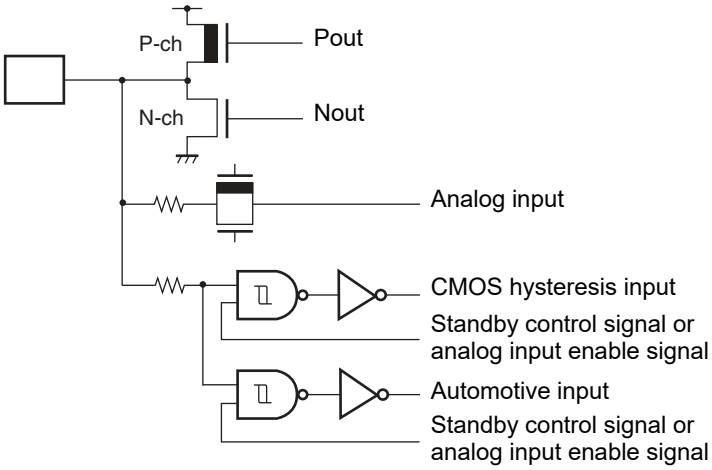
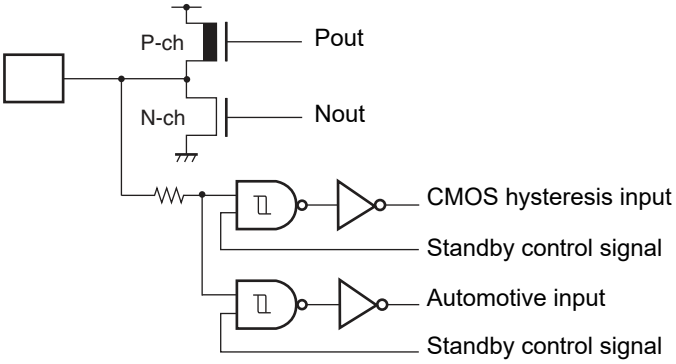
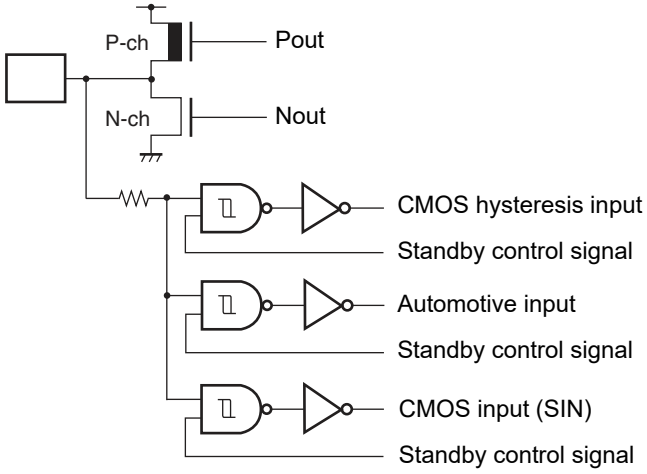
*1: For I/O circuit type, refer to I/O Circuit Type.

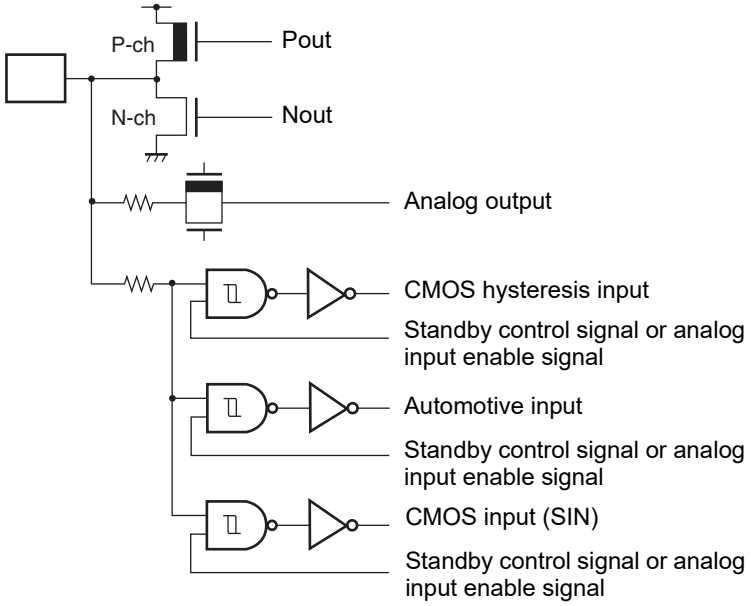
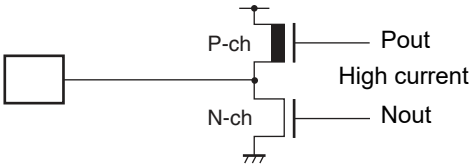
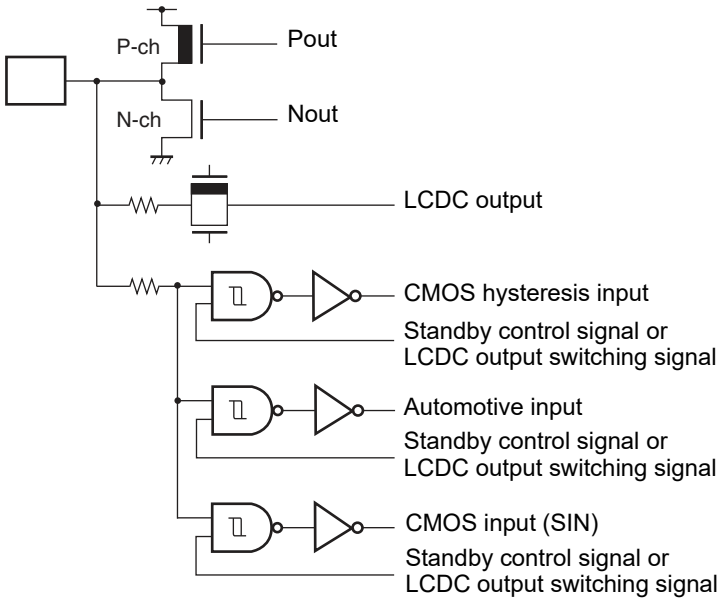
*2: The I/O circuit type is D for Flash memory products and E for evaluation products.

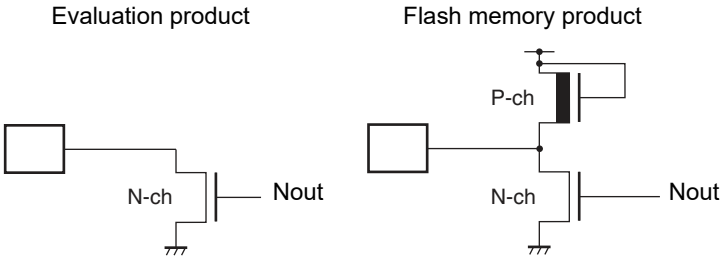
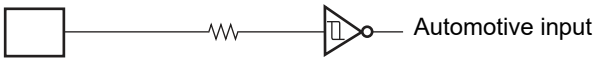
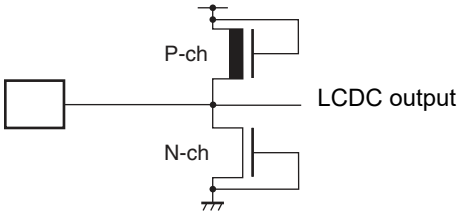
4. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistance: approx. 1 MΩ (Flash memory product/MASK ROM product/Evaluation product)
B		Oscillation circuit Low-speed oscillation feedback resistance: approx. 10 MΩ
C		Input-only pin (with pull-up resistance) ■ Attached pull-up resistor: approx. 50 kΩ ■ CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC})
D		Input-only pin ■ CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) Note: The MD2 pin of the Flash memory products uses this circuit type.
E		Input-only pin (with pull-down resistance) ■ Attached pull-down resistance: approx. 50 kΩ ■ CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) Note: The MD2 pin of the evaluation products uses this circuit type.

Type	Circuit	Remarks
F		LCD output common general-purpose port ■ CMOS output (I_{OH}/I_{OL} = ± 4 mA) ■ Hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) ■ Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
G		LCDC reference power supply common general-purpose port ■ CMOS output (I_{OH}/I_{OL} = ± 4 mA) ■ CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) ■ Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

Type	Circuit	Remarks
H		A/D converter input common general-purpose port ■ CMOS output (I_{OH}/I_{OL} = ±4 mA) ■ CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) ■ Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
I		General-purpose port ■ CMOS output (I_{OH}/I_{OL} = ±4 mA) ■ CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) ■ Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
J		General-purpose port (serial input) ■ CMOS output (I_{OH}/I_{OL} = ±4 mA) ■ CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) ■ CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) ■ Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

Type	Circuit	Remarks
K		A/D converter input common general-purpose port (serial input) ■ CMOS output (I_{OH}/I_{OL} = ± 4 mA) ■ CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) ■ CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) ■ Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
L		High current output port (SMC pin) CMOS output (I_{OH}/I_{OL} = ± 30 mA)
M		LCDC output common general-purpose port (serial input)) ■ CMOS output (I_{OH}/I_{OL} = ± 4 mA) ■ CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) ■ CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) ■ Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

Type	Circuit	Remarks
N		N-ch open-drain pin I_{OL} = 4 mA
O		Input-only pin Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
P		LCDC output pin (COM pin)

5. Handling Devices

Strictly Observe Maximum Rated Voltages (Preventing Latch-up)

In CMOS IC devices, a condition known as latch-up may occur if voltages higher than V_{CC} or lower than V_{SS} are applied to input or output pins other than medium or high withstand voltage pins, or if the voltage applied between VCC and VSS pins exceeds the rated voltage level. If a latch-up occurs, the power supply current may increase dramatically and may destroy semiconductor elements. When using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

When the analog system power supply is switched on or off, be careful not to apply the analog power supply (AV_{CC}, AVRH), the analog input voltages and the power supply voltage for the high current output buffer pins (DV_{CC}) in excess of the digital power supply voltage (V_{CC}).

Once the digital power supply voltage (V_{CC}) has been disconnected, the analog power supply (AV_{CC}, AVRH) and the power supply voltage for the high current output buffer pins (DV_{CC}) may be turned on in any sequence.

Supply Voltage Stabilization

Rapid fluctuations in the power supply voltage can cause malfunctions even if the Vcc power supply voltage remains within the warranted operating range. It is recommended that the power supply be stabilized such that ripple fluctuations (P-P value) at commercial frequencies (50 Hz/60 Hz) be limited to within 10% of the standard V_{CC} value, and that transient fluctuations due to power supply switching, etc. be limited to a rate of 0.1 V/ms or less.

Precautions when Turning the Power On

In order to prevent the built-in step-down circuits from malfunctioning, the time taken for the voltage to rise (0.2 V to 2.7 V) during power-on should be less than 50 μs.

Handling Unused Pins

If unused input pins are left open, they may cause malfunctions or latch-up which may lead to permanent damage to the semiconductor. Unused input pins should therefore be pulled up or pulled down through a resistor of at least 2 kΩ.

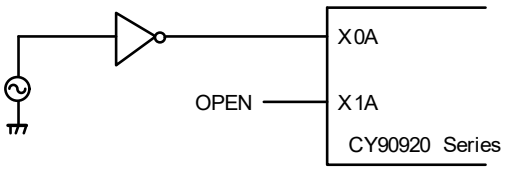
Unused input/output pins may be set to the output state and left open, or set to the input state and connected to a pull-up or pull-down resistance of 2 kΩ or more.

Handling A/D Converter Power Supply Pins

Even if the A/D converter is not used, the power supply pins should be connected such as $AV_{CC} = V_{CC}$, and $AV_{SS} = AVRH = V_{SS}$.

Notes on Using an External Clock

Even when an external clock is used, an oscillation stabilization wait time is required following power-on reset or release from sub clock mode or stop mode. Furthermore, only the X0A pin should be driven when an external clock is used, with the X1A pin open as shown in the following diagram. Do not use high-speed oscillation pins (X0 and X1) for external clock input.



Sample external clock connection

Notes on Operating in PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Cypress will not guarantee results of operations if such failure occurs.

Crystal Oscillator Circuit

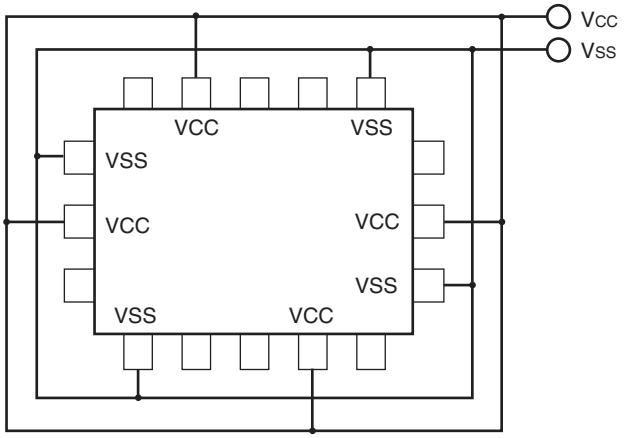
Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

Power Supply Pins

Devices including multiple VCC or VSS pins are designed such that pins that need to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the VCC and VSS pins to the power supply and ground externally.

Always connect all of the VCC pins to the same potential and all of the VSS pins to ground as shown in the following diagram. The device will not operate correctly if multiple VCC or VSS pins are connected to different voltages, even if those voltages are within the guaranteed operating ranges.



Power supply input pins (Vcc/Vss)

In addition, care must be given to connecting the VCC and VSS pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 μF bypass capacitor be connected between the VCC and VSS pins as close to the pins as possible.

Sequence for Connecting the A/D Converter Power Supply and Analog Inputs

The A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN7) must be applied after the digital power supply (V_{CC}) is switched on. When turning the power off, the A/D converter power supply and analog inputs must be disconnected before the digital power supply is switched off (V_{CC}). Ensure that AVRH does not exceed AVcc during either power-on or power-off. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

Handling the Power Supply for High-current Output Buffer Pins (DV_{CC}, DV_{SS})

■ Flash memory products and MASK ROM products (CY90F922NC/F922NCS/922NCS/F923NC/F923NCS/F924NC/F924NCS)

In the Flash memory products and MASK ROM products, the power supply for the high-current output buffer pins (DV_{CC}, DV_{SS}) is isolated from the digital power supply (V_{CC}).
Therefore, DVcc can therefore be set to a higher voltage than Vcc. If the power supply for the high-current output buffer pins (DV_{CC}, DV_{SS}) is supplied before the digital power supply (V_{CC}), however, care needs to be taken because it is possible that the port 7 or port 8 stepping motor outputs may momentarily output an “H” or “L” level. In order to prevent this, connect the digital power supply (V_{CC}) prior to connecting the power supply for the high-current output buffer pins. Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins (DV_{CC}, DV_{SS}).

■ Evaluation product (CY90V920-101/CY90V920-102)

In the evaluation products, the power supply for the high-current output buffer pins (DV_{CC}, DV_{SS}) is not isolated from the digital power supply (V_{CC}). Therefore, DV_{CC} must therefore be set to a lower voltage than Vcc. The power supply for the high-current output buffer pins (DV_{CC}, DV_{SS}) must always be applied after the digital power supply (V_{CC}) has been connected, and disconnected before the digital power supply (Vcc) is disconnected (the power supply for the high-current output buffer pins may also be connected and disconnected simultaneously with the digital power supply).
Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins (DV_{CC}, DV_{SS}).

Pull-up/Pull-down Resistors

CY90920 series does not support internal pull-up/pull-down resistors. Use external components as necessary.

Precautions When Not Using a Sub Clock Signal

If the X0A and X1A pins are not connected to an oscillator, apply a pull-down resistance to the X0A pin and leave the X1A pin open.

Notes on Operating When the External Clock is Stopped

The CY90920 series is not guaranteed to operate correctly using the internal oscillator circuit when there is no external oscillator or the external clock input is stopped.

Flash Memory Security Function

A security bit is located within the Flash memory region. The security function is activated by writing the protection code 01_H to the security bit.
Do not write the value 01_H to this address if you are not using the security function.
Please refer to following table for the address of the security bit.

	Flash Memory Size	Address for Security Bit
CY90F922NC CY90F922NCS	Built-in 2 Mbits Flash Memory	$FC0001_H$
CY90F923NCS	Built-in 3 Mbits Flash Memory	$F80001_H$
CY90F924NCS	Built-in 4 Mbits Flash Memory	$F80001_H$

Serial Communication

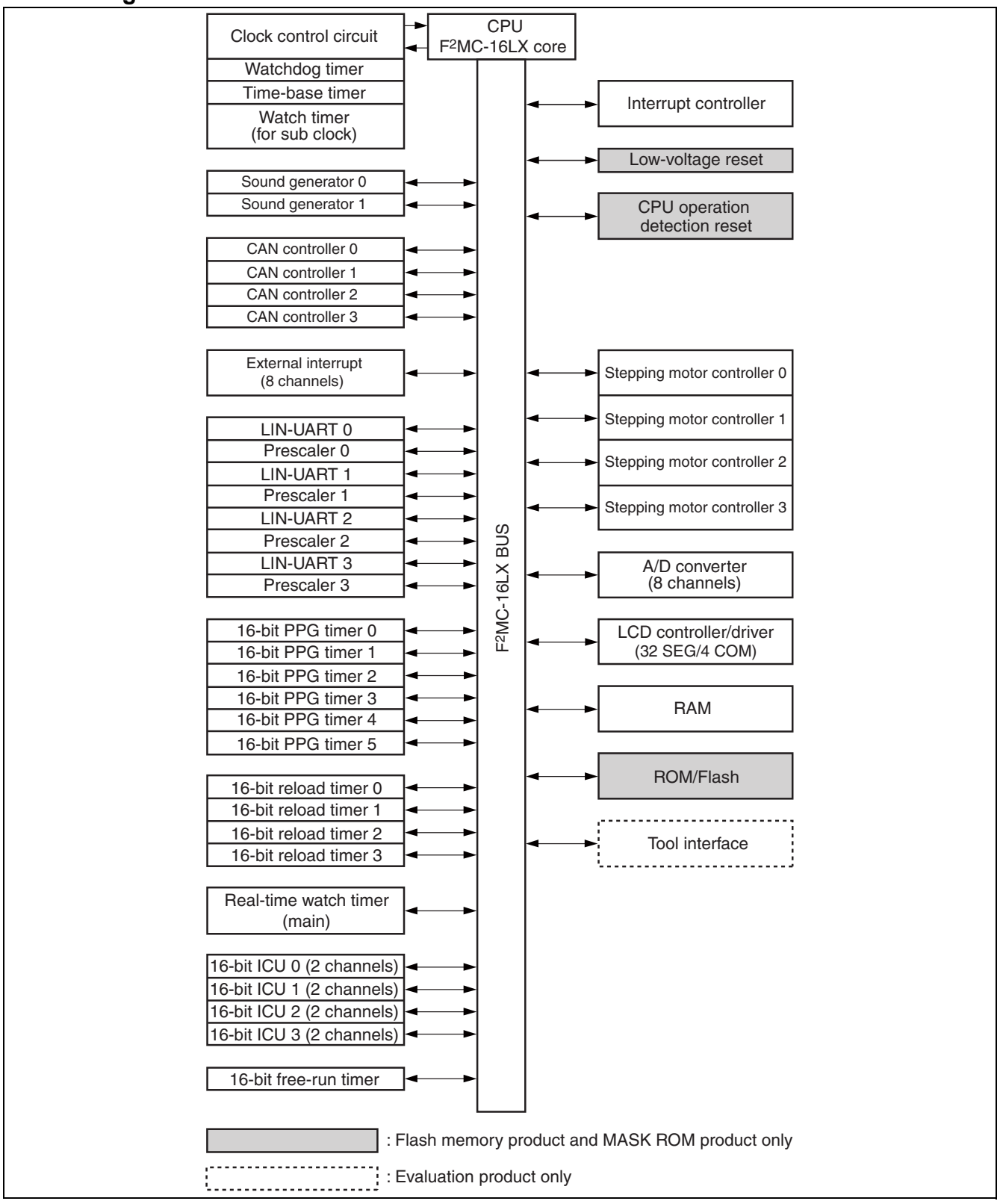
In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, detect errors by measures such as adding a checksum to the end of data. If an error is detected, retransmit the data.

Characteristic Difference Between Flash Device and MASK ROM Device

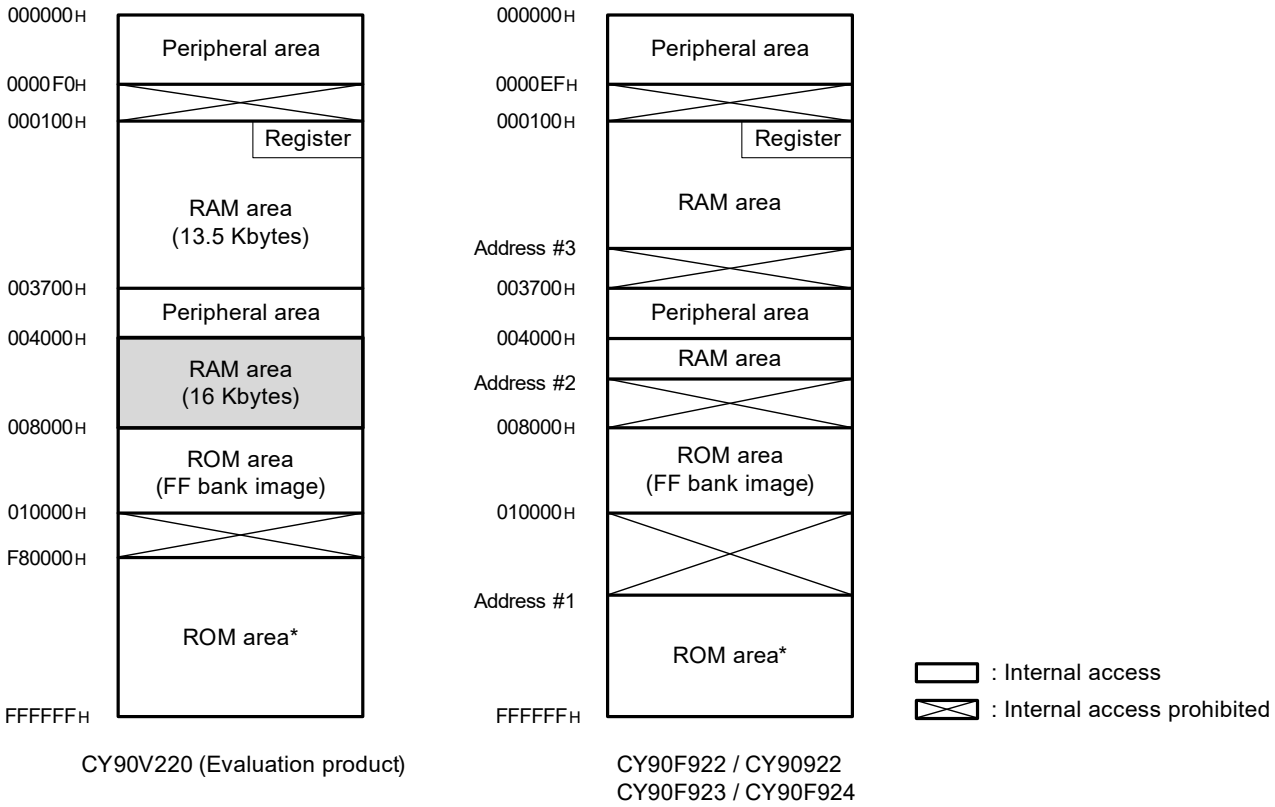
In the flash device and the MASK ROM device, the electrical characteristic including current consumption, ESD, latch-up, the noise characteristic, and oscillation characteristic, etc. is different according to the difference between the chip layout and the memory structure.

Reconfirm the electrical characteristic when the product is replaced by another product of the same series.

6. Block Diagram



7. Memory Map



Parts No.	ROM (Flash) Capacitance	RAM Capacitance	Address #1	Address #2	Address #3
CY90F922NC/F922NCS/922NCS	256 Kbytes	10 Kbytes	$FC0000_H$	004000_H	002900_H
CY90F923NC/F923NCS	384 Kbytes	16 Kbytes	$FA0000_H$	$004A00_H$	003700_H
CY90F924NC/F924NCS	512 Kbytes	24 Kbytes	$F80000_H$	$006A00_H$	003700_H

*:Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note:

To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address $00C000_H$, the actual address to be accessed is $FFC000_H$ in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from $FF8000_H$ to $FFFFFF_H$ appears in the image from 008000_H to $00FFFF_H$, it is recommended that ROM data tables be stored in the area from $FF8000_H$ to $FFFFFF_H$.

8. I/O Map

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
000000_H	Port 0 data register	PDR0	R/W	Port 0	$XXXXXXXX_B$
000001_H	Port 1 data register	PDR1	R/W	Port 1	$XXXXXXXX_B$
000002_H	Port 2 data register	PDR2	R/W	Port 2	$XXXXXXXX_B$
000003_H	Port 3 data register	PDR3	R/W	Port 3	$XXXXXXXX_B$
000004_H	Port 4 data register	PDR4	R/W	Port 4	$XXXXXXXX_B$
000005_H	Port 5 data register	PDR5	R/W	Port 5	$XXXXXXXX_B$
000006_H	Port 6 data register	PDR6	R/W	Port 6	$XXXXXXXX_B$
000007_H	Port 7 data register	PDR7	R/W	Port 7	$XXXXXXXX_B$
000008_H	Port 8 data register	PDR8	R/W	Port 8	$XXXXXXXX_B$
000009_H	Port 9 data register	PDR9	R/W	Port 9	$XXXXXXXX_B$
$00000A_H$, $00000B_H$	(Disabled)				
$00000C_H$	Port C data register	PDRC	R/W	Port C	$XXXXXXXX_B$
$00000D_H$	Port D data register	PDRD	R/W	Port D	$XXXXXXXX_B$
$00000E_H$	Port E data register	PDRE	R/W	Port E	$XXXXXXXX_B$
$00000F_H$	(Disabled)				
000010_H	Port 0 direction register	DDR0	R/W	Port 0	00000000_B
000011_H	Port 1 direction register	DDR1	R/W	Port 1	$XX000000_B$
000012_H	Port 2 direction register	DDR2	R/W	Port 2	$000000XX_B$
000013_H	Port 3 direction register	DDR3	R/W	Port 3	00000000_B
000014_H	Port 4 direction register	DDR4	R/W	Port 4	00000000_B
000015_H	Port 5 direction register	DDR5	R/W	Port 5	00000000_B
000016_H	Port 6 direction register	DDR6	R/W	Port 6	00000000_B
000017_H	Port 7 direction register	DDR7	R/W	Port 7	00000000_B
000018_H	Port 8 direction register	DDR8	R/W	Port 8	00000000_B
000019_H	Port 9 direction register	DDR9	R/W	Port 9	$X0000000_B$
$00001A_H$	Analog input enable	ADER6	R/W	Port 6, A/D	11111111_B
$00001B_H$	(Disabled)				
$00001C_H$	Port C direction register	DDRC	R/W	Port C	00000000_B
$00001D_H$	Port D direction register	DDRD	R/W	Port D	$X0000000_B$
$00001E_H$	Port E direction register	DDRE	R/W	Port E	$XXXXX000_B$
$00001F_H$	(Disabled)				
000020_H	Lower A/D control status register	ADCS0	R/W	A/D converter	$000XXXX0_B$
000021_H	Higher A/D control status register	ADCS1	R/W		$0000000X_B$
000022_H	Lower A/D control status register	ADCR0	R		00000000_B
000023_H	Higher A/D data register	ADCR1	R		$XXXXXX00_B$

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
000024_H	Compare clear register	CPCLR	R/W	16-bit free-run timer	$XXXXXXXX_B$
000025_H			R/W		$XXXXXXXX_B$
000026_H	Timer data register	TCDT	R/W		00000000_B
000027_H			R/W		00000000_B
000028_H	Lower timer control status register	TCCSL	R/W		00000000_B
000029_H	Higher timer control status register	TCCSH	R/W		$01\text{-}00000_B$
$00002A_H$	Lower PPG0 control status register	PCNTL0	R/W	16-bit PPG0	00000000_B
$00002B_H$	Higher PPG0 control status register	PCNTH0	R/W		00000001_B
$00002C_H$	Lower PPG1 control status register	PCNTL1	R/W	16-bit PPG1	00000000_B
$00002D_H$	Higher PPG1 control status register	PCNTH1	R/W		00000001_B
$00002E_H$	Lower PPG2 control status register	PCNTL2	R/W	16-bit PPG2	00000000_B
$00002F_H$	Higher PPG2 control status register	PCNTH2	R/W		00000001_B
000030_H	External interrupt enable	ENIR	R/W	External interrupt	00000000_B
000031_H	External interrupt request	EIRR	R/W		00000000_B
000032_H	Lower external interrupt level	ELVRL	R/W		00000000_B
000033_H	Higher external interrupt level	ELVRH	R/W		00000000_B
000034_H	Serial mode register 0	SMR0	R/W, W	UART (LIN/SCI) 0	00000000_B
000035_H	Serial control register 0	SCR0	R/W, W		00000000_B
000036_H	Reception/transmission data register 1	RDR0/ TDR0	R/W		00000000_B
000037_H	Serial status register 0	SSR0	R/W, R		00001000_B
000038_H	Extended communication control register 0	ECCR0	R/W, R		$000000XX_B$
000039_H	Extended status control register 0	ESCR0	R/W		00000100_B
$00003A_H$	Baud rate generator register 00	BGR00	R/W		00000000_B
$00003B_H$	Baud rate generator register 01	BGR01	R/W, R		00000000_B
$00003C_H$ to $00003F_H$	(Disabled)				
000040_H to $00004F_H$	Area reserved for CAN Controller 0. Refer to CAN Controllers				
000050_H	Lower timer control status register 0	TMCSR0L	R/W	16-bit reload timer 0	00000000_B
000051_H	Higher timer control status register 0	TMCSR0H	R/W		$XXX10000_B$
000052_H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		$XXXXXXXX_B$
000053_H					$XXXXXXXX_B$
000054_H	Lower timer control status register 1	TMCSR1L	R/W	16-bit reload timer 1	00000000_B
000055_H	Higher timer control status register 1	TMCSR1H	R/W		$XXX10000_B$
000056_H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		$XXXXXXXX_B$
000057_H					$XXXXXXXX_B$
000058_H	LCD output control register 1	LOCR1	R/W	LCDC	11111111_B
000059_H	LCD output control register 2	LOCR2	R/W		00000000_B

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
$00005A_H$	Lower sound control register 0	SGCRL0	R/W	Sound generator 0	00000000_B
$00005B_H$	Higher sound control register 0	SGCRH0	R/W		$0XXXX100_B$
$00005C_H$	Frequency data register 0	SGFR0	R/W		$XXXXXXXX_B$
$00005D_H$	Amplitude data register 0	SGAR0	R/W		00000000_B
$00005E_H$	Decrement grade register 0	SGDR0	R/W		$XXXXXXXX_B$
$00005F_H$	Tone count register 0	SGTR0	R/W		$XXXXXXXX_B$
000060_H	Input capture register 0	IPCP0	R	Input capture 0/1	$XXXXXXXX_B$
000061_H					$XXXXXXXX_B$
000062_H	Input capture register 1	IPCP1	R		$XXXXXXXX_B$
000063_H					$XXXXXXXX_B$
000064_H	Input capture register 2	IPCP2	R	Input capture 2/3	$XXXXXXXX_B$
000065_H					$XXXXXXXX_B$
000066_H	Input capture register 3	IPCP3	R		$XXXXXXXX_B$
000067_H					$XXXXXXXX_B$
000068_H	Input capture control status 0/1	ICS01	R/W	Input capture 0/1	00000000_B
000069_H	Input capture edge register 0/1	ICE01	R/W		$XXX0X0XX_B$
$00006A_H$	Input capture control status 2/3	ICS23	R/W	Input capture 2/3	00000000_B
$00006B_H$	Input capture edge register 2/3	ICE23	R/W		$XXXXXXXX_B$
$00006C_H$	Lower LCD control register	LCRL	R/W	LCD controller/ driver	00010000_B
$00006D_H$	Higher LCD control register	LCRH	R/W		00000000_B
$00006E_H$	Low voltage/CPU operation detection reset control register	LVRC	R/W	Low voltage/CPU operation detection reset	00111000_B
$00006F_H$	ROM mirror	ROMM	W	ROM mirror	$XXXXXXX1_B$
000070_H to $00007F_H$	Area reserved for CAN Controller 1. Refer to CAN Controllers				
000080_H	PWM control register 0	PWC0	R/W	Stepping motor controller 0	$000000X0_B$
000081_H	(Disabled)				
000082_H	PWM control register 1	PWC1	R/W	Stepping motor controller 1	$000000X0_B$
000083_H	(Disabled)				
000084_H	PWM control register 2	PWC2	R/W	Stepping motor controller 2	$000000X0_B$
000085_H	(Disabled)				
000086_H	PWM control register 3	PWC3	R/W	Stepping motor controller 3	$000000X0_B$
000087_H	(Disabled)				
000088_H	LCD output control register 3	LOCR3	R/W	LCDC	$XXXXX111_B$
000089_H	(Disabled)				
$00008A_H$	A/D setting register 0	ADSR0	R/W	A/D converter	00000000_B
$00008B_H$	A/D setting register 1	ADSR1	R/W		00000000_B

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
$00008C_H$	Port input level select 0	PIL0	R/W	Port input level select	00000000_B
$00008D_H$	Port input level select 1	PIL1	R/W		$XXXX0000_B$
$00008E_H$	Port input level select 2	PIL2	R/W		$XXXX0000_B$
$00008F_H$ to $00009D_H$	(Disabled)				
$00009E_H$	Program address detection control register	PACSR	R/W	Address match detection	$XXXX0X0X_B$
$00009F_H$	Delayed Interrupt/Release Register	DIRR	R/W	Delay interrupt	$XXXXXXX0_B$
$0000A0_H$	Power saving mode control register	LPMCR	R/W	Power saving control circuit	00011000_B
$0000A1_H$	Clock select register	CKSCR	R/W, R		11111100_B
$0000A2_H$ to $0000A7_H$	(Disabled)				
$0000A8_H$	Watchdog timer control register	WDTC	R, W	Watchdog timer	$XXXXX111_B$
$0000A9_H$	Time-base timer control register	TBTC	R/W, W	Time-base timer	$1XX00100_B$
$0000AA_H$	Watch timer control register	WTC	R/W, W, R	Watch timer (sub clock)	10001000_B
$0000AB_H$ to $0000AD_H$	(Disabled)				
$0000AE_H$	Flash memory control status register	FMCS	R/W	Flash interface	$000X0000_B$
$0000AF_H$	(Disabled)				
$0000B0_H$	Interrupt control register 00	ICR00	R/W	Interrupt controller	00000111_B
$0000B1_H$	Interrupt control register 01	ICR01	R/W		00000111_B
$0000B2_H$	Interrupt control register 02	ICR02	R/W		00000111_B
$0000B3_H$	Interrupt control register 03	ICR03	R/W		00000111_B
$0000B4_H$	Interrupt control register 04	ICR04	R/W		00000111_B
$0000B5_H$	Interrupt control register 05	ICR05	R/W		00000111_B
$0000B6_H$	Interrupt control register 06	ICR06	R/W		00000111_B
$0000B7_H$	Interrupt control register 07	ICR07	R/W		00000111_B
$0000B8_H$	Interrupt control register 08	ICR08	R/W		00000111_B
$0000B9_H$	Interrupt control register 09	ICR09	R/W		00000111_B
$0000BA_H$	Interrupt control register 10	ICR10	R/W		00000111_B
$0000BB_H$	Interrupt control register 11	ICR11	R/W		00000111_B
$0000BC_H$	Interrupt control register 12	ICR12	R/W		00000111_B
$0000BD_H$	Interrupt control register 13	ICR13	R/W		00000111_B
$0000BE_H$	Interrupt control register 14	ICR14	R/W		00000111_B
$0000BF_H$	Interrupt control register 15	ICR15	R/W		00000111_B
$0000C0_H$ to $0000C3_H$	(Disabled)				

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
$0000C4_H$	Serial mode register 1	SMR1	R/W, W	UART (LIN/SCI) 1	00000000_B
$0000C5_H$	Serial control register 1	SCR1	R/W, W		00000000_B
$0000C6_H$	Reception/transmission data register 1	RDR1/TDR1	R/W		00000000_B
$0000C7_H$	Serial status register 1	SSR1	R/W, R		00001000_B
$0000C8_H$	Extended communication control register 1	ECCR1	R/W, R		$000000XX_B$
$0000C9_H$	Extended status control register 1	ESCR1	R/W		00000100_B
$0000CA_H$	Baud rate generator register 10	BGR10	R/W		00000000_B
$0000CB_H$	Baud rate generator register 11	BGR11	R/W, R		00000000_B
$0000CC_H$	Lower watch timer control register	WTCRL	R/W	Real-time watch timer	$000XXXX0_B$
$0000CD_H$	Middle watch timer control register	WTCRM	R/W		00000000_B
$0000CE_H$	Higher watch timer control register	WTCRH	R/W		$XXXXXX00_B$
$0000CF_H$	Sub clock control register	PSCCR	W	Sub clock	$XXXX0000_B$
$0000D0_H$	Input capture control status 4/5	ICS45	R/W	Input capture 4/5	00000000_B
$0000D1_H$	Input capture edge register 4/5	ICE45	R/W, R		$XXXXXXXX_B$
$0000D2_H$	Input capture control status 6/7	ICS67	R/W	Input capture 6/7	00000000_B
$0000D3_H$	Input capture edge register 6/7	ICE67	R/W, R		$XXX0X0XX_B$
$0000D4_H$	Lower timer control status register 2	TMCSR2L	R/W	16-bit reload timer 2	00000000_B
$0000D5_H$	Higher timer control status register 2	TMCSR2H	R/W		$XXX10000_B$
$0000D6_H$	Lower timer control status register 3	TMCSR3L	R/W	16-bit reload timer 3	00000000_B
$0000D7_H$	Higher timer control status register 3	TMCSR3H	R/W		$XXX10000_B$
$0000D8_H$	Lower sound control register 1	SGCRL1	R/W	Sound generator 1	00000000_B
$0000D9_H$	Higher sound control register 1	SGCRH1	R/W		$0XXXX100_B$
$0000DA_H$	Lower PPG3 control status register	PCNTL3	R/W	16-bit PPG3	00000000_B
$0000DB_H$	Higher PPG3 control status register	PCNTH3	R/W		00000001_B
$0000DC_H$	Lower PPG4 control status register	PCNTL4	R/W	16-bit PPG4	00000000_B
$0000DD_H$	Higher PPG4 control status register	PCNTH4	R/W		00000001_B
$0000DE_H$	Lower PPG5 control status register	PCNTL5	R/W	16-bit PPG5	00000000_B
$0000DF_H$	Higher PPG5 control status register	PCNTH5	R/W		00000001_B
$0000E0_H$	Serial mode register 2	SMR2	R/W, W	UART (LIN/SCI) 2	00000000_B
$0000E1_H$	Serial control register 2	SCR2	R/W, W		00000000_B
$0000E2_H$	Reception/transmission data register 2	RDR2/TDR2	R/W		00000000_B
$0000E3_H$	Serial status register 2	SSR2	R/W, R		00001000_B
$0000E4_H$	Extended communication control register 2	ECCR2	R/W, R		$000000XX_B$
$0000E5_H$	Extended status control register 2	ESCR2	R/W		00000100_B
$0000E6_H$	Baud rate generator register 20	BGR20	R/W		00000000_B
$0000E7_H$	Baud rate generator register 21	BGR21	R/W, R		00000000_B

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
$0000E8_H$	Serial mode register 3	SMR3	R/W, W	UART (LIN/SCI) 3	00000000_B
$0000E9_H$	Serial control register 3	SCR3	R/W, W		00000000_B
$0000EA_H$	Reception/transmission data register 3	RDR3/TDR3	R/W		00000000_B
$0000EB_H$	Serial status register 3	SSR3	R/W, R		00001000_B
$0000EC_H$	Extended communication control register 3	ECCR3	R/W, R		$000000XX_B$
$0000ED_H$	Extended status control register 3	ESCR3	R/W		00000100_B
$0000EE_H$	Baud rate generator register 30	BGR30	R/W		00000000_B
$0000EF_H$	Baud rate generator register 31	BGR31	R/W, R		00000000_B
$001FF0_H$	Program address detection register 0	PADR0	R/W	Address match detection	$XXXXXXXX_B$
$001FF1_H$	Program address detection register 1	PADR0	R/W		$XXXXXXXX_B$
$001FF2_H$	Program address detection register 2	PADR0	R/W		$XXXXXXXX_B$
$001FF3_H$	Program address detection register 3	PADR1	R/W		$XXXXXXXX_B$
$001FF4_H$	Program address detection register 4	PADR1	R/W		$XXXXXXXX_B$
$001FF5_H$	Program address detection register 5	PADR1	R/W		$XXXXXXXX_B$
003700_H to $0037FF_H$	Area reserved for CAN Controller 2. Refer to CAN Controllers				
003800_H to $0038FF_H$	Area reserved for CAN Controller 3. Refer to CAN Controllers				
003900_H to $00391F_H$	(Disabled)				
003920_H	PPG0 down counter register	PDCR0	R	16-bit PPG0	11111111_B
003921_H					11111111_B
003922_H	PPG0 cycle setting register	PCSR0	W		11111111_B
003923_H					11111111_B
003924_H	PPG0 duty setting register	PDUT0	W	16-bit PPG0	00000000_B
003925_H					00000000_B
003926_H	PPG0 output division setting register	PPGDIV0	R/W, R		11111100_B
003927_H	(Disabled)				
003928_H	PPG1 down counter register	PDCR1	R	16-bit PPG1	11111111_B
003929_H					11111111_B
$00392A_H$	PPG1 cycle setting register	PCSR1	W		11111111_B
$00392B_H$					11111111_B
$00392C_H$	PPG1 duty setting register	PDUT1	W		00000000_B
$00392D_H$					00000000_B
$00392E_H$	PPG1output division setting register	PPGDIV1	R/W, R		11111100_B
$00392F_H$	(Disabled)				

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
003930_H	PPG2 down counter register	PDCR2	R	16-bit PPG2	11111111_B
003931_H					11111111_B
003932_H	PPG2 cycle setting register	PCSR2	W		11111111_B
003933_H					11111111_B
003934_H	PPG2 duty setting register	PDUT2	W		00000000_B
003935_H					00000000_B
003936_H	PPG2 output division setting register	PPGDIV2	R/W, R		11111100_B
003937_H to $00393F_H$	(Disabled)				
003940_H	Input capture register 4	IPCP4	R	Input capture 4/5	$XXXXXXXX_B$
003941_H					$XXXXXXXX_B$
003942_H	Input capture register 5	IPCP5	R		$XXXXXXXX_B$
003943_H					$XXXXXXXX_B$
003944_H	Input capture register 6	IPCP6	R	Input capture 6/7	$XXXXXXXX_B$
003945_H					$XXXXXXXX_B$
003946_H	Input capture register 7	IPCP7	R		$XXXXXXXX_B$
003947_H					$XXXXXXXX_B$
003948_H to $00394F_H$	(Disabled)				
003950_H	Minute data register 2/Reload register 2	TMR2/ TMRLR2	R/W	16-bit reload timer 2	$XXXXXXXX_B$
003951_H					$XXXXXXXX_B$
003952_H	Minute data register 3/Reload register 3	TMR3/ TMRLR3	R/W	16-bit reload timer 3	$XXXXXXXX_B$
003953_H					$XXXXXXXX_B$
003954_H to 003957_H	(Disabled)				
003958_H	Sub second data register	WTBR	R/W	Real time watch timer	$XXXXXXXX_B$
003959_H					$XXXXXXXX_B$
$00395A_H$					$XXXXXXXX_B$
$00395B_H$	Second data register	WTSR	R/W		$XX000000_B$
$00395C_H$	Minute data register	WTMR	R/W		$XX000000_B$
$00395D_H$	Hour data register	WTHR	R/W		$XXX00000_B$
$00395E_H$	Day data register	WTDR	R/W		$00X00001_B$
$00395F_H$	(Disabled)				

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
003960_H	LCD display RAM	VRAM	R/W	LCD controller/driver	$XXXXXXXX_B$
003961_H					$XXXXXXXX_B$
003962_H					$XXXXXXXX_B$
003963_H					$XXXXXXXX_B$
003964_H					$XXXXXXXX_B$
003965_H					$XXXXXXXX_B$
003966_H					$XXXXXXXX_B$
003967_H					$XXXXXXXX_B$
003968_H					$XXXXXXXX_B$
003969_H					$XXXXXXXX_B$
$00396A_H$					$XXXXXXXX_B$
$00396B_H$					$XXXXXXXX_B$
$00396C_H$					$XXXXXXXX_B$
$00396D_H$					$XXXXXXXX_B$
$00396E_H$					$XXXXXXXX_B$
$00396F_H$					$XXXXXXXX_B$
003970_H to 003973_H	(Disabled)				
003974_H	Frequency data register 1	SGFR1	R/W	Sound generator 1	$XXXXXXXX_B$
003975_H	Amplitude data register 1	SGAR1	R/W		00000000_B
003976_H	Decrement grade register 1	SGDR1	R/W		$XXXXXXXX_B$
003977_H	Tone count register 1	SGTR1	R/W		$XXXXXXXX_B$
003978_H to $00397F_H$	(Disabled)				
003980_H	PWM1 compare register 0	PWC10	R/W	Stepping motor controller 0	$XXXXXXXX_B$
003981_H					$XXXXXXXX_B$
003982_H	PWM2 compare register 0	PWC20	R/W		$XXXXXXXX_B$
003983_H					$XXXXXXXX_B$
003984_H	PWM1 select register 0	PWS10	R/W		00000000_B
003985_H	PWM2 select register 0	PWS20	R/W		$X0000000_B$
003986_H, 003987_H	(Disabled)				
003988_H	PWM1 compare register 1	PWC11	R/W	Stepping motor controller 1	$XXXXXXXX_B$
003989_H					$XXXXXXXX_B$
$00398A_H$	PWM2 compare register 1	PWC21	R/W		$XXXXXXXX_B$
$00398B_H$					$XXXXXXXX_B$
$00398C_H$	PWM1 select register 1	PWS11	R/W		00000000_B
$00398D_H$	PWM2 select register 1	PWS21	R/W		$X0000000_B$
$00398E_H$, $00398F_H$	(Disabled)				

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
003990_H	PWM1 compare register 2	PWC12	R/W	Stepping motor controller 2	$XXXXXXXX_B$
003991_H					$XXXXXXXX_B$
003992_H	PWM2 compare register 2	PWC22	R/W		$XXXXXXXX_B$
003993_H					$XXXXXXXX_B$
003994_H	PWM1 select register 2	PWS12	R/W		00000000_B
003995_H	PWM2 select register 2	PWS22	R/W		$X0000000_B$
003996_H, 003997_H	(Disabled)				
003998_H	PWM1 compare register 3	PWC13	R/W	Stepping motor controller 3	$XXXXXXXX_B$
003999_H					$XXXXXXXX_B$
$00399A_H$	PWM2 compare register 3	PWC23	R/W		$XXXXXXXX_B$
$00399B_H$					$XXXXXXXX_B$
$00399C_H$	PWM1 select register 3	PWS13	R/W		00000000_B
$00399D_H$	PWM2 select register 3	PWS23	R/W		$X0000000_B$
$00399E_H$ to $0039A5_H$	(Disabled)				
$0039A6_H$	Flash write control register 0	FWR0	R/W	Flash I/F	00000000_B
$0039A7_H$	Flash write control register 1	FWR1			00000000_B
$0039A8_H$ to $0039BF_H$	(Disabled)				
$0039C0_H$ to $0039DF_H$	Area reserved for CAN Controller 2. Refer to CAN Controllers				
$0039E0_H$ to $0039FF_H$	Area reserved for CAN Controller 3. Refer to CAN Controllers				
$003A00_H$ to $003AFF_H$	Area reserved for CAN Controller 0. Refer to CAN Controllers				
$003B00_H$ to $003BFF_H$	Area reserved for CAN Controller 1. Refer to CAN Controllers				
$003C00_H$ to $003CFF_H$	Area reserved for CAN Controller 0. Refer to CAN Controllers				
$003D00_H$ to $003DFF_H$	Area reserved for CAN Controller 1. Refer to CAN Controllers				
$003E00_H$ to $003EFF_H$	Area reserved for CAN Controller 2. Refer to CAN Controllers				
$003F00_H$ to $003FFF_H$	Area reserved for CAN Controller 3. Refer to CAN Controllers				

9. CAN Controllers

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

Table 9-1. List of Control Registers(1)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
$003C00_H$	$003D00_H$	$003E00_H$	$003F00_H$	Control status register	CSR	R/W, R	$00---000_B$ $0----0-1_B$
$003C01_H$	$003D01_H$	$003E01_H$	$003F01_H$				
$003C02_H$	$003D02_H$	$003E02_H$	$003F02_H$	Last event indicator register	LEIR	R/W	$--------_B$ $000-0000_B$
$003C03_H$	$003D03_H$	$003E03_H$	$003F03_H$				
$003C04_H$	$003D04_H$	$003E04_H$	$003F04_H$	RX/TX error counter	RTEC	R	00000000_B 00000000_B
$003C05_H$	$003D05_H$	$003E05_H$	$003F05_H$				
$003C06_H$	$003D06_H$	$003E06_H$	$003F06_H$	Bit timing register	BTR	R/W	-1111111_B 11111111_B
$003C07_H$	$003D07_H$	$003E07_H$	$003F07_H$				

Table 9-2. List of Control Registers(2)

Address				Register	Abbrevi-ation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
000040_H	000070_H	$0039C0_H$	$0039D0_H$	Message buffer valid register	BVALR	R/W	00000000_B 00000000_B
000041_H	000071_H	$0039C1_H$	$0039D1_H$				
000042_H	000072_H	$0039C2_H$	$0039D2_H$	Transmit request register	TREQR	R/W	00000000_B 00000000_B
000043_H	000073_H	$0039C3_H$	$0039D3_H$				
000044_H	000074_H	$0039C4_H$	$0039D4_H$	Transmit cancel register	TCANR	W	00000000_B 00000000_B
000045_H	000075_H	$0039C5_H$	$0039D5_H$				
000046_H	000076_H	$0039C6_H$	$0039D6_H$	Transmit complete register	TCR	R/W	00000000_B 00000000_B
000047_H	000077_H	$0039C7_H$	$0039D7_H$				
000048_H	000078_H	$0039C8_H$	$0039D8_H$	Receive complete register	RCR	R/W	00000000_B 00000000_B
000049_H	000079_H	$0039C9_H$	$0039D9_H$				
$00004A_H$	$00007A_H$	$0039CA_H$	$0039DA_H$	Remote request receive register	RRTRR	R/W	00000000_B 00000000_B
$00004B_H$	$00007B_H$	$0039CB_H$	$0039DB_H$				
$00004C_H$	$00007C_H$	$0039CC_H$	$0039DC_H$	Receive overrun register	ROVRR	R/W	00000000_B 00000000_B
$00004D_H$	$00007D_H$	$0039CD_H$	$0039DD_H$				

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
$00004E_H$	$00007E_H$	$0039CE_H$	$0039DE_H$	Receive interrupt enable register	RIER	R/W	00000000_B 00000000_B
$00004F_H$	$00007F_H$	$0039CF_H$	$0039DF_H$				
$003C08_H$	$003D08_H$	$003E08_H$	$003F08_H$	IDE register	IDER	R/W	$XXXXXXXX_B$
$003C09_H$	$003D09_H$	$003E09_H$	$003F09_H$				$XXXXXXXX_B$
$003C0A_H$	$003D0A_H$	$003E0A_H$	$003F0A_H$	Transmit RTR register	TRTRR	R/W	00000000_B
$003C0B_H$	$003D0B_H$	$003E0B_H$	$003F0B_H$				00000000_B
$003C0C_H$	$003D0C_H$	$003E0C_H$	$003F0C_H$	Remote frame receive wait register	RFWTR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003C0D_H$	$003D0D_H$	$003E0D_H$	$003F0D_H$				
$003C0E_H$	$003D0E_H$	$003E0E_H$	$003F0E_H$	Transmit interrupt enable register	TIER	R/W	00000000_B 00000000_B
$003C0F_H$	$003D0F_H$	$003E0F_H$	$003F0F_H$				
$003C10_H$	$003D10_H$	$003E10_H$	$003F10_H$	Acceptance mask select register	AMSR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003C11_H$	$003D11_H$	$003E11_H$	$003F11_H$				
$003C12_H$	$003D12_H$	$003E12_H$	$003F12_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$003C13_H$	$003D13_H$	$003E13_H$	$003F13_H$				
$003C14_H$	$003D14_H$	$003E14_H$	$003F14_H$	Acceptance mask register 0	AMR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003C15_H$	$003D15_H$	$003E15_H$	$003F15_H$				
$003C16_H$	$003D16_H$	$003E16_H$	$003F16_H$				$XXXXX---_B$ $XXXXXXXX_B$
$003C17_H$	$003D17_H$	$003E17_H$	$003F17_H$				
$003C18_H$	$003D18_H$	$003E18_H$	$003F18_H$	Acceptance mask register 1	AMR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003C19_H$	$003D19_H$	$003E19_H$	$003F19_H$				
$003C1A_H$	$003D1A_H$	$003E1A_H$	$003F1A_H$				$XXXXX---_B$ $XXXXXXXX_B$
$003C1B_H$	$003D1B_H$	$003E1B_H$	$003F1B_H$				

Table 9-3. List of Message Buffers (ID Registers)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
$003A00_H$ to $003A1F_H$	$003B00_H$ to $003B1F_H$	003700_H to $00371F_H$	003800_H to $00381F_H$	General-purpose RAM	—	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003A20_H$	$003B20_H$	003720_H	003820_H	ID register 0	IDR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A21_H$	$003B21_H$	003721_H	003821_H				
$003A22_H$	$003B22_H$	003722_H	003822_H				$XXXXX---_B$ $XXXXXXXX_B$
$003A23_H$	$003B23_H$	003723_H	003823_H				
$003A24_H$	$003B24_H$	003724_H	003824_H	ID register 1	IDR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A25_H$	$003B25_H$	003725_H	003825_H				
$003A26_H$	$003B26_H$	003726_H	003826_H				$XXXXX---_B$ $XXXXXXXX_B$
$003A27_H$	$003B27_H$	003727_H	003827_H				

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
$003A28_H$	$003B28_H$	003728_H	003828_H	ID register 2	IDR2	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A29_H$	$003B29_H$	003729_H	003829_H				
$003A2A_H$	$003B2A_H$	$00372A_H$	$00382A_H$				$XXXXX---_B$ $XXXXXXXX_B$
$003A2B_H$	$003B2B_H$	$00372B_H$	$00382B_H$				
$003A2C_H$	$003B2C_H$	$00372C_H$	$00382C_H$	ID register 3	IDR3	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A2D_H$	$003B2D_H$	$00372D_H$	$00382D_H$				
$003A2E_H$	$003B2E_H$	$00372E_H$	$00382E_H$				$XXXXX---_B$ $XXXXXXXX_B$
$003A2F_H$	$003B2F_H$	$00372F_H$	$00382F_H$				
$003A30_H$	$003B30_H$	003730_H	003830_H	ID register 4	IDR4	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A31_H$	$003B31_H$	003731_H	003831_H				
$003A32_H$	$003B32_H$	003732_H	003832_H				$XXXXX---_B$ $XXXXXXXX_B$
$003A33_H$	$003B33_H$	003733_H	003833_H				
$003A34_H$	$003B34_H$	003734_H	003834_H	ID register 5	IDR5	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A35_H$	$003B35_H$	003735_H	003835_H				
$003A36_H$	$003B36_H$	003736_H	003836_H				$XXXXX---_B$ $XXXXXXXX_B$
$003A37_H$	$003B37_H$	003737_H	003837_H				
$003A38_H$	$003B38_H$	003738_H	003838_H	ID register 6	IDR6	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A39_H$	$003B39_H$	003739_H	003839_H				
$003A3A_H$	$003B3A_H$	$00373A_H$	$00383A_H$				$XXXXX---_B$ $XXXXXXXX_B$
$003A3B_H$	$003B3B_H$	$00373B_H$	$00383B_H$				
$003A3C_H$	$003B3C_H$	$00373C_H$	$00383C_H$	ID register 7	IDR7	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A3D_H$	$003B3D_H$	$00373D_H$	$00383D_H$				
$003A3E_H$	$003B3E_H$	$00373E_H$	$00383E_H$				$XXXXX---_B$ $XXXXXXXX_B$
$003A3F_H$	$003B3F_H$	$00373F_H$	$00383F_H$				
$003A40_H$	$003B40_H$	003740_H	003840_H	ID register 8	IDR8	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A41_H$	$003B41_H$	003741_H	003841_H				
$003A42_H$	$003B42_H$	003742_H	003842_H				$XXXXX---_B$ $XXXXXXXX_B$
$003A43_H$	$003B43_H$	003743_H	003843_H				
$003A44_H$	$003B44_H$	003744_H	003844_H	ID register 9	IDR9	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A45_H$	$003B45_H$	003745_H	003845_H				
$003A46_H$	$003B46_H$	003746_H	003846_H				$XXXXX---_B$ $XXXXXXXX_B$
$003A47_H$	$003B47_H$	003747_H	003847_H				
$003A48_H$	$003B48_H$	003748_H	003848_H	ID register 10	IDR10	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A49_H$	$003B49_H$	003749_H	003849_H				
$003A4A_H$	$003B4A_H$	$00374A_H$	$00384A_H$				$XXXXX---_B$ $XXXXXXXX_B$
$003A4B_H$	$003B4B_H$	$00374B_H$	$00384B_H$				
$003A4C_H$	$003B4C_H$	$00374C_H$	$00384C_H$	ID register 11	IDR11	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A4D_H$	$003B4D_H$	$00374D_H$	$00384D_H$				
$003A4E_H$	$003B4E_H$	$00374E_H$	$00384E_H$				$XXXXX---_B$ $XXXXXXXX_B$
$003A4F_H$	$003B4F_H$	$00374F_H$	$00384F_H$				

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
$003A50_H$	$003B50_H$	003750_H	003850_H	ID register 12	IDR12	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A51_H$	$003B51_H$	003751_H	003851_H				
$003A52_H$	$003B52_H$	003752_H	003852_H				$XXXXX---_B$ $XXXXXXXX_B$
$003A53_H$	$003B53_H$	003753_H	003853_H				
$003A54_H$	$003B54_H$	003754_H	003854_H	ID register 13	IDR13	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A55_H$	$003B55_H$	003755_H	003855_H				
$003A56_H$	$003B56_H$	003756_H	003856_H				$XXXXX---_B$ $XXXXXXXX_B$
$003A57_H$	$003B57_H$	003757_H	003857_H				
$003A58_H$	$003B58_H$	003758_H	003858_H	ID register 14	IDR14	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A59_H$	$003B59_H$	003759_H	003859_H				
$003A5A_H$	$003B5A_H$	$00375A_H$	$00385A_H$				$XXXXX---_B$ $XXXXXXXX_B$
$003A5B_H$	$003B5B_H$	$00375B_H$	$00385B_H$				
$003A5C_H$	$003B5C_H$	$00375C_H$	$00385C_H$	ID register 15	IDR15	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$003A5D_H$	$003B5D_H$	$00375D_H$	$00385D_H$				
$003A5E_H$	$003B5E_H$	$00375E_H$	$00385E_H$				$XXXXX---_B$ $XXXXXXXX_B$
$003A5F_H$	$003B5F_H$	$00375F_H$	$00385F_H$				

Table 9-4. List of Message Buffers (DLC Registers)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
$003A60_H$	$003B60_H$	003760_H	003860_H	DLC register 0	DLCR0	R/W	$----XXXX_B$
$003A61_H$	$003B61_H$	003761_H	003861_H				
$003A62_H$	$003B62_H$	003762_H	003862_H	DLC register 1	DLCR1	R/W	$----XXXX_B$
$003A63_H$	$003B63_H$	003763_H	003863_H				
$003A64_H$	$003B64_H$	003764_H	003864_H	DLC register 2	DLCR2	R/W	$----XXXX_B$
$003A65_H$	$003B65_H$	003765_H	003865_H				
$003A66_H$	$003B66_H$	003766_H	003866_H	DLC register 3	DLCR3	R/W	$----XXXX_B$
$003A67_H$	$003B67_H$	003767_H	003867_H				
$003A68_H$	$003B68_H$	003768_H	003868_H	DLC register 4	DLCR4	R/W	$----XXXX_B$
$003A69_H$	$003B69_H$	003769_H	003869_H				
$003A6A_H$	$003B6A_H$	$00376A_H$	$00386A_H$	DLC register 5	DLCR5	R/W	$----XXXX_B$
$003A6B_H$	$003B6B_H$	$00376B_H$	$00386B_H$				
$003A6C_H$	$003B6C_H$	$00376C_H$	$00386C_H$	DLC register 6	DLCR6	R/W	$----XXXX_B$
$003A6D_H$	$003B6D_H$	$00376D_H$	$00386D_H$				
$003A6E_H$	$003B6E_H$	$00376E_H$	$00386E_H$	DLC register 7	DLCR7	R/W	$----XXXX_B$
$003A6F_H$	$003B6F_H$	$00376F_H$	$00386F_H$				
$003A70_H$	$003B70_H$	003770_H	003870_H	DLC register 8	DLCR8	R/W	$----XXXX_B$
$003A71_H$	$003B71_H$	003771_H	003871_H				
$003A72_H$	$003B72_H$	003772_H	003872_H	DLC register 9	DLCR9	R/W	$----XXXX_B$
$003A73_H$	$003B73_H$	003773_H	003873_H				

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
$003A74_H$	$003B74_H$	003774_H	003874_H	DLC register 10	DLCR10	R/W	$----XXXX_B$
$003A75_H$	$003B75_H$	003775_H	003875_H				
$003A76_H$	$003B76_H$	003776_H	003876_H	DLC register 11	DLCR11	R/W	$----XXXX_B$
$003A77_H$	$003B77_H$	003777_H	003877_H				
$003A78_H$	$003B78_H$	003778_H	003878_H	DLC register 12	DLCR12	R/W	$----XXXX_B$
$003A79_H$	$003B79_H$	003779_H	003879_H				
$003A7A_H$	$003B7A_H$	$00377A_H$	$00387A_H$	DLC register 13	DLCR13	R/W	$----XXXX_B$
$003A7B_H$	$003B7B_H$	$00377B_H$	$00387B_H$				
$003A7C_H$	$003B7C_H$	$00377C_H$	$00387C_H$	DLC register 14	DLCR14	R/W	$----XXXX_B$
$003A7D_H$	$003B7D_H$	$00377D_H$	$00387D_H$				
$003A7E_H$	$003B7E_H$	$00377E_H$	$00387E_H$	DLC register 15	DLCR15	R/W	$----XXXX_B$
$003A7F_H$	$003B7F_H$	$00377F_H$	$00387F_H$				

Table 9-5. List of Message Buffers (Data register)

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
$003A80_H$ to $003A87_H$	$003B80_H$ to $003B87_H$	003780_H to 003787_H	003880_H to 003887_H	Data register 0 (8 bytes)	DTR0	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003A88_H$ to $003A8F_H$	$003B88_H$ to $003B8F_H$	003788_H to $00378F_H$	003888_H to $00388F_H$	Data register 1 (8 bytes)	DTR1	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003A90_H$ to $003A97_H$	$003B90_H$ to $003B97_H$	003790_H to 003797_H	003890_H to 003897_H	Data register 2 (8 bytes)	DTR2	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003A98_H$ to $003A9F_H$	$003B98_H$ to $003B9F_H$	003798_H to $00379F_H$	003898_H to $00389F_H$	Data register 3 (8 bytes)	DTR3	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003AA0_H$ to $003AA7_H$	$003BA0_H$ to $003BA7_H$	$0037A0_H$ to $0037A7_H$	$0038A0_H$ to $0038A7_H$	Data register 4 (8 bytes)	DTR4	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003AA8_H$ to $003AAF_H$	$003BA8_H$ to $003BAF_H$	$0037A8_H$ to $0037AF_H$	$0038A8_H$ to $0038AF_H$	Data register 5 (8 bytes)	DTR5	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003AB0_H$ to $003AB7_H$	$003BB0_H$ to $003BB7_H$	$0037B0_H$ to $0037B7_H$	$0038B0_H$ to $0038B7_H$	Data register 6 (8 bytes)	DTR6	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003AB8_H$ to $003ABF_H$	$003BB8_H$ to $003BBF_H$	$0037B8_H$ to $0037BF_H$	$0038B8_H$ to $0038BF_H$	Data register 7 (8 bytes)	DTR7	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003AC0_H$ to $003AC7_H$	$003BC0_H$ to $003BC7_H$	$0037C0_H$ to $0037C7_H$	$0038C0_H$ to $0038C7_H$	Data register 8 (8 bytes)	DTR8	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003AC8_H$ to $003ACF_H$	$003BC8_H$ to $003BCF_H$	$0037C8_H$ to $0037CF_H$	$0038C8_H$ to $0038CF_H$	Data register 9 (8 bytes)	DTR9	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

Address				Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3				
$003AD0_H$ to $003AD7_H$	$003BD0_H$ to $003BD7_H$	$0037D0_H$ to $0037D7_H$	$0038D0_H$ to $0038D7_H$	Data register 10 (8 bytes)	DTR10	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003AD8_H$ to $003ADF_H$	$003BD8_H$ to $003BDF_H$	$0037D8_H$ to $0037DF_H$	$0038D8_H$ to $0038DF_H$	Data register 11 (8 bytes)	DTR11	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003AE0_H$ to $003AE7_H$	$003BE0_H$ to $003BE7_H$	$0037E0_H$ to $0037E7_H$	$0038E0_H$ to $0038E7_H$	Data register 12 (8 bytes)	DTR12	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003AE8_H$ to $003AEF_H$	$003BE8_H$ to $003BEF_H$	$0037E8_H$ to $0037EF_H$	$0038E8_H$ to $0038EF_H$	Data register 13 (8 bytes)	DTR13	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003AF0_H$ to $003AF7_H$	$003BF0_H$ to $003BF7_H$	$0037F0_H$ to $0037F7_H$	$0038F0_H$ to $0038F7_H$	Data register 14 (8 bytes)	DTR14	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$003AF8_H$ to $003AFF_H$	$003BF8_H$ to $003BFF_H$	$0037F8_H$ to $0037FF_H$	$0038F8_H$ to $0038FF_H$	Data register 15 (8 bytes)	DTR15	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

10. Interrupt Sources, Interrupt Vectors, and Interrupt Control Registers

Interrupt source	EI^{2}OS Corresponding	Interrupt Vector			Interrupt Control Register		Priority *2
		Number		Address	ICR	Address	
Reset	×	#08	08_H	$FFFFDC_H$	—	—	High
INT9 instruction	×	#09	09_H	$FFFFD8_H$	—	—	
Exception processing	×	#10	$0A_H$	$FFFFD4_H$	—	—	
CAN0 received/CAN2 received	×	#11	$0B_H$	$FFFFD0_H$	ICR00	$0000B0_H$*1	
CAN0 transmitted/node status/ CAN2 transmitted/node status	×	#12	$0C_H$	$FFFFCC_H$			
CAN1 received/CAN3 received	×	#13	$0D_H$	$FFFFC8_H$	ICR01	$0000B1_H$*1	
CAN1 transmitted/node status/ CAN3 transmitted/node status/SIO	×	#14	$0E_H$	$FFFFC4_H$			
Input capture 0	△	#15	$0F_H$	$FFFFC0_H$	ICR02	$0000B2_H$*1	
DTP/ external interrupt - ch.0/ch.1 detected	△	#16	10_H	$FFFFBC_H$			
Reload timer 0	△	#17	11_H	$FFFFB8_H$	ICR03	$0000B3_H$*1	
Reload timer 2	△	#18	12_H	$FFFFB4_H$			
Input capture 1	△	#19	13_H	$FFFFB0_H$	ICR04	$0000B4_H$*1	
DTP/ external interrupt - ch.2/ch.3 detected	△	#20	14_H	$FFFFAC_H$			
Input capture 2	△	#21	15_H	$FFFFA8_H$	ICR05	$0000B5_H$*1	
Reload timer 3	△	#22	16_H	$FFFFA4_H$			
Input capture 3/4/5/6/7	△	#23	17_H	$FFFFA0_H$	ICR06	$0000B6_H$*1	
DTP/ external interrupt - ch.4/ ch.5 detected UART3 RX	△	#24	18_H	$FFFF9C_H$			
PPG timer 0	△	#25	19_H	$FFFF98_H$	ICR07	$0000B7_H$*1	
DTP/ external interrupt - ch.6/ ch.7 detected UART3 TX	△	#26	$1A_H$	$FFFF94_H$			
PPG timer 1	△	#27	$1B_H$	$FFFF90_H$	ICR08	$0000B8_H$*1	
Reload timer 1	△	#28	$1C_H$	$FFFF8C_H$			
PPG timer 2/3/4/5	○	#29	$1D_H$	$FFFF88_H$	ICR09	$0000B9_H$*1	
Real time watch timer watch timer (sub clock)	×	#30	$1E_H$	$FFFF84_H$			
Free-run timer overflow/clear	×	#31	$1F_H$	$FFFF80_H$	ICR10	$0000BA_H$*1	
A/D converter conversion complete	○	#32	20_H	$FFFF7C_H$			
Sound generator 0/1	×	#33	21_H	$FFFF78_H$	ICR11	$0000BB_H$*1	
Time-base timer	×	#34	22_H	$FFFF74_H$			
UART2 RX	○	#35	23_H	$FFFF70_H$	ICR12	$0000BC_H$*1	
UART2 TX	△	#36	24_H	$FFFF6C_H$			Low

Interrupt source	EI^{2}OS Corresponding	Interrupt Vector			Interrupt Control Register		Priority *2
		Number		Address	ICR	Address	
UART 1 RX	◎	#37	25_H	$FFFF68_H$	ICR13	$0000BD_H$*1	High
UART 1 TX	△	#38	26_H	$FFFF64_H$			
UART 0 RX	◎	#39	27_H	$FFFF60_H$	ICR14	$0000BE_H$*1	
UART 0 TX	△	#40	28_H	$FFFF5C_H$			
Flash memory status	×	#41	29_H	$FFFF58_H$	ICR15	$0000BF_H$*1	
Delay interrupt generator module	×	#42	$2A_H$	$FFFF54_H$			Low

◎ : Usable, and has expanded intelligent I/O services (EI^{2}OS) stop function
○ : Usable
△ : Usable when interrupt sources sharing ICR are not in use
× : Unusable

*1: • Peripheral functions that share the ICR register have the same interrupt level.
- If the expanded intelligent I/O service (EI^{2}OS) is used with peripheral functions that share the ICR register, only one of the peripheral functions that share the register can be used.
- When the expanded intelligent I/O service (EI^{2}OS) is specified for one of the peripheral functions that shares the ICR register, interrupts cannot be used from the other peripheral functions that share the register.

*2: Priority applies when interrupts of the same level are generated.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	$AV_{CC} = V_{CC}$*2
	AVRH	V_{SS} − 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH*2
	DV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	$DV_{CC} = V_{CC}$*2
Input voltage*1	V_I	V_{SS} − 0.3	V_{CC} + 0.3	V	*3
Output voltage*1	V_O	V_{SS} − 0.3	V_{CC} + 0.3	V	
Maximum clamp current	I_{CLAMP}	− 4	+ 4	mA	*7
Total maximum clamp current	$\Sigma\lvert I_{CLAMP} \rvert$	—	40	mA	*7
“L” level maximum output current*4	I_{OL1}	—	15	mA	Except P70 to P77 and P80 to P87
	I_{OL2}	—	40	mA	P70 to P77 and P80 to P87
“L” level average output current*5	I_{OLAV1}	—	4	mA	Except P70 to P77 and P80 to P87
	I_{OLAV2}	—	30	mA	P70 to P77 and P80 to P87
“L” level maximum total output current	ΣI_{OL1}	—	100	mA	Except P70 to P77 and P80 to P87
	ΣI_{OL2}	—	330	mA	P70 to P77 and P80 to P87
“L” level average total output current	ΣI_{OLAV1}	—	50	mA	Except P70 to P77 and P80 to P87
	ΣI_{OLAV2}	—	250	mA	P70 to P77 and P80 to P87
“H” level maximum output current	I_{OH1}*4	—	−15	mA	Except P70 to P77 and P80 to P87
	I_{OH2}*4	—	−40	mA	P70 to P77 and P80 to P87
“H” level average output current	I_{OHAV1}*5	—	−4	mA	Except P70 to P77 and P80 to P87
	I_{OHAV2}*5	—	−30	mA	P70 to P77 and P80 to P87
“H” level maximum total output current	ΣI_{OH1}	—	−100	mA	Except P70 to P77 and P80 to P87
	ΣI_{OH2}	—	−330	mA	P70 to P77 and P80 to P87
“H” level average total output current	ΣI_{OHAV1}*6	—	−50	mA	Except P70 to P77 and P80 to P87
	ΣI_{OHAV2}*6	—	−250	mA	P70 to P77 and P80 to P87
Power consumption	P_D	—	625	mW	
Operating temperature	T_A	− 40	+ 105	°C	
Storage temperature	T_{STG}	− 55	+ 150	°C	

*1 : The parameter is based on $V_{SS} = AV_{SS} = DV_{SS} = 0.0$ V.

*2 : AV_{CC}, AVRH must not exceed V_{CC}, and AVRH must not exceed AV_{CC}.
When using an evaluation product, DV_{CC} must not exceed V_{CC} (however, DV_{CC} can be set to a higher voltage than V_{CC} when using a Flash memory product).

*3 : If the input current or the maximum input current is limited using external components, I_{CLAMP} is the applicable rating instead of V_I.

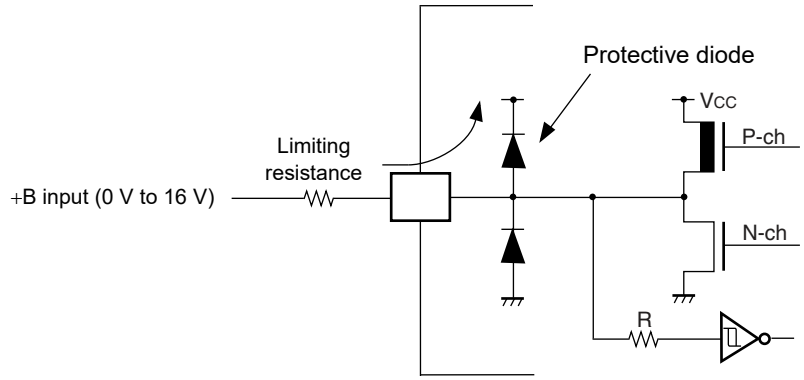
*4 : Maximum output current is defined as the peak value of current through any one of the corresponding pins.

*5 : Average output current is defined as the average value of the current flowing through any one of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.

*6 : Average total output current is defined as the average value of the current flowing through all of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.

*7 : • Applicable to pins: P10 to P15,P50 to P57,P60 to P67,P70 to P77,P80 to P87,PC0 to PC7,PD0 to PD6, PE0 to PE2
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the microcontroller may partially malfunction on power supplied through the +B signal pin.
- Note that if the +B input is applied during power-on, the power supply voltage may reach a level such that the power-on reset does not function due to the power supplied from the +B signal.
- Care must be taken not to leave +B input pins open.
- Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal inputs.
- Sample recommended circuit :

■ Input/output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

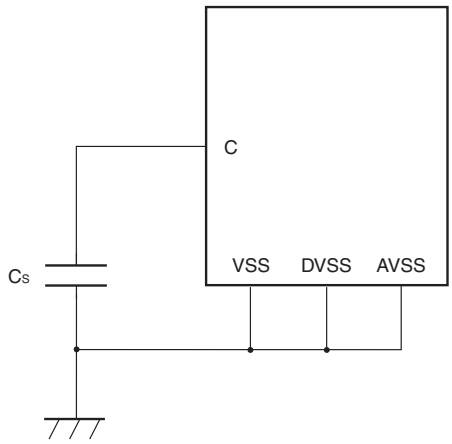
11.2 Recommended Operating Conditions

(V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC} DV_{CC}	4.0	5.5	V	The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V.
		4.4	5.5	V	Maintain stop operation status The low voltage detection reset operates when the power supply voltage reaches 4.2 V ± 0.2 V.
Smoothing capacitor*	C_S	0.1	1.0	µF	Use a ceramic capacitor or other capacitor of equivalent frequency characteristics. Use a capacitor with a capacitance greater than this capacitor as the bypass capacitor for the V_{CC} pin.
Operating temperature	T_A	− 40	+ 105	°C	

*: Refer to the following diagram for details on the connection of the smoothing capacitor C_S.

■ C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.
Users considering application outside the listed conditions are advised to contact their representatives beforehand.

11.3 DC Characteristics

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHA}	—	—	0.8 V_{CC}	—	—	V	Pin inputs if Automotive input levels are selected
	V_{IHS}	—	—	0.8 V_{CC}	—	—	V	Pin inputs if CMOS hysteresis input levels are selected
	V_{IHC}	—	—	0.7 V_{CC}	—	—	V	$\overline{RST}$ input pin (CMOS hysteresis)
"L" level input voltage	V_{ILA}	—	—	—	—	0.5 V_{CC}	V	Pin inputs if Automotive input levels are selected
	V_{ILS}	—	—	—	—	0.2 V_{CC}	V	Pin inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	—	—	0.3 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	Maximum operating frequency F_{CP} = 32 MHz, normal operation	—	35	45	mA	
			Maximum operating frequency F_{CP} = 32 MHz, writing Flash memory	—	55	65	mA	
	I_{CCS}		Operating frequency F_{CP} = 32 MHz, sleep mode	—	13	20	mA	
	I_{CTS}		Operating frequency F_{CP} = 2 MHz, time-base timer mode	—	0.6	1.0	mA	
	I_{CTSPLL}		Operating frequency F_{CP} = 32 MHz, PLL timer mode, External frequency = 4 MHz	—	2.5	4	mA	
	I_{CCL}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, sub clock operation	—	120	270	µA	
	I_{CCLS}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, sub sleep operation	—	100	200	µA	
	I_{CCT}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, watch mode	—	90	180	µA	
	I_{CCH}		T_A = + 25 °C, stop mode	—	80	170	µA	
Input leakage current	I_{IL}	All input pins	V_{CC} = DV_{CC} = AV_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	—	—	10	µA	
Input capacitance 1	C_{IN1}	All pins except VCC, VSS, DVCC, DVSS, AVCC, AVSS, C, P70 to P77, P80 to P87	—	—	—	15	pF	
Input capacitance 2	C_{IN2}	P70 to P77, P80 to P87	—	—	—	45	pF	
Pull-up resistance	R_{UP}	RST	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	—	—	100	kΩ	Excluding Flash memory product
General-purpose output “H” voltage	V_{OH1}	All pins except P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Stepping motor output “H” voltage	V_{OH2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OH} = –30.0 mA	V_{CC} – 0.5	—	—	V	
General-purpose output “L” voltage	V_{OL1}	All pins except P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Stepping motor output “L” voltage	V_{OL2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V, I_{OL} = 30.0 mA	—	—	0.55	V	
Stepping motor output phase variation “H”	ΔV_{OH}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V_{CC} = 4.5 V, I_{OH} = −30.0 mA, maximum deviation V_{OH2}	—	—	90	mV	
Stepping motor output phase variation “L”	ΔV_{OL}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V_{CC} = 4.5 V, I_{OL} = 30.0 mA, maximum deviation V_{OH2}	—	—	90	mV	
LCD internal divider resistance	R_{LCD}	Between V0 and V1, Between V1 and V2, Between V2 and V3	—	50	100	200	kΩ	Evaluation product
				8.75	12.5	17.0	kΩ	Flash memory product
LCDC leakage current	I_{LCDC}	V0 to V3, COMm (m = 0 to 3) , SEGn, (n = 00 to 31)	—	—	—	5.0	μA	
LCD output impedance	Rvcom	COMn (n = 0 to 3)	—	—	—	4.5	kΩ	
	Rvseg	SEGn (n = 00 to 31)	—	—	—	17	kΩ	

*: Power supply current values assume an external clock supplied to the X1 pin and X1A pin. Users must be aware that power supply current levels differ depending on whether an external clock or oscillator is used.

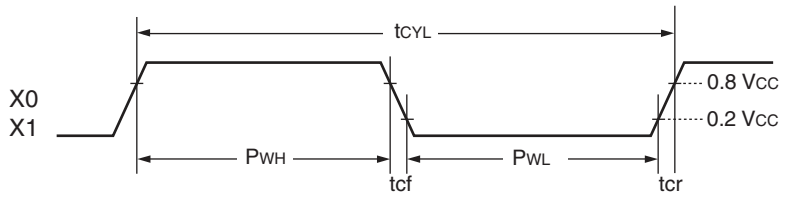
11.4 AC Characteristics

11.4.1 Clock Timing

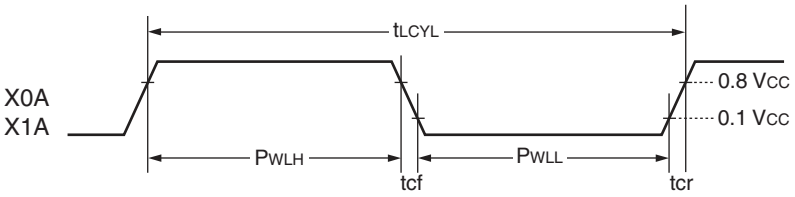
(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Condi-tions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_C	X0, X1	—	3	—	16	MHz	1/2 (PLL stopped) When using the oscillator circuit
				3	—	32	MHz	1/2 (PLL stopped) When using an external clock
				4	—	32	MHz	PLL multiplied by 1
				3	—	16	MHz	PLL multiplied by 2
				3	—	10.7	MHz	PLL multiplied by 3
				3	—	8	MHz	PLL multiplied by 4
				3	—	5.33	MHz	PLL multiplied by 6
				3	—	4	MHz	PLL multiplied by 8
	F_{LC}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{CYL}	X0, X1		62.5	—	333	ns	When using an oscillator
				31.25	—	333	ns	External clock input
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0		5	—	—	ns	Use duty ratio of 50% ± 3% as a guideline
	P_{WLH}, P_{WLL}	X0A		—	15.2	—	µs	
Input clock rise and fall time	tcr, tcf	X0		—	—	5	ns	When using an external clock signal
Internal operating clock frequency	F_{CP}	—		1.5	—	32	MHz	Using main clock (PLL clock)
	F_{LCP}	—		—	8.192	—	kHz	Using sub clock
Internal operating clock cycle time	t_{CP}	—		31.25	—	666	ns	Using main clock (PLL clock)
	t_{LCP}	—		—	122.1	—	µs	Using sub clock

■ X0, X1 clock timing

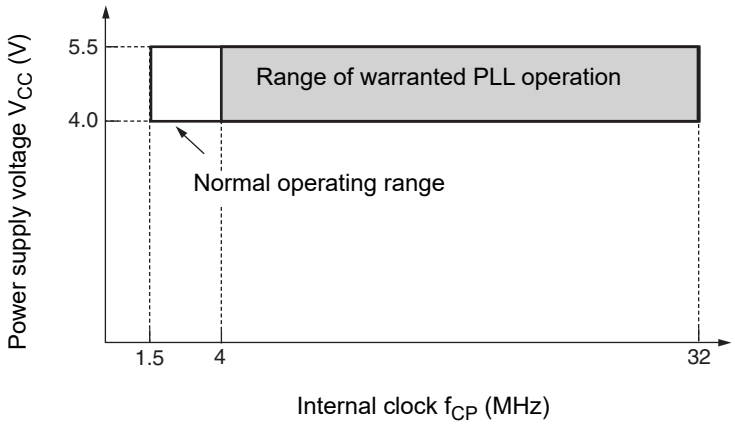


■ X0A, X1A clock timing



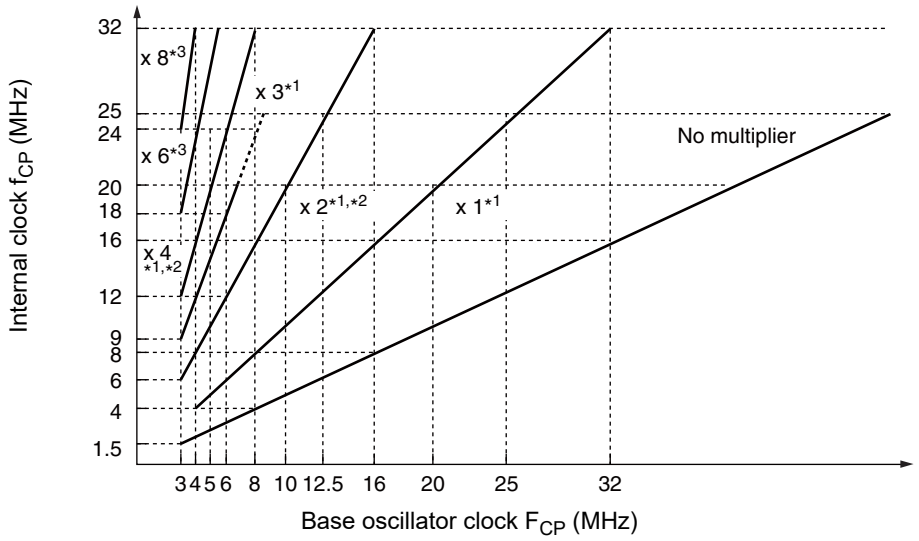
■ Guaranteed PLL Operation Range

Internal operating clock frequency vs. Power supply voltage



Notes:
- For PLL 1 × only, use with tcp = 4 MHz or greater.
- Refer to Electrical Characteristics on page 55 of A/D Converter for details on the A/D converter operating frequency.

Base oscillator frequency vs. Internal operating clock frequency



*1: When the PLL multiplier is × 1, × 2, × 3 or × 4 and the internal clock is 20 MHz < f_{CP} ≤ 32 MHz, set DIV2 bit = "1"*4, CS2 bit = "1" in the PSCCR register.
[Example]When using a base oscillator frequency of 24 MHz at PLL × 1:
CKSCR register: CS1 bit = "0", CS0 bit = "0"
PSCCR register: DIV2 bit = "1"*4,CS2 bit = "1"
[Example]When using a base oscillator frequency of 6 MHz at PLL × 3:
CKSCR register: CS1 bit = "1", CS0 bit = "0"
PSCCR register: DIV2 bit = "1"*4, CS2 bit = "1"

*2: When the PLL multiplier is × 2 or × 4 and the internal clock is 20 MHz < f_{CP} ≤ 32 MHz, the following settings are also supported.
PLL × 2: CKSCR register: CS1 bit = "0", CS0 bit = "0"
PSCCR register: DIV2 bit = "0"*4, CS2 bit = "0"
PLL × 4: CKSCR register: CS1 bit = "0", CS0 bit = "1"
PSCCR register: DIV2 bit = "0"*4, CS2 bit = "0"

*3: When the PLL multiplier is set to × 6 or × 8 set "DIV2 bit = "0"*4 CS2 bit = "1" and "PLL2 bit = 1" in the PSCCR register.
[Example]When using a base oscillator frequency of 4 MHz at PLL × 6:
CKSCR register: CS1 bit = "1", CS0 bit = "0"
PLLOS register: DIV2 bit = "0"*4, CS2 bit = "1"
[Example]When using a base oscillator frequency of 3 MHz at PLL × 8:
CKSCR register: CS1 bit = "1", CS0 bit = "1"
PLLOS register: DIV2 bit = "0"*4, CS2 bit = "1"

*4: The DIV2 bit is assigned to bit 9 of the PSCCR register and the CS2 bit is assigned to bit 8 of the PSCCR register. Both bits have a default value of "0".

11.4.2 Reset Input

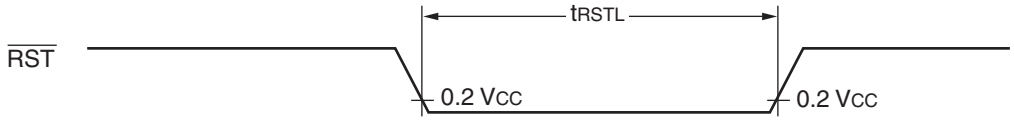
(V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	RST	500	—	ns	During normal operation
			Oscillator oscillation time* + 16 t_{CP}	—	ms	In stop mode, sub clock mode, sub sleep mode, and watch mode
			100	—	µs	In time-base timer mode

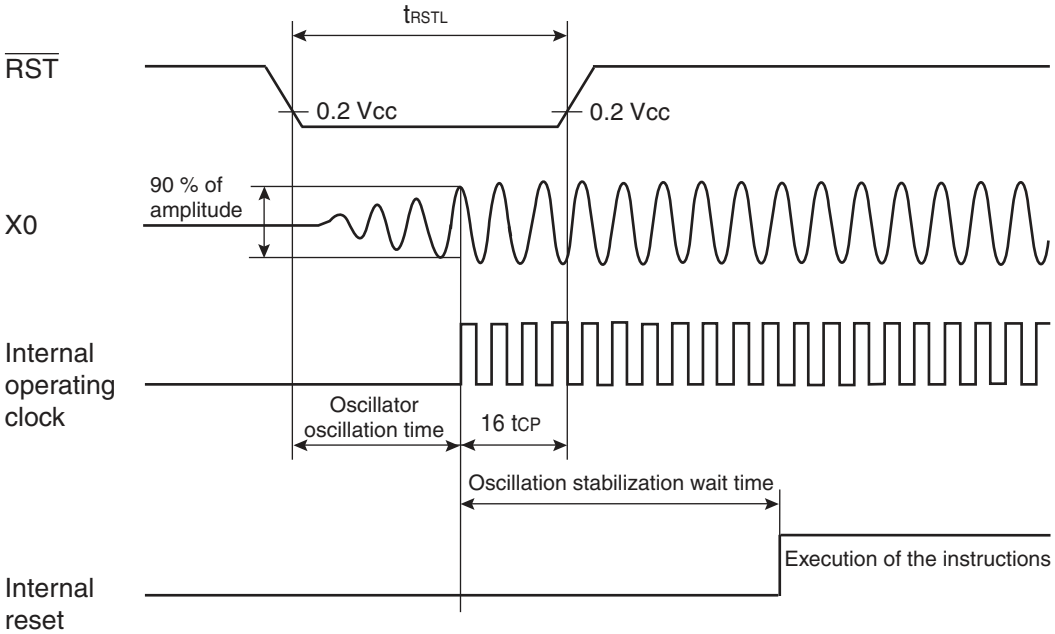
*: The oscillation time of the oscillator is the time taken to reach 90% of the amplitude. The oscillation time of a crystal oscillator is between several ms and tens of ms. The oscillation time of a ceramic oscillator is between hundreds of µs and several ms. The oscillation time of an external clock is 0 ms.

Note: t_{CP} is the internal operating clock cycle time. (Unit: ns)

■ During normal operation



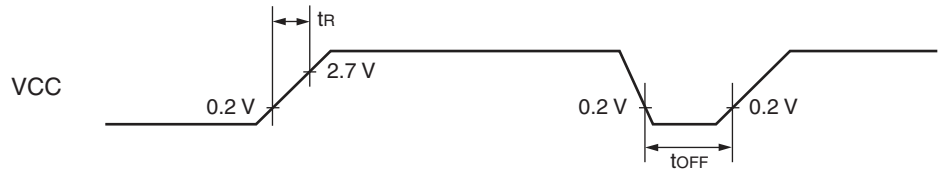
■ In stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



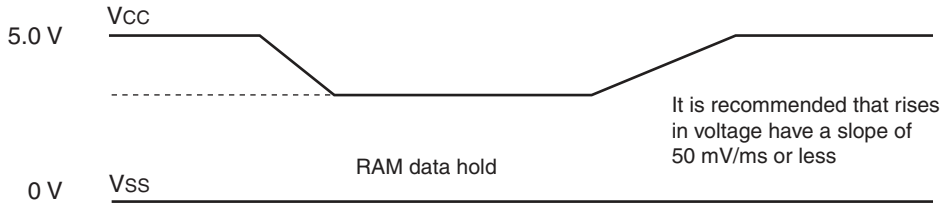
11.4.3 Power-On Reset

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	VCC	—	0.05	30	ms	
Power off time	t_{OFF}			1	—	ms	Waiting time until power-on



Note: Extreme variations in power supply voltage may trigger a power-on reset. When the power supply voltage is changed during operation, it is recommended that increases in the voltage smoothed out as shown in the following diagram. The PLL clock of the device should not be in use when varying the voltage. However, the PLL clock may continue to be used if the rate of the voltage drop is 1 V/s or less.



11.4.4 UART0/1/2/3 (LIN/SCI)

■ Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=0

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

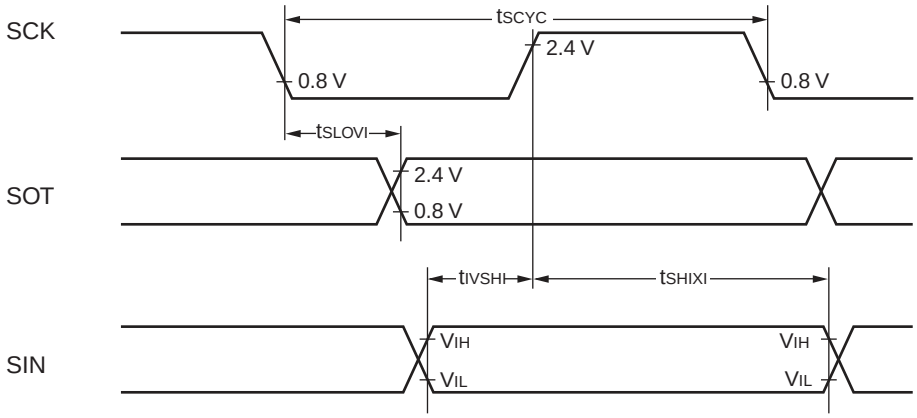
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		− 50	+ 50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}			0	—	ns

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

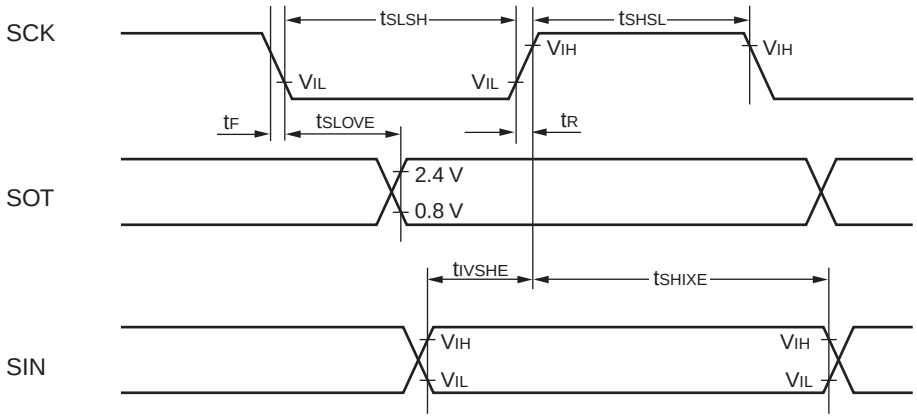
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK3	External shift clock mode output pin C_L = 80 pF + 1TTL	3 t_{CP} − t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}			t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}			t_{CP} + 30	—	ns
SCK ↓ time	t_F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t_R			—	10	ns

Notes:
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “CY90920 series hardware manual”.
- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to Clock Timing.

■ Internal shift clock mode



■ External shift clock mode



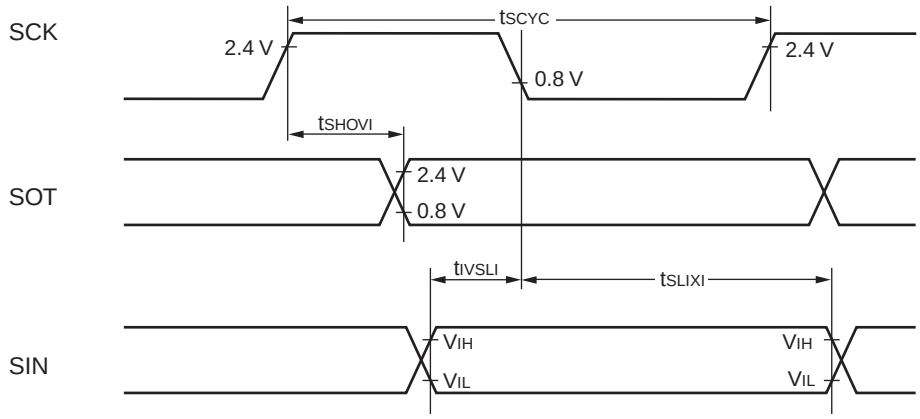
■ Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=0

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to +105 °C)

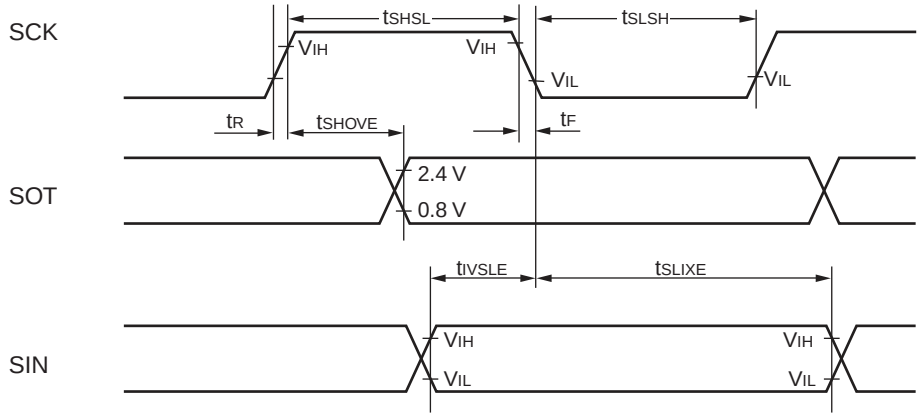
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		− 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}			0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pin C_L = 80 pF + 1TTL	3 t_{CP} − t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}			t_{CP} + 10	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXE}			t_{CP} + 30	—	ns
SCK ↓ time	t_F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t_R			—	10	ns

Notes:
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “CY90920 series hardware manual”.
- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to Clock Timing.

■ Internal shift clock mode



■ External shift clock mode

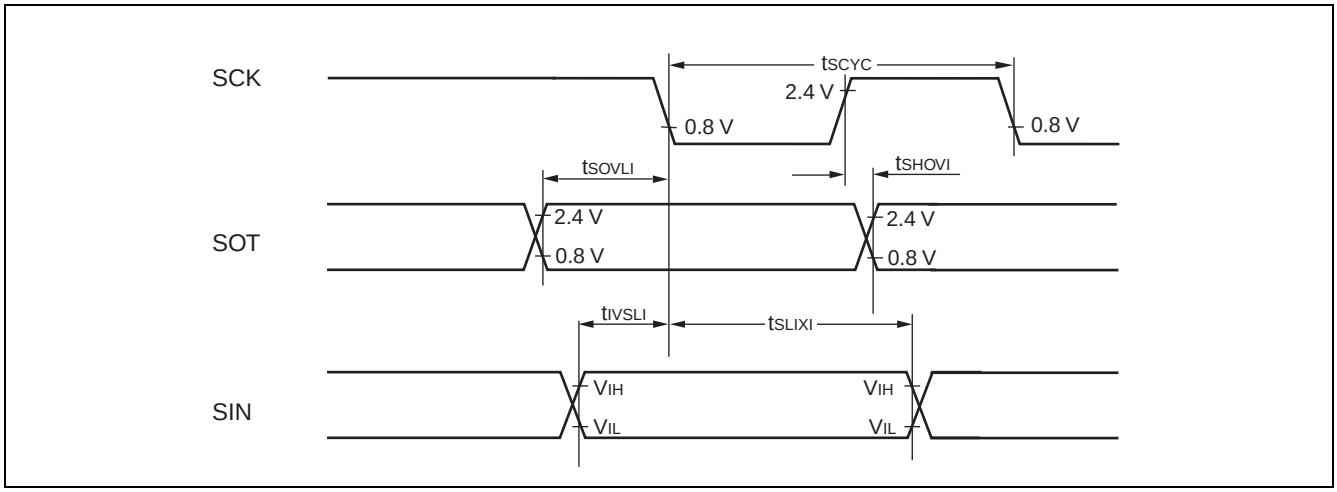


■ Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=1

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}			0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} – 70	—	ns

Notes:
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “CY90920 series hardware manual”.
- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to Clock Timing.

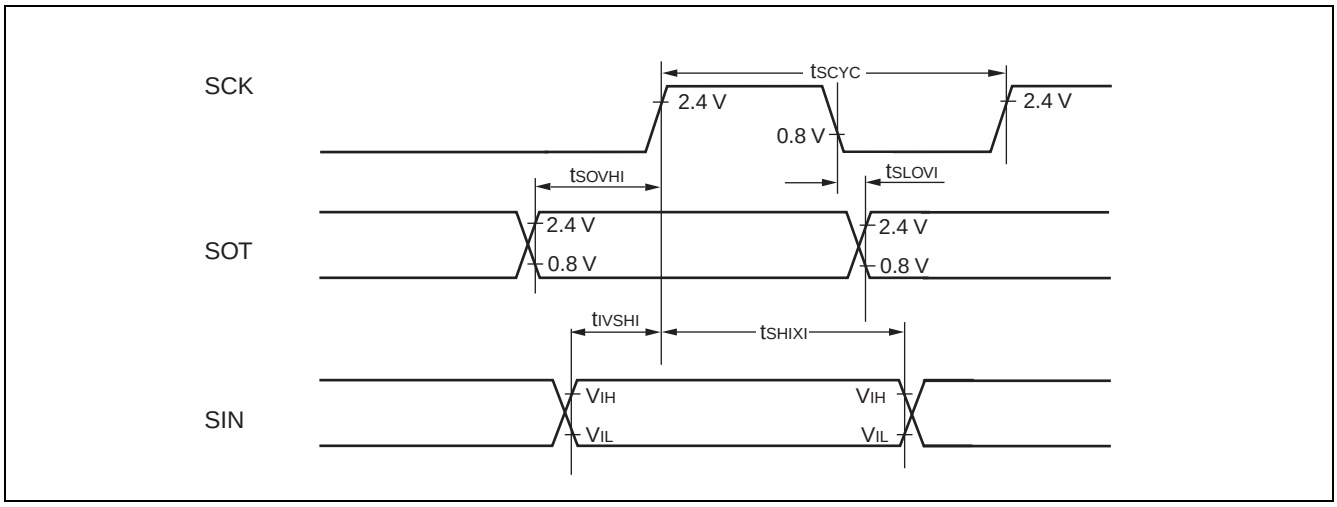


■ Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=1

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}			0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} – 70	—	ns

Notes:
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “CY90920 series hardware manual”.
- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to Clock Timing.



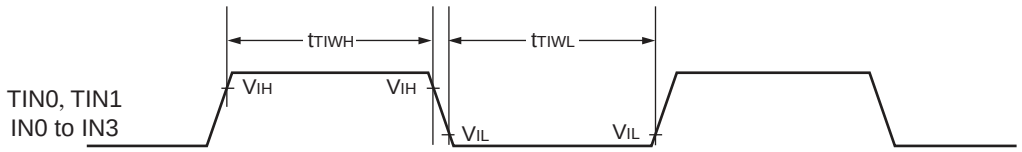
11.4.5 Timer Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0, TIN1, IN0 to IN3	—	4 t_{CP}	—	ns

Note: t_{CP} is the internal operating clock cycle time. Refer to Clock Timing.

■ Timer input timing



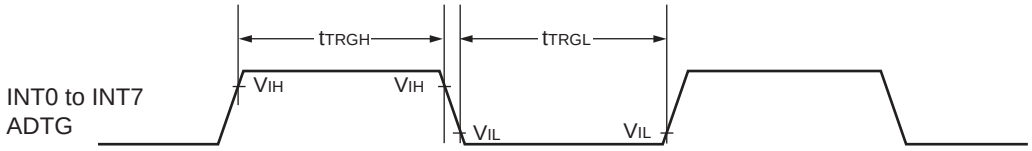
11.4.6 Trigger Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT7	—	200	—	ns	During normal operation
		ADTG	—	t_{CP} + 200	—	ns	

Note: t_{CP} is the internal operating clock cycle time. Refer to Clock Timing.

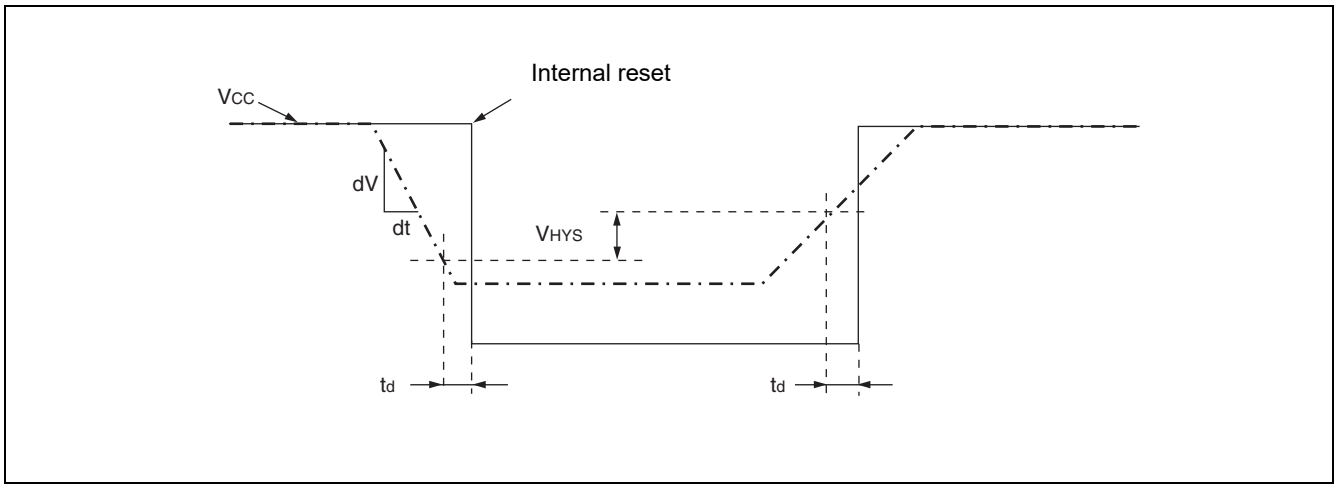
■ Trigger input timing



11.4.7 Low Voltage Detection

(V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Detection voltage	V_{DL}	VCC	—	4.0	4.2	4.4	V	Flash memory product, during voltage drop
				3.7	4.0	4.3	V	Evaluation product, during voltage drop
Hysteresis width	V_{HYS}	VCC	—	190	—	—	mV	Flash memory product, during voltage rise
				0.1	—	—	V	Evaluation product, during voltage rise
Power supply voltage change rate	dV/dt	VCC	—	– 0.1	—	+ 0.1	V/µs	Flash memory product, dV/dt at low voltage reset
				–0.004	—	+ 0.004	V/µs	Flash memory product, dV/dt at standard value of low voltage detection/release voltage
				– 0.1	—	+ 0.02	V/µs	Evaluation product
Detection delay time	td	—	—	—	—	3.2	µs	Flash memory product, when dV/dt ≤ 0.004 V/µs
				—	—	35	µs	Evaluation product



11.5 A/D Converter

11.5.1 Electrical Characteristics

(V_{CC} = AV_{CC} = AVRH = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	– 3.0	—	+ 3.0	LSB	
Non-linear error	—	—	– 2.5	—	+ 2.5	LSB	
Differential linear error	—	—	– 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVRH – AV_{SS}) / 1024
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V	
Sampling time	t_{SMP}	—	0.4	—	16500	µs	4.5 V ≤ AVcc ≤ 5.5 V
			1.0				4.0 V ≤ AVcc ≤ 4.5 V
Compare time	t_{CMP}	—	0.66	—	—	µs	4.5 V ≤ AVcc ≤ 5.5 V
			2.2				4.0 V ≤ AVcc ≤ 4.5 V
A/D conversion time	t_{CNV}	—	1.44	—	—	µs	*1
Analog port input current	I_{AIN}	AN0 to AN7	– 0.3	—	+ 10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	0	—	AVRH	V	
Reference voltage	AV+	AVRH	AVss + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	2.3	6.0	mA	
	I_{AH}		—	—	5	µA	*2
Reference voltage supply current	I_R	AVRH	—	520	900	µA	V_{AVRH} = 5.0 V
	I_{RH}		—	—	5	µA	*2
Inter-channel variation	—	AN0 to AN7	—	—	4	LSB	

*1: The time per channel (4.5 V ≤ AV_{CC} ≤ 5.5 V, and internal operating frequency = 32 MHz) .

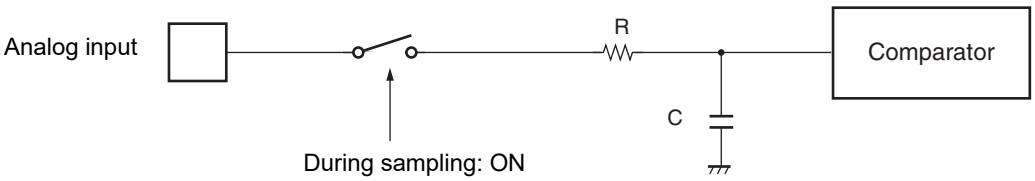
*2: Defined as supply current (when V_{CC} = AV_{CC} = AVRH = 5.0 V) with A/D converter not operating, and CPU in stop mode.

■ Notes on the external impedance and sampling time of analog inputs

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

If the sampling time is still not sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

■ Analog input equivalent circuit



CY90F922NC/F922NCS/ F923NC/F923NCS/F924NC/F924NCS
CY90922NCS

	R	C
4.5 V ≤ AVcc ≤ 5.5 V:	2.6 kΩ (Max)	8.5 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V:	12.1 kΩ (Max)	8.5 pF (Max)

CY90V920-101/102

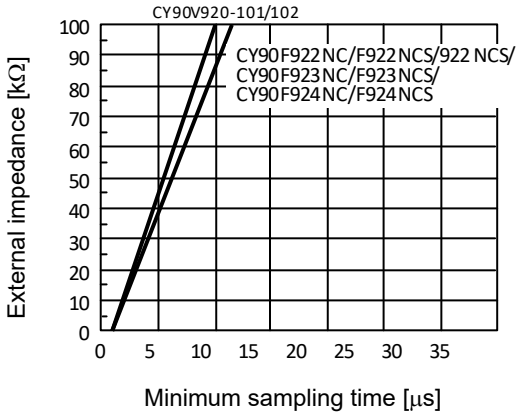
4.5 V ≤ AVcc ≤ 5.5 V:	2.0 kΩ (Max)	14.4 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V:	8.2 kΩ (Max)	14.4 pF (Max)

Note: The values are reference values.

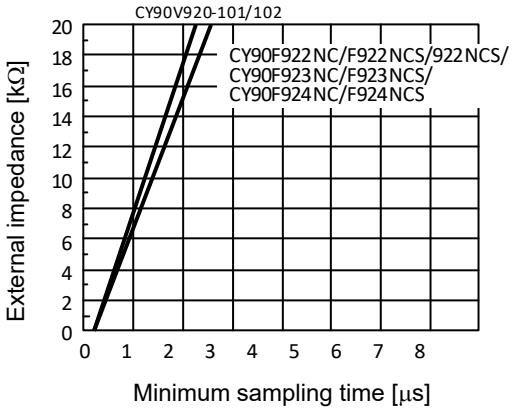
■ The relationship between the external impedance and minimum sampling time

■ At 4.5 V ≤ AVcc ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)

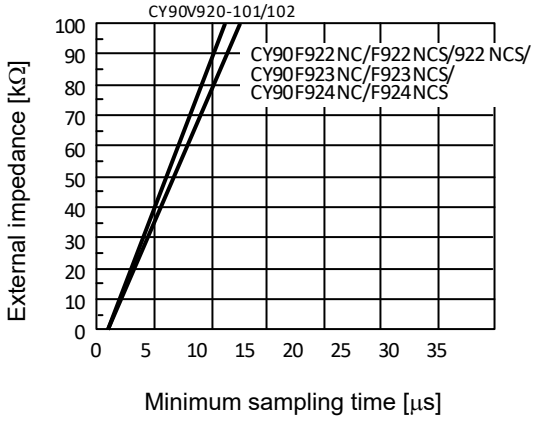


(External impedance = 0 kΩ to 20 kΩ)

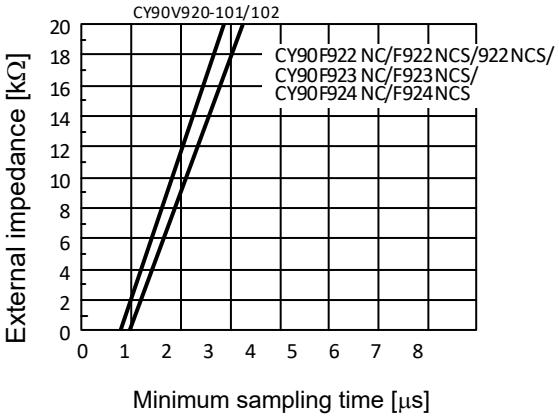


■ At 4.0 V ≤ AVcc ≤ 4.5 V

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)

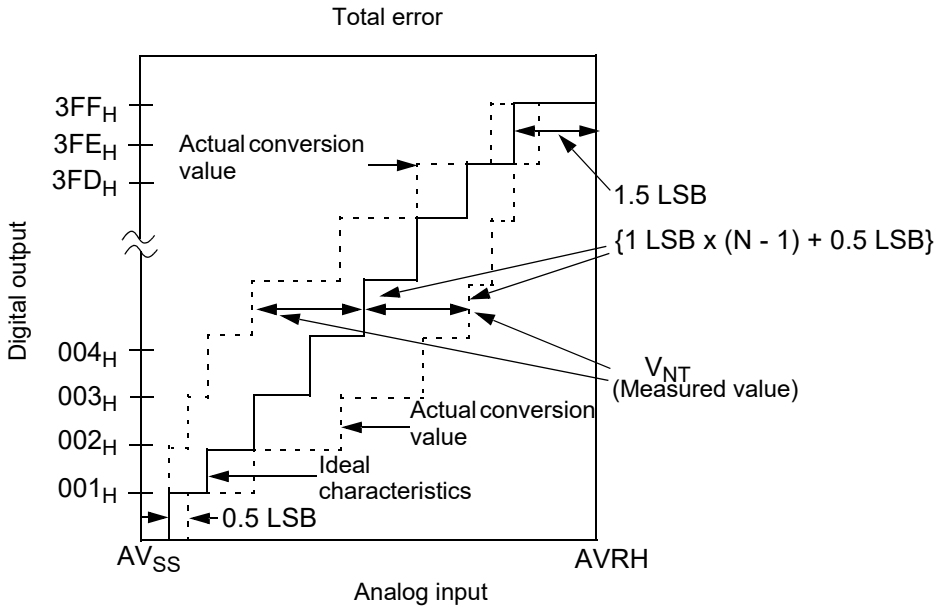


■ About errors

As $|AVRH - AV_{SS}|$ becomes smaller, the relative errors grow larger.

11.5.2 Definition of Terms

Resolution:	Analog changes that are identifiable by the A/D converter.
Non-Linear error:	The deviation of the straight line connecting the zero transition point ("00 0000 0000" ⟷ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ⟷ "11 1111 1111") from actual conversion characteristics.
Differential linear error:	The deviation from the ideal value of the input voltage needed to change the output code by 1 LSB.
Total error:	The total error is the difference between the actual value and the theoretical value, and includes zero-transition error/full-scale transition error and linear error.



$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

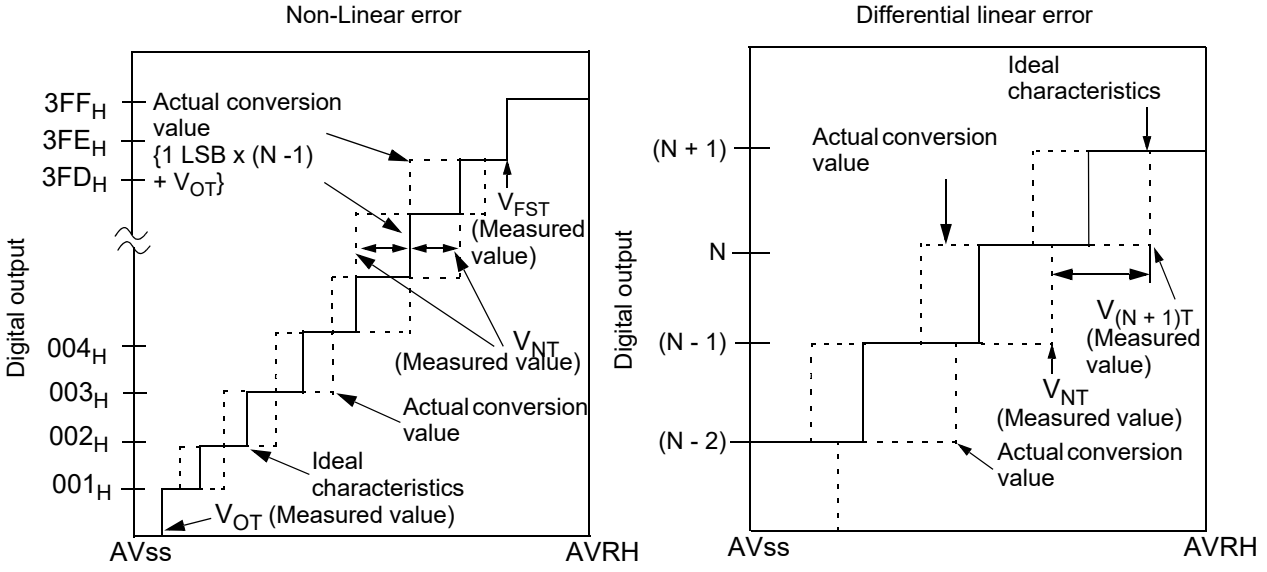
$$1\ \text{LSB (Ideal)} = \frac{\text{AVRH} - \text{AV}_{SS}}{1024}\ [\text{V}]$$

N: A/D converter digital output value

V_{OT} (Ideal) = AVss + 0.5 LSB [V]

V_{FST} (Ideal) = AVRH − 1.5 LSB [V]

V_{NT}: Voltage when the digital output changes from (N - 1) to N



$$\text{Non-linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N: A/D converter digital output value
V_{OT}: Voltage when digital output changes from 000_H to 001_H
V_{FST}: Voltage when digital output changes from $3FE_H$ to $3FF_H$

11.6 Flash Memory Program/Erase Characteristics

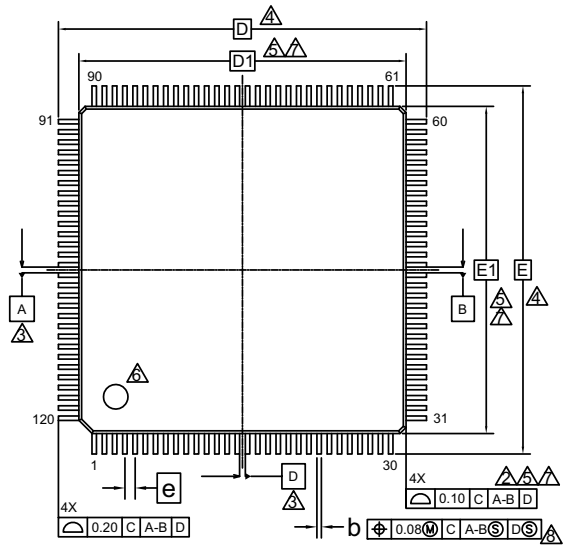
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C V_{CC} = 5.0 V	—	0.9	3.6	s	Excludes pre-programming before erase
Word (16-bit width) programming time		—	23	370	µs	Excludes system-level overhead
Chip programming time	T_A = + 25 °C, V_{CC} = 5.0 V	—	3.4	55	s	
Erase/program cycle	—	10000	—	—	cycle	
Flash memory data retention time	Average T_A = + 85 °C	20	—	—	year	*

*: This value is calculated from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

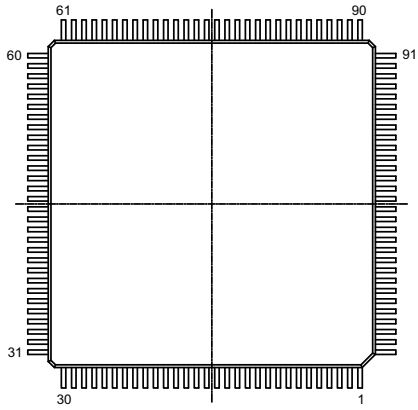
12. Ordering Information

Part Number	Package	Remarks
CY90922NCSPMC-GSE1 CY90F922NCSPMC-GS-UJE1	120-pin plastic LQFP (LQM120)	

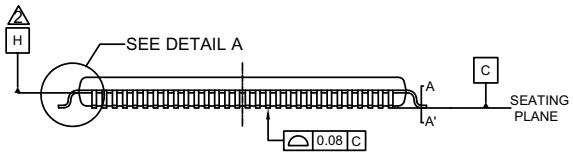
13. Package Dimension



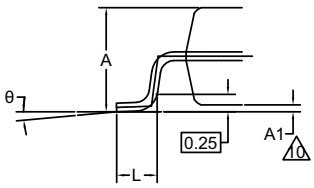
TOP VIEW



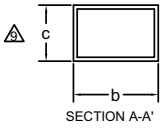
BOTTOM VIEW



SIDE VIEW



DETAIL A



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D		18.00 BSC	
D1		16.00 BSC	
e		0.50 BSC	
E		18.00 BSC	
E1		16.00 BSC	
L	0.45	0.60	0.75
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

002-16172 **

14. Major Changes

Spansion Publication Number: DS07-13750-4E

Page	Section	Change Results
12	■I/O CIRCUIT TYPE	Corrected the circuit type B.
20	■ HANDLING DEVICES	Added the following items; ■ Serial communication ■ Characteristic difference between flash device and MASK ROM device
31	■ I/O MAP	Corrected “Address: 003970_H”. Clock supervisor control register → (Disabled)
46	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics	Added the item for “LCD output impedance”.
68	■ ORDERING INFORMATION	Corrected the part numbers; MB90V920-101 → MB90V920-101CR MB90V920-102 → MB90V920-102CR
Rev.*A		
	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
4, 60, 61	2. Pin Assignments 12. Ordering Information 13. Package Dimension	Package description modified to JEDEC description. (before) FPT-120P-M21 (after) LQM120
60	12. Ordering Information	Deleted the following parts number. - MB90F922NCPMC - MB90F922NCSPMC - MB90922NCSPMC - MB90F923NCPMC - MB90F923NCSPMC - MB90F924NCPMC - MB90F924NCSPMC - MB90V920-101CR - MB90V920-102CR (for evaluation) Revised the following parts number. (before) - MB90922NCSPMC - MB90F922NCSPMC (after) - CY90922NCSPMC-GSE1 - CY90F922NCSPMC-GS-UJE1

NOTE: Please see “Document History” for later revised information.

Document History

Document Title: CY90F922NC/F922NCS/922NCS, CY90F923NC/F923NCS/F924NC, CY90F924NCS/V920-101/102, F²MC-16LX CY90920 Series Document Number: 002-07917				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	TORS	09/17/2010	Migrated to Cypress and assigned document number 002-07917. No change to document contents or format.
*A	6483925	GSHI	02/13/2019	Updated to Cypress template. Revised the following items: - Changed marketing part numbers from prefix MB to CY. - Updated package code as LQM120 on 2. Pin Assignments and 13. Package Dimension For details, please see 14.Major Changes

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