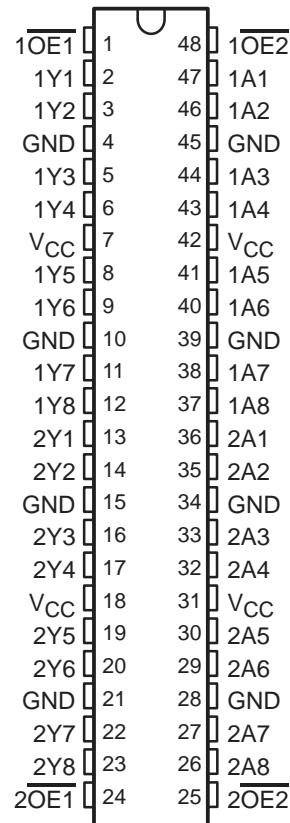


SN54AHC16540, SN74AHC16540 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS331F – MARCH 1996 – REVISED JANUARY 2000

- **Members of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V V_{CC}**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHC16540 . . . WD PACKAGE
SN74AHC16540 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

These 16-bit buffers and bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHC16540 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHC16540 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit buffer/driver)

| INPUTS | | | OUTPUT Y |
|------------------|------------------|---|-------------|
| $\overline{OE1}$ | $\overline{OE2}$ | A | |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |



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 **TEXAS
INSTRUMENTS**

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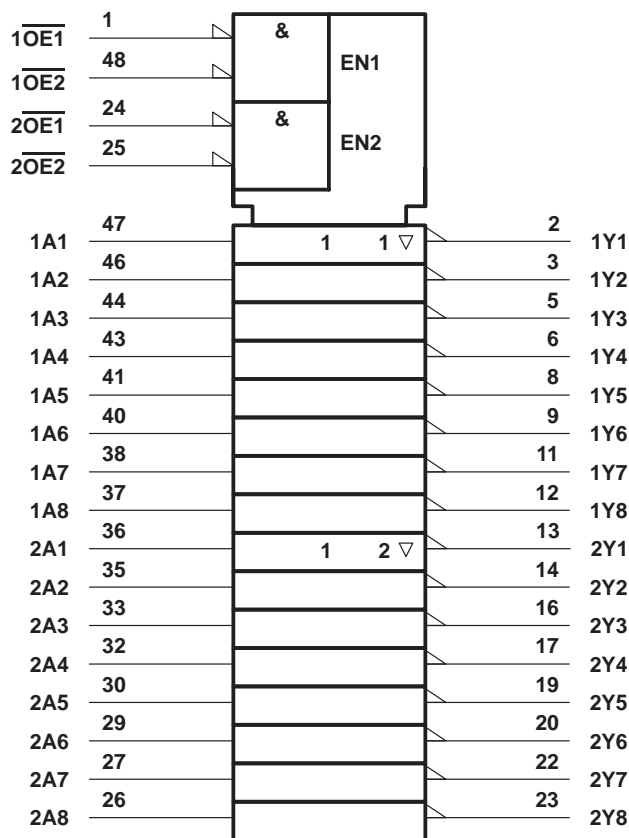
SN54AHC16540, SN74AHC16540

16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

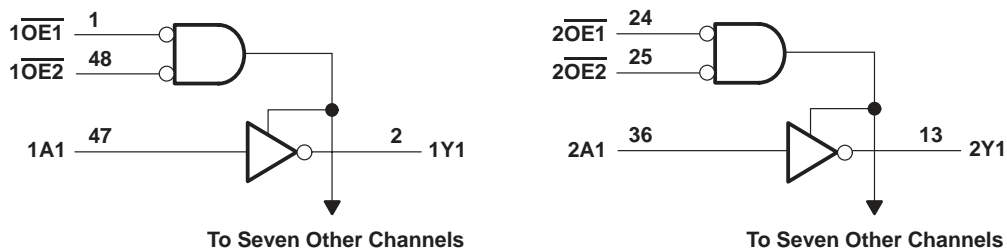
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54AHC16540, SN74AHC16540 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Output voltage range, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through each V_{CC} or GND | ±75 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DGG package | 70°C/W |
| DGV package | 58°C/W |
| DL package | 63°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

| | | SN54AHC16540 | | SN74AHC16540 | | UNIT |
|---------------------|------------------------------------|--------------------------|----------|--------------|----------|---------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 2 | 5.5 | 2 | 5.5 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | | 1.5 | | V |
| | | $V_{CC} = 3$ V | | 2.1 | | |
| | | $V_{CC} = 5.5$ V | | 3.85 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | 0.5 | | V |
| | | $V_{CC} = 3$ V | | 0.9 | | |
| | | $V_{CC} = 5.5$ V | | 1.65 | | |
| V_I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V_O | Output voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 2$ V | | –50 | | μ A |
| | | $V_{CC} = 3.3$ V ± 0.3 V | | –4 | | mA |
| | | $V_{CC} = 5$ V ± 0.5 V | | –8 | | mA |
| I_{OL} | Low-level output current | $V_{CC} = 2$ V | | 50 | | μ A |
| | | $V_{CC} = 3.3$ V ± 0.3 V | | 4 | | mA |
| | | $V_{CC} = 5$ V ± 0.5 V | | 8 | | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 3.3$ V ± 0.3 V | | 100 | | ns/V |
| | | $V_{CC} = 5$ V ± 0.5 V | | 20 | | |
| T_A | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54AHC16540, SN74AHC16540

16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54AHC16540 | | SN74AHC16540 | | UNIT |
|-----------------|--|-----------------|-----------------------|-----|-------|--------------|------|--------------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | V | |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | I _{OH} = -4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | I _{OH} = -8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| V _{OL} | I _{OL} = 50 μA | 2 V | | | 0.1 | | 0.1 | | V | |
| | | 3 V | | | 0.1 | | 0.1 | | | |
| | | 4.5 V | | | 0.1 | | 0.1 | | | |
| | I _{OL} = 4 mA | 3 V | | | 0.36 | | 0.5 | | | 0.44 |
| | I _{OL} = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | | 0.44 |
| I _I | V _I = V _{CC} or GND | 0 V to 5.5 V | | | ±0.1 | | ±1* | | ±1 | μA |
| I _{OZ} | V _O = V _{CC} or GND, V _I (OE) = V _{IL} or V _{IH} | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| C _i | V _I = V _{CC} or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| C _o | V _O = V _{CC} or GND | 5 V | | 3 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54AHC16540 | | SN74AHC16540 | | UNIT |
|--------------------|------------------------|-------------|------------------------|-----------------------|-------|--------|--------------|--------|--------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A | Y | C _L = 15 pF | | 4.8** | 8.4** | 1** | 10** | 1 | 10 | ns |
| t _{PHL} | | | | | | | | | | | |
| t _{PZH} | $\overline{\text{OE}}$ | Y | C _L = 15 pF | | 6.8** | 10.6** | 1** | 12.5** | 1 | 12.5 | ns |
| t _{PZL} | | | | | | | | | | | |
| t _{PHZ} | $\overline{\text{OE}}$ | Y | C _L = 15 pF | | 6.8** | 11.5** | 1** | 12.5** | 1 | 12.5 | ns |
| t _{PLZ} | | | | | | | | | | | |
| t _{PLH} | A | Y | C _L = 50 pF | | 7.7 | 11 | 1 | 12.5 | 1 | 12.5 | ns |
| t _{PHL} | | | | | | | | | | | |
| t _{PZH} | $\overline{\text{OE}}$ | Y | C _L = 50 pF | | 9.7 | 14.1 | 1 | 16 | 1 | 16 | ns |
| t _{PZL} | | | | | | | | | | | |
| t _{PHZ} | $\overline{\text{OE}}$ | Y | C _L = 50 pF | | 9.4 | 14 | 1 | 16 | 1 | 16 | ns |
| t _{PLZ} | | | | | | | | | | | |
| t _{sk(o)} | | | C _L = 50 pF | | | 1.5*** | | | | 1.5 | ns |

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

*** On products compliant to MIL-PRF-38535, this parameter does not apply.

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SN54AHC16540, SN74AHC16540 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54AHC16540 | | SN74AHC16540 | | UNIT |
|--------------------|-----------------|-------------|------------------------|-----------------------|------|-----|--------------|-----|--------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A | Y | C _L = 15 pF | 3.7* | 6* | 1* | 7* | 1 | 7 | ns | |
| t _{PHL} | | | | 3.7* | 6* | 1* | 7* | 1 | 7 | | |
| t _{PZH} | \overline{OE} | Y | C _L = 15 pF | 4.7* | 7.3* | 1* | 8.5* | 1 | 8.5 | ns | |
| t _{PZL} | | | | 4.7* | 7.3* | 1* | 8.5* | 1 | 8.5 | | |
| t _{PHZ} | \overline{OE} | Y | C _L = 15 pF | 4.5* | 7.2* | 1* | 8.5* | 1 | 8.5 | ns | |
| t _{PLZ} | | | | 4.5* | 7.2* | 1* | 8.5* | 1 | 8.5 | | |
| t _{PLH} | A | Y | C _L = 50 pF | 5.2 | 8 | 1 | 9 | 1 | 8.5 | ns | |
| t _{PHL} | | | | 5.2 | 8 | 1 | 9 | 1 | 8.5 | | |
| t _{PZH} | \overline{OE} | Y | C _L = 50 pF | 6.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | ns | |
| t _{PZL} | | | | 6.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | | |
| t _{PHZ} | \overline{OE} | Y | C _L = 50 pF | 6 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns | |
| t _{PLZ} | | | | 6 | 9.2 | 1 | 10.5 | 1 | 10.5 | | |
| t _{sk(o)} | | | C _L = 50 pF | | 1** | | | | 1 | ns | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

| PARAMETER | | SN74AHC16540 | | | UNIT |
|--------------------|---|--------------|------|-----|------|
| | | MIN | TYP | MAX | |
| V _{OL(P)} | Quiet output, maximum dynamic V _{OL} | | 0.6 | | V |
| V _{OL(V)} | Quiet output, minimum dynamic V _{OL} | | -0.3 | | V |
| V _{OH(V)} | Quiet output, minimum dynamic V _{OH} | | 4.7 | | V |
| V _{IH(D)} | High-level dynamic input voltage | 3.5 | | | V |
| V _{IL(D)} | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------------|-------------------------------|--------------------|-----|------|
| C _{pd} | Power dissipation capacitance | No load, f = 1 MHz | 13 | pF |

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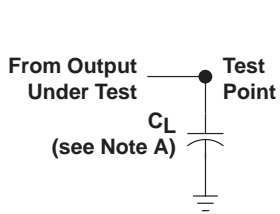


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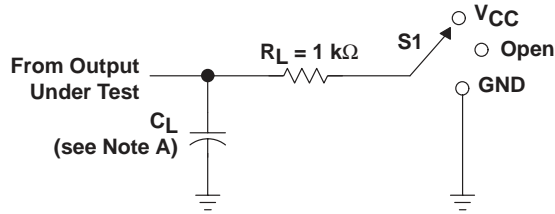
SN54AHC16540, SN74AHC16540 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION

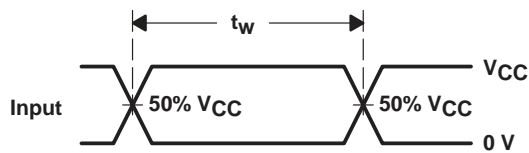


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

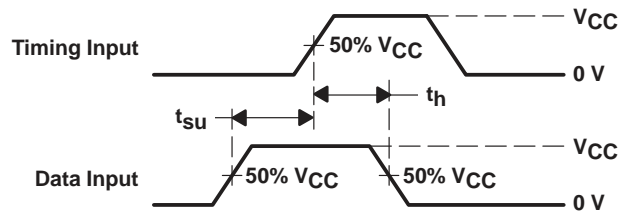


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

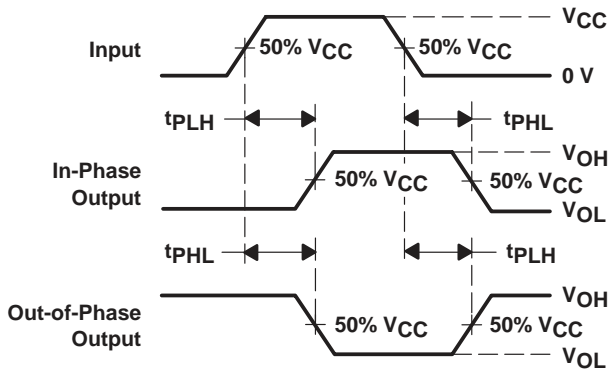
| TEST | S1 |
|-------------------|----------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{CC} |
| t_{PHZ}/t_{PZH} | GND |
| Open Drain | V_{CC} |



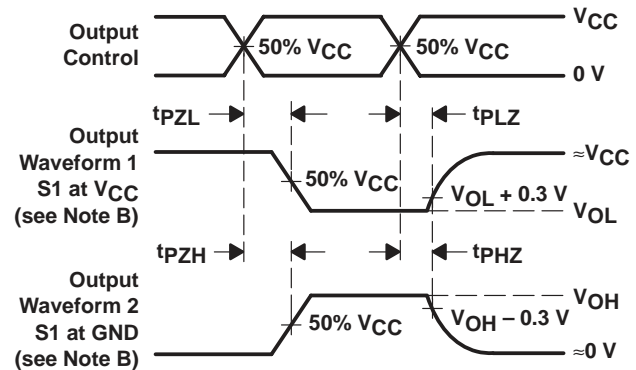
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 74AHC16540DGGRE4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74AHC16540DGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74AHC16540DGVRE4 | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74AHC16540DGVRG4 | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC16540DGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC16540DGVR | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC16540DL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC16540DLG4 | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL BOX DIMENSIONS



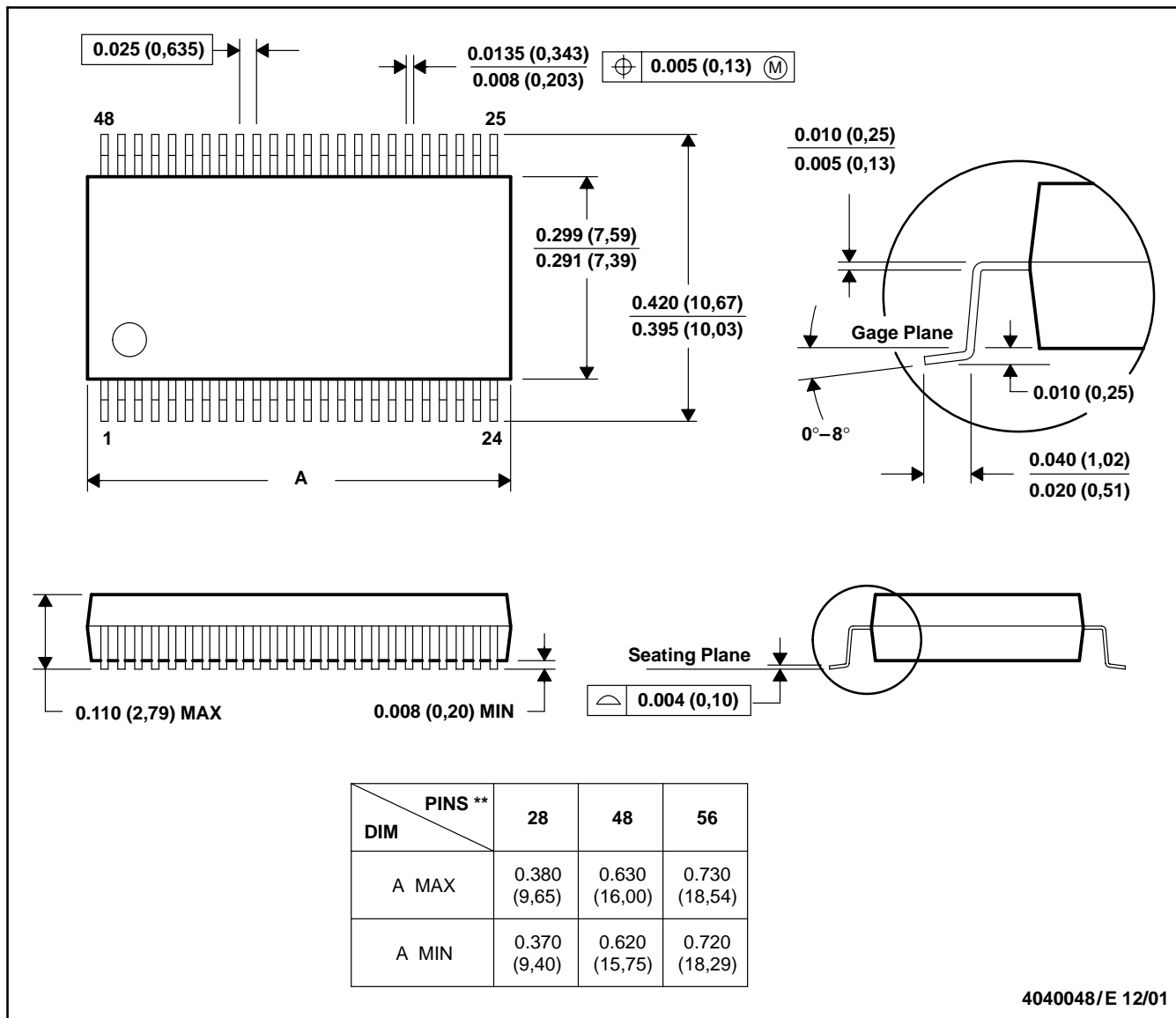
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC16540DGGR | TSSOP | DGG | 48 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74AHC16540DGVR | TVSOP | DGV | 48 | 2000 | 346.0 | 346.0 | 33.0 |

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

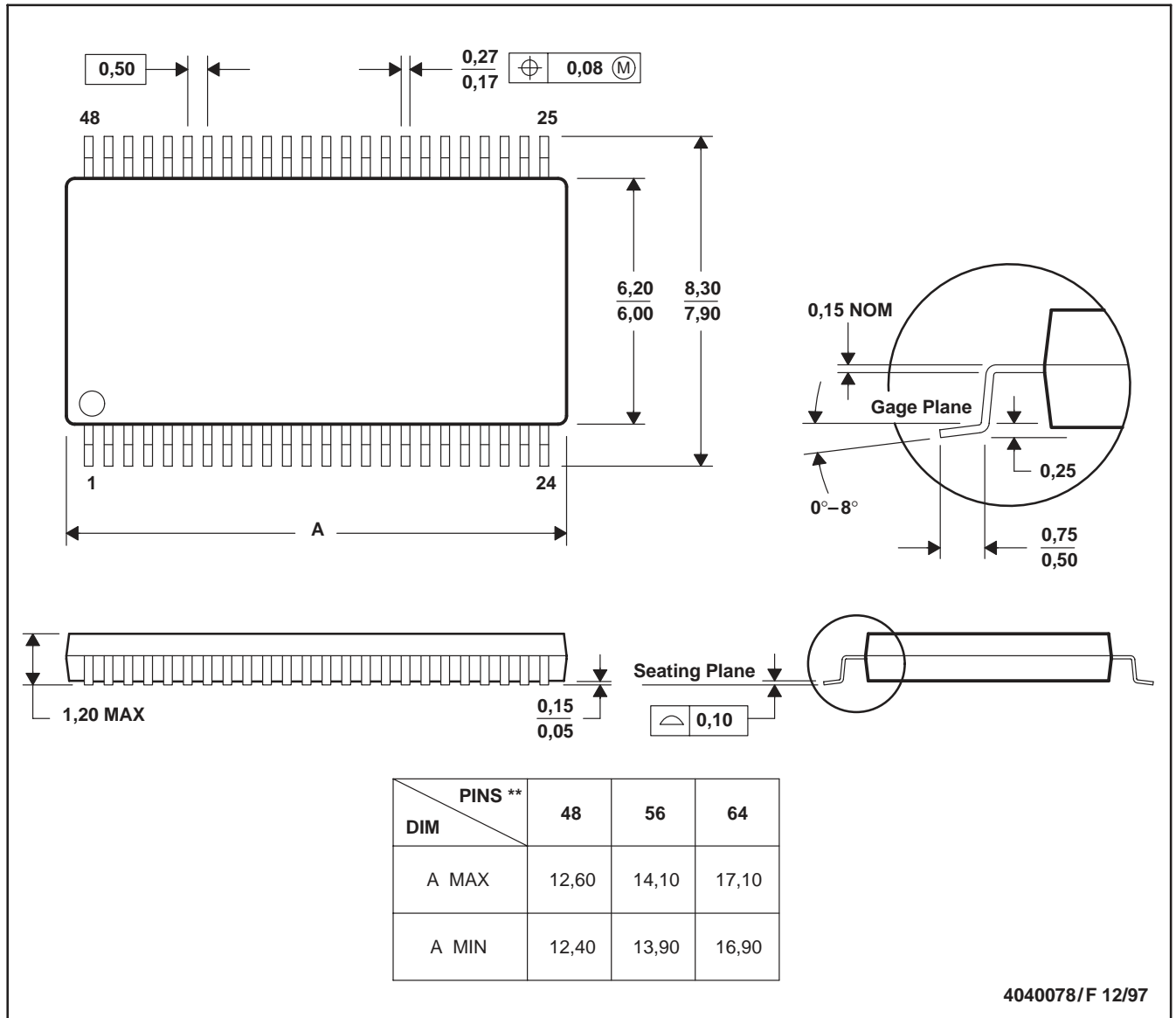


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

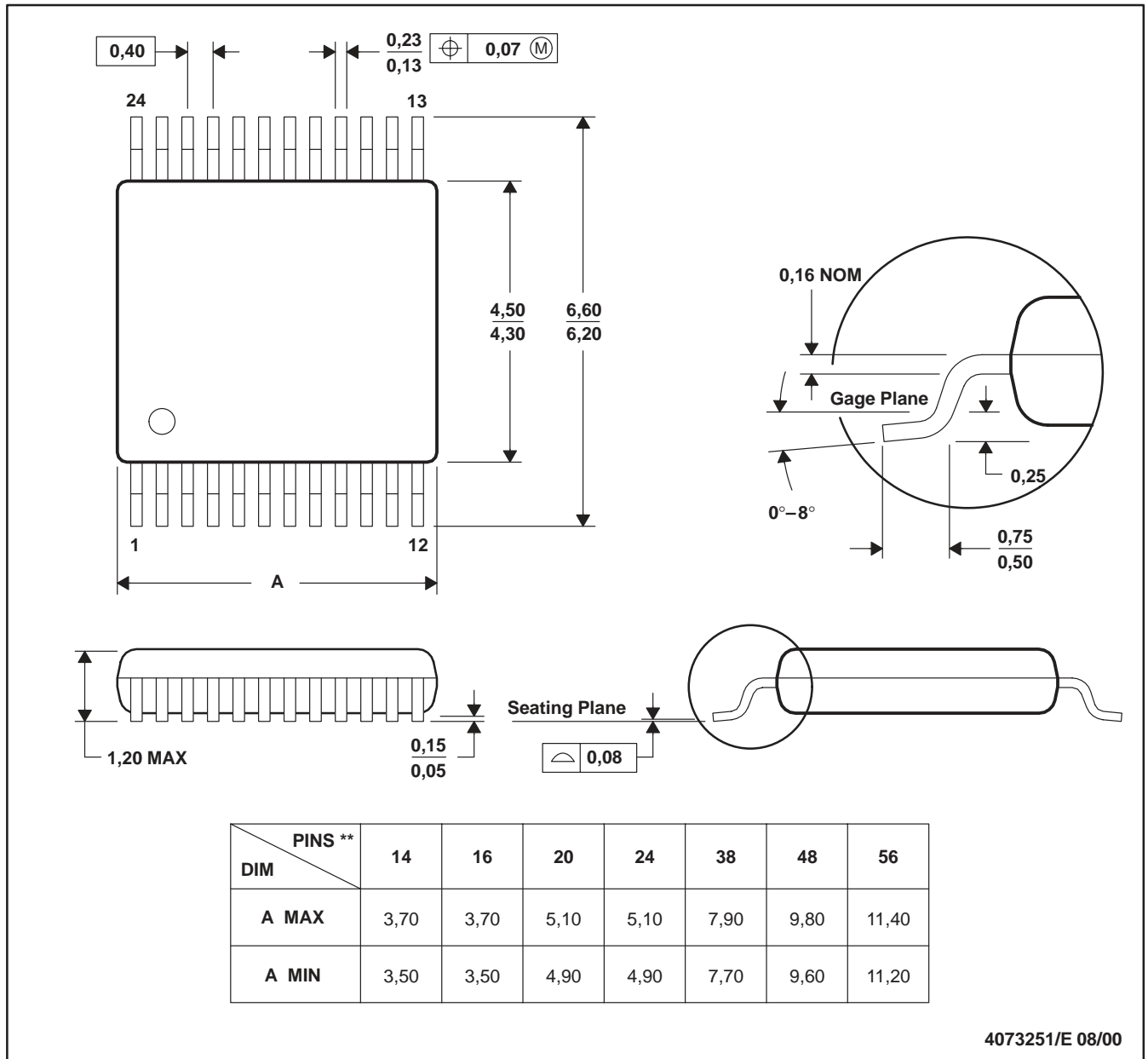


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

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