Data Sheet, V 1.3, Jun. 2006

CIC751

Companion IC

Microcontrollers

Never stop thinking

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Page	Subjects (major changes since last revision)
25	chapter 4.4.4. Power Sequencing was reworked for version 1.2
25	chapter 4.4.4. Power Sequencing was reworked for version 1.3
33	table 4-13 updated for version 1.3

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Table of Contents

1 Summary of Features

This section provides a high-level description of the features on the CIC751.

- 5 V Analog to Digital Converter
- 16 analog input channels
- Internal low power oscillator
- Slave (SPI) SSC interface operating on 5 V or 3.3 V
- MLI Interface operating on 5 V or 3.3 V
- Maximum system frequency of 40 MHz
- Low-power design
- Single power supply concept design (for pad and core supply)
- Separated ADC supply
- Input and output pins with 3.3 V and 5.0 V
- Flexible clocking concept
- Crossbar bus architecture

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the CIC751 please refer to the "**Product Catalog Microcontrollers**", which summarizes all available microcontroller variants.

2 General Device Information

2.1 Introduction

The CIC751 is a companion IC for the Infineon AUDO-NG family of 32-bit microcontrollers. The major function of the CIC751 is to provide the AUDO-NG 32-bit microcontrollers with the capability of a 5 V Analog to Digital Converter (ADC). The interconnection of the CIC751 and the microcontroller is accomplished via either the Micro Link Interface (MLI) or the Synchronous Serial Interface (SSC). Internal operations of the CIC751 are supported by the very flexible on-chip DMA controller.

2.2 Pin Configuration and Definition

The pins of the CIC751 are described in detail in **Table 2-1**, including all their alternate functions.

Table 2-1 Pin Definitions and Functions

Symbol	Pin/Port	I/O	Function
AIN0	35 P1.0	I	Analog Input 0[1)] For this pin a Multiplexer Test Mode is available.
AIN1	36 P1.1	I	Analog Input 1[1)]
AIN2	37 P1.2	I	Analog Input 2[1)]
AIN3	38 P1.3	I	Analog Input 3[1)]
AIN4	1 P1.4	I	Analog Input 4[1)]
AIN5	2 P1.5	I	Analog Input 5[1)]
AIN6	7 P1.6	I	Analog Input 6[1)]
AIN7	8 P1.7	I	Analog Input 7[1)]
AIN8	5 P1.8	I	Analog Input 8[1)]
AIN9	6 P1.9	I	Analog Input 9[1)]

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin/Port	I/O	Function
AIN10	3 P1.10	I	Analog Input 10[1)]
AIN11	4 P1.11	I	Analog Input 11[1)]
AIN12	11 P1.12	I	Analog Input 12[1)]
AIN13	12 P1.13	I	Analog Input 13[1)]
AIN14	13 P1.14	I	Analog Input 14[1)]
AIN15	14 P1.15	I	Analog Input 15[1)]
VAREF	9	I	Analog Reference Voltage
VAGND	10	I	Analog Ground
TCLK/SR3	17 P0.0	I/O	MODE = 0: MLI Transmit Channel Clock Output MODE = 1: Event output line 3
TREADY/SR4	19 P0.1	I/O	MODE = 0: MLI Transmit Channel Ready Input MODE = 1: Event request output line 4
TVALID/SCLK	20 P0.2	I/O	MODE = 0: MLI Transmit Channel Valid Output MODE = 1: SPI Serial Channel Clock
TDATA/MRST	21 P0.3	I/O	MODE = 0: MLI Transmit Channel Data Output MODE = 1: SPI Master Receive Slave Transmit
RCLK	22 P0.4	I/O	MODE = 0: MLI Receive Channel Clock Input MODE = 1: GPIO

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin/Port	I/O	Function
RREADY/RDY	23 P0.5	I/O	MODE = 0: MLI Receive Channel Ready Output MODE = 1: SSC Ready Signal
RVALID/$\overline{SLS}$	24 P0.6	I/O	MODE = 0: MLI Receive Channel Valid Input MODE = 1: SSC Select Slave
RDATA/MTSR	25 P0.7	I/O	MODE = 0: MLI Receive Channel Data Input MODE = 1: SPI Master Transmit Slave Receive
MODE [2]	26 P0.8	I/O	Interface Selection Pin MODE selects whether the on-chip MLI or SSC are used to access the CIC751 device. 0: On-chip MLI 1: On-chip SSC Event request output line 5 (SR5)
$\overline{TESTMODE}$ [3]	27 P0.9	I/O	Test Mode Selection [4] 0: Reserved; do no use 1: Normal Mode
SR0	28 P0.10	I/O	Event request output line 0
SR1	29 P0.11	I/O	External Trigger
SR2	30 P0.12	I/O	External Trigger
$\overline{PORST}$	31	I	Power-on Reset[5]
V_{DDM}	34	+5 V	Power Supply, supply for ADC module
V_{DDP}	18, 33	+3.3 V or +5.0 V	Power Supply, supply for I/O pads
V_{DDC}	16	+2.5 V	Power Supply, supply for digital module cores[6]
V_{SS}	15, 32	0 V	Ground

1) In addition to the analog input function of pin P1.x, a digital input stage is available. This input stage is activated while STCU_SYSCON.P1DIDIS = 0.
2) The initial logic state on pin MODE is latched while the $\overline{\text{PORST}}$ input is active. A weak pull-up can be disabled if used as the SR5 pin.
3) The initial logic state on pin $\overline{\text{TESTMODE}}$ is latched while the $\overline{\text{PORST}}$ input is active.
4) The meaning of 0 and 1 is only valid while this pin is latched. Thereafter it can be used as GPIO pin.
5) This pin has no internal pulls. If required an external pull has to be provided.
6) An external capacitance of 220 nF is required for this pin.

Figure 2-1 shows the pin-out for a 38-pin package

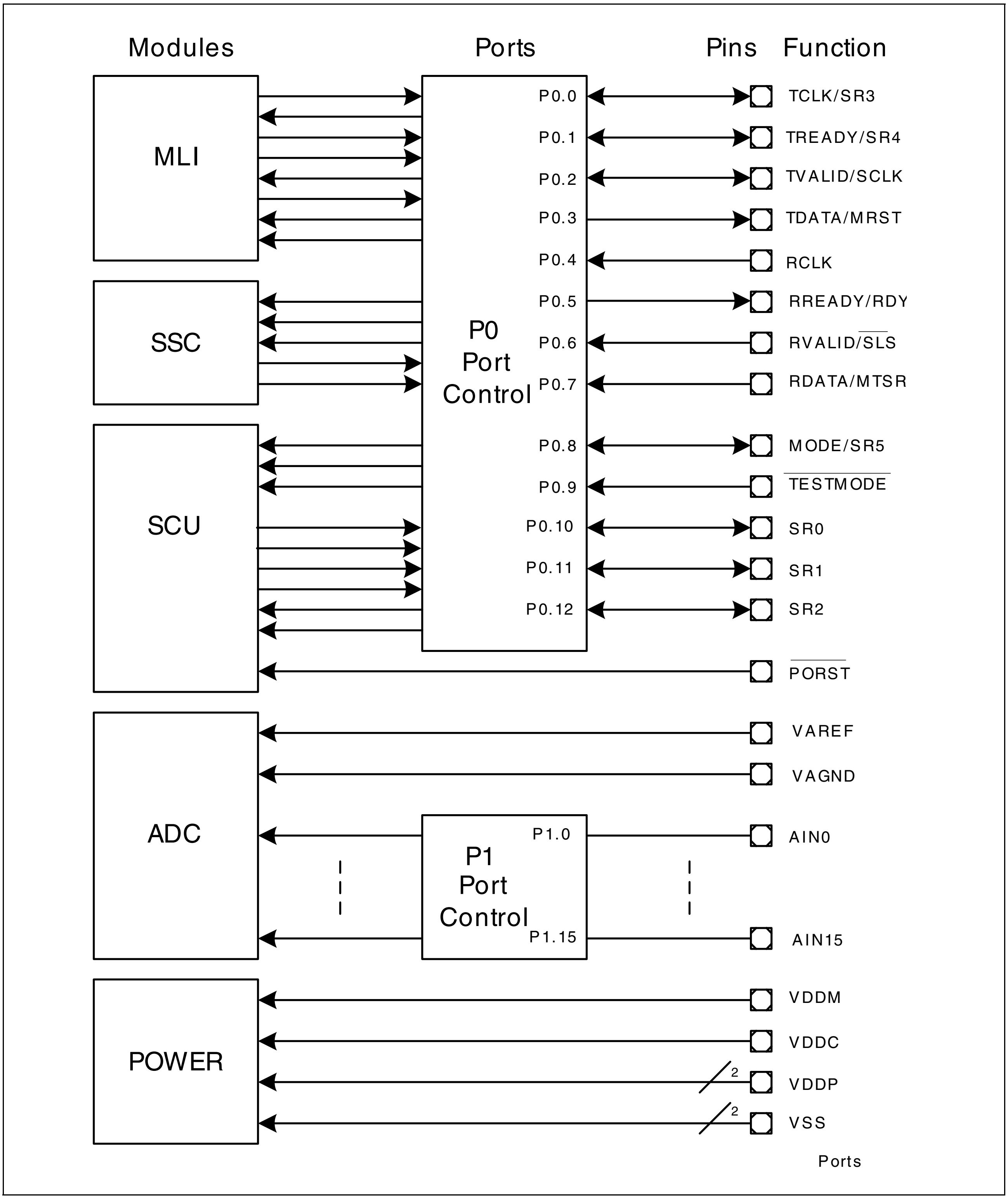


Figure 2-1 Pins for P/PG-TSSOP-38 Package

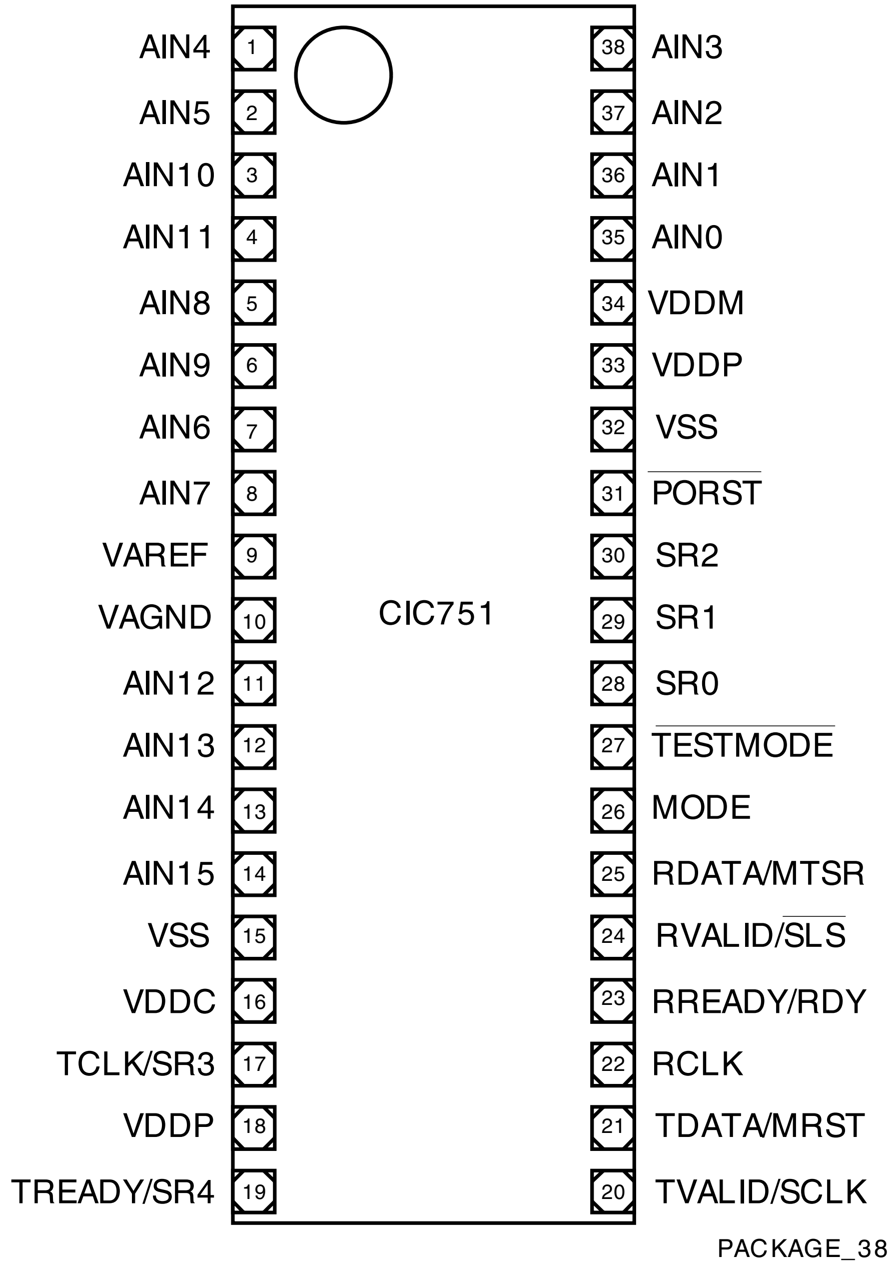


Figure 2-2 Pin Numbering for P/PG-TSSOP-38 Package

3 Functional Description

Figure 3-1 provides the block diagram of the CIC751 companion chip. This design allows access to the ADC by the host CPU without sacrificing any of the features of the ADC. This can be achieved because all registers of the ADC are mapped to the on-chip bus. This bus can be accessed via one of the two serial interfaces. Selection of the interface is made via pin MODE, which can be directly connected to the supply voltage or via pull-up/down resistors.

The bus domain is completely separated from the address domain on the CPU chip. The addresses of all modules on the companion chip are 32-bit addresses. Transactions between the CPU and the SSC are executed with the SSC transmission protocol; transactions between the MLI and the CPU use the MLI transmission protocol.

Each transaction via any of the two serial interfaces is defined by address, data, data width, and type of frame. The address from which data is read or written to, is related to the address domain. The data width may be 8, 16 or 32 bits for the MLI and 16 bits for the SSC. The ADC and the MLI may send request triggers to the DMA Controller.

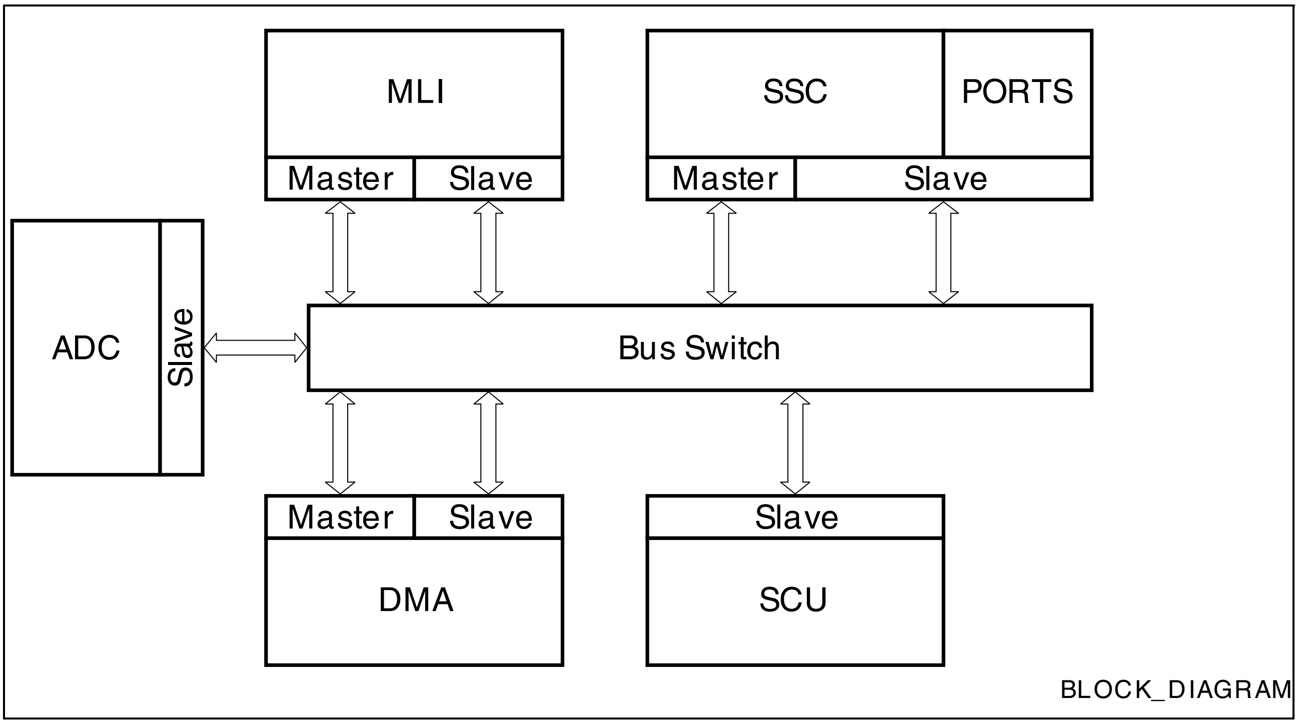


Figure 3-1 CIC751 Block Diagram

3.1 Detailed Features

The following sections provide detailed information about each of the on-chip modules.

3.1.1 ADC

The CIC751 provides an Analog/Digital Converter with 8-bit or 10-bit resolution and a sample & hold circuit on-chip. An input multiplexer selects between up to 16 analog input channels either via software (Fixed Channel Modes) or automatically (Auto Scan Modes).

To fulfill most requirements of embedded control applications, the ADC supports the following conversion modes:

- **Standard Conversions**
  - **Fixed Channel Single Conversion**
    produces just one result from the selected channel
  - **Fixed Channel Continuous Conversion**
    repeatedly converts the selected channel
  - **Auto Scan Single Conversion**
    produces one result from each of a selected group of channels
  - **Auto Scan Continuous Conversion**
    repeatedly converts the selected group of channels
  - **Wait for Read Mode**
    start a conversion automatically when the previous result was read
- **Channel Injection Mode**
  can insert the conversion of a specific channel into a group conversion (auto scan)

The key features of the ADC are:

- Use of Successive Approximation Method
- Integrated sample and hold functionality
- Analog Input Voltage Range from 0V to 5V
- 16 Analog Input Channels
- 16 ADC result registers
- Resolution:
  8-Bit or 10-Bit in Compatibility Mode
- Minimum Conversion Time:2.55 µs @ 10-Bit
- Total Unadjusted Error (TUE):±1 LSB @ 8-Bit, ± 2 LSB @10-Bit
- Support of several Conversion Modes
  Fixed Channel Single Conversion
  Fixed Channel Continuous Conversion
  Auto Scan Single Conversion
  Auto Scan Continuous Conversion
  Wait for Result Read and Start Next Conversion
  Channel Injection during Group Conversion
- Programmable Conversion and Sample Timing Scheme
- Automatic Self-Calibration to changing temperatures or process variations

3.1.2 MLI

The Micro Link Interface (MLI) is a fast synchronous serial interface that makes it possible to exchange data between microcontrollers or other devices.

The key features of the MLI are:

- Synchronous serial communication between an MLI transmitter and an MLI receiver
- Different system clock speeds are supported in the MLI transmitter and MLI receiver due to full handshake protocol (4 lines between a transmitter and a receiver)
- Fully transparent read/write access is supported (= remote programming)
- Complete address range of target device (Remote Controller) is available
- Specific frame protocol to transfer commands, addresses, and data
- Error detection by parity bit
- 32-bit, 16-bit, or 8-bit data transfers are supported
- Programmable baud rate: $f_{MLI}/2$ (max.: $f_{MLI} = f_{SYS}$)
- Multiple receiving devices are supported

3.1.3 SSC

The SSC supports full-duplex and half-duplex serial synchronous communication up to 10 Mbit/s (@ 40 MHz module clock). The serial clock signal is received from an external master (Slave Mode). Data width, shift direction, clock polarity, and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A shift clock generator provides the SSC with a separate serial clock signal.

This section describes only the use of the SSC module as a slave because the CIC751 always operates as a slave to a host.

Features

- Slave Mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: Idle low or idle high state for the shift clock
  - Programmable clock/data phase: Data shift with leading or trailing edge of the shift clock
- Internal Master Function
  - Access to the all addresses
  - Automatic address handling
  - Automatic data handling

4 Electrical Parameters

The Electrical Specifications comprise parameters to ensure the product's lifetime (Absolute Maximum Parameters) as well as parameters to describe the product's operating conditions.

4.1 General Parameters

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

*Note: **Table 4-2** and **Table 4-3** are valid for port 0 only.*

Table 4-1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condit ion
		Min.	Typ.	Max.		
Storage temperature	T_{ST}	-65	–	150	°C	–
Voltage on V_{DDC} pins with respect to ground (V_{SS})	V_{DDC}	-0.5	–	3.25	V	–
Voltage on V_{DDP} pins with respect to ground (V_{SS})	V_{DDP}	-0.5	–	6.2	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	–	V_{DDP} + 0.5	V	–
Input current on any pin during overload condition	–	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	–	–	–	|100|	mA	–
Junction temperature	T_J	-40	–	150	°C	under bias

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the CIC751. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 4-2 Operating Condition Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
System frequency	f_{SYS}	–	–	40	MHz	–
RCOSC output frequency	f_{RCOSC}	8	9	10	MHz	over all conditions
Digital supply voltage for the core	V_{DDC}	2.25	–	2.75	V	Active Mode, f_{SYS} = f_{SYSmax} [1]
Digital supply voltage for IO pads for 5 V Mode	V_{DDP}	4.5	5.0	5.5	V	Active Mode[2][3]
Digital supply voltage for IO pads for 3.3 V Mode	V_{DDP}	3.13	3.3	3.47	V	Active Mode[4][5]
Supply Voltage Difference for IO pads in 5.0 V Mode	ΔV_{DD}	-0.5	–	–	V	V_{DDP} - V_{DDC} [6]
Digital ground voltage	V_{SS}	0	–	–	V	Reference voltage
Overload current	I_{OV}	-5	–	5	mA	Per IO pin[7][8]
		-2	–	5	mA	Per analog input pin[7][8]
Overload current coupling factor for analog inputs[9]	K_{OVA}	–	–	1.0×10^{-4}	–	$I_{OV} > 0$
		–	–	1.5×10^{-3}	–	$I_{OV} < 0$
Overload current coupling factor for digital I/O pins[9]	K_{OVD}	–	–	5.0×10^{-3}	–	$I_{OV} > 0$
		–	–	1.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	$\Sigma\lvert I_{OV}\rvert$	–	–	50	mA	[8]
External Load Capacitance	C_L	–	–	50	pF	

1) f_{SYSmax} = 40 MHz
2) External circuitry must guarantee low-level at the $\overline{\text{PORST}}$ pin at least until both power supply voltages have reached the operating range.
3) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of V_{DDP} = 4.5 V to 5.5 V.
4) External circuitry must guarantee low-level at the $\overline{\text{PORST}}$ pin at least until both power supply voltages have reached the operating range.

5) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of V_{DDP} = 4.5 V to 5.5 V.

6) This limitation must be fulfilled under all operating conditions including power-ramp-up and power-ramp-down.

7) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{DDP} + 0.5$ V ($I_{OV} > 0$) or $V_{OV} < V_{SS} - 0.5$ V ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins.

8) Not subject to production test - verified by design/characterization.

9) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pin's leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it.
The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.

4.2 DC Parameters

The following chapter describes the DC parameters of the device.

Table 4-3 DC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage TTL	V_{IL}	–	–	$0.3 \times V_{DDP}$	V	[2)]
Input low voltage (Special Threshold)	V_{ILS}	–	–	$0.45 \times V_{DDP}$	V	[3)]
Input high voltage TTL	V_{IH}	$0.7 \times V_{DDP}$	–	–	V	[2)]
Input high voltage (Special Threshold)	V_{IHS}	$0.8 \times V_{DDP} - 0.2$	–	$V_{DDP} + 0.5$	V	[3)]
Input Hysteresis (Special Threshold)	HYS	$0.02 \times V_{DDP}$	–	–	V	V_{DDP} in [V], Series resistance = 0 Ω[3)]
Output low voltage	V_{OL}	–	–	1.0	V	I_{OL} = 8 mA[4)]
		–	–	0.45	V	I_{OL} = 2.5 mA[4)5)]
Output high voltage[6)]	V_{OH}	$V_{DDP} - 1.0$	–	–	V	I_{OH} = - 8 mA[4)]
		$V_{DDP} - 0.45$	–	–	V	I_{OH} = - 2.5 mA[4)5)]
Input leakage current (Port 1)[7)]	I_{OZ1}	–	–	±300	nA	$0 V < V_{IN} < V_{DDM}$, $T_A \leq 125$ °C

Table 4-3 DC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Leakage current of pin VAREF (Idle Mode)	$I_{VAREFIM}$	–	–	±800	nA	$0\ V < V_{IN} < V_{DDP}$, $T_A \leq 125\ °C$
Leakage current of pin VAREF (Active Mode)	$I_{VAREFAM}$	–	–	±20 + $I_{VAREFIM}$	µA	$0\ V < V_{IN} < V_{DDP}$, $T_A \leq 125\ °C$
Input leakage current (Port 0)[7]	I_{OZ2}	–	–	±500	nA	$0.45\ V < V_{IN} < V_{DDP}$
Configuration pull-up current[8]	I_{CPUH}[9]	–	–	-5	µA	$V_{IN} = V_{IHmin}$
	I_{CPUL}[10]	-100	–	–	µA	$V_{IN} = V_{ILmax}$
Level active hold current	I_{LHA}[11]	-100	–	–	µA	$V_{OUT} = 0.45\ V$
Pin capacitance[12] digital inputs/outputs	C_{IO}	–	–	10	pF	–

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) This parameter is tested for $\overline{PORST}$

3) This parameter is tested for P0.

4) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 4-4**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

5) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are guaranteed.

6) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

7) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

8) This specification is valid during Reset for configuration on PORT0.

9) The maximum current may be drawn while the respective signal line remains inactive.

10) The minimum current must be drawn to drive the respective signal line active.

11) The minimum current must be drawn to drive the respective signal line active.

12) Only one point on the curve is tested in production. The rest of the curve is verified by design/characterization.

Table 4-4 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1)]	Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)
Strong driver[2)3)]	8 mA	2.5 mA
Strong driver[4)5)]	10 mA	2.5 mA
Medium driver[6)]	4.0 mA	1.0 mA
Weak driver[6)]	0.5 mA	0.1 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and $\Sigma\text{-}I_{OH}$) must remain below 50 mA.
2) For 3.3 V operation.
3) The strong driver is used for all pins beside pin 35 (AIN0)
4) For 5.0 V operation.
5) The strong driver is used for all pins beside pin 35 (AIN0)
6) The medium / weak driver is only used for pin 35 (AIN0)

Table 4-5 Power Consumption CIC751

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active	I_{DDC}	–	–	30	mA	at 40 MHz system frequency
Power supply current (active) with all peripherals active	I_{DDC}	–	–	18	mA	at 20 MHz system frequency
Pad I/O current	I_{DDP}	–	4	–	mA	
V_{DDM} supply current	I_{DDM}	–	–	5	mA	

4.3 Analog/Digital Converter Parameters

The parameters of the ADC module are described below.

Table 4-6 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog supply voltage	V_{DDM}	4.5	5.0	5.5	V	[1)]
Analog reference supply	V_{AREF}	4.5	–	V_{DDM} + 0.1	V	[2)]
Analog reference ground	V_{AGND}	V_{SS} - 0.1	–	V_{SS} + 0.1	V	–
Analog input voltage range	V_{AIN}	V_{AGND}	–	V_{AREF}	V	[3)]
Basic clock frequency	f_{BC}	0.5	–	20	MHz	[4)]
Conversion time for 10-bit result[5)]	t_{C10P}	$52 \times t_{BC} + t_S + 6 \times t_{SYS}$	–	–	–	Post-calibr. on
	t_{C10}	$40 \times t_{BC} + t_S + 6 \times t_{SYS}$	–	–	–	Post-calibr. off
Conversion time for 8-bit result[5)]	t_{C8P}	$44 \times t_{BC} + t_S + 6 \times t_{SYS}$	–	–	–	Post-calibr. on
	t_{C8}	$32 \times t_{BC} + t_S + 6 \times t_{SYS}$	–	–	–	Post-calibr. off
Calibration time after reset	t_{CAL}	484	–	11,696	t_{BC}	[6)]
Total unadjusted error	TUE	–	–	±2	LSB	[2)]
Total capacitance of an analog input	C_{AINT}	–	–	15	pF	[7)]
Switched capacitance of an analog input	C_{AINS}	–	–	10	pF	[7)]
Resistance of the analog input path	R_{AIN}	–	–	2	kΩ	[7)]
Total capacitance of the reference input	C_{AREFT}	–	–	20	pF	[7)]
Switched capacitance of the reference input	C_{AREFS}	–	–	15	pF	[7)]
Resistance of the reference input path	R_{AREF}	–	–	1	kΩ	[7)]

1) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of V_{DDM} = 4.5 V to 5.5 V.
2) TUE is tested at $V_{AREF} = V_{DDP} + 0.1$ V, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range.
   If the analog reference supply voltage drops below 4.5 V (i.e. $V_{AREF} \geq 4.0$ V) or exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} = V_{DDP} + 0.2$ V) the maximum TUE is increased to ±3 LSB. This range is not subject to production test.
   The specified TUE is guaranteed only, if the absolute sum of input overload currents on Port 1 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the respective period of time. During the reset calibration sequence the maximum TUE may be ±4 LSB.
3) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.
4) The limit values for f_{BC} must not be exceeded when selecting the peripheral frequency and the ADCTC setting.
5) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result ($t_{SYS} = 1/f_{SYS}$).
   Values for the basic clock t_{BC} depend on programming and can be taken from **Table 4-7**.
   When the post-calibration is switched off, the conversion time is reduced by 12 x t_{BC}.
6) The actual duration of the reset calibration depends on the noise on the reference signal. Conversions executed during the reset calibration increase the calibration time. The TUE for those conversions may be increased.
7) Not subject to production test - verified by design/characterization.
   The given parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) reduced values can be used for calculations. At room temperature and nominal supply voltage the following typical values can be used:
   $C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 7 pF, R_{AINtyp} = 1.5 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 13 pF, $R_{AREFtyp}$ = 0.7 kΩ.

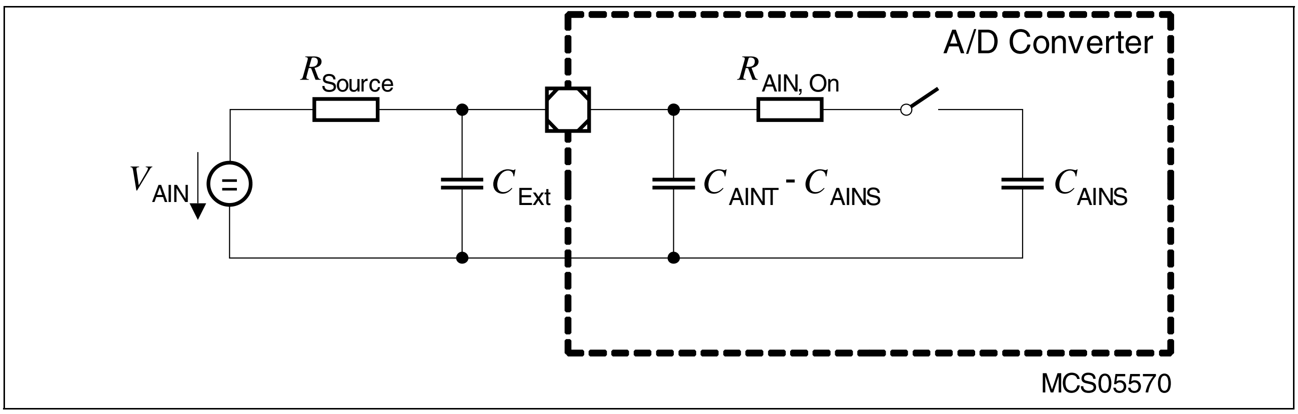


Figure 4-1 Equivalent Circuitry for Analog Inputs

Sample time and conversion time of the CIC751's A/D Converter are programmable. In compatibility mode, the above timing can be calculated using **Table 4-7**. The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 4-7 A/D Converter Computation Table[1)]

ADCON.15l14 (ADCTC)	A/D Converter Basic Clock f_{BC}	ADCON.13l12 (ADSTC)	Sample Time t_S
00	f_{SYS} / 4	00	$t_{BC} \times 8$
01	f_{SYS} / 2	01	$t_{BC} \times 16$
10	f_{SYS} / 16	10	$t_{BC} \times 32$
11	f_{SYS} / 8	11	$t_{BC} \times 64$

1) These selections are available in compatibility mode. An improved mechanism to control the ADC input clock can be selected.

Converter Timing Example

Assumptions:	f_{SYS}	= 40 MHz (i.e. t_{SYS} = 25 ns), ADCTC = '01', ADSTC = '00'
Basic clock	f_{BC}	= f_{SYS} / 2 = 20 MHz, i.e. t_{BC} = 50 ns
Sample time	t_S	= $t_{BC} \times 8 = 400$ ns
Conversion 10-bit:		
With post-calibr.	t_{C10P}	= $52 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2600 + 400 + 150) ns = 3.15 µs
Post-calibr. off	t_{C10}	= $40 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2000 + 400 + 150) ns = 2.55 µs
Conversion 8-bit:		
With post-calibr.	t_{C8P}	= $44 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2200 + 400 + 150) ns = 2.75 µs
Post-calibr. off	t_{C8}	= $32 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (1600 + 400 + 150) ns = 2.15 µs

4.4 AC Characteristics

The internal operation and consequently the timings of the CIC751 are based on the internal system clock f_{SYS}.

4.4.1 Definition of Internal Timing

The system clock signal f_{SYS} can be generated from the oscillator clock signal f_{OSC} or from the clock applied to the RCLK pin via different mechanisms. The duration of system clock periods and their variation (and also the derived external timing) depend on the used mechanism to generate f_{SYS}. This influence must be regarded when calculating the timings for the CIC751.

The used mechanism to generate the system clock is selected by register PLLCON.

4.4.1.1 Prescaler Mode

When Prescaler Mode is configured (SCU_PLLCON.PLLCTRL = 01_B) the system clock is derived from the internal oscillator through the P- and K-dividers:

$f_{SYS} = f_{OSC}$ / ((SCU_PLLCON.PDIV+1)×(SCU_PLLCON.KDIV+1)).

If both divider factors are selected as '1' (SCU_PLLCON.PDIV = SCU_PLLCON.KDIV = '0') the frequency of f_{SYS} directly follows the frequency of f_{OSC} so the high and low time of f_{SYS} is defined by the duty cycle of the input clock f_{OSC}.

The lowest system clock frequency is achieved by selecting the maximum values for both divider factors:

$f_{SYS} = f_{OSC} / ((3+1)\times(14+1)) = f_{OSC} / 60$.

4.4.1.2 Phase Locked Loop (PLL)

When PLL operation is configured (SCU_PLLCON.PLLCTRL = 11_B) the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor F ($f_{SYS} = f_{OSC} \times$ F) which results from the input divider, the multiplication factor, and the output divider (F = SCU_PLLCON.NDIV+1 / (SCU_PLLCON.PDIV+1 × SCU_PLLCON.KDIV+1)). The PLL circuit synchronizes the system clock to the input clock. This synchronization is done smoothly, i.e. the system clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{SYS} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{SYS} which also affects the duration of individual TCMs.

The actual minimum value for TCM depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency the relative deviation for periods of more than one TCM is lower than for one single TCM (see formula and **Figure 4-2**).

This is especially important for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective time frame. The VCO output clock is divided by the output prescaler (K = SCU_PLLCON.KDIV+1) to generate the system clock signal f_{SYS}. Therefore, the number of VCO cycles can be represented as $K \times N$, where N is the number of consecutive f_{SYS} cycles (TCM).

For a period of $N_N \times$ TCM the accumulated PLL jitter is defined by the deviation D:

D_N [ns] = $\pm(1.5 + 6.32 \times N / f_{SYS})$; f_{SYS} in [MHz], N = number of consecutive TCMs.

So, for a period of 3 TCMs @ 20 MHz and K = 12: $D_3 = \pm(1.5 + 6.32 \times 3 / 20) = 2.448$ ns.

This formula is applicable for $K \times N < 95$. For longer periods the $K \times N$=95 value can be used. This steady value can be approximated by: D_{Nmax} [ns] = $\pm(1.5 + 600 / (K \times f_{SYS}))$.

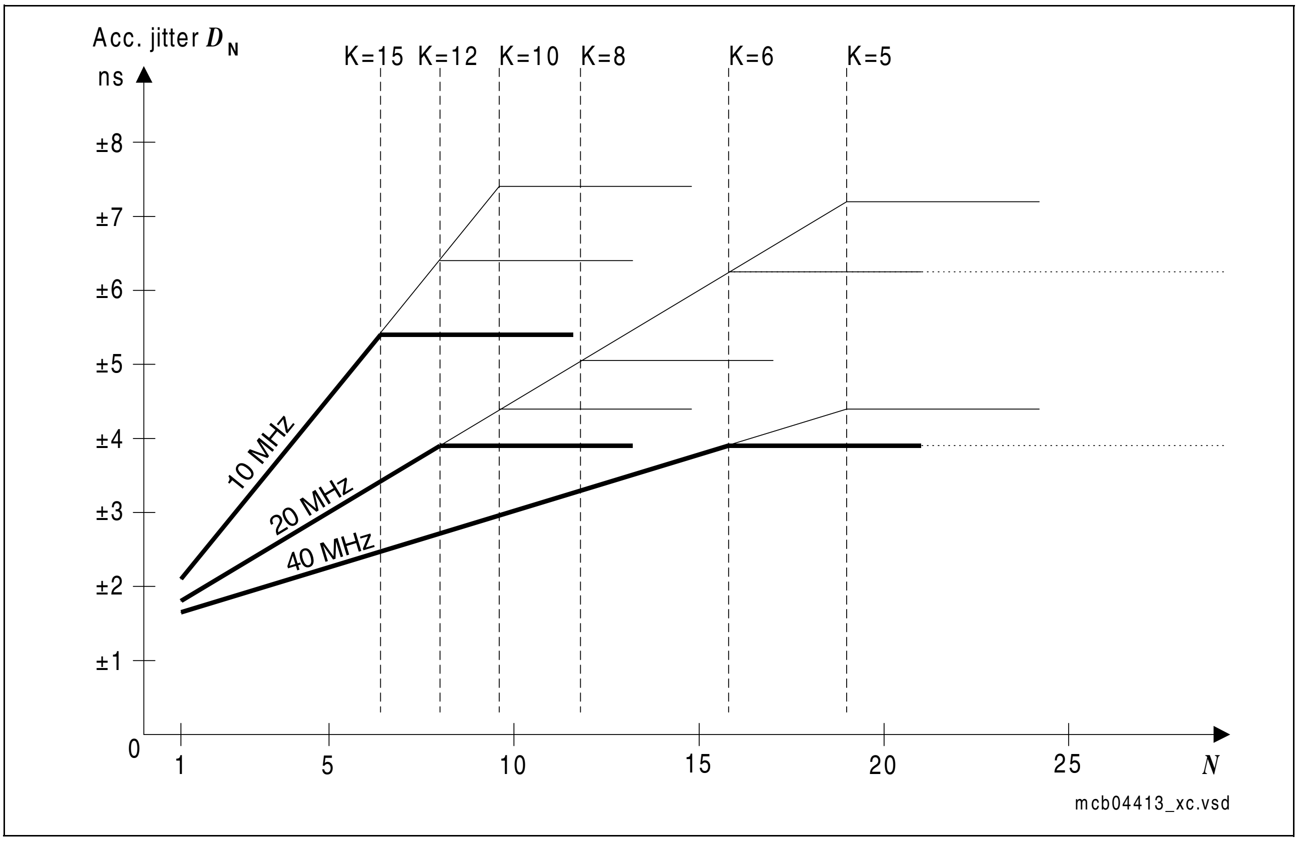


Figure 4-2 Approximated Accumulated PLL Jitter

Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.

Different frequency bands can be selected for the VCO, so the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 4-8 VCO Bands for PLL Operation[1)]

PLLCON.PLLVB	VCO Frequency Range	Base Frequency Range
00	100 … 150 MHz	20 … 80 MHz
01	150 … 200 MHz	40 … 130 MHz
10	200 … 250 MHz	60 … 180 MHz
11	Reserved	

1) Not subject to production test - verified by design/characterization.

4.4.2 Testing Waveforms of the digital input/output signals

The relation between a real and the ideal digital waveform, together with the characteristically measurement levels is shown below.

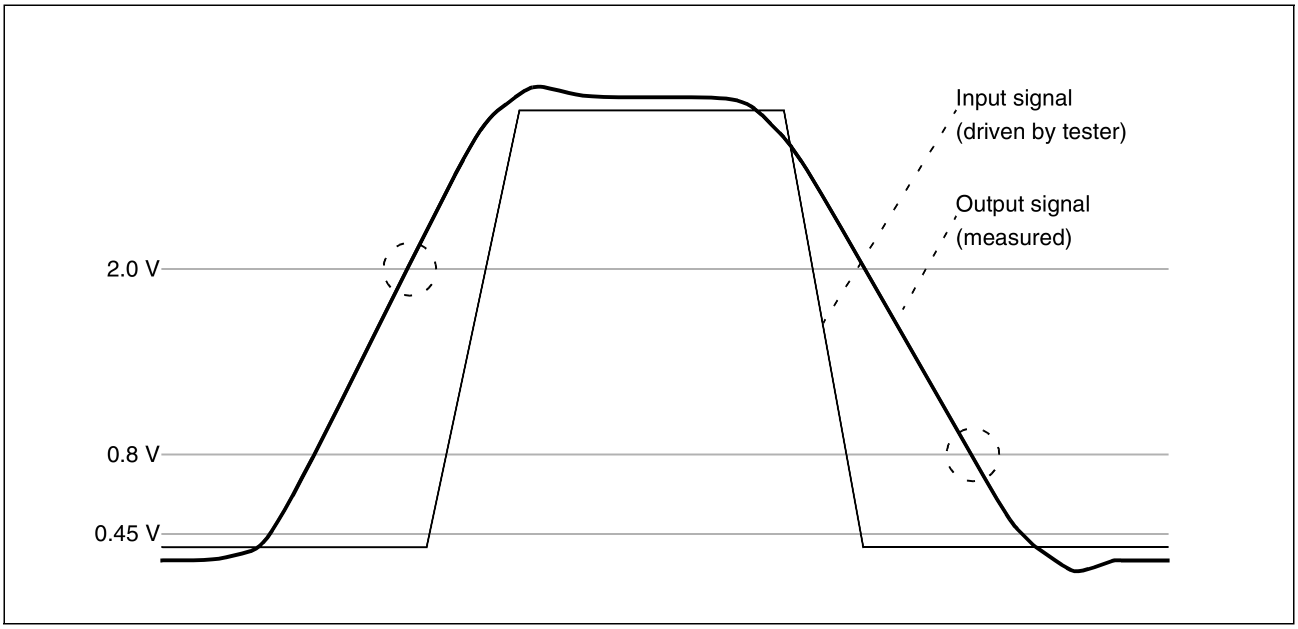
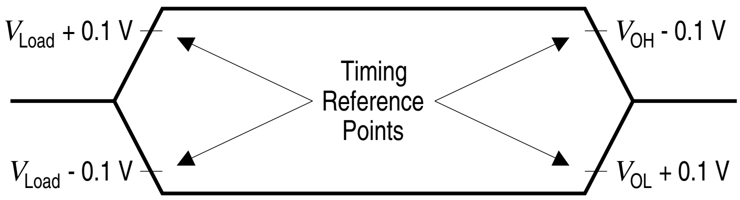


Figure 4-3 Input Output Waveforms

The figure below shows the transition between an actively driven digital output level and three-state (input state).



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH} / V_{OL} level occurs (I_{OH} / I_{OL} = 20 mA).

MCA00763

Figure 4-4 Float Waveforms

4.4.3 Output Rise and Fall Times

The Output Rise/Fall time of a GPIO is $t_r = t_f$ = 14ns, at C_L = 50pF.

4.4.4 Power Sequencing

The CIC751 device needs two power supply voltages: digital ports power supply voltage V_{DDP}, analog supply voltage V_{DDM}. The digital core supply voltage V_{DDC} is derived from V_{DDP} by embedded voltage regulator of the CIC751. The following section defines the time and voltage constraints and relations between these two power supplies that have to be satisfied at power up and power down of the device.

Figure 4-5 describes the requirements that the external power supplies V_{DDP}, and V_{DDM} must satisfy in order to provide the correct operation of the device.

The following rules should be applied in order to guarantee a stable power-up behavior:

- The active $\overline{\text{PORST}}$ should not be released before V_{DDP} reached 2.7 V
- At any time it is not allowed that $V_{DDM} > V_{DDP}$ if $V_{DDP} < 2.1$ V.

The second rule can be violated (without operation lifetime reduction) if instead the following conditions are not violated:

- The external resistor on the Analog Inputs AIN0 to AIN15 has to be equal or greater than 2 KΩ
- The accumulated time the second rule is violated is less than 4 % of the total product operation lifetime.

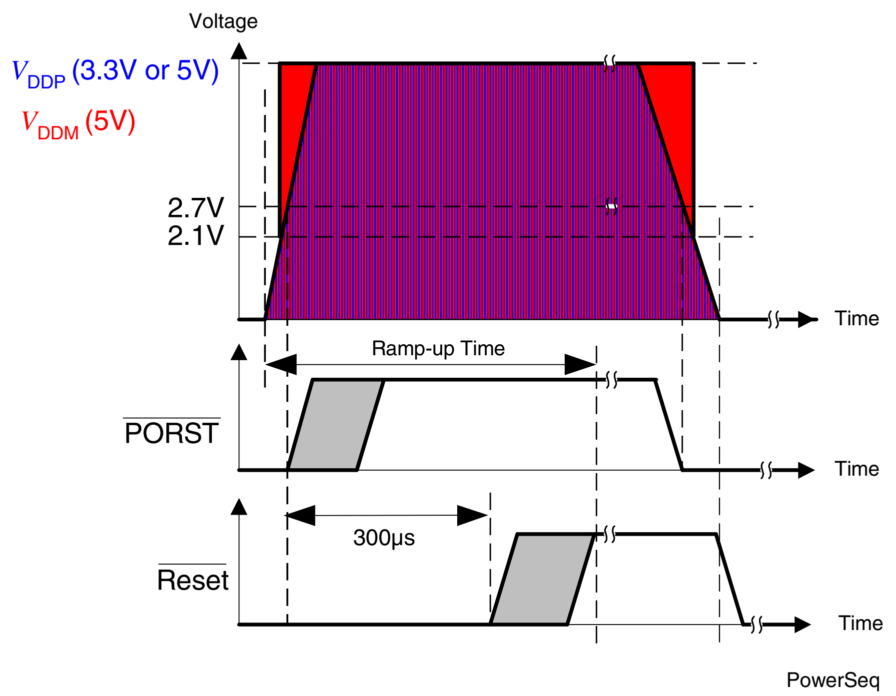


Figure 4-5 Power-up Sequence

Table 4-9 Ramp-up Times

Case	Time
Ramp-up after a power-on event	max. 500 µs
Ramp-up after a reset event	max. 450 µs

4.4.5 Timing Parameters

Peripheral timing parameters are not subject to production test. They are verified by design/characterization.

4.4.5.1 Micro Link Interface (MLI) Timing

The timing of the MLI handshake signals refer to the system clock frequency f_{SYS}. This frequency is the base for the generation of the MLI baud rate f_{TCLK}.

Table 4-10 MLI Timing (V_{SS} = 0 V; f_{MLI} <= 40MHz V_{DDP} = 3.13 to 3.47 V; T_A = -40 °C to +125 °C; C_L = 50 pF)

Parameter	Symbol	Values			Unit	Note / Test Con dition
		Min.	Typ.	Max.		
TCLK clock period	t_{10}	2 * t_{SYS}	–	–	ns	t_{SYS} = 1 / f_{SYS}
TCLK high period	t_{11}	20%	50%	80%	t_{10}	
TCLK low period	t_{12}	20%	50%	80%	t_{10}	
TCLK rise time	t_{13}	–	–	35%	t_{10}	
TCLK fall time	t_{14}	–	–	35%	t_{10}	
TDATA and TVALID setup time to TCLK raising edge	t_{20}	–	–	10%	t_{10}	
TDATA and TVALID hold time to TCLK raising edge	t_{21}	–	–	10%	t_{10}	
TREADY setup time to TCLK raising edge[1)]	t_{30}	10%	–	–	t_{10}	
TREADY hold time to TCLK raising edge [2)]	t_{31}	10%	–	–	t_{10}	
RCLK clock period	t_{40}	< 2 * t_{SYS}	–	–	ns	t_{SYS} = 1 / f_{SYS}
RCLK high period	t_{41}	20%	50%	80%	t_{40}	
RCLK low period	t_{42}	20%	50%	80%	t_{40}	
RCLK rise time	t_{43}	–	–	35%	t_{40}	
RCLK fall time	t_{44}	–	–	35%	t_{40}	
RDATA and RVALID setup time to RCLK falling edge	t_{50}	10%	–	–	t_{40}	

Table 4-10 MLI Timing (V_{SS} = 0 V; f_{MLI} <= 40MHz V_{DDP} = 3.13 to 3.47 V; T_A = -40 °C to +125 °C; C_L = 50 pF)

Parameter	Symbol	Values			Unit	Note / Test Con dition
		Min.	Typ.	Max.		
RDATA and RVALID hold time to RCLK falling edge	t_{51}	10%	–	–	t_{40}	
RREADY setup time to RCLK falling edge [3)]	t_{60}	50%	–	–	t_{40}	
RREADY hold time to RCLK falling edge [4)]	t_{61}	–	–	50%	t_{40}	

1) Referring to the TCLK edge when TVALID becomes 0 and the TCLK edge when the ready delay time elapses.
2) Referring to the TCLK edge when TVALID becomes 0 and the TCLK edge when the ready delay time elapses.
3) Referring to the former value at the RCLK edge when RVALID changes.
4) Referring to the new value at the RCLK edge when RVALID changes.

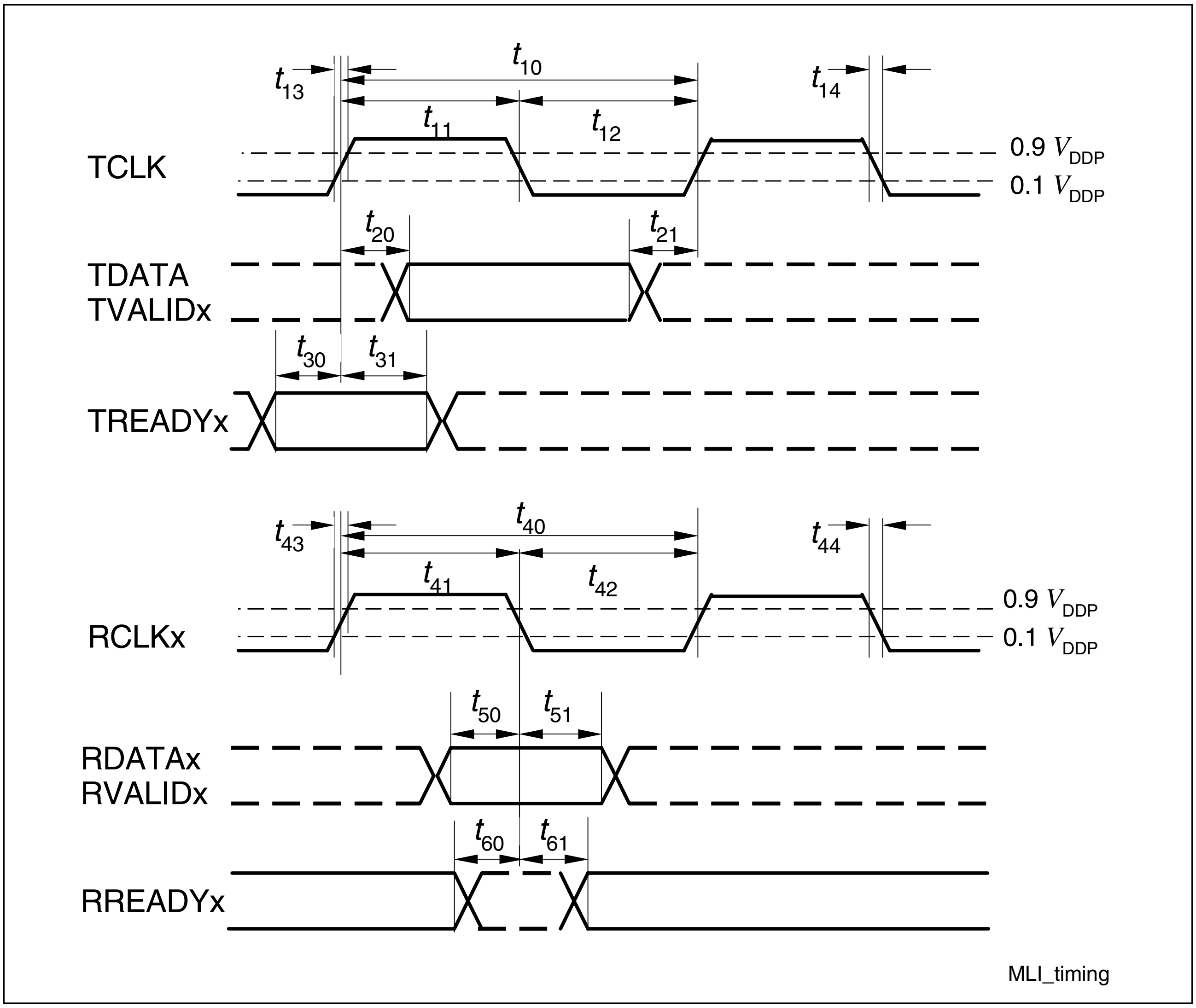


Figure 4-6 MLI Timing

4.4.6 Synchronous Serial Channel (SSC) Slave Mode Timing

The timing of the Synchronous Serial Channel in slave mode is defined below.

Table 4-11 SSC Timing (VSS = 0 V; f_{SSC} <= 40MHz VDDP = 3.13 to 3.47 V (Class A); TA = -40 °C to +125 °C; CL = 50 pF)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period	t_{20} CC	T_{SSC}		–	ns	
MRST delay from SCLK Rising/Falling Edge from SCLK RE (CON.PO,CON.PH = 00) from SCLK FE (CON.PO,CON.PH = 10)	t_{21} CC	4		12	ns	
MRST hold from SLS Rising Edge	t_{26} CC	–		14	ns	
MTSR setup to SCLK Rising/Falling Edge to SCLK RE (CON.PO,CON.PH = 00) to SCLK FE (CON.PO,CON.PH = 10)	t_{22} SR	0		–	ns	
MTSR hold from SCLK Rising/Falling Edge from SCLK RE (CON.PO,CON.PH = 00) from SCLK FE (CON.PO,CON.PH = 10)	t_{23} SR	$2 + T_{SSC}$		–	ns	
SLSI lead delay from SCLK Rising/Falling Edge from SCLK RE (CON.PO,CON.PH = 00) from SCLK FE (CON.PO,CON.PH =10)	t_{24} SR	6		–	ns	1)
RDY lead delay to SLS RE	t_{25} CC	13		15	ns	
SLS hold from RDY RE	t_{27} SR	4		–	ns	

1) This is only valid if SSC move engine is idle (RDY = 1).

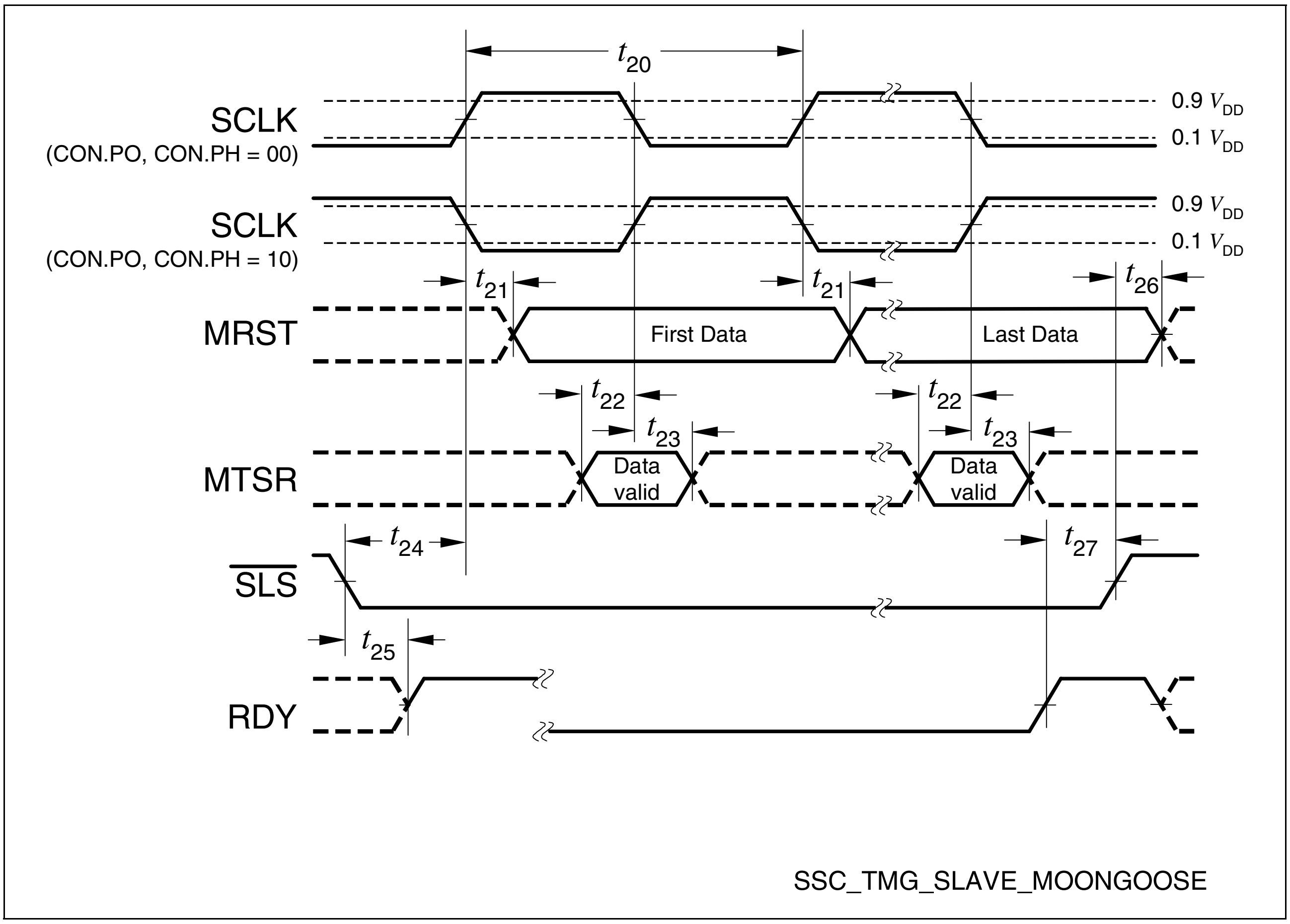


Figure 4-7 SSC Slave Mode Timing

4.5 Package and Reliability

This chapter defines the parameters related to the Package and Reliability of the device.

4.5.1 Packaging

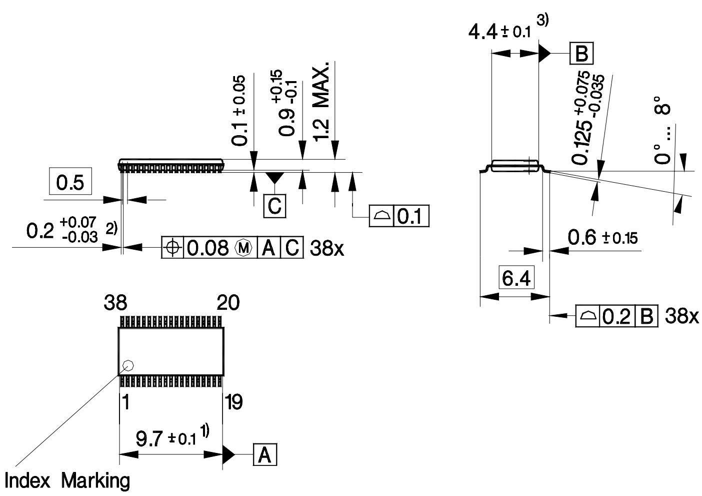
The parameters of the package of the CIC751 are defined below.

Table 4-12 Package Parameters (P/PG-TSSOP-38)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Power dissipation	P_{DISS}	–	tbd.	W	–
Thermal resistance	R_{THJA}	–	59	K/W	Chip-Ambient

4.5.2 Package Outlines

The physical characteristics of the package are described below.



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side
3) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 4-8 Package Outlines for P/PG-TSSOP-38

4.5.3 Quality Declarations

The following chapter defines some quality parameters of CIC751.

Table 4-13 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Operation Lifetime	t_{OP}	–	18000	hours	at average weighted junction temperature T_J = 116°C (ambient temperature T_A = 102°C)
		–	24000[1)]	hours	at average weighted junction temperature T_J = 106°C (ambient temperature T_A = 92°C)
Life Expectancy	t_B	20	–	years	
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	–	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Socketed Device Model (SDM)	V_{SDM}	–	500	V	Conforming to ESDA Std DS5.3-1993
Moisture Sensitivity Level (MSL)	–	–	3	–	Conforming to Jedec J-STD-020C for 240°C

1) One example of a detailed temperature profile is:
1200 hours at T_J = 140 °C (T_A = 125 °C)
3600 hours at T_J = 115 °C (T_A = 100 °C)
7200 hours at T_J = 100 °C (T_A = 85 °C)
12000 hours at T_J = 90 °C (T_A = 75 °C)

Note: Information about soldering can be found on the "package" information page under: ***http://www.infineon.com/products***.

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