# National Semiconductor

# 9314/DM9314 Quad Latch

## General Description

The '9314 is a multifunctional 4-bit latch designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good noise immunity.
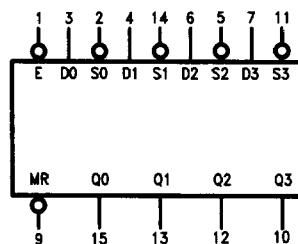
## Connection Diagram

### Dual-In-Line Package
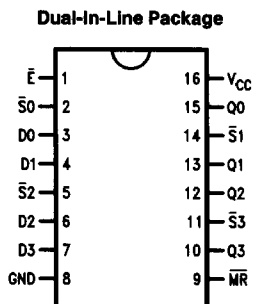


TL/F/9788–1

**Order Number 9314DMQB, 9314FMQB or DM9314N**
**See NS Package Number J16A, N16E or W16A**

## Logic Symbol



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$V_{CC}$ = Pin 16
GND = Pin 8

| Pin Names | Description |
|-----------|-------------|
| $\bar{E}$ | Enable Input (Active LOW) |
| D0–D3 | Data Inputs |
| $\bar{S}0$–$\bar{S}3$ | Set Inputs (Active LOW) |
| $\overline{MR}$ | Master Reset Input (Active LOW) |
| Q0–Q3 | Latch Outputs |

## Absolute Maximum Ratings (Note)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 5.5V |
| Operating Free Air Temperature Range | |
| Military | $-55°C$ to $+125°C$ |
| Commercial | $0°C$ to $+70°C$ |
| Storage Temperature Range | $-65°C$ to $+150°C$ |

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

## Recommended Operating Conditions

| Symbol | Parameter | Military | | | Commercial | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High Level Input Voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High Level Output Current | | | $-0.8$ | | | $-0.8$ | mA |
| $I_{OL}$ | Low Level Output Current | | | 16 | | | 16 | mA |
| $T_A$ | Free Air Operating Temperature | $-55$ | | 125 | 0 | | 70 | °C |
| $t_s$ (H) $t_s$ (L) | Setup Time HIGH or LOW $D_n$ to $\overline{E}$ | 5.0 18 | | | 5.0 18 | | | ns |
| $t_h$ (H) $t_h$ (L) | Hold Time HIGH or LOW $D_n$ to $\overline{E}$ | 0 5.0 | | | 0 5.0 | | | ns |
| $t_s$ (H) | Setup Time HIGH, $D_n$ to $\overline{S}_n$ | 8.0 | | | 8.0 | | | ns |
| $t_h$ (L) | Hold Time LOW, $D_n$ to $\overline{S}_n$ | 8.0 | | | 8.0 | | | ns |
| $t_w$ (L) | $\overline{E}$ Pulse Width LOW | 18 | | | 18 | | | ns |
| $t_w$ (L) | $\overline{MR}$ Pulse Width LOW | 18 | | | 18 | | | ns |
| $t_{rec}$ | Recovery Time, $\overline{MR}$ to $\overline{E}$ | 0 | | | 0 | | | ns |

## Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = $-12$ mA | | | | $-1.5$ | V |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max $V_{IL}$ = Max | | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max $V_{IH}$ = Min | | | 0.2 | 0.4 | V |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Min, $V_I$ = 5.5V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4V | | | | 40 | μA |
| | | Data Inputs | | | | 60 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4V | | | | $-1.6$ | mA |
| | | Data Inputs | | | | $-2.7$ | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (Note 2) | MIL | $-20$ | | $-70$ | mA |
| | | | COM | $-20$ | | $-70$ | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | | 55 | mA |

**Note 1:** All typicals are at $V_{CC}$ = 5V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time.

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## Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

| Symbol | Parameter | $C_L$ = 15 pF | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{E}$ to $Q_n$ | | 24<br>24 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$D_n$ to $Q_n$ | | 12<br>24 | ns |
| $t_{PLH}$ | Propagation Delay<br>$\overline{MR}$ to $Q_n$ | | 18 | ns |
| $t_{PHL}$ | Propagation Delay<br>$\overline{S}_n$ to $Q_n$ | | 24 | ns |

## Functional Description

The '9314 consists of four latches with a common active LOW Enable input and active LOW Master Reset input. When the Enable goes HIGH, data present in the latches is stored and the state of the latch is no longer affected by the $\overline{S}_n$ and $D_n$ inputs. The Master Reset when activated overrides all other input conditions forcing all latch outputs LOW. Each of the four latches can be operated in one of two modes:

D-TYPE LATCH—For D-type operation the $\overline{S}$ input of a latch is held LOW. While the common Enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the Enable goes HIGH.

SET/RESET LATCH—During set/reset operation when the common Enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the $\overline{S}$ input if the D input is HIGH. If both $\overline{S}$ and D inputs are LOW, the D input will dominate and the latch will be reset. When the Enable goes HIGH, the latch remains in the last state prior to disablement. The two modes of latch operation are shown in the Truth Table.

## Truth Table

| $\overline{MR}$ | $\overline{E}$ | D | $\overline{S}$ | $Q_n$ | Operation |
|---|---|---|---|---|---|
| H | L | L | L | L | D Mode |
| H | L | H | L | H | |
| H | H | X | X | $Q_{n-1}$ | |
| H | L | L | L | L | R/S Mode |
| H | L | H | L | H | |
| H | L | L | H | L | |
| H | L | H | H | $Q_{n-1}$ | |
| H | H | X | X | $Q_{n-1}$ | |
| L | X | X | X | L | Reset |

H = HIGH Voltage Level
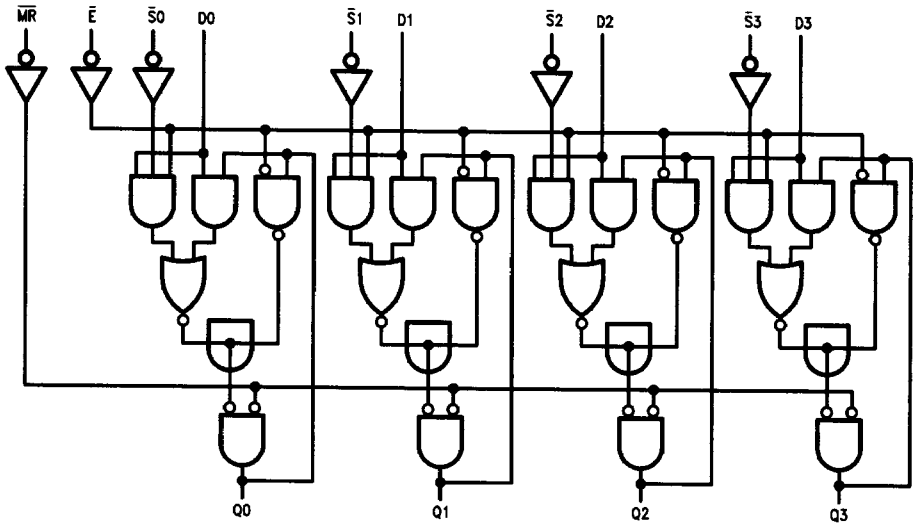L = LOW Voltage Level
X = Immaterial
$Q_{n-1}$ = Previous Output State
$Q_n$ = Present Output State

# Logic Diagram



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