A6280

3-Channel Constant-Current LED Driver with Programmable PWM Control

Last Time Buy

This part is in production but has been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change:
A6280EA-T September 3, 2013
A6280EESTR-T June 3, 2013

Deadline for receipt of LAST TIME BUY orders: November 29, 2013

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

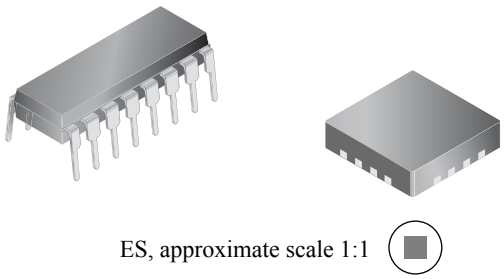
NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

3-Channel Constant-Current LED Driver with Programmable PWM Control

Features and Benefits

- 3 × 10-bit PWM brightness settings
- 3 × 7-bit dot correction current settings
- 5 to 17 V operation
- Wide output current range, 10 to 150 mA per channel
- Serial port/PWM clock operates at up to 5 MHz
- Data and clock logic architecture allows single microcontroller control of large quantities of serially-connected A6280s at fast data transfer rate
- Buffered logic outputs to drive cables
- Thermal shutdown and UVLO protection
- Power-On Reset

Packages: 16-pin DIP (suffix A), and 16-contact QFN (suffix ES)



ES, approximate scale 1:1

Description

The A6280 is a 3-channel constant current LED driver that has a wide range of output currents. The A6280 controls LED brightness with a Pulse Width Modulation (PWM) scheme that gives the application the capability of displaying a billion colors in an RGB cluster. The maximum current is set by an external resistor.

The LED brightness is controlled by performing PWM control on the outputs. The brightness data of the PWM signal for each LED is stored in three 10-bit registers. The peak value for each LED can be adjusted (dot-corrected) to compensate for mismatch, aging, and temperature effects. All the internal latched registers are loaded by a 31-bit shift register. One address bit controls whether dot correction/clock divider ratio or brightness data is loaded into the registers. The remaining bits are used for the data. This helps reduce the pin count of the A6280. To further lower the A6280 pin count, the PWM clock and the serial bus clock share the same pin and work concurrently to control LED brightness and to load data.

The A6280 is designed to minimize the number of components needed to drive LEDs with large pixel spacing. A large number of A6280s can be daisy chained together and controlled by just four control signals (clock, serial data, latch, and output enable). Each of these inputs has buffered outputs to drive the next chip in the chain. Also, VIN can be tied to the LED

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Application Diagram

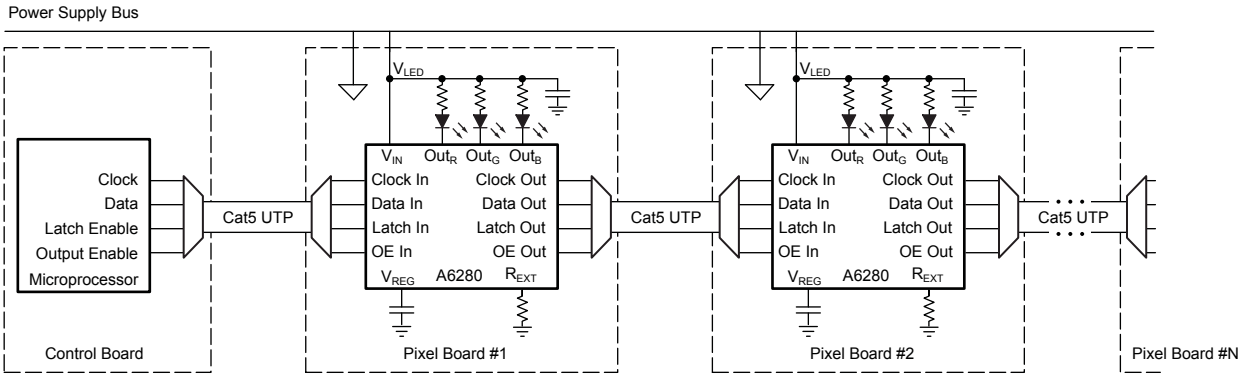


Figure 1. Functional drawing of daisy chained display application. Additional pixel boards with A6280 ICs can be applied.

Description (continued)

voltage supply bus, thus eliminating the need for a separate chip supply bus or an external regulator.

The A6280 is supplied in a 16-pin dual in-line (DIP) package (suffix 'A') and in a 16-contact QFN (suffix 'ES') package. The packages are lead (Pb) free with 100% matte-tin leadframe plating.

Applications include:

- Colored, large-character LED signs
- Scrolling, colored marquees
- Architectural lighting
- High intensity monochrome displays
- Large video and graphic displays

Selection Guide

Part Number	Packing[1]	Mounting
A6280EA-T	25 pieces/tube	16 pin DIP
~~A6280EESTR-T~~[2]	1500 pieces/reel	16 pin QFN

[1]Contact Allegro for additional packing options.

[2]Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change June 3, 2013. Deadline for receipt of LAST TIME BUY orders is November 29, 2013.

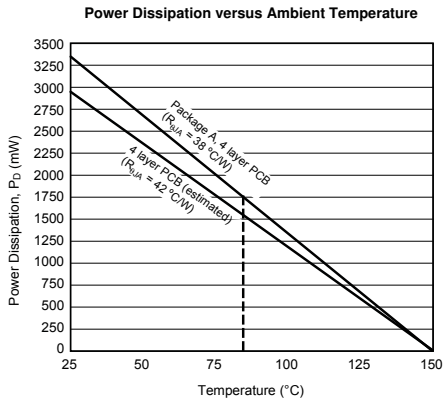
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{IN}		17	V
Output Voltage	V_{OUT}	OUT0, OUT1, OUT2	–0.5 to 17	V
Output Current	I_{OUT}		170	mA
Ground Current	I_{GND}		600	mA
VREG Pin	V_{REG}		6	V
Logic Outputs	V_O	CO, LO, OEO, SDO	7	V
Logic Input Voltage Range	V_I	CI, LI, OEI, SDI	–0.3 to 7	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

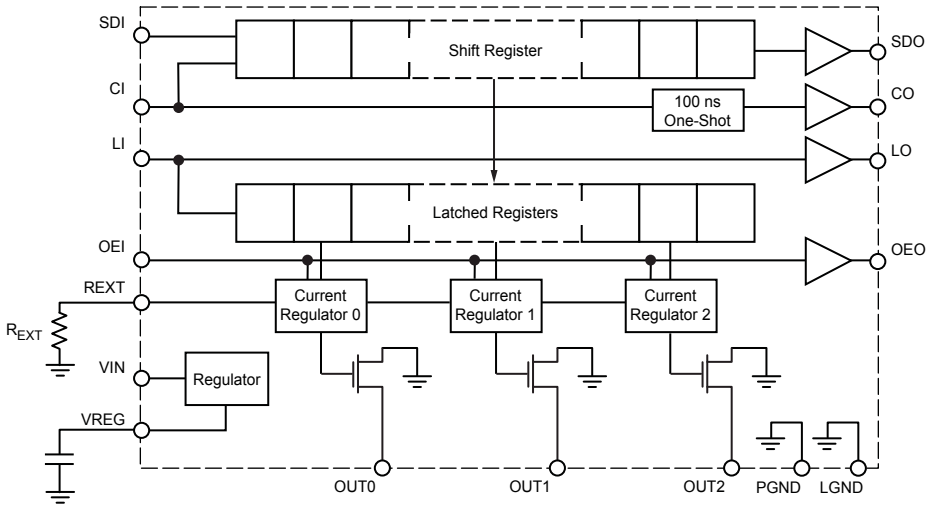
Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Rating	Units
Package Thermal Resistance	$R_{\theta JA}$	Package A, 4 layer PCB	38	ºC/W
		4-layer PCB based on JEDEC standard (estimated performance)	42	ºC/W

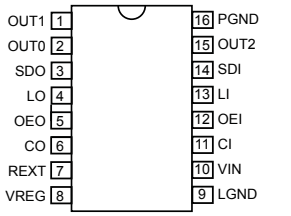
*For additional information, refer to the Allegro website.



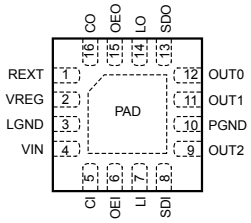
Functional Block Diagram



Pin-out Drawings



Package A



Package ES

Terminal List Table

Name	Number		Description
	A Package	ES Package	
OUT1	1	11	Sinking output terminal
OUT0	2	12	Sinking output terminal
SDO	3	13	Buffered serial data output after shift register
LO	4	14	Buffered latch output
OEO	5	15	Buffered output enable output
CO	6	16	Buffered clock output
REXT	7	1	An external resistor at this terminal establishes overall output current
VREG	8	2	Regulator decoupling
LGND	9	3	Logic ground
VIN	10	4	Chip power supply voltage
CI	11	5	Serial and PWM clock input
OEI	12	6	Output enable input; when low (active), the output drivers are enabled; when high (inactive), all output drivers are turned off (blanked)
LI	13	7	Latch input terminal; serial data is latched with high-level input
SDI	14	8	Serial data input to shift register
OUT2	15	9	Sinking output terminal
PGND	16	10	Power ground
PAD	n.a.	–	Exposed thermal pad, not internally connected; connect externally to LGND and PGND.

OPERATING CHARACTERISTICS, valid at T_A = 25°C, V_{IN} = 4.75 to 17.0 V, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS						
Quiescent Supply Current	I_{DD}	f_{CLKIN} = 0.0 Hz	–	–	5.0	mA
Operating Supply Current	I_{DD}	f_{CLKIN} = 5 Mhz	–	–	15.0	mA
Load Supply Voltage	V_{IN}		4.75	–	17	V
Undervoltage Lockout	$V_{IN(UV)}$	V_{IN} rising	3.5	–	4.5	V
		V_{IN} falling	3.0	–	4.0	V
VREG Voltage Range[1]	V_{REG}	I_O =15 mA, V_{IN} = 17 V	4.6	–	5.4	V
Output Current (any single output)	I_{OUT}	R_{EXT} = 5 kΩ, scalar = 100%	135	150.0	165	mA
		R_{EXT} = 15 kΩ, scalar = 100%	45	51	57	mA
Output to Output Matching Error[2]	Err	Output to output variation—all outputs on, R_{EXT} = 5 kΩ	–7	–	7	%
Output Voltage Range	$V_{DS(min)}$		1.0	–	3.0	V
Load Regulation ($I_{\%Diff}$ / ΔV_{DS})		R_{EXT} = 5 kΩ, V_{DS} = 1 to 3 V	–	±1	±3	%/V
Output Leakage Current	I_{DSX}	V_{OH} = 17 V	–	–	1.0	µA
Logic Input Voltage	V_{IH}		2.0	–	–	V
	V_{IL}		–	–	0.8	V
Logic Input Voltage Hysteresis		All digital inputs	–	150	–	mV
Logic Output Voltage	V_{OL}	V_{IN} ≥ 5.0 V, I_O = ±2 mA	–	–	0.4	V
	V_{OH}		3.8	–	–	V
Input Resistance	R_I	OEI pin, pull-up	150	300	600	kΩ
		LI pin, pull-down	100	200	400	kΩ
CI and SDI Pins Logic Input Current	I_{IN}	V_{IN} = 0 to 5 V	–20	–	20	µA
Output Dot Correction Error		R_{EXT} = 5 kΩ; LSB	–	±1	–	bit
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	T_{Jhys}		–	15	–	°C
SWITCHING CHARACTERISTICS						
Clock Hold Time	$t_{H(CLK)}$		20	–	–	ns
Data Setup Time	$t_{SU(D)}$		20	–	–	ns
Data Hold Time	$t_{H(D)}$		20	–	–	ns
Latch Setup Time[3]	$t_{SU(LI)}$		20	–	–	ns
Latch Hold Time	$t_{H(LI)}$		20	–	–	ns
Output Enable Set Up Time	$t_{SU(OE)}$		40	–	–	ns
Output Enable Falling to Outputs Turning ON Propagation Delay Time	$t_{P(OE)2}$		–	200	–	ns
Clock to Output Propagation Delay Time	$t_{P(OUT)}$	V_{DS} = 1.0 V, I_{OUT} = 150 mA	–	200	–	ns
Logic Output Fall Time	t_{BF}	C_{OB} = 50 pF, 4.5 to 0.5 V	–	50	100	ns
Logic Output Rise Time	t_{BR}	C_{OB} = 50 pF, 0.5 to 4.5 V	–	30	60	ns
Output Fall Time (Turn Off)	t_f	C_O = 10 pF, 90% to 10% of I_{OUT} = 10 mA	–	10	–	ns
		C_O = 10 pF, 90% to 10% of I_{OUT} = 150 mA	–	10	–	ns
Output Rise Time (Turn On)	t_r	C_O = 10 pF, 10% to 90% of I_{OUT} = 10 mA	–	50	–	ns
		C_O = 10 pF, 10% to 90% of I_{OUT} = 150 mA	–	100	–	ns
Clock Falling Edge to Serial Data Out Propagation Delay Time	$t_{P(SDO)}$		–	50	100	ns
Output Enable In to Output Enable Out Propagation Delay	$t_{P(OE)}$		–	50	100	ns
Latch In to Latch Out Propagation Delay	$t_{P(LE)}$		–	50	100	ns
Clock In to Clock Out Propagation Delay	$t_{P(CLK)}$		–	50	100	ns
Clock Out Pulse Duration	$t_{w(CLK)}$		70	100	130	ns
Maximum CLKIN Frequency	f_{CLKIN}		–	–	6	MHz

[1]If V_{IN} is a 4.75 to 5.5 V supply, connect VIN to VREG externally

[2]Err = [I_{OUT}(min or max) – I_{OUT}(av)] / I_{OUT}(av), where I_{OUT}(av) is the average of 3 output current values.

[3]In daisy-chained applications, $t_{SU(LI)}$ must be increased for the quantity of pixels in the chain (see Application Information section).

Timing Diagrams

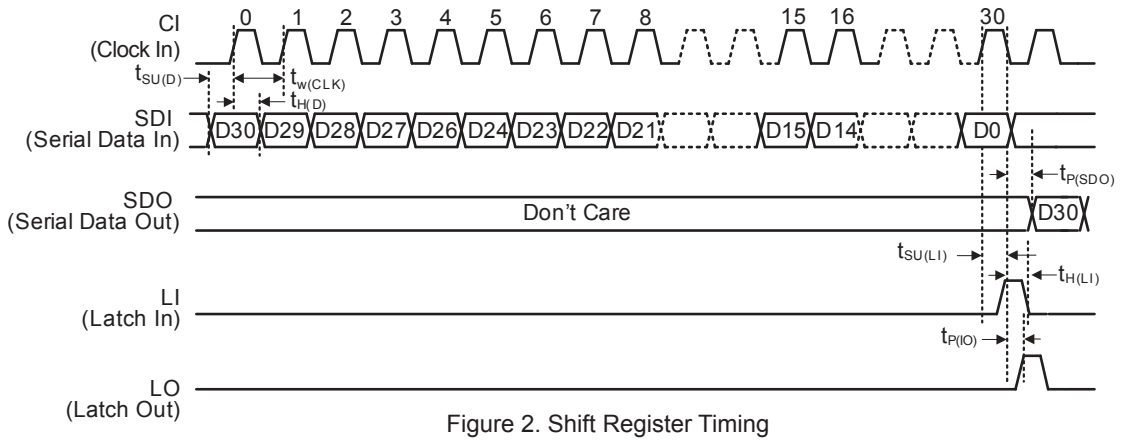


Figure 2. Shift Register Timing

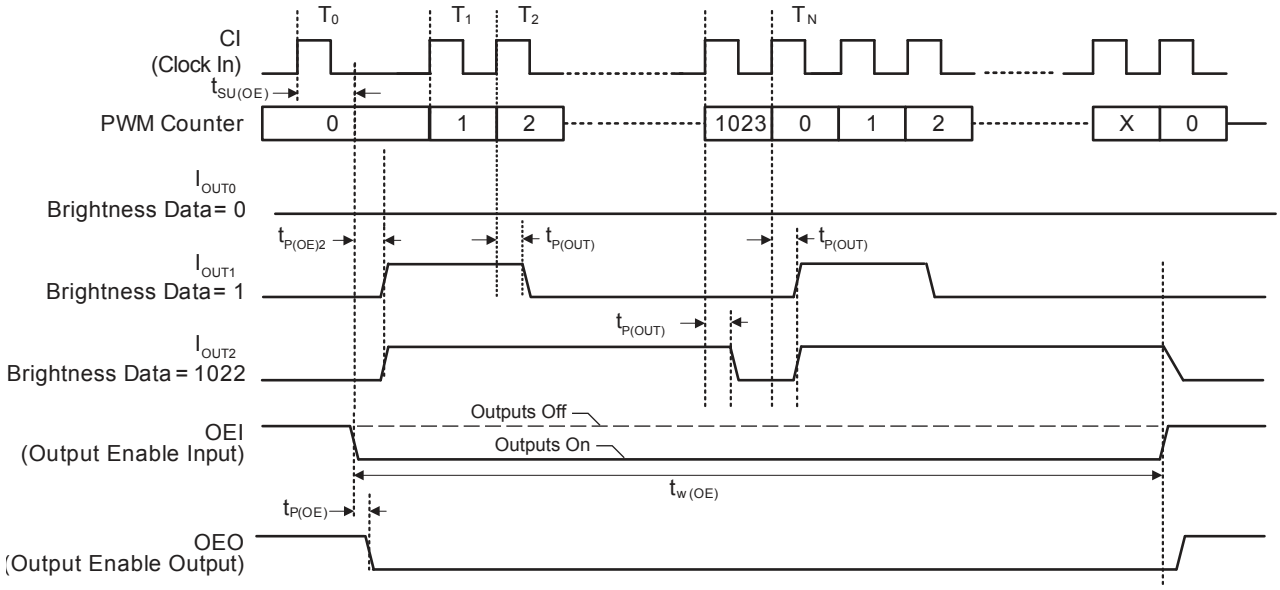


Figure 3. PWM Counter and Output Timing

NOTE: At least one rising edge on the CI pin is needed while OE is high in order to reset the PWM counter and start a new PWM cycle. Otherwise, when OE is brought low, the outputs will operate according to the current PWM data and PWM count, and will finish the current cycle before resetting the count to 0. Therefore, if the counter is not reset (as explained above) after new PWM data has been latched, the outputs will complete the current PWM cycle (up to 1024 clock pulses if no clock divider is selected, 2048 clock pulses if a divide-by count of 2 is selected, and so forth) before starting a new PWM cycle with the new data.

Functional Description

Shift Register

The A6280 has a 31 bit shift register that loads data through the SDI (Serial Data In) pin. The shift register operates by a first-in first-out (FIFO) method. The most significant bit (MSB, bit 30) is the first bit shifted in and the least significant bit (LSB, bit 0) is shifted in last. The serial data is clocked by a rising edge of the CI (Clock In) pin. The SDO (Serial Data Out) pin is updated to the state of bit 30 on the falling edge of the CI pin. This will prevent any race conditions and erroneous data that might occur while propagating information through multiple A6280 that are daisy chained together. The contents of the shift register will continue to propagate on every rising edge of the CI pin. The information in the shift register is latched on a rising edge of the LI (Latch In) pin. The LI pin must be brought low before the rising edge of the next clock pulse, to avoid latching erroneous data. The latched data remains latched on a rising OEI (Output Enable In) signal.

Output Buffers

The A6280 is designed to allow daisy chaining many A6280s together. It can pass the clock, data, latch, and output enable signals from one A6820 to the next without any loss of data due to duty cycle skewing or signal degradation.

The A6820 is equipped with output buffers that allow the data signals to travel over long distances through strings of A6280s without the need for extra driving hardware. The A6280 drives these signals to TTL levels. Each of the A6280 inputs have a corresponding buffered output:

- CI (Clock In) pin to CO (Clock Out) pin
- LI (Latch In) pin to LO (Latch Out) pin
- OEI (Output Enable In) pin to OEO (Output Enable Out) pin
- SDI (Serial Data In) pin to SDO (Serial Data Out) pin

The CO (Clock Out) pin is driven by an internal one-shot circuit. When the CI pin detects an edge rising through the input threshold, the one-shot circuitry drives the CO pin high for 100 ns. The CI pin input threshold has hysteresis to prevent false triggering of the CO signal. The implementation on the one-shot solution allows many A6280s to be daisy chained together with a consistent clock signal throughout the entire chain without degradation or loss of synchronicity to the data line.

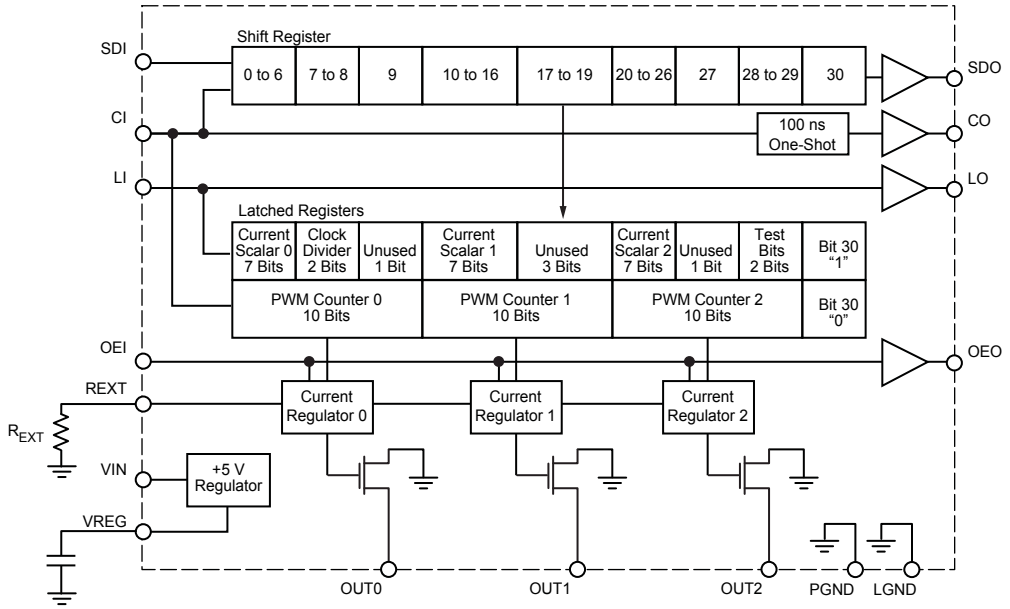


Figure 4. Functional Diagram

PWM Brightness Control

The A6280 controls the intensity of each LED by pulse width modulating the current of each output. The A6280 has three 10-bit brightness registers, one for each output. These brightness registers set the PWM count value at which the outputs switch off during each PWM cycle. Each 10-bit brightness register gives 1023 levels of light intensity. The duty cycle, DC (%), can be determined by the following equation:

$$DC = [(PWM_n + 1) / 1024] \times 100 \quad (\%),$$

where PWM_n is the PWM value greater than zero that is stored in the brightness register.

The relationship of the PWM_n value to the output duty cycle is given in the following table:

PWM_n	Duty Cycle
0	0/1024 (0 %)
1	2/1024
2	3/1024
. . .	. . .
1023	1024/1024 (100 %)

When the brightness register is set to zero, the outputs remain off for the duration of the PWM cycle for a 0% DC. When a brightness register is set to 1023, the LED for that output remains on (100% DC) when OEI is active and begins the PWM cycle. The output remains on when the PWM counter rolls over and begins a new count.

The PWM counter begins counting at zero and increments only when the OEI pin is held low. When the PWM counter reaches the count of 1024, the counter resets to zero and continues incrementing. The counter resets to zero on a rising edge of CI when OEI is high, upon recovery from UVLO, and when powering-up. Latching new data into the brightness registers will not reset the PWM counter.

Table 1. Clock Divider Configurations

Bits		Divide By Count
7	8	
0	0	÷ 1 (no division)
1	0	÷ 2
0	1	÷ 4
1	1	÷ 8

There is a programmable clock divider that can slow the PWM counter relative to the CI pin. See table 1 for bit assignments of the programmable clock divider. The PWM counter is incremented on every rising edge of the CI pin divided by the clock divider count value when the OEI pin is low. For example, if the clock divider is programmed to divide the CI by 2, then the PWM counter will increment once every 2 CI cycles. Given a 5 MHz CI frequency, the clock period would be 200 ns.

The clock divider data in the shift register is latched on a rising edge of the LI (Latch In) pin. The latched clock divider data remains latched on a rising OEI signal.

The total number of possible colors of an RGB pixel is over 1 billion. Refer to figure 6 for the mapping of shift register bits to latches.

Output Current Selection

The overall maximum current is set by the external resistor, R_{EXT}, connected between the REXT and LGND pins. Once set, the maximum current remains constant regardless of the LED voltage variation, supply voltage variation, temperature, or other circuit parameters that could otherwise affect LED current. The maximum output current can be calculated using the following equation:

$$I_{OUT}(max) = 753.12 / R_{EXT}.$$

The relationship of the value selected for R_{EXT} and I_{OUT} is shown in figure 5.

Internal Linear Regulator

The A6280 has a built-in linear regulator. The regulator operates from a supply voltage of 5.5 to 17 V. It allows the VIN pin of the A6280 to connect to the same supply as the LEDs. This simplifies board design by eliminating the need for a chip supply bus

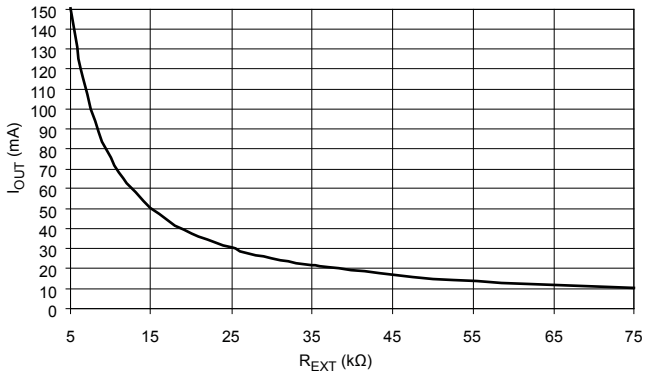


Figure 5. Output Current versus External Resistor, R_{EXT}

and external voltage regulators. For 5 V supplies, connect VIN to VREG externally. Note: When using 5 V supplies, ensure that VIN does not exceed the absolute maximum rating of the VREG pin (6 V).

The VREG pin is used by the internal linear regulator to connect to a bypass capacitor. This pin is for internal use only and is not intended as an external power source. There should be a 1.0 µF, 10 V ceramic capacitor connected between the VREG pin and LGND. The capacitor should be located as close to the VREG pin as possible.

Dot Correction Control

The A6280 can further control the maximum output current for each output by setting the three 7-bit dot correction registers with scale data that ranges from 36.5% to 100% of the overall maximum output current that is set by the R_{EXT} resistor. This feature is useful because not every type of LED (red, green, or blue, for example) has the same level of brightness for a given current, and the brightness could be different even from LED to LED of the same type. By scaling the output currents so that all the LEDs have matched intensities, the application will have full color depth when using the PWM counters. The dot correction current can be calculated by the following equation:

$$I_{OUTn} = I_{OUTn}(max) \times (Scale_n / 2 + 36.5) / 100$$

Where $Scale_n$ is in the range 0 to 127, as shown in the following table:

Scale	$I_{OUT}/I_{OUT}(max)$ (%)
0	36.5
1	37.0
2	37.5
. . .	. . .
127	100

Refer to figure 6 for the bit configurations for the scalar registers.

The dot correction data in the shift register is latched on a rising edge of the LI (Latch In) pin. The dot correction data remains latched on a rising OEI signal. The default output current when the A6280 is powered-up or recovers from a UVLO is 36.5% of the current set by the R_{EXT} resistor.

Package Power Dissipation

The maximum allowable package power dissipation is determined as:

$$P_D(max) = (150 - T_A) / R_{\theta JA} \ .$$

The actual package power dissipation is:

$$P_{D(act)} = DC_0 \times V_{DS0} \times I_{OUT0} + DC_1 \times V_{DS1} \times I_{OUT1} + DC_2 \times V_{DS2} \times I_{OUT2} + V_{IN} \times I_{IN} \ .$$

where DC_i is the PWM duty cycle for channel *i*, and I_{OUTi} is the output current for channel *i*, determined by the dot correction current for that channel and REXT.

When calculating power dissipation, the total number of available device outputs is usually used for the worst-case situation (i.e., displaying all 3 LEDs at 100% DC).

Thermal Shutdown (TSD)

When the junction temperature of the A6280 reaches the thermal shutdown temperature threshold, T_{JTSD} (165°C typical), the outputs will shut off until the junction temperature cools down below the recovery threshold, $T_{JTSD} - \Delta T_J$ (15°C typical). The shift register and output latches will remain active during the TSD event. Therefore there is no need to reset the data in the output latches.

Bits

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30[a]
PWM Counter 0										PWM Counter 1										PWM Counter 2										Address “0”
Dot Correction Register 0								Clock Mode	0	Dot Correction Register 1							0	0	0	Dot Correction Register 2							0	ATB[b]	ATB[b]	Address “1”

[a]Selects which word is written to: Dot Correction/Clock Mode selection or PWM counter.
[b]Allegro Test Bit (ATB). Reserved for Allegro internal testing. Always set to zero (0) in the application.

Figure 6. Register Configuration

Undervoltage Lockout

The A6280 includes an internal undervoltage lockout (UVLO) circuit that disables the driver outputs in the event of the logic supply voltage dropping below a minimum acceptable level. This prevents the display of erroneous information, a necessary function for some critical applications. The shift register will not shift any data in a UVLO condition. Upon recovery of the logic supply voltage and on power up, the internal shift register and all latches will be set to zero.

Ballast Resistors

The voltage on the outputs should be kept in the range 1 to 3 V. If the voltage goes below 1V, the current will begin to rolloff as the driver runs out of headroom. At V_{OUT} above 3 V, the power dissipation may become a problem, as each output contributes $V_{OUT} \times I_{LED}$ of power loss in the output sink driver. Typically the power supply nominal voltage is chosen to keep the output voltage in this range. Alternatively, series resistors can be added to dissipate the extra power and keep the output voltage within the recommended range.

Application Information

Timing Considerations

A6280s can be used in large numbers to drive many LEDs with the control signals connected serially together, with short cables between each pixel (see figure 8). Because the clock negative edge drives the data to the SDO (Serial Data Out) pin, and the CO pin is driven by a 100 ns one-shot function, the clock and data signals remain synchronized with each other as you move from the first pixel in the chain to the last.

After all of the data is written to each A6280 in the chain, the data is latched into each A6280 via a low-to-high transition on the LI pin. The LO pin of pixel #1 drives the LI pin of pixel #2, and so on down the chain. These signals are buffered and are driven asynchronously relative to the CI and SDI pins. Therefore the mismatch in delays between CO and LO must be taken into consideration.

Although the mismatches in delays are quite small, they must be considered when creating the timing pattern for driving the chain. The key parameter is the setup time from the last CI clock rising edge to the rising edge of LI.

The minimum A6280 setup time from CI to LI is 20 ns. There may be a 5 ns per pixel mismatch in the propagation delays of the CI and LI signals (the delay from CI to CO compared to the delay from LI to LO). As a rule of thumb, use a setup time, t_{su}, at the first A6280 in the chain as calculated below:

$$t_{su} = 20 \text{ ns} + n \times 5 \text{ ns} \ ,$$

where n is the number of pixels in the chain.

This will ensure that the setup time at the last pixel in the chain is at least 20 ns.

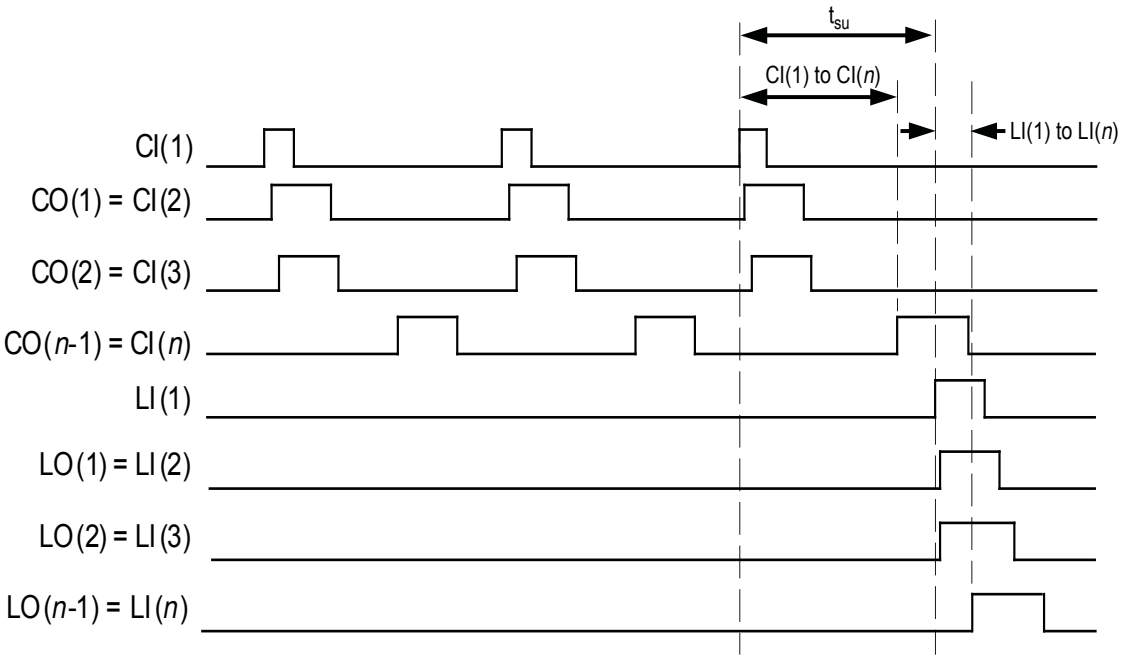


Figure 7. Signal Delay Mismatch Timing Diagram. t_{su} is the setup time for signals (CI to LI) applied to the first pixel in the chain. Note the difference in delay for CI(1) to CI(n) compared to the delay for LI(1) to LI(n). This must be compensated by increasing t_{su}.

Applications Drawings

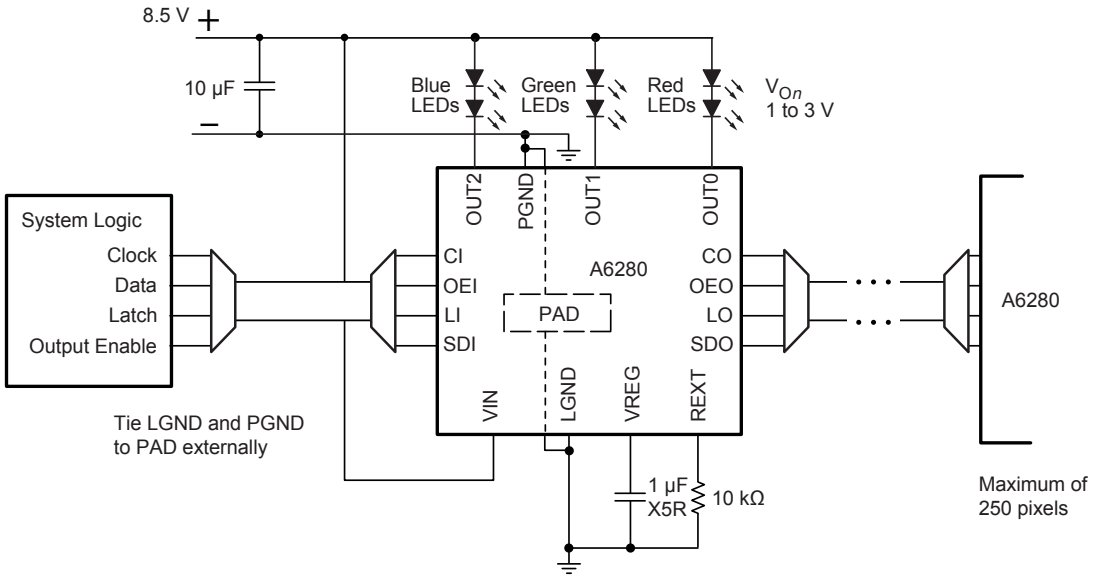


Figure 8. Application Driving 3 RGB LEDs at 75 mA Peak

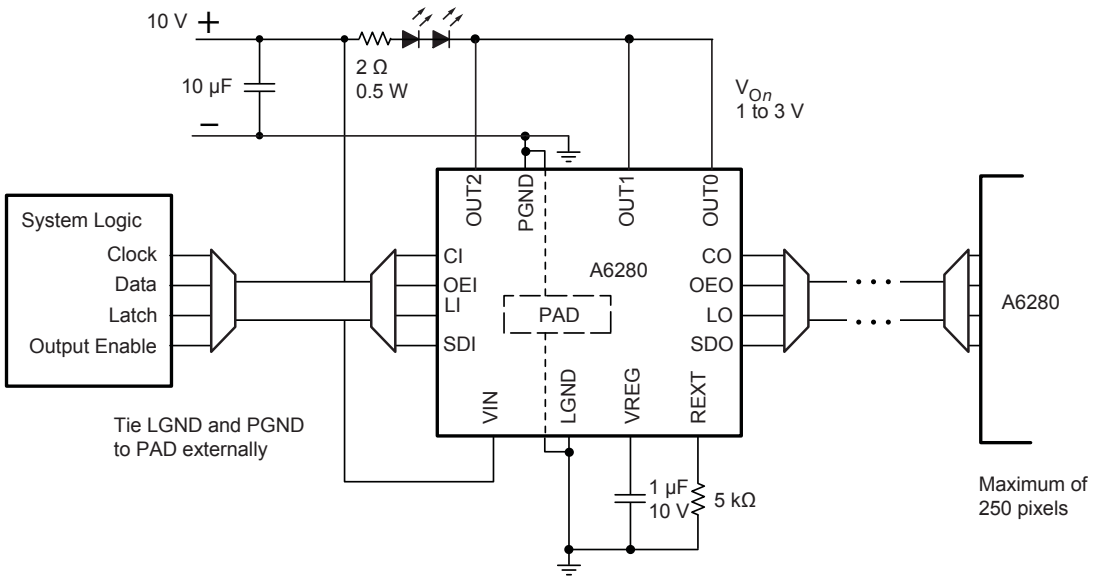
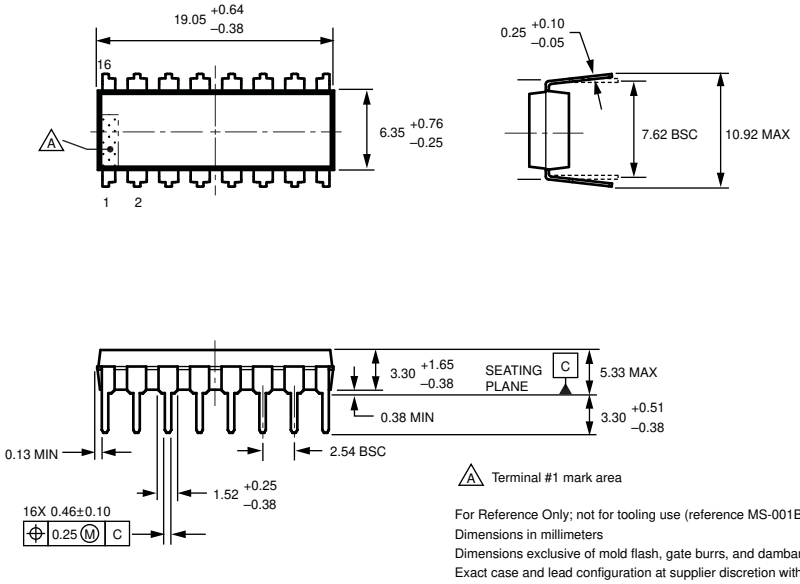


Figure 9. Application Driving High Power LED at 450 mA

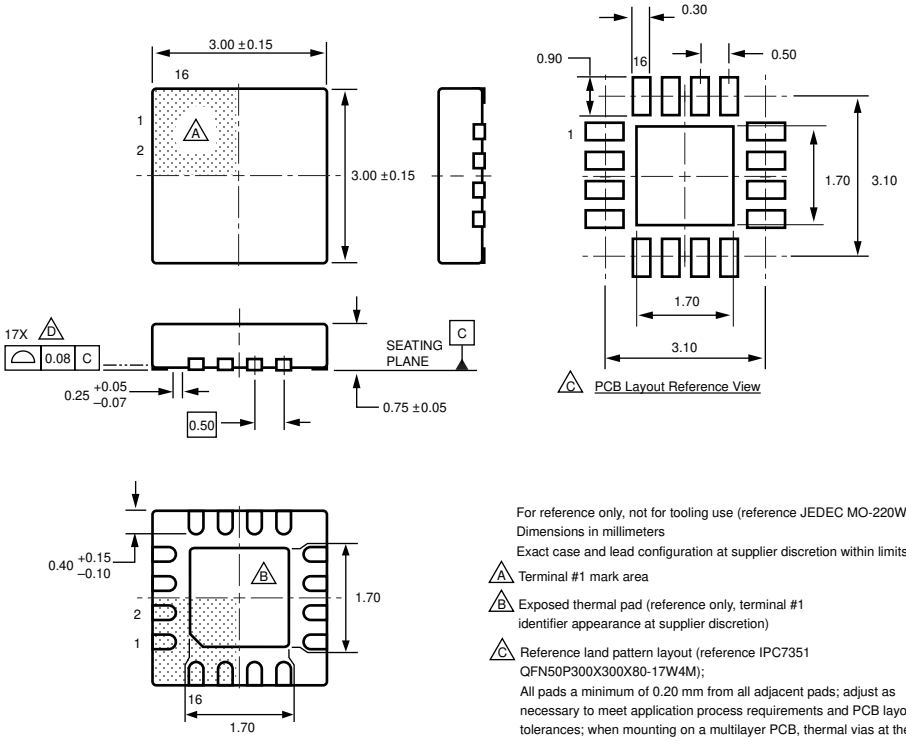
A Package, 16-Pin DIP



A Terminal #1 mark area

For Reference Only; not for tooling use (reference MS-001BB)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

ES Package, 16-Contact QFN



For reference only, not for tooling use (reference JEDEC MO-220WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Revision History

Revision	Revision Date	Description of Revision
Rev. 7	June 3, 2013	Update package availability

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