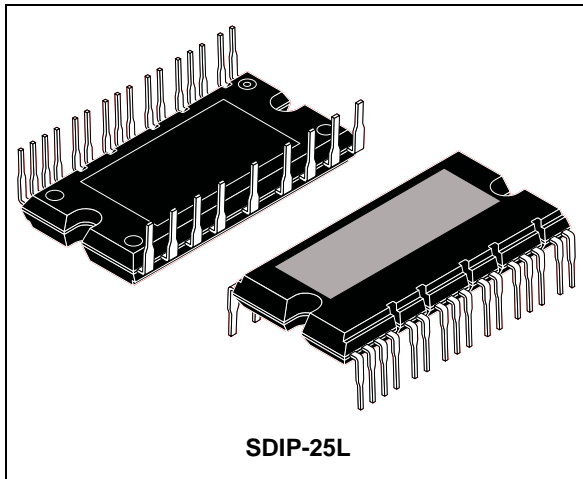


SLLIMM™ small low-loss intelligent molded module IPM, 3-phase inverter - 15 A, 600 V short-circuit rugged IGBT

Datasheet - production data



Applications

- 3-phase inverters for motor drives
- Home appliance, air conditioners

Description

This intelligent power module provides a compact, high performance AC motor drive in a simple, rugged design. Combining ST proprietary control ICs with the most advanced short-circuit-rugged IGBT system technology, this device is ideal for 3-phase inverters in applications such as motor drives and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

Features

- IPM 15 A, 600 V 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- Short-circuit rugged IGBTs
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull-down / pull-up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Smart shutdown function
- Comparator for fault protection against overtemperature and overcurrent
- DBC leading to low thermal resistance
- Isolation rating of 2500 V_{rms}/min
- UL recognized: UL1557 file E81734

Table 1. Device summary

| Order code | Marking | Package | Packing |
|-------------|-----------|----------|---------|
| STGIPS15C60 | GIPS15C60 | SDIP-25L | Tube |

Contents

- 1 Internal block diagram and pin configuration 3**
- 2 Electrical ratings 5**
 - 2.1 Absolute maximum ratings 5
 - 2.2 Thermal data 6
- 3 Electrical characteristics 7**
 - 3.1 Control part 9
 - 3.2 Waveform definitions 11
- 4 Smart shutdown function 12**
- 5 Application information 14**
 - 5.1 Recommendations 15
- 6 Package information 16**
 - 6.1 SDIP-25L package information 16
 - 6.2 Packing information 18
- 7 Revision history 19**

1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

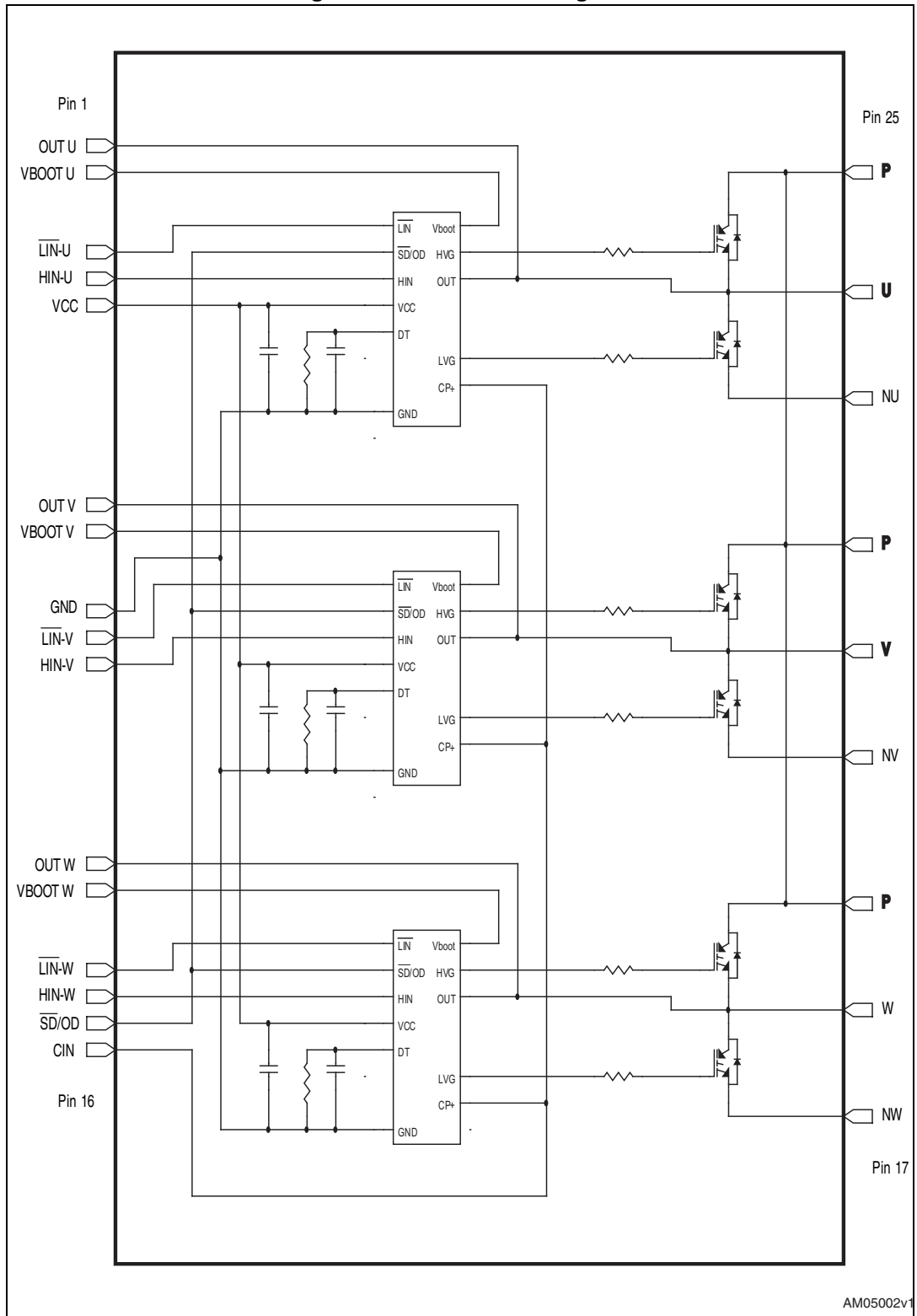
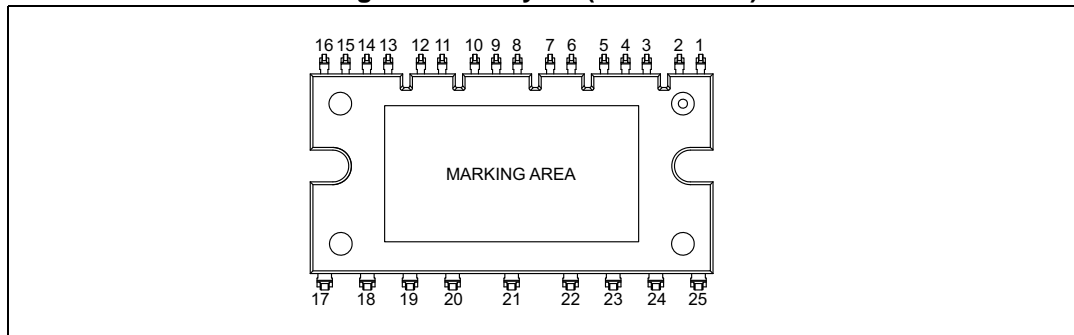


Table 2. Pin description

| Pin n° | Symbol | Description |
|--------|------------------------------------|--|
| 1 | OUT _U | High-side reference output for U phase |
| 2 | V _{bootU} | Bootstrap voltage for U phase |
| 3 | $\overline{\text{LIN}}_{\text{U}}$ | Low-side logic input for U phase |
| 4 | HIN _U | High-side logic input for U phase |
| 5 | V _{CC} | Low voltage power supply |
| 6 | OUT _V | High-side reference output for V phase |
| 7 | V _{boot V} | Bootstrap voltage for V phase |
| 8 | GND | Ground |
| 9 | $\overline{\text{LIN}}_{\text{V}}$ | Low-side logic input for V phase |
| 10 | HIN _V | High-side logic input for V phase |
| 11 | OUT _W | High-side reference output for W phase |
| 12 | V _{boot W} | Bootstrap voltage for W phase |
| 13 | $\overline{\text{LIN}}_{\text{W}}$ | Low-side logic input for W phase |
| 14 | HIN _W | High-side logic input for W phase |
| 15 | $\overline{\text{SD}} / \text{OD}$ | Shutdown logic input (active low) / open-drain (comparator output) |
| 16 | CIN | Comparator input |
| 17 | N _W | Negative DC input for W phase |
| 18 | W | W phase output |
| 19 | P | Positive DC input |
| 20 | N _V | Negative DC input for V phase |
| 21 | V | V phase output |
| 22 | P | Positive DC input |
| 23 | N _U | Negative DC input for U phase |
| 24 | U | U phase output |
| 25 | P | Positive DC input |

Figure 2. Pin layout (bottom view)



2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

| Symbol | Parameter | Value | Unit |
|--------------------|--|-------|---------------|
| V_{PN} | Supply voltage applied between P - N_U , N_V , N_W | 450 | V |
| $V_{PN(surge)}$ | Supply voltage (surge) applied between P - N_U , N_V , N_W | 500 | V |
| V_{CES} | Each IGBT collector emitter voltage ($V_{IN}^{(1)} = 0$) | 600 | V |
| $\pm I_C$ | Each IGBT continuous collector current at $T_C = 25^\circ\text{C}$ | 15 | A |
| $\pm I_{CP}^{(2)}$ | Each IGBT pulsed collector current | 30 | A |
| P_{TOT} | Each IGBT total dissipation at $T_C = 25^\circ\text{C}$ | 42 | W |
| t_{scw} | Short circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$ $T_J = 125^\circ\text{C}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN(1)} = 0 - 5\text{ V}$ | 5 | μs |

1. Applied between HIN_i , \overline{LIN}_i and GND for $i = U, V, W$
2. Pulse width limited by max junction temperature

Table 4. Control part

| Symbol | Parameter | Value | Unit |
|------------------------|---|-------------------------------------|------|
| V_{OUT} | Output voltage applied between OUT_U , OUT_V , OUT_W - GND | $V_{boot} - 21$ to $V_{boot} + 0.3$ | V |
| V_{CC} | Low voltage power supply | - 0.3 to +21 | V |
| V_{CIN} | Comparator input voltage | - 0.3 to $V_{CC} + 0.3$ | V |
| V_{boot} | Bootstrap voltage applied between $V_{boot\ i} - OUT_i$ for $i = U, V, W$ | - 0.3 to 620 | V |
| V_{IN} | Logic input voltage applied between HIN , \overline{LIN} and GND | - 0.3 to 15 | V |
| $V_{\overline{SD}/OD}$ | Open drain voltage | - 0.3 to 15 | V |
| dV_{OUT}/dt | Allowed output slew rate | 50 | V/ns |

Table 5. Total system

| Symbol | Parameter | Value | Unit |
|-----------|--|-------------|------------------|
| V_{ISO} | Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, $t = 60\text{ s}$) | 2500 | V |
| T_J | Power chips operating junction temperature | - 40 to 150 | $^\circ\text{C}$ |
| T_C | Module case operation temperature | - 40 to 125 | $^\circ\text{C}$ |

2.2 Thermal data

Table 6. Thermal data

| Symbol | Parameter | Value | Unit |
|------------|---|-------|------|
| R_{thJC} | Thermal resistance junction-case single IGBT | 3 | °C/W |
| | Thermal resistance junction-case single diode | 5.5 | °C/W |

3 Electrical characteristics

$T_J = 25\text{ °C}$ unless otherwise specified.

Table 7. Inverter part

| Symbol | Parameter | Test conditions | Value | | | Unit |
|---|--|---|-------|------|------|---------------|
| | | | Min. | Typ. | Max. | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 - 5\text{ V}$, $I_C = 15\text{ A}$ | - | 1.6 | 2 | V |
| | | $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 - 5\text{ V}$, $I_C = 15\text{ A}$, $T_J = 125\text{ °C}$ | - | 1.7 | | |
| I_{CES} | Collector-cut off current ($V_{IN}^{(1)} = 0$ "logic state") | $V_{CE} = 550\text{ V}$, $V_{CC} = V_{Boot} = 15\text{ V}$ | - | | 100 | μA |
| V_F | Diode forward voltage | $V_{IN}^{(1)} = 0$ "logic state", $I_C = 15\text{ A}$ | - | | 2.3 | V |
| Inductive load switching time and energy | | | | | | |
| t_{on} | Turn-on time | $V_{PN} = 300\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 - 5\text{ V}$, $I_C = 15\text{ A}$ (see Figure 3) | - | 330 | - | ns |
| $t_{c(on)}$ | Crossover time (on) | | - | 150 | - | |
| t_{off} | Turn-off time | | - | 925 | - | |
| $t_{c(off)}$ | Crossover time (off) | | - | 135 | - | |
| t_{rr} | Reverse recovery time | | - | 190 | - | μJ |
| E_{on} | Turn-on switching losses | | - | 385 | - | |
| E_{off} | Turn-off switching losses | | - | 294 | - | |

1. Applied between HIN_i , \overline{LIN}_i and GND for $i = U, V, W$. (\overline{LIN} inputs are active-low).

Note: t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

Figure 3. Switching time test circuit

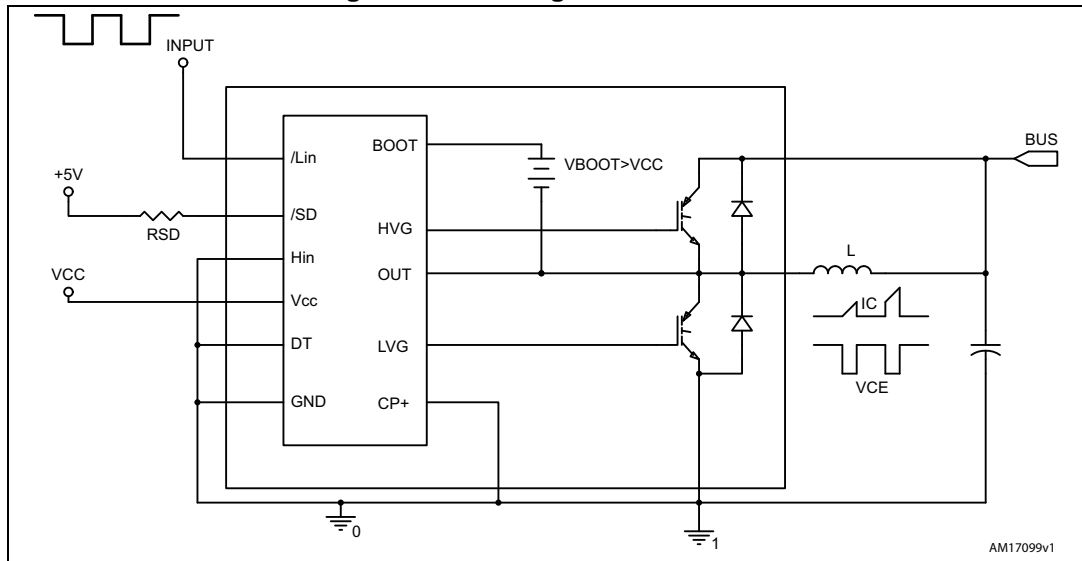
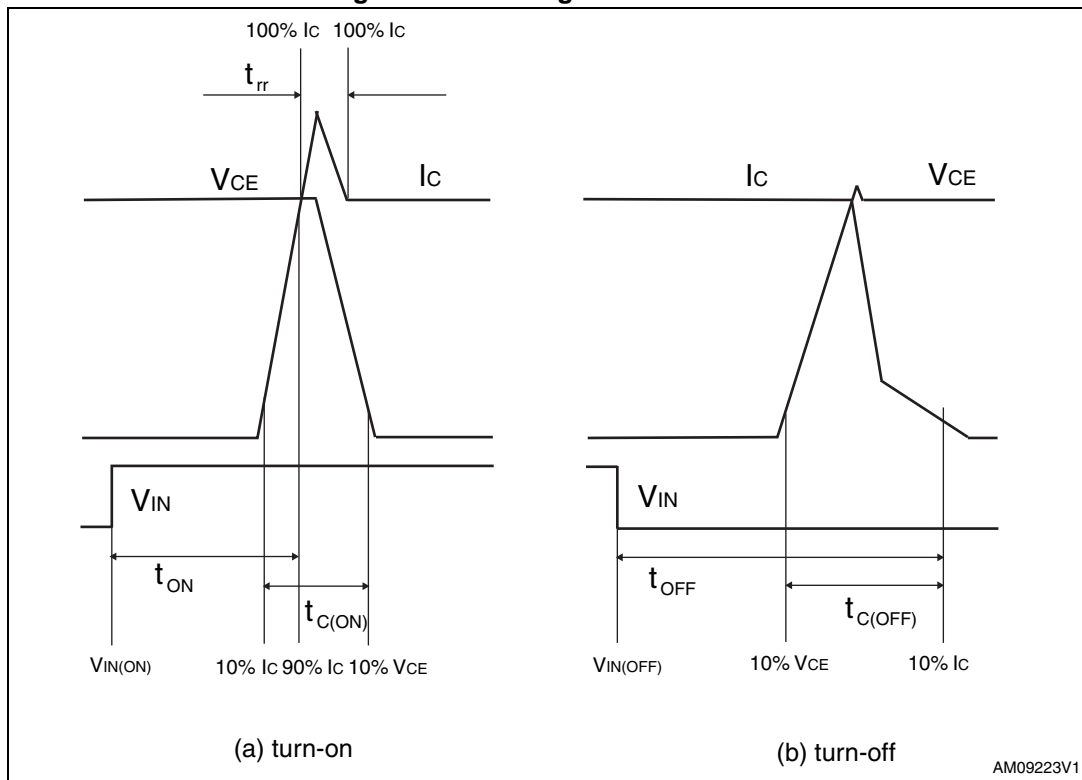


Figure 4. Switching time definition



Note: Figure 4 "Switching time definition" refers to HIN inputs (active high). For LIN inputs (active low), VIN polarity must be inverted for turn-on and turn-off.

3.1 Control part

Table 8. Low voltage power supply ($V_{CC} = 15\text{ V}$ unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|---|--|------|------|------|---------------|
| V_{CC_hys} | V_{CC} UV hysteresis | | 1.2 | 1.5 | 1.8 | V |
| V_{CC_thON} | V_{CC} UV turn ON threshold | | 11.5 | 12 | 12.5 | V |
| V_{CC_thOFF} | V_{CC} UV turn OFF threshold | | 10 | 10.5 | 11 | V |
| I_{qccu} | Undervoltage quiescent supply current | $V_{CC} = 10\text{ V}$ $\overline{SD}/OD = 5\text{ V}$; $\overline{LIN} = 5\text{ V}$; $H_{IN} = 0$, $C_{IN} = 0$ | | | 450 | μA |
| I_{qcc} | Quiescent current | $V_{CC} = 15\text{ V}$ $\overline{SD}/OD = 5\text{ V}$; $\overline{LIN} = 5\text{ V}$ $H_{IN} = 0$, $C_{IN} = 0$ | | | 3.5 | mA |
| V_{ref} | Internal comparator (CIN) reference voltage | | 0.5 | 0.54 | 0.58 | V |

Table 9. Bootstrapped voltage ($V_{CC} = 15\text{ V}$ unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|---|--|------|------|------|---------------|
| V_{BS_hys} | V_{BS} UV hysteresis | | 1.2 | 1.5 | 1.8 | V |
| V_{BS_thON} | V_{BS} UV turn ON threshold | | 11.1 | 11.5 | 12.1 | V |
| V_{BS_thOFF} | V_{BS} UV turn OFF threshold | | 9.8 | 10 | 10.6 | V |
| I_{QBSU} | Undervoltage V_{BS} quiescent current | $V_{BS} < 9\text{ V}$ $\overline{SD}/OD = 5\text{ V}$; \overline{LIN} and $H_{IN} = 5\text{ V}$; $C_{IN} = 0$ | | 70 | 110 | μA |
| I_{QBS} | V_{BS} quiescent current | $V_{BS} = 15\text{ V}$ $\overline{SD}/OD = 5\text{ V}$; \overline{LIN} and $H_{IN} = 5\text{ V}$; $C_{IN} = 0$ | | 200 | 300 | μA |
| $R_{DS(on)}$ | Bootstrap driver on resistance | $LIN = 5\text{ V}$; $HIN = 0\text{ V}$ | | 120 | | Ω |

Table 10. Logic inputs ($V_{CC} = 15\text{ V}$ unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------|---|---|------|------|------|---------------|
| V_{il} | Low level logic threshold voltage | | 0.8 | | 1.1 | V |
| V_{ih} | High level logic threshold voltage | | 1.9 | | 2.25 | V |
| I_{HINh} | HIN logic "1" input bias current | $HIN = 15\text{ V}$ | 110 | 175 | 260 | μA |
| I_{HINl} | HIN logic "0" input bias current | $HIN = 0\text{ V}$ | | | 1 | μA |
| I_{LINl} | \overline{LIN} logic "1" input bias current | $\overline{LIN} = 0\text{ V}$ | 3 | 6 | 20 | μA |
| I_{LINh} | \overline{LIN} logic "0" input bias current | $\overline{LIN} = 15\text{ V}$ | | | 1 | μA |
| I_{SDh} | \overline{SD} logic "0" input bias current | $\overline{SD} = 15\text{ V}$ | 30 | 120 | 300 | μA |
| I_{SDl} | \overline{SD} logic "1" input bias current | $\overline{SD} = 0\text{ V}$ | | | 3 | μA |
| Dt | Dead time | see Figure 5 and Table 13 | | 1.2 | | μs |

Table 11. Sense comparator characteristics ($V_{CC} = 15\text{ V}$ unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|---|------|------|------|--------------------|
| I_{ib} | Input bias current | $V_{CIN} = 1\text{ V}$ | - | | 3 | μA |
| V_{ol} | Open-drain low-level output voltage | $I_{od} = 3\text{ mA}$ | - | | 0.5 | V |
| t_{d_comp} | Comparator delay | $\overline{\text{SD/OD}}$ pulled to 5 V through 100 k Ω resistor | - | 90 | 130 | ns |
| SR | Slew rate | $C_L = 180\text{ pF}$; $R_{pu} = 5\text{ k}\Omega$ | - | 60 | | V/ μsec |
| t_{sd} | Shut down to high / low side driver propagation delay | $V_{OUT} = 0$, $V_{boot} = V_{CC}$, $V_{IN} = 0$ to 3.3 V | 50 | 125 | 200 | ns |
| t_{isd} | Comparator triggering to high / low side driver turn-off propagation delay | Measured applying a voltage step from 0 V to 3.3 V to pin CIN | 50 | 200 | 250 | |

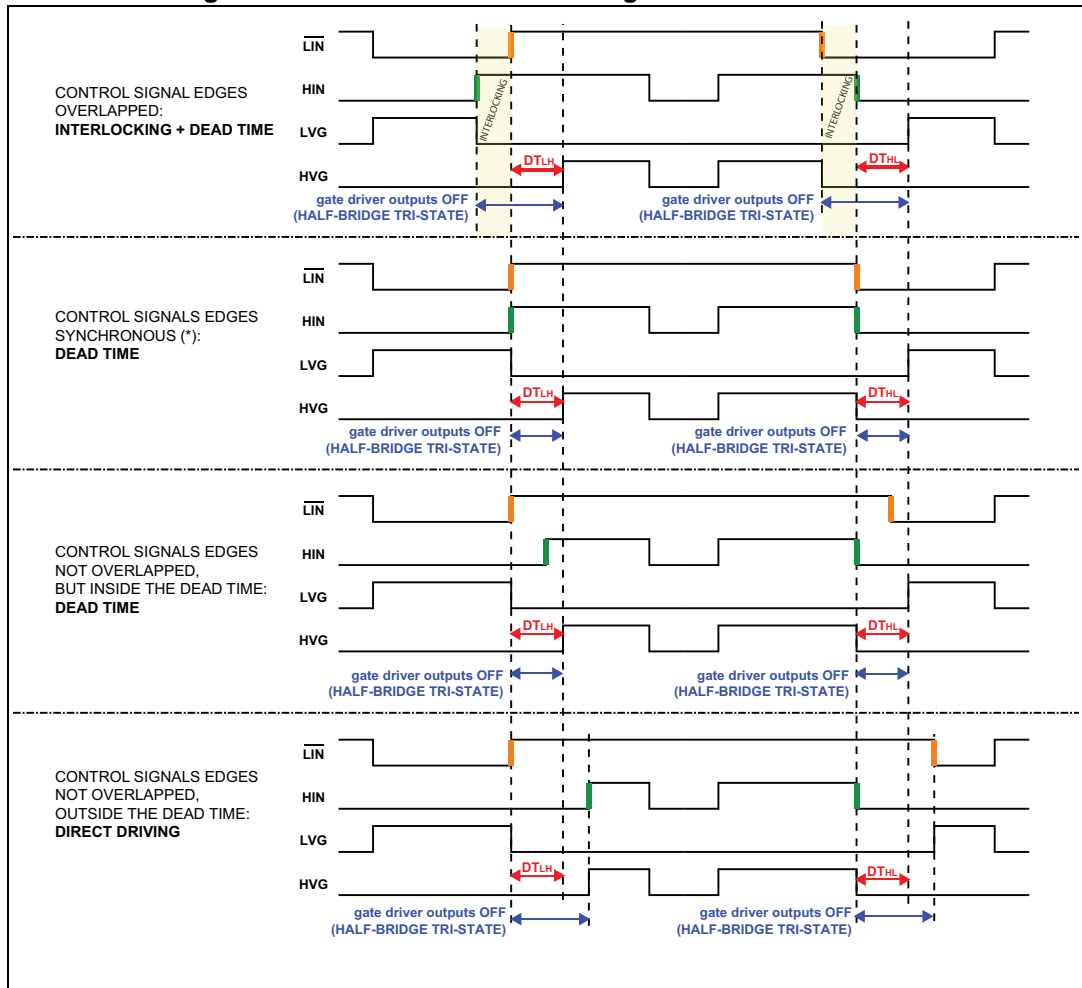
Table 12. Truth table

| Condition | Logic input (V_I) | | | Output | |
|--|---------------------------|-------------------------|-----|--------|-----|
| | $\overline{\text{SD/OD}}$ | $\overline{\text{LIN}}$ | HIN | LVG | HVG |
| Shutdown enable half-bridge tri-state | L | X | X | L | L |
| Interlocking half-bridge tri-state | H | L | H | L | L |
| 0 "logic state" half-bridge tri-state | H | H | L | L | L |
| 1 "logic state" low side direct driving | H | L | L | H | L |
| 1 "logic state" high side direct driving | H | H | H | L | H |

Note: X: don't care

3.2 Waveform definitions

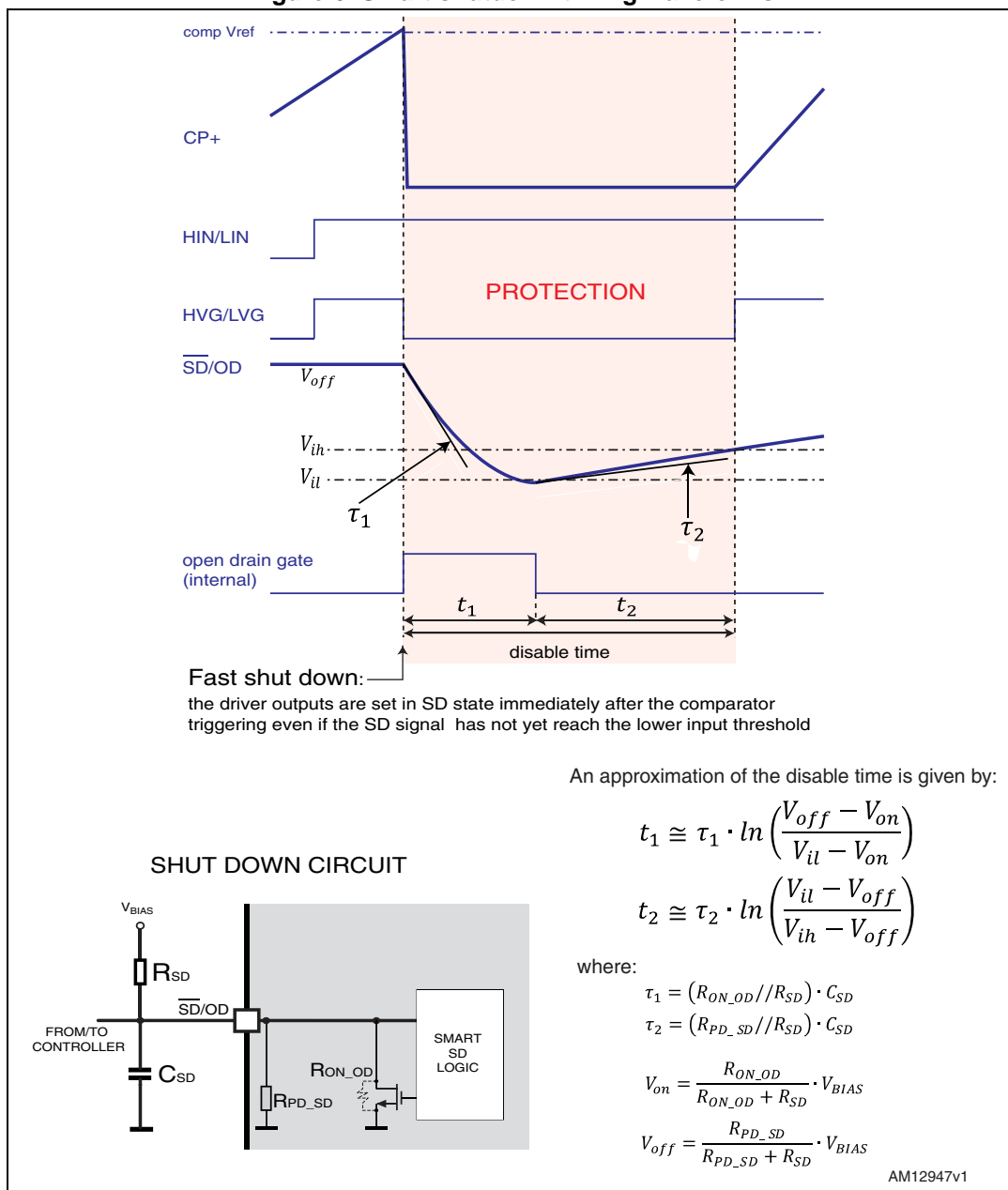
Figure 5. Dead time and interlocking waveforms definition



4 Smart shutdown function

The STGIPS15C60 integrates a comparator for fault sensing purposes. The comparator has an internal voltage reference V_{ref} connected to the inverting input, while the non-inverting input, available on pin (C_{IN}), can be connected to an external shunt resistor in order to implement a simple over-current protection function. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low-level leading the halfbridge in tri-state. In the common overcurrent protection architectures the comparator output is usually connected to the shutdown input through a RC network, in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Our smart shutdown architecture allows to immediately turn-off the output gate driver in case of overcurrent, the fault signal has a preferential path which directly switches off the outputs. The time delay between the fault and the outputs turn-off is no more dependent on the RC values of the external network connected to the shutdown pin. At the same time the DMOS connected to the open-drain output (pin $\overline{SD/OD}$) is turned on by the internal logic which holds it on until the shutdown voltage is lower than the logic input lower threshold (V_{il}). Finally the smart shutdown function provides the possibility to increase the real disable time without increasing the constant time of the external RC network.

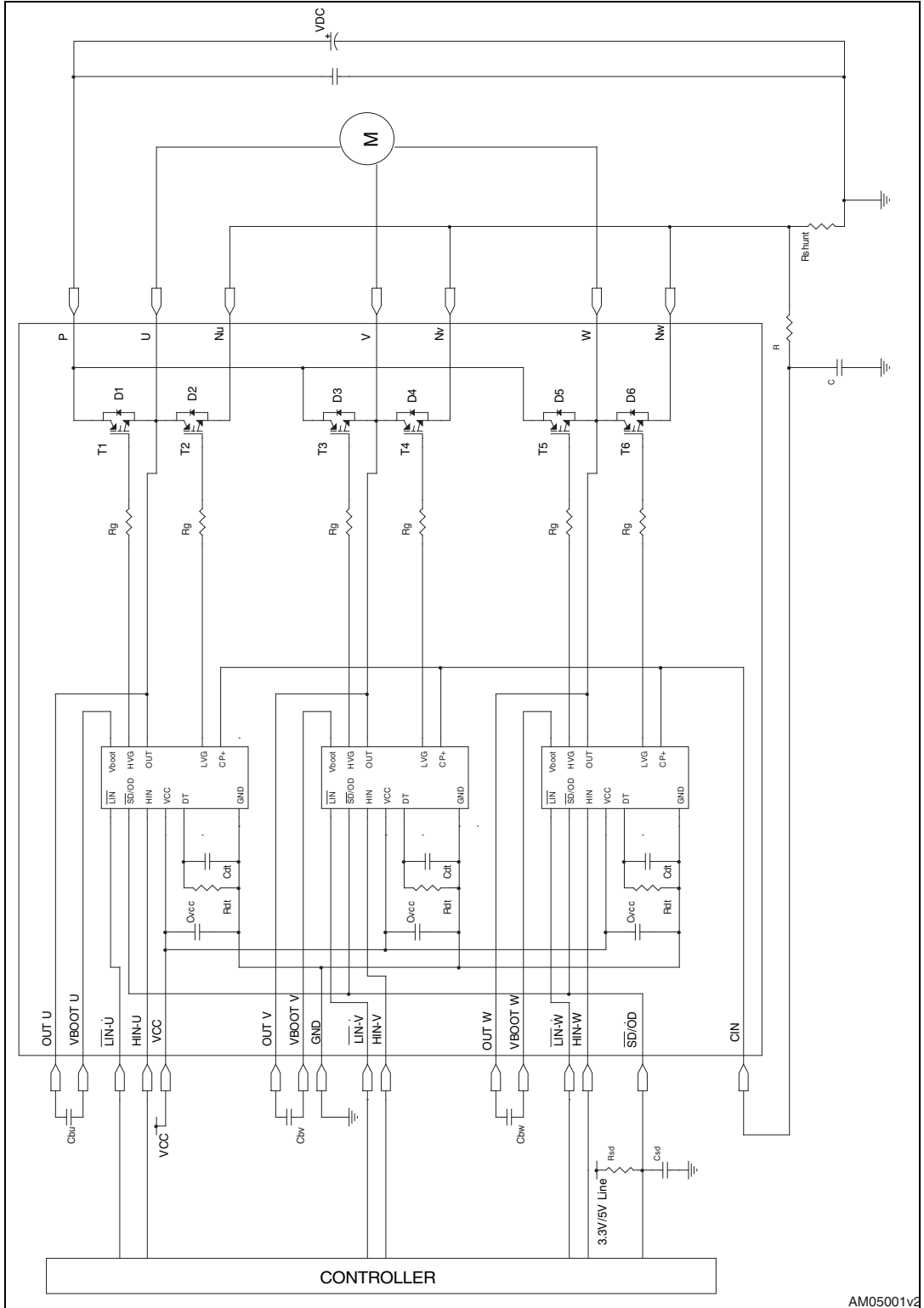
Figure 6. Smart shutdown timing waveforms



Please refer to [Table 11](#) for internal propagation delay time details.

5 Application information

Figure 7. Typical application circuit



AM05001v2

5.1 Recommendations

- Input signal HIN is active high logic. A 85 k Ω (typ.) pull down resistor is built-in for each high side input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.
- Input signal $\overline{\text{LIN}}$ is active low logic. A 720 k Ω (typ.) pull-up resistor, connected to an internal 5 V regulator through a diode, is built-in for each low side input.
- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The $\overline{\text{SD/OD}}$ signal should be pulled up to 5 V / 3.3 V with an external resistor (see [Section 4: Smart shutdown function](#) for detailed info).

Table 13. Recommended operating conditions

| Symbol | Parameter | Conditions | Value | | | Unit |
|-------------------|------------------------------------|--|-------|------|------|---------------|
| | | | Min. | Typ. | Max. | |
| V _{PN} | Supply Voltage | Applied between P-Nu,Nv,Nw | | 300 | 400 | V |
| V _{CC} | Control supply voltage | Applied between V _{CC} -GND | 13.5 | 15 | 18 | V |
| V _{BS} | High side bias voltage | Applied between V _{BOOTi} -OUT _i for i=U,V,W | 13 | | 18 | V |
| t _{dead} | Blanking time to prevent Arm-short | For each input signal | 1.5 | | | μs |
| f _{PWM} | PWM input signal | -40°C < T _c < 100°C -40°C < T _j < 125°C | | | 20 | kHz |
| T _C | Case operation temperature | | | | 100 | °C |

Note: For further details refer to AN3338.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

6.1 SDIP-25L package information

Figure 8. SDIP-25L package outline

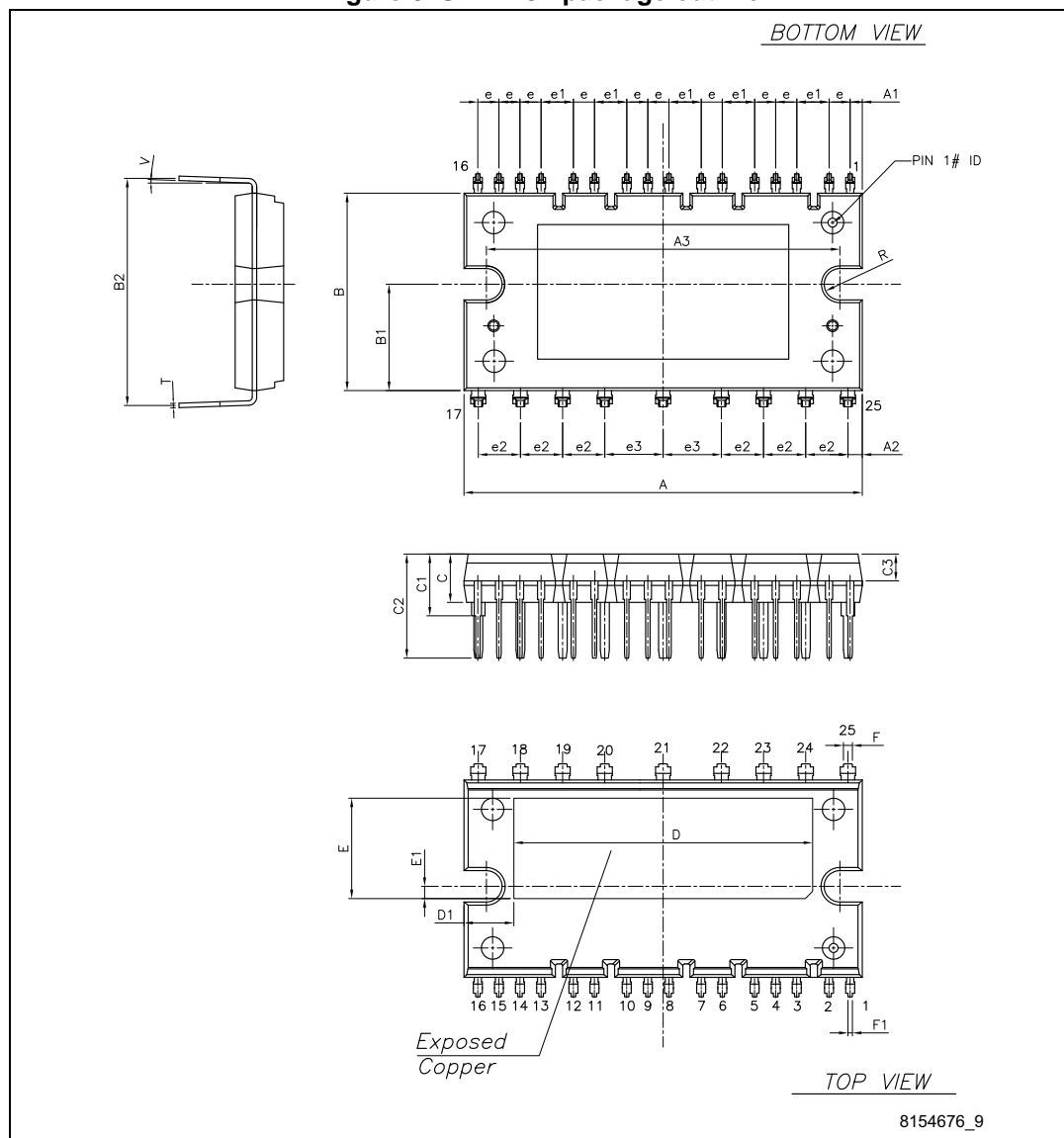
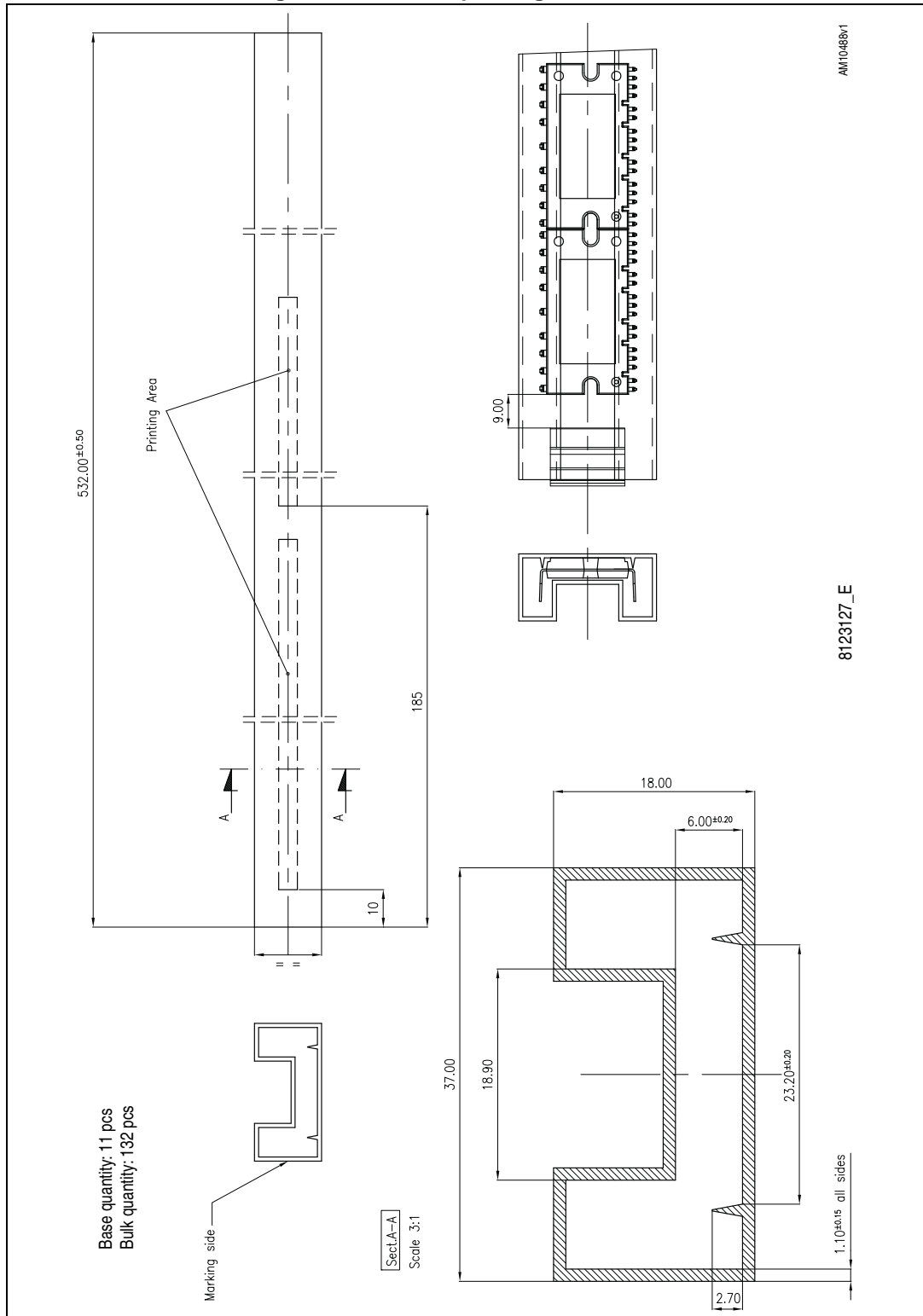


Table 14. SDIP-25L mechanical data

| Dim. | mm | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 43.90 | 44.40 | 44.90 |
| A1 | 1.15 | 1.35 | 1.55 |
| A2 | 1.40 | 1.60 | 1.80 |
| A3 | 38.90 | 39.40 | 39.90 |
| B | 21.50 | 22.00 | 22.50 |
| B1 | 11.25 | 11.85 | 12.45 |
| B2 | 24.83 | 25.23 | 25.63 |
| C | 5.00 | 5.40 | 6.00 |
| C1 | 6.50 | 7.00 | 7.50 |
| C2 | 11.20 | 11.70 | 12.20 |
| C3 | 2.90 | 3.00 | 3.10 |
| e | 2.15 | 2.35 | 2.55 |
| e1 | 3.40 | 3.60 | 3.80 |
| e2 | 4.50 | 4.70 | 4.90 |
| e3 | 6.30 | 6.50 | 6.70 |
| D | | 33.30 | |
| D1 | | 5.55 | |
| E | | 11.20 | |
| E1 | | 1.40 | |
| F | 0.85 | 1.00 | 1.15 |
| F1 | 0.35 | 0.50 | 0.65 |
| R | 1.55 | 1.75 | 1.95 |
| T | 0.45 | 0.55 | 0.65 |
| V | 0° | | 6° |

6.2 Packing information

Figure 9. SDIP-25L packing information



7 Revision history

Table 15. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 19-Aug-2013 | 1 | Initial release. |
| 16-May-2014 | 2 | Updated Table 3: Inverter part , Table 6: Thermal data , Table 7: Inverter part and Section 6.2: Packing information . Minor text changes. |
| 09-Apr-2015 | 3 | Text edits and formatting changes throughout document Updated Figure 2: Pin layout (bottom view) Updated Section 6: Package information |

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