

## FEATURES

- JESD204B (Subclass 1) coded serial digital outputs**
- 1.5 W total power per channel at 1 GSPS (default settings)**
- SFDR**
  - 79 dBFS at 340 MHz (1 GSPS)**
  - 85 dBFS at 340 MHz (500 MSPS)**
- SNR**
  - 63.4 dBFS at 340 MHz ( $A_{IN} = -1.0$  dBFS, 1 GSPS)**
  - 65.6 dBFS at 340 MHz ( $A_{IN} = -1.0$  dBFS, 500 MSPS)**
- ENOB = 10.4 bits at 10 MHz (1 GSPS)**
- DNL =  $\pm 0.16$  LSB; INL =  $\pm 0.35$  LSB (1 GSPS)**
- Noise density**
  - 151 dBFS/Hz (1 GSPS)**
  - 150 dBFS/Hz (500 MSPS)**
- 1.25 V, 2.5 V, and 3.3 V dc supply operation**
- Low swing full-scale input**
  - 1.34 V p-p typical (1 GSPS)**
  - 1.63 V p-p typical (500 MSPS)**
- No missing codes**
- Internal ADC voltage reference**
- Flexible termination impedance**
  - 400  $\Omega$ , 200  $\Omega$ , 100  $\Omega$ , and 50  $\Omega$  differential**
- 2 GHz usable analog input full power bandwidth**
- 95 dB channel isolation/crosstalk**
- Amplitude detect bits for efficient AGC implementation**
- Differential clock input**
- Optional decimate by 2 DDC per channel**
- Differential clock input**
- Integer clock divide by 1, 2, 4, or 8**
- Flexible JESD204B lane configurations**
- Small signal dither**

## APPLICATIONS

- Communications**
- Diversity multiband, multimode digital receivers**
  - 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE**
- Point to point radio systems**
- Digital predistortion observation path**
- General-purpose software radios**
- Ultrawideband satellite receiver**
- Instrumentation (spectrum analyzers, network analyzers,  
integrated RF test solutions)**
- Digital oscilloscopes**
- High speed data acquisition systems**
- DOCSIS 3.0 CMTS upstream receive paths**
- HFC digital reverse path receivers**

Rev. B

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## FUNCTIONAL BLOCK DIAGRAM

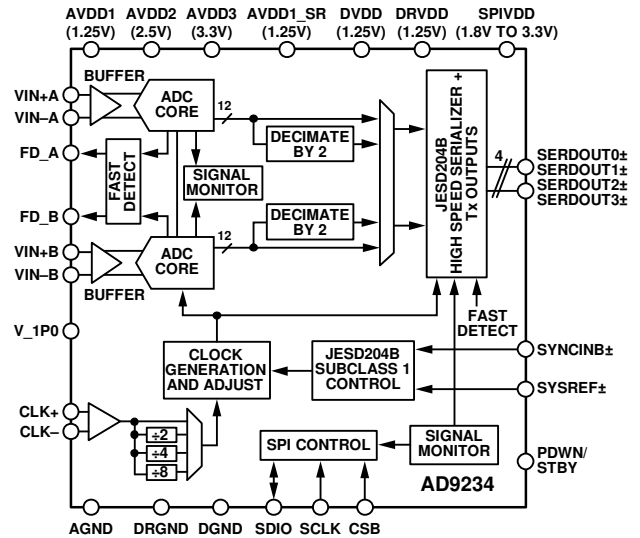


Figure 1.

## PRODUCT HIGHLIGHTS

1. Low power consumption analog core, 12-bit, 1.0 GSPS dual analog-to-digital converter (ADC) with 1.5 W per channel.
2. Wide full power bandwidth supports IF sampling of signals up to 2 GHz.
3. Buffered inputs with programmable input termination eases filter design and implementation.
4. Flexible serial port interface (SPI) controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection.
6. 9 mm × 9 mm 64-lead LFCSP.
7. Pin compatible with the [AD9680](#) 14-bit, 1 GSPS/500 MSPS dual ADC.

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**REVISION HISTORY****1/2018—Rev. A to Rev. B**

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| Change to Junction Temperature Range Parameter, Table 6.....   | 11 |
| Changes to Figure 38 and Figure 39 .....   | 19 |
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**3/2015—Rev. 0 to Rev. A**

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**8/2014—Revision 0: Initial Version**

## GENERAL DESCRIPTION

The AD9234 is a dual, 12-bit, 1 GSPS/500 MSPS ADC. The device has an on-chip buffer and sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed for sampling wide bandwidth analog signals. The AD9234 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth buffered inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. Each ADC data output is internally connected to an optional decimate by 2 block.

The AD9234 has several functions that simplify the automatic gain control (AGC) function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn

down the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the AD9234 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

Users can configure the Subclass 1 JESD204B-based high speed serialized output in a variety of one-, two-, or four-lane configurations, depending on the acceptable lane rate of the receiving logic device and the sampling rate of the ADC. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD9234 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V to 3.3 V capable 3-wire SPI.

The AD9234 is available in a Pb-free, 64-lead LFCSP and is specified over the -40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

# SPECIFICATIONS

## DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1\_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate,  $A_{IN} = -1.0$  dBFS, clock divider = 2, default SPI settings,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

| Parameter                                   | Temperature | AD9234-500 |           |       | AD9234-1000 |                  |       | Unit    |
|---|-------------|------------|-----------|-------|-------------|------------------|-------|---------|
|   |             | Min        | Typ       | Max   | Min         | Typ              | Max   |         |
| RESOLUTION                                  | Full        | 12         |           |       | 12          |                  |       | Bits    |
| ACCURACY                                    |             | Guaranteed |           |       | Guaranteed  |                  |       |         |
| No Missing Codes                            | Full        |            |           |       |             |                  |       |         |
| Offset Error                                | Full        | -0.22      | 0         | +0.20 | -0.22       | 0                | +0.20 | % FSR   |
| Offset Matching                             | Full        |            | 0         | +0.19 |             | 0                | +0.19 | % FSR   |
| Gain Error                                  | Full        | -13.8      | -5.1      | +3.6  |             | 0                |       | % FSR   |
| Gain Matching                               | Full        | -3.9       | +1        | +5.9  |             | 1                | +4.8  | % FSR   |
| Differential Nonlinearity (DNL)             | Full        | -0.3       |           | +0.3  | -0.3        | $\pm 0.16$       | +0.3  | LSB     |
| Integral Nonlinearity (INL)                 | Full        | -0.8       |           | +1.1  | -1.2        | $\pm 35$         | +1.4  | LSB     |
| TEMPERATURE DRIFT                           |             |            |           |       |             |                  |       |         |
| Offset Error                                | 25°C        |            | $\pm 2.6$ |       |             | $\pm 6$          |       | ppm/°C  |
| Gain Error                                  | 25°C        |            | $\pm 36$  |       |             | $\pm 36$         |       | ppm/°C  |
| INTERNAL VOLTAGE REFERENCE                  |             |            |           |       |             |                  |       |         |
| Voltage                                     | Full        | 1.0        |           |       | 1.0         |                  |       | V       |
| INPUT-REFERRED NOISE                        |             |            |           |       |             |                  |       |         |
| $V_{REF} = 1.0$ V                           | 25°C        | 0.74       |           |       | 1.02        |                  |       | LSB rms |
| ANALOG INPUTS                               |             |            |           |       |             |                  |       |         |
| Differential Input Voltage Range            | Full        | 1.63       |           |       | 1.34        |                  |       | V p-p   |
| Common-Mode Voltage ( $V_{CM}$ )            | 25°C        | 2.05       |           |       | 2.05        |                  |       | V       |
| Differential Input Capacitance <sup>1</sup> | 25°C        | 1.5        |           |       | 1.5         |                  |       | pF      |
| Analog Input Full Power Bandwidth           | 25°C        | 2          |           |       | 2           |                  |       | GHz     |
| POWER SUPPLY                                |             |            |           |       |             |                  |       |         |
| AVDD1                                       | Full        | 1.22       | 1.25      | 1.28  | 1.22        | 1.25             | 1.28  | V       |
| AVDD2                                       | Full        | 2.44       | 2.50      | 2.56  | 2.44        | 2.50             | 2.56  | V       |
| AVDD3                                       | Full        | 3.2        | 3.3       | 3.4   | 3.2         | 3.3              | 3.4   | V       |
| AVDD1_SR                                    | Full        | 1.22       | 1.25      | 1.28  | 1.22        | 1.25             | 1.28  | V       |
| DVDD  | Full        | 1.22       | 1.25      | 1.28  | 1.22        | 1.25             | 1.28  | V       |
| DRVDD                                       | Full        | 1.22       | 1.25      | 1.28  | 1.22        | 1.25             | 1.28  | V       |
| SPIVDD                                      | Full        | 1.7        | 1.8       | 3.4   | 1.7         | 1.8              | 3.4   | V       |
| $I_{AVDD1}$                                 | Full        |            | 430       | 480   |             | 675              | 740   | mA      |
| $I_{AVDD2}$                                 | Full        |            | 380       | 430   |             | 525              | 590   | mA      |
| $I_{AVDD3}$                                 | Full        |            | 65        | 75    |             | 75               | 91    | mA      |
| $I_{AVDD1\_SR}$                             | Full        |            | 15        | 18    |             | 16               | 18    | mA      |
| $I_{DVDD}^2$                                | Full        |            | 140       | 152   |             | 230              | 236   | mA      |
| $I_{DRVDD}^1$                               | Full        |            | 190       | 246   |             | 205              | 225   | mA      |
| $I_{DRVDD}$ (L = 2 mode)                    | 25°C        |            | 140       |       |             | N/A <sup>3</sup> |       | mA      |
| $I_{SPIVDD}$                                | Full        |            | 5         | 6     |             | 5                | 6     | mA      |

| Parameter   | Temperature | AD9234-500 |      |     | AD9234-1000 |                  |     | Unit |
|---|-------------|------------|------|-----|-------------|------------------|-----|------|
|   |             | Min        | Typ  | Max | Min         | Typ              | Max |      |
| POWER CONSUMPTION   |             |            |      |     |             |                  |     |      |
| Total Power Dissipation (Including Output Drivers) <sup>2</sup> | Full        |            | 2.15 | 2.5 |             | 3.0              | 3.3 | W    |
| Total Power Dissipation (L = 2 Mode)                            | 25°C        |            | 2.08 |     |             | N/A <sup>3</sup> |     | W    |
| Power-Down Dissipation  | Full        |            | 670  |     |             | 750              |     | mW   |
| Standby <sup>4</sup>  | Full        |            | 1.1  |     |             | 1.25             |     | W    |

<sup>1</sup> All lanes running. Power dissipation on DRVDD changes with lane rate and number of lanes used.

<sup>2</sup> Default mode. No DDCs used. L = 4, M = 2, F = 1.

<sup>3</sup> N/A = not applicable. At the maximum sample rate, it is not applicable to use L = 2 mode on the JESD204B output interface because this exceeds the maximum lane rate of 12.5 Gbps. L = 2 mode is supported when the equation  $((M \times N' \times (10/8) \times f_{OUT})/L)$  results in a line rate that is  $\leq 12.5$  Gbps.  $f_{OUT}$  is the output sample rate and is denoted by  $f_s/DCM$ , where DCM = decimation ratio.

<sup>4</sup> Can be controlled by the SPI.

## AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1\_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate,  $A_{IN} = -1.0$  dBFS, clock divider = 2, default SPI settings,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

| Parameter <sup>1</sup>                          | Temperature | AD9234-500 |      |     | AD9234-1000 |      |     | Unit    |
|---|-------------|------------|------|-----|-------------|------|-----|---------|
|   |             | Min        | Typ  | Max | Min         | Typ  | Max |         |
| ANALOG INPUT FULL SCALE                         | Full        |            | 1.63 |     |             | 1.34 |     | V p-p   |
| NOISE DENSITY <sup>2</sup>                      | Full        |            | -150 |     |             | -151 |     | dBFS/Hz |
| SIGNAL-TO-NOISE RATIO (SNR) <sup>3</sup>        |             |            |      |     |             |      |     |         |
| $f_{IN} = 10$ MHz                               | 25°C        |            | 65.9 |     |             | 64.2 |     | dBFS    |
| $f_{IN} = 170$ MHz                              | Full        | 65.1       | 65.8 |     | 61.6        | 63.9 |     | dBFS    |
| $f_{IN} = 340$ MHz                              | 25°C        |            | 65.6 |     |             | 63.4 |     | dBFS    |
| $f_{IN} = 450$ MHz                              | 25°C        |            | 65.3 |     |             | 63.1 |     | dBFS    |
| $f_{IN} = 737$ MHz                              | 25°C        |            | 64.2 |     |             | 61.6 |     | dBFS    |
| $f_{IN} = 985$ MHz                              | 25°C        |            | 63.6 |     |             | 60.7 |     | dBFS    |
| $f_{IN} = 1410$ MHz                             | 25°C        |            | 62.2 |     |             | 58.8 |     | dBFS    |
| SNR AND DISTORTION RATIO (SINAD) <sup>3</sup>   |             |            |      |     |             |      |     |         |
| $f_{IN} = 10$ MHz                               | 25°C        |            | 65.8 |     |             | 64.1 |     | dBFS    |
| $f_{IN} = 170$ MHz                              | Full        | 65.0       | 65.7 |     | 61.2        | 63.8 |     | dBFS    |
| $f_{IN} = 340$ MHz                              | 25°C        |            | 65.5 |     |             | 63.3 |     | dBFS    |
| $f_{IN} = 450$ MHz                              | 25°C        |            | 65.2 |     |             | 63.0 |     | dBFS    |
| $f_{IN} = 737$ MHz                              | 25°C        |            | 63.7 |     |             | 61.5 |     | dBFS    |
| $f_{IN} = 985$ MHz                              | 25°C        |            | 63.1 |     |             | 60.6 |     | dBFS    |
| $f_{IN} = 1410$ MHz                             | 25°C        |            | 61.2 |     |             | 58.7 |     | dBFS    |
| EFFECTIVE NUMBER OF BITS (ENOB)                 |             |            |      |     |             |      |     |         |
| $f_{IN} = 10$ MHz                               | 25°C        |            | 10.7 |     |             | 10.4 |     | Bits    |
| $f_{IN} = 170$ MHz                              | Full        | 10.5       | 10.6 |     | 9.9         | 10.3 |     | Bits    |
| $f_{IN} = 340$ MHz                              | 25°C        |            | 10.6 |     |             | 10.2 |     | Bits    |
| $f_{IN} = 450$ MHz                              | 25°C        |            | 10.5 |     |             | 10.2 |     | Bits    |
| $f_{IN} = 737$ MHz                              | 25°C        |            | 10.3 |     |             | 9.9  |     | Bits    |
| $f_{IN} = 985$ MHz                              | 25°C        |            | 10.2 |     |             | 9.8  |     | Bits    |
| $f_{IN} = 1410$ MHz                             | 25°C        |            | 9.9  |     |             | 9.5  |     | Bits    |
| SPURIOUS-FREE DYNAMIC RANGE (SFDR) <sup>3</sup> |             |            |      |     |             |      |     |         |
| $f_{IN} = 10$ MHz                               | 25°C        |            | 84   |     |             | 89   |     | dBFS    |
| $f_{IN} = 170$ MHz                              | Full        | 77         | 85   |     | 70          | 80   |     | dBFS    |
| $f_{IN} = 340$ MHz                              | 25°C        |            | 85   |     |             | 79   |     | dBFS    |
| $f_{IN} = 450$ MHz                              | 25°C        |            | 87   |     |             | 80   |     | dBFS    |
| $f_{IN} = 737$ MHz                              | 25°C        |            | 75   |     |             | 81   |     | dBFS    |
| $f_{IN} = 985$ MHz                              | 25°C        |            | 75   |     |             | 79   |     | dBFS    |
| $f_{IN} = 1410$ MHz                             | 25°C        |            | 71   |     |             | 78   |     | dBFS    |

| Parameter <sup>1</sup>   | Temperature | AD9234-500 |     |     | AD9234-1000 |     |     | Unit |
|--|-------------|------------|-----|-----|-------------|-----|-----|------|
|  |             | Min        | Typ | Max | Min         | Typ | Max |      |
| WORST HARMONIC, SECOND OR THIRD <sup>3</sup>                                 |             |            |     |     |             |     |     |      |
| $f_{IN} = 10$ MHz  | 25°C        |            | -84 |     | -89         |     |     | dBFS |
| $f_{IN} = 170$ MHz   | Full        |            | -85 | -77 | -80         | -70 |     | dBFS |
| $f_{IN} = 340$ MHz   | 25°C        |            | -85 |     | -79         |     |     | dBFS |
| $f_{IN} = 450$ MHz   | 25°C        |            | -87 |     | -80         |     |     | dBFS |
| $f_{IN} = 737$ MHz   | 25°C        |            | -75 |     | -82         |     |     | dBFS |
| $f_{IN} = 985$ MHz   | 25°C        |            | -75 |     | -79         |     |     | dBFS |
| $f_{IN} = 1410$ MHz  | 25°C        |            | -71 |     | -78         |     |     | dBFS |
| WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC <sup>3</sup>                 |             |            |     |     |             |     |     |      |
| $f_{IN} = 10$ MHz  | 25°C        |            | -96 |     | -89         |     |     | dBFS |
| $f_{IN} = 170$ MHz   | Full        | -82        | -95 |     | -85         | -76 |     | dBFS |
| $f_{IN} = 340$ MHz   | 25°C        |            | -94 |     | -83         |     |     | dBFS |
| $f_{IN} = 450$ MHz   | 25°C        |            | -93 |     | -82         |     |     | dBFS |
| $f_{IN} = 737$ MHz   | 25°C        |            | -88 |     | -81         |     |     | dBFS |
| $f_{IN} = 985$ MHz   | 25°C        |            | -89 |     | -85         |     |     | dBFS |
| $f_{IN} = 1410$ MHz  | 25°C        |            | -86 |     | -80         |     |     | dBFS |
| TWO-TONE INTERMODULATION DISTORTION (IMD), $A_{IN1}$ AND $A_{IN2} = -7$ dBFS |             |            |     |     |             |     |     |      |
| $f_{IN1} = 187$ MHz, $f_{IN2} = 190$ MHz                                     | 25°C        |            | -90 |     | -81         |     |     | dBFS |
| $f_{IN1} = 338$ MHz, $f_{IN2} = 341$ MHz                                     | 25°C        |            | -86 |     | -78         |     |     | dBFS |
| CROSSTALK <sup>4</sup>   |             |            |     |     |             |     |     |      |
|  | 25°C        |            | 95  |     | 95          |     |     | dB   |
| FULL POWER BANDWIDTH <sup>5</sup>  |             |            |     |     |             |     |     |      |
|  | 25°C        |            | 2   |     | 2           |     |     | GHz  |

<sup>1</sup> See the [AN-835 Application Note, Understanding High Speed ADC Testing and Evaluation](#), for definitions and for details on how these tests were completed.

<sup>2</sup> Noise density is measured at a low analog input frequency (30 MHz).

<sup>3</sup> See Table 9 for recommended settings for the buffer current setting optimized for SFDR.

<sup>4</sup> Crosstalk is measured at 170 MHz with a -1.0 dBFS analog input on one channel and no input on the adjacent channel.

<sup>5</sup> Measured with circuit shown in Figure 64.

**DIGITAL SPECIFICATIONS**

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1\_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate,  $A_{IN} = -1.0$  dBFS, default SPI settings,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

| Parameter   | Temperature         | Min                        | Typ              | Max  | Unit       |
|---|---------------------|----------------------------|------------------|------|------------|
| <b>CLOCK INPUTS (CLK+, CLK–)</b>  |                     |                            |                  |      |            |
| Logic Compliance  | Full                |                            | LVDS/LVPECL      |      |            |
| Differential Input Voltage  | Full                | 600                        | 1200             | 1800 | mV p-p     |
| Input Common-Mode Voltage   | Full                |                            | 0.85             |      | V          |
| Input Resistance (Differential)   | Full                |                            | 35               |      | k $\Omega$ |
| Input Capacitance   | Full                |                            |                  | 2.5  | pF         |
| <b>SYSTEM REFERENCE INPUTS (SYSREF+, SYSREF–)</b>                             |                     |                            |                  |      |            |
| Logic Compliance  | Full                |                            | LVDS/LVPECL      |      |            |
| Differential Input Voltage  | Full                | 400                        | 1200             | 1800 | mV p-p     |
| Input Common-Mode Voltage   | Full                | 0.6                        | 0.85             | 2.0  | V          |
| Input Resistance (Differential)   | Full                |                            | 35               |      | k $\Omega$ |
| Input Capacitance (Differential)  | Full                |                            |                  | 2.5  | pF         |
| <b>LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY)</b>                              |                     |                            |                  |      |            |
| Logic Compliance  | Full                |                            | CMOS             |      |            |
| Logic 1 Voltage   | Full                | $0.8 \times \text{SPIVDD}$ |                  |      | V          |
| Logic 0 Voltage   | Full                | 0                          |                  | 0.5  | V          |
| Input Resistance  | Full                |                            | 30               |      | k $\Omega$ |
| <b>LOGIC OUTPUT (SDIO)</b>  |                     |                            |                  |      |            |
| Logic Compliance  | Full                |                            | CMOS             |      |            |
| Logic 1 Voltage ( $I_{OH} = 800 \mu\text{A}$ )                                | Full                | $0.8 \times \text{SPIVDD}$ |                  |      | V          |
| Logic 0 Voltage ( $I_{OL} = 50 \mu\text{A}$ )                                 | Full                | 0                          |                  | 0.5  | V          |
| <b>SYNC INPUTS (SYNCINB+, SYNCINB–)</b>                                       |                     |                            |                  |      |            |
| Logic Compliance  | Full                |                            | LVDS/LVPECL/CMOS |      |            |
| Differential Input Voltage  | Full                | 400                        | 1200             | 1800 | mV p-p     |
| Input Common-Mode Voltage   | Full                | 0.6                        | 0.85             | 2.0  | V          |
| Input Resistance (Differential)   | Full                |                            | 35               |      | k $\Omega$ |
| Input Capacitance   | Full                |                            |                  | 2.5  | pF         |
| <b>LOGIC OUTPUTS (FD_A, FD_B)</b>   |                     |                            |                  |      |            |
| Logic Compliance  | Full                |                            | CMOS             |      |            |
| Logic 1 Voltage   | Full                | $0.8 \times \text{SPIVDD}$ |                  |      | V          |
| Logic 0 Voltage   | Full                | 0                          |                  | 0.5  | V          |
| Input Resistance  | Full                |                            | 30               |      | k $\Omega$ |
| <b>DIGITAL OUTPUTS (SERDOUT<math>x_{\pm}</math>, <math>x = 0</math> TO 3)</b> |                     |                            |                  |      |            |
| Logic Compliance  | Full                |                            | CML              |      |            |
| Differential Output Voltage   | Full                | 360                        |                  | 770  | mV p-p     |
| Output Common-Mode Voltage ( $V_{CM}$ )                                       |                     |                            |                  |      |            |
| AC-Coupled  | 25 $^\circ\text{C}$ | 0                          |                  | 1.8  | V          |
| Short-Circuit Current ( $I_{Dshort}$ )  | 25 $^\circ\text{C}$ | –100                       |                  | +100 | mA         |
| Differential Return Loss ( $RL_{DIFF}$ ) <sup>1</sup>                         | 25 $^\circ\text{C}$ | 8                          |                  |      | dB         |
| Common-Mode Return Loss ( $RL_{CM}$ ) <sup>1</sup>                            | 25 $^\circ\text{C}$ | 6                          |                  |      | dB         |
| Differential Termination Impedance  | Full                | 80                         | 100              | 120  | $\Omega$   |

<sup>1</sup> Differential and common-mode return loss is measured from 100 MHz to 0.75 MHz  $\times$  baud rate.



**SWITCHING SPECIFICATIONS**

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1\_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate,  $A_{IN} = -1.0$  dBFS, default SPI settings,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

| Parameter   | Temperature | AD9234-500 |     |      | AD9234-1000 |     |      | Unit         |
|---|-------------|------------|-----|------|-------------|-----|------|--------------|
|   |             | Min        | Typ | Max  | Min         | Typ | Max  |              |
| <b>CLOCK</b>  |             |            |     |      |             |     |      |              |
| Clock Rate (at CLK+/CLK- Pins)                          | Full        | 0.3        |     | 4    | 0.3         |     | 4    | GHz          |
| Maximum Sample Rate <sup>1</sup>                        | Full        | 500        |     |      | 1000        |     |      | MSPS         |
| Minimum Sample Rate <sup>2</sup>                        | Full        | 300        |     |      | 300         |     |      | MSPS         |
| Clock Pulse Width High                                  | Full        | 1000       |     |      | 500         |     |      | ps           |
| Clock Pulse Width Low                                   | Full        | 1000       |     |      | 500         |     |      | ps           |
| <b>OUTPUT PARAMETERS</b>                                |             |            |     |      |             |     |      |              |
| Unit Interval (UI) <sup>3</sup>                         | Full        | 80         | 200 |      | 80          | 100 |      | ps           |
| Rise Time ( $t_R$ ) (20% to 80% into 100 $\Omega$ Load) | 25°C        | 24         | 32  |      | 24          | 32  |      | ps           |
| Fall Time ( $t_F$ ) (20% to 80% into 100 $\Omega$ Load) | 25°C        | 24         | 32  |      | 24          | 32  |      | ps           |
| PLL Lock Time   | 25°C        |            | 2   |      |             | 2   |      | ms           |
| Data Rate per Channel (NRZ) <sup>4</sup>                | 25°C        | 3.125      | 5   | 12.5 | 3.125       | 10  | 12.5 | Gbps         |
| <b>LATENCY<sup>5</sup></b>                              |             |            |     |      |             |     |      |              |
| Pipeline Latency  | Full        |            | 55  |      |             | 55  |      | Clock cycles |
| Fast Detect Latency                                     | Full        |            |     | 28   |             |     | 28   | Clock cycles |
| Wake-Up Time <sup>6</sup>                               |             |            |     |      |             |     |      |              |
| Standby   | 25°C        |            | 1   |      |             | 1   |      | ms           |
| Power-Down  | 25°C        |            |     | 4    |             |     | 4    | ms           |
| <b>APERTURE</b>   |             |            |     |      |             |     |      |              |
| Aperture Delay ( $t_A$ )                                | Full        |            | 530 |      |             | 530 |      | ps           |
| Aperture Uncertainty (Jitter, $t_j$ )                   | Full        |            | 55  |      |             | 55  |      | fs rms       |
| Out-of-Range Recovery Time                              | Full        |            | 1   |      |             | 1   |      | Clock Cycles |

<sup>1</sup> The maximum sample rate is the clock rate after the divider.

<sup>2</sup> The minimum sample rate operates at 300 MSPS with  $L = 2$  or  $L = 1$ .

<sup>3</sup> Baud rate =  $1/UI$ . A subset of this range can be supported.

<sup>4</sup> Default  $L = 4$ . This number can be changed based on the sample rate and decimation ratio.

<sup>5</sup> No DDCs used.  $L = 4$ ,  $M = 2$ ,  $F = 1$ .

<sup>6</sup> Wake-up time is defined as the time required to return to normal operation from power-down mode.

**TIMING SPECIFICATIONS****Table 5.**

| Parameter                                  | Test Conditions/Comments  | Min | Typ | Max | Unit |
|--|---|-----|-----|-----|------|
| <b>CLK+ to SYSREF+ TIMING REQUIREMENTS</b> |   |     |     |     |      |
| $t_{SU\_SR}$                               | See Figure 2<br>Device clock to SYSREF+ setup time  |     | 117 |     | ps   |
| $t_{H\_SR}$                                | Device clock to SYSREF+ hold time   |     | -96 |     | ps   |
| <b>SPI TIMING REQUIREMENTS</b>             |   |     |     |     |      |
| $t_{DS}$                                   | See Figure 3<br>Setup time between the data and the rising edge of SCLK   | 2   |     |     | ns   |
| $t_{DH}$                                   | Hold time between the data and the rising edge of SCLK  | 2   |     |     | ns   |
| $t_{CLK}$                                  | Period of the SCLK  | 40  |     |     | ns   |
| $t_S$                                      | Setup time between CSB and SCLK   | 2   |     |     | ns   |
| $t_H$                                      | Hold time between CSB and SCLK  | 2   |     |     | ns   |
| $t_{HIGH}$                                 | Minimum period that SCLK must be in a logic high state  | 10  |     |     | ns   |
| $t_{LOW}$                                  | Minimum period that SCLK must be in a logic low state   | 10  |     |     | ns   |
| $t_{ACCESS}$                               | Maximum time delay between falling edge of SCLK and output data valid for a read operation                                    |     | 6   | 10  | ns   |
| $t_{EN\_SDIO}$                             | Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 3) | 10  |     |     | ns   |
| $t_{DIS\_SDIO}$                            | Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 3)  | 10  |     |     | ns   |

Timing Diagrams

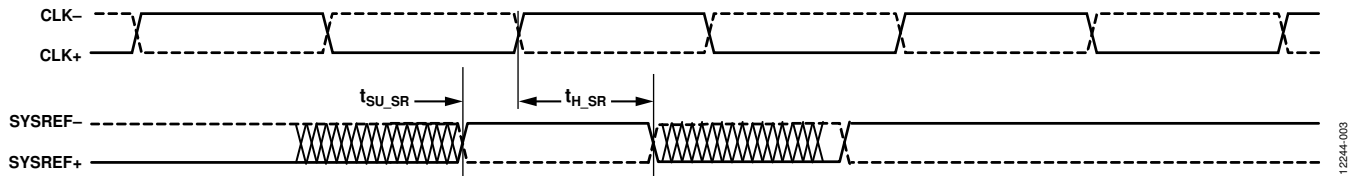


Figure 2. SYSREF± Setup and Hold Timing

12244-003

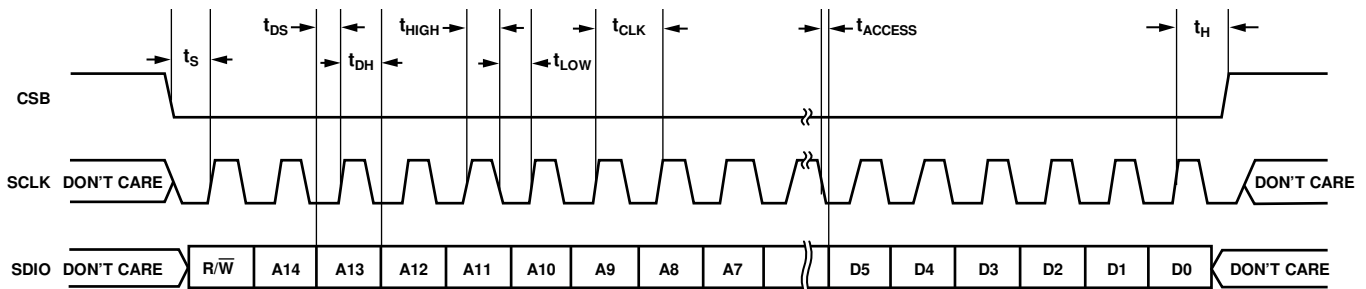


Figure 3. Serial Port Interface Timing Diagram

12244-004

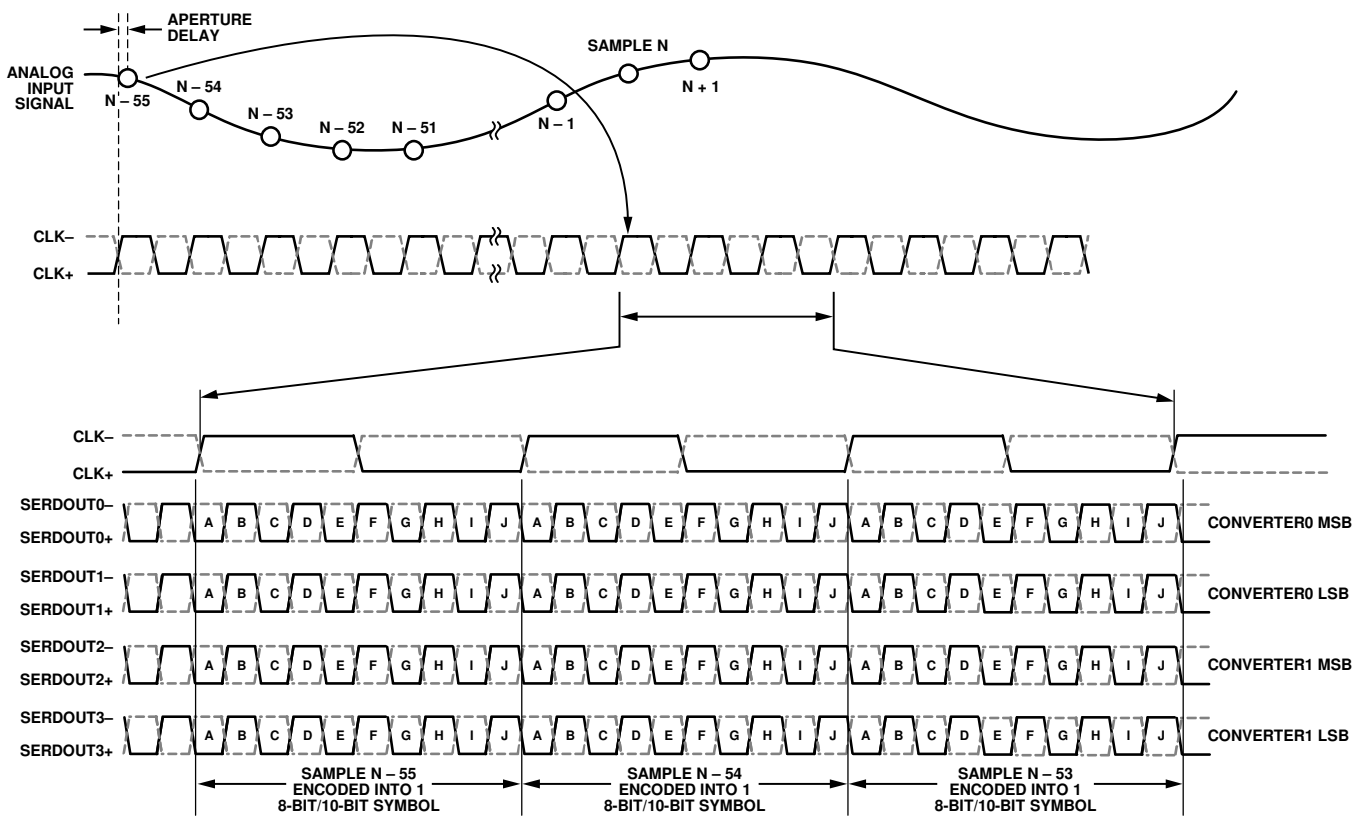


Figure 4. Data Output Timing (Full Bandwidth Mode; L = 4; M = 2; F = 1)

12244-002

## ABSOLUTE MAXIMUM RATINGS

Table 6.

| Parameter                           | Rating                   |
|-------------------------------------|--------------------------|
| Electrical                          |                          |
| AVDD1 to AGND                       | 1.32 V                   |
| AVDD1_SR to AGND                    | 1.32 V                   |
| AVDD2 to AGND                       | 2.75 V                   |
| AVDD3 to AGND                       | 3.63 V                   |
| DVDD to DGND                        | 1.32 V                   |
| DRVDD to DRGND                      | 1.32 V                   |
| SPIVDD to AGND                      | 3.63 V                   |
| AGND to DRGND                       | -0.3 V to +0.3 V         |
| VIN±x to AGND                       | 3.2 V                    |
| SCLK, SDIO, CSB to AGND             | -0.3 V to SPIVDD + 0.3 V |
| PDWN/STBY to AGND                   | -0.3 V to SPIVDD + 0.3 V |
| Operating Temperature Range         | -40°C to +85°C           |
| Junction Temperature Range          | -40°C to +125°C          |
| Storage Temperature Range (Ambient) | -65°C to +150°C          |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL CHARACTERISTICS

Typical  $\theta_{JA}$ ,  $\theta_{JB}$ , and  $\theta_{JC}$  are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing  $\theta_{JA}$  and  $\theta_{JB}$ . In addition, metal in direct contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes, reduces the  $\theta_{JA}$ . Thermal performance for actual applications requires careful inspection of the conditions in an application. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 6.

Table 7. Thermal Resistance Values

| PCB Type | Airflow Velocity (m/sec) | $\theta_{JA}$       | $\Psi_{JB}$        | $\theta_{JC\_TOP}$ | $\theta_{JC\_BOT}$ | Unit |
|----------|--------------------------|---------------------|--------------------|--------------------|--------------------|------|
| JEDEC    | 0.0                      | 17.8 <sup>1,2</sup> | 6.3 <sup>1,3</sup> | 4.7 <sup>1,5</sup> | 1.2 <sup>1,5</sup> | °C/W |
| 2s2p     | 1.0                      | 15.6 <sup>1,2</sup> | 5.9 <sup>1,3</sup> | N/A <sup>4</sup>   |                    | °C/W |
| Board    | 2.5                      | 15.0 <sup>1,2</sup> | 5.7 <sup>1,3</sup> | N/A <sup>4</sup>   |                    | °C/W |

<sup>1</sup> Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.

<sup>2</sup> Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).

<sup>3</sup> Per JEDEC JESD51-8 (still air).

<sup>4</sup> N/A = not applicable.

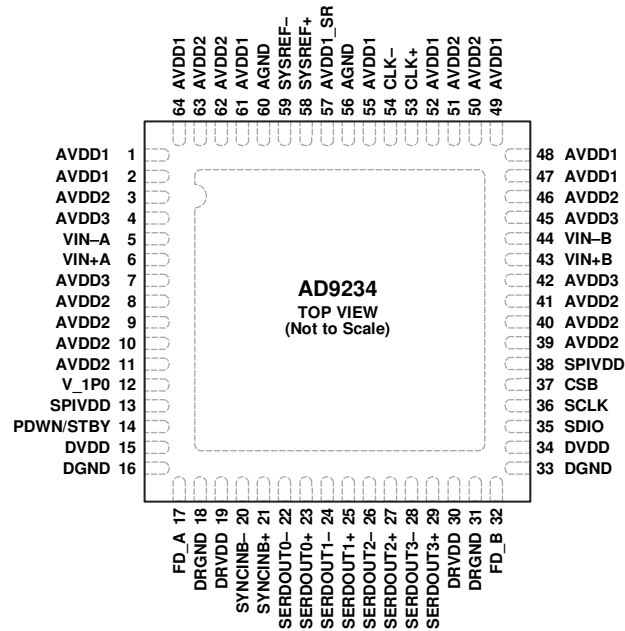
<sup>5</sup> Per MIL-STD 883, Method 1012.1.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE GROUND REFERENCE FOR AVDDx. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

12244-005

Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

| Pin No.   | Mnemonic              | Type      | Description   |
|---|-----------------------|-----------|---|
| Power Supplies                                  |                       |           |   |
| 0   | EPAD                  | Ground    | Exposed Pad. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx. This exposed pad must be connected to ground for proper operation.   |
| 1, 2, 47, 48, 49, 52, 55, 61, 64                | AVDD1                 | Supply    | Analog Power Supply (1.25 V Nominal).   |
| 3, 8, 9, 10, 11, 39, 40, 41, 46, 50, 51, 62, 63 | AVDD2                 | Supply    | Analog Power Supply (2.5 V Nominal).  |
| 4, 7, 42, 45                                    | AVDD3                 | Supply    | Analog Power Supply (3.3 V Nominal).  |
| 13, 38  | SPIVDD                | Supply    | Digital Power Supply for SPI (1.8 V to 3.3 V).  |
| 15, 34  | DVDD                  | Supply    | Digital Power Supply (1.25 V Nominal).  |
| 16, 33  | DGND                  | Ground    | Ground Reference for DVDD.  |
| 18, 31  | DRGND                 | Ground    | Ground Reference for DRVDD.   |
| 19, 30  | DRVDD                 | Supply    | Digital Driver Power Supply (1.25 V Nominal).   |
| 56, 60  | AGND <sup>1</sup>     | Ground    | Ground Reference for SYSREF±.   |
| 57  | AVDD1_SR <sup>1</sup> | Supply    | Analog Power Supply for SYSREF± (1.25 V Nominal).   |
| Analog  |                       |           |   |
| 5, 6  | VIN-A, VIN+A          | Input     | ADC A Analog Input Complement/True.   |
| 12  | V_1P0                 | Input/DNC | 1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source. |
| 43, 44  | VIN+B, VIN-B          | Input     | ADC B Analog Input True/Complement.   |
| 53, 54  | CLK+, CLK-            | Input     | Clock Input True/Complement.  |
| CMOS Outputs                                    |                       |           |   |
| 17, 32  | FD_A, FD_B            | Output    | Fast Detect Outputs for Channel A and Channel B.  |

| Pin No.   | Mnemonic   | Type  | Description  |
|---|--|---|--|
| Digital Inputs<br>20, 21<br>58, 59                              | SYNCINB–, SYNCINB+<br>SYSREF+, SYSREF–   | Input<br>Input                              | Active Low JESD204B LVDS Sync Input Complement/True.<br>Active High JESD204B LVDS System Reference Input<br>True/Complement.   |
| Data Outputs<br>22, 23<br>24, 25<br>26, 27<br>28, 29            | SERDOUT0–, SERDOUT0+<br>SERDOUT1–, SERDOUT1+<br>SERDOUT2–, SERDOUT2+<br>SERDOUT3–, SERDOUT3+ | Output<br>Output<br>Output<br>Output        | Lane 0 Output Data Complement/True.<br>Lane 1 Output Data Complement/True.<br>Lane 2 Output Data Complement/True.<br>Lane 3 Output Data Complement/True.   |
| Device Under Test (DUT)<br>Controls<br>14<br><br>35<br>36<br>37 | PDWN/STBY<br><br>SDIO<br>SCLK<br>CSB   | Input<br><br>Input/output<br>Input<br>Input | Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.<br><br>SPI Serial Data Input/Output.<br>SPI Serial Clock.<br>SPI Chip Select (Active Low). |

<sup>1</sup> To ensure proper ADC operation, connect AVDD1\_SR and AGND separately from the AVDD1 and EPAD connection. For more information, refer to the Applications Information section.

# TYPICAL PERFORMANCE CHARACTERISTICS

## AD9234-1000

AVDD1 = 1.25 V, AVDD1\_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, 1.34 V p-p full-scale differential input,  $A_{IN} = -1.0$  dBFS, default SPI settings, clock divider = 2,  $T_A = 25^\circ\text{C}$ , 128k FFT sample, unless otherwise noted.

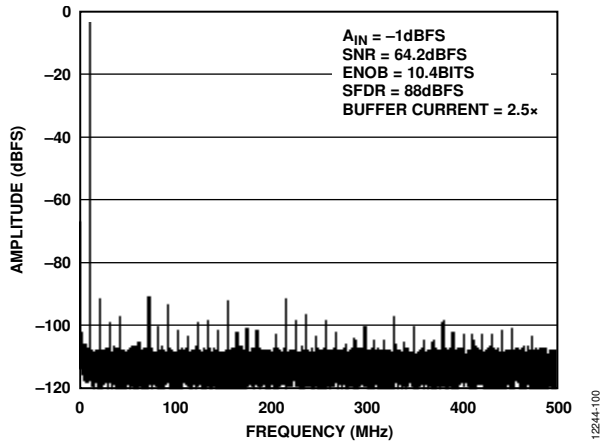


Figure 6. Single-Tone FFT with Input Frequency ( $f_{IN}$ ) = 10.3 MHz

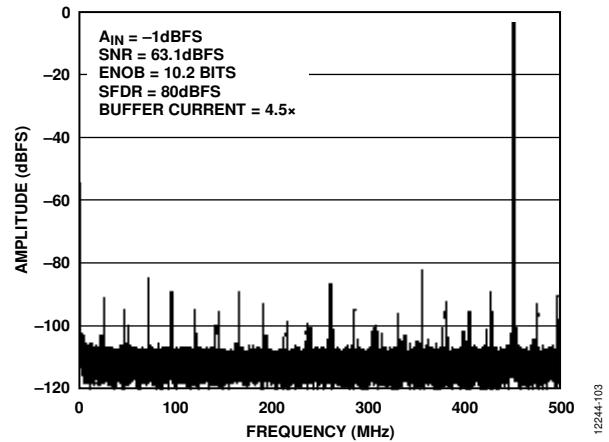


Figure 9. Single-Tone FFT with  $f_{IN} = 450.3$  MHz

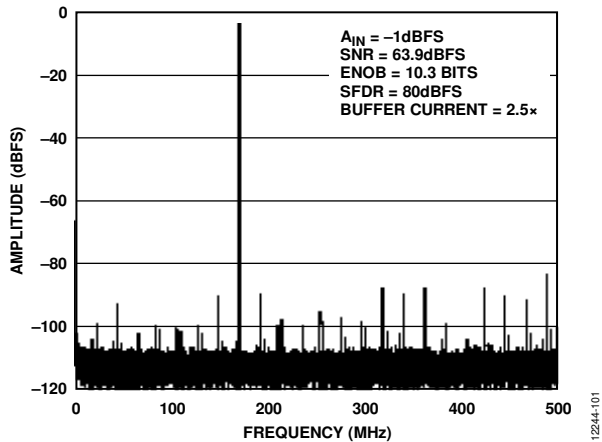


Figure 7. Single-Tone FFT with  $f_{IN} = 170.3$  MHz

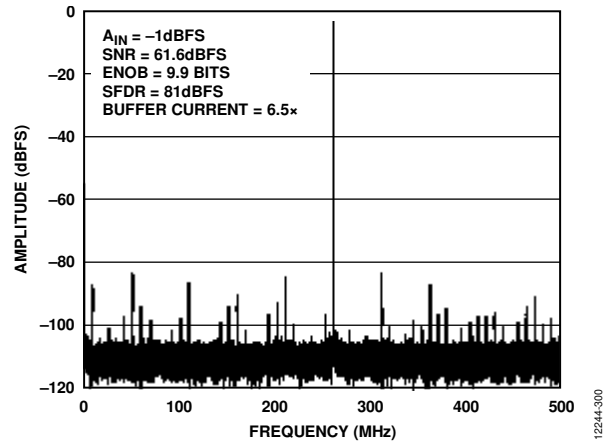


Figure 10. Single-Tone FFT with  $f_{IN} = 737.3$  MHz

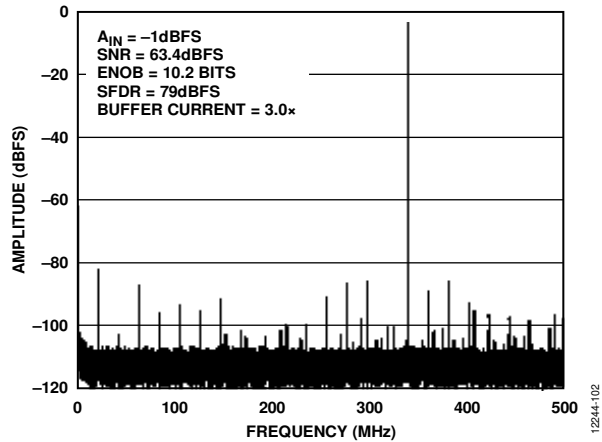


Figure 8. Single-Tone FFT with  $f_{IN} = 340.3$  MHz

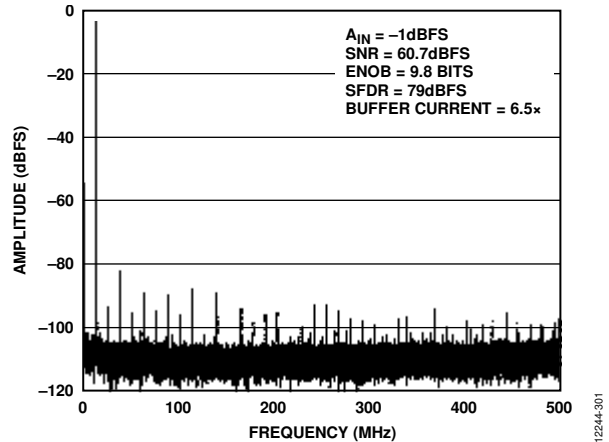


Figure 11. Single-Tone FFT with  $f_{IN} = 985.3$  MHz

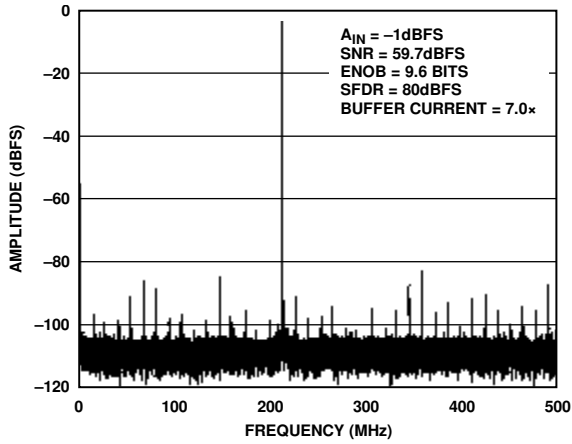


Figure 12. Single-Tone FFT with  $f_{IN} = 1213.3$  MHz

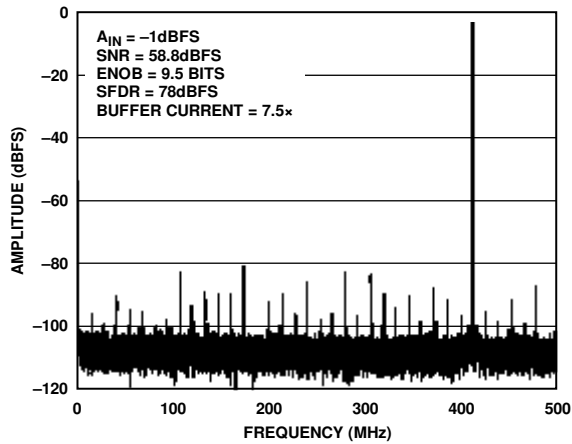


Figure 13. Single-Tone FFT with  $f_{IN} = 1413.3$  MHz

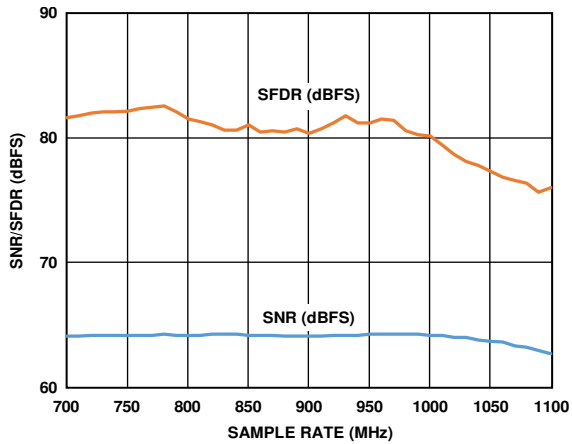


Figure 14. SNR/SFDR vs. Sample Rate ( $f_s$ ),  $f_{IN} = 170.3$  MHz; Buffer Current =  $3.0\times$

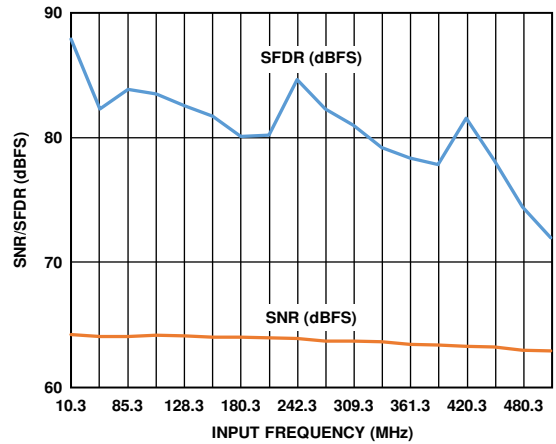


Figure 15. SNR/SFDR vs. Input Frequency ( $f_{IN}$ );  $f_{IN} < 500$  MHz; Buffer Current =  $3.5\times$  (Uses Circuit Shown in Figure 63)

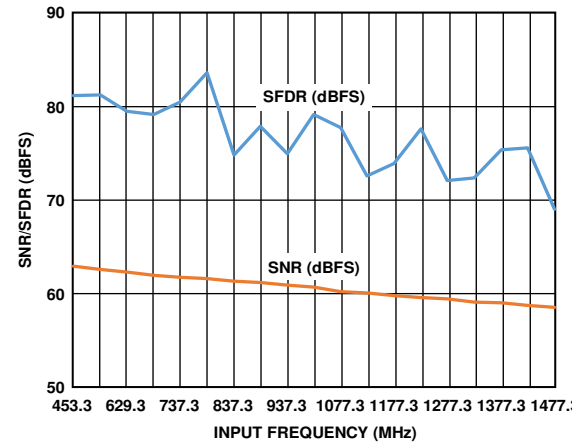


Figure 16. SNR/SFDR vs. Input Frequency;  $450$  MHz  $< f_{IN} < 1500$  MHz; Buffer Current =  $7.5\times$  (Uses Circuit Shown in Figure 64)

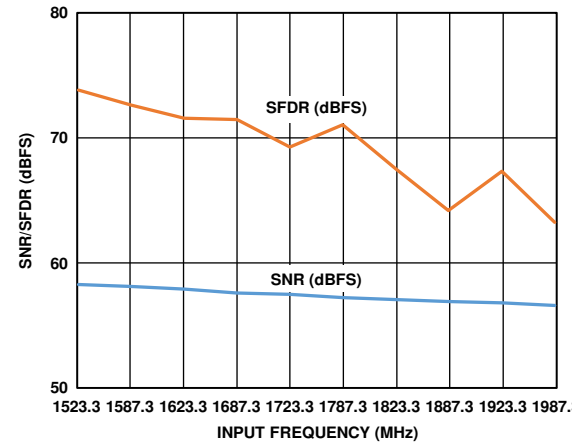


Figure 17. SNR/SFDR vs. Input Frequency;  $1500$  MHz  $< f_{IN} < 2000$  MHz; Buffer Current =  $8.5\times$  (Uses Circuit Shown in Figure 64)

12244-302

12244-306

12244-303

12244-307

12244-304

12244-308

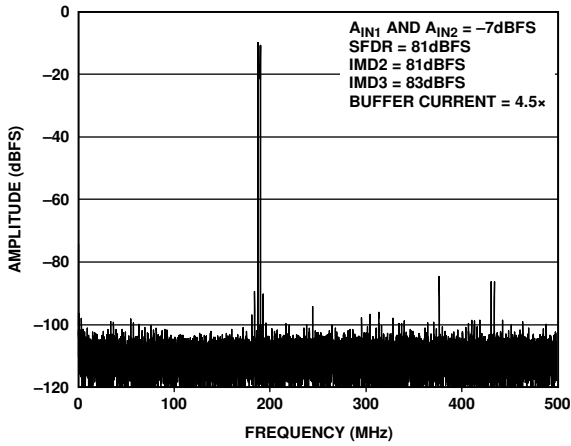


Figure 18. Two-Tone FFT;  $f_{IN1} = 184$  MHz,  $f_{IN2} = 187$  MHz

12244-205

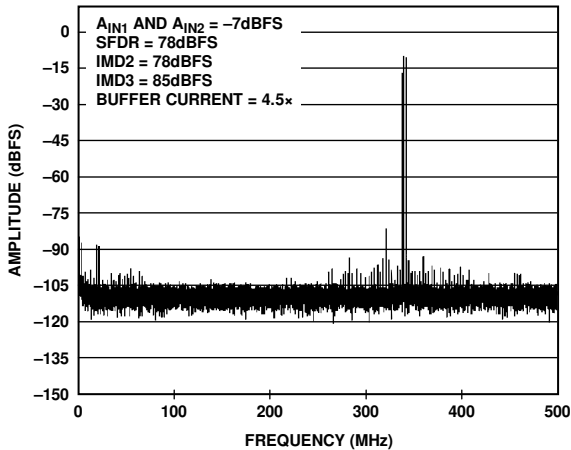


Figure 19. Two-Tone FFT;  $f_{IN1} = 338$  MHz,  $f_{IN2} = 341$  MHz

12244-206

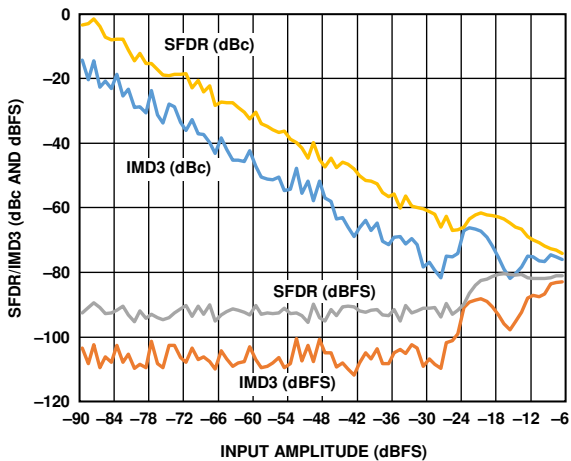


Figure 20. Two-Tone SFDR/IMD3 vs. Input Amplitude ( $A_{IN}$ ) with  $f_{IN1} = 184$  MHz and  $f_{IN2} = 187$  MHz

12244-207

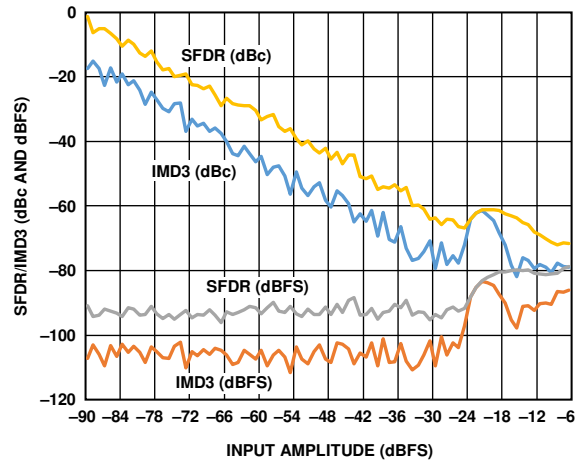


Figure 21. Two-Tone SFDR/IMD3 vs. Input Amplitude ( $A_{IN}$ ) with  $f_{IN1} = 338$  MHz and  $f_{IN2} = 341$  MHz

12244-208

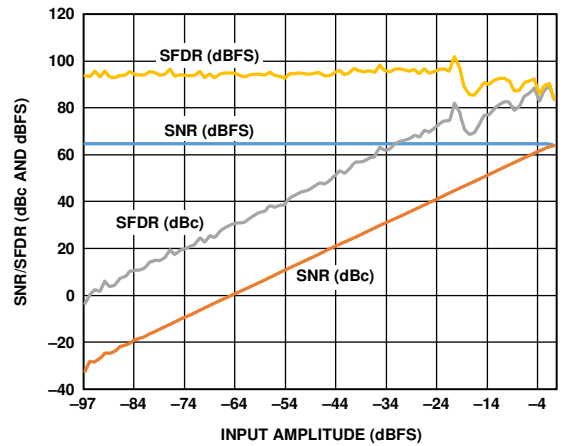


Figure 22. SNR/SFDR vs. Analog Input Level,  $f_{IN} = 10.3$  MHz; Buffer Current =  $2.0\times$

12244-209

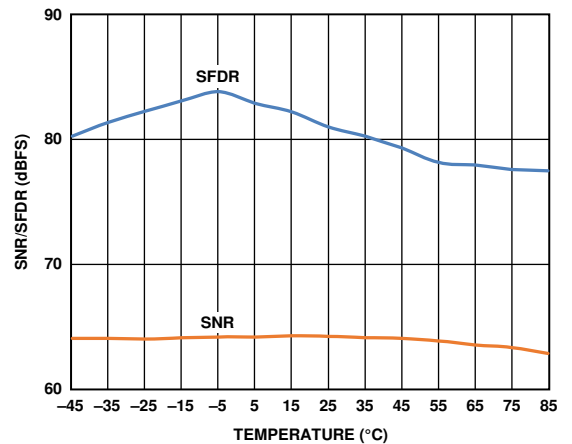


Figure 23. SNR/SFDR vs. Temperature,  $f_{IN} = 170.3$  MHz

12244-400



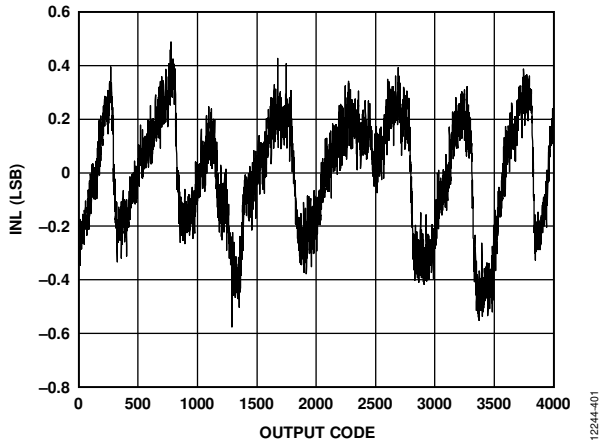


Figure 24. INL,  $f_{IN} = 10.3$  MHz

12244-401

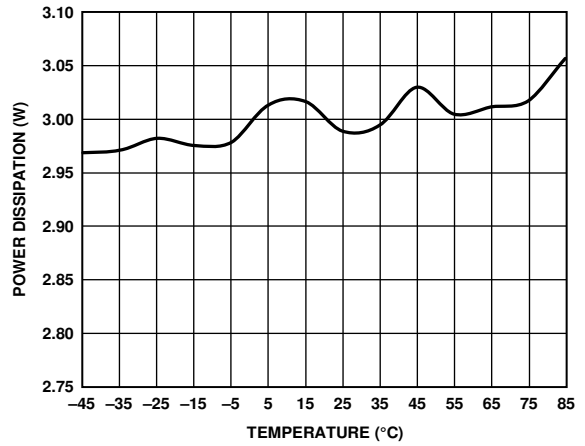


Figure 27. Power Dissipation vs. Temperature

12244-404

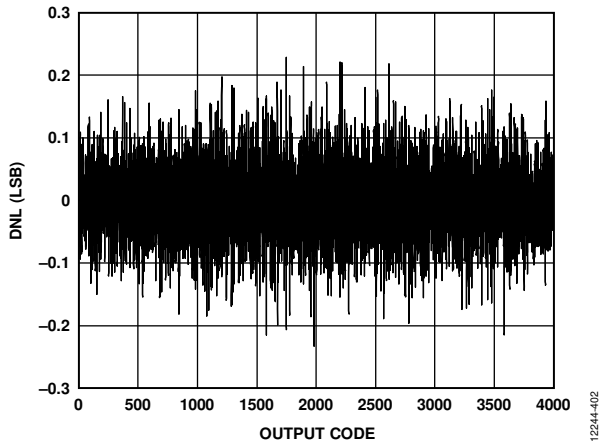


Figure 25. DNL,  $f_{IN} = 10$  MHz

12244-402

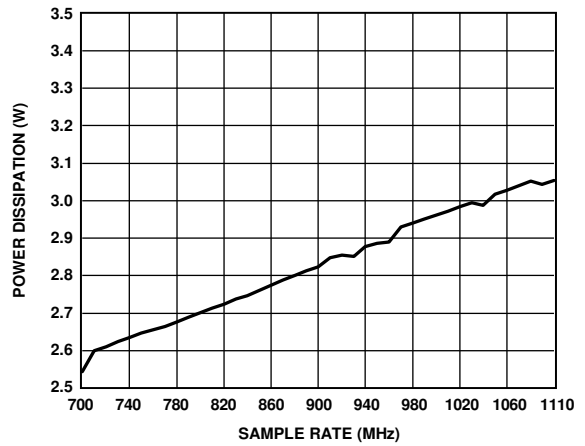


Figure 28. Power Dissipation vs. Sample Rate ( $f_s$ )

12244-405

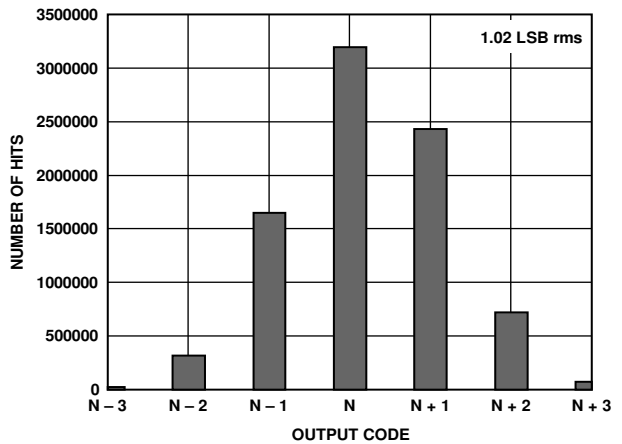


Figure 26. Input Referred Noise Histogram

12244-403

AD9234-500

AVDD1 = 1.25 V, AVDD1\_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, 1.63 V p-p full-scale differential input,  $A_{IN} = -1.0$  dBFS, default SPI settings, clock divider = 2,  $T_A = 25^\circ\text{C}$ , 128k FFT sample, unless otherwise noted.

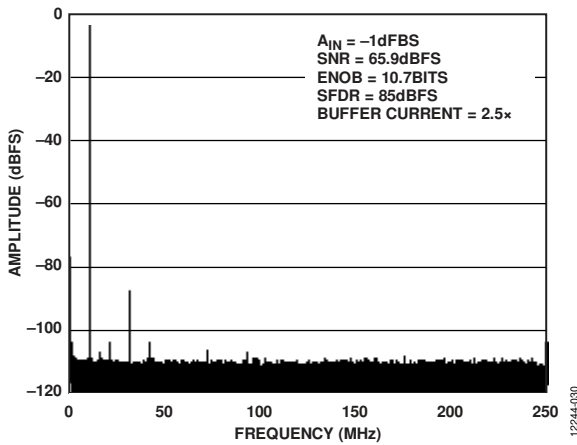


Figure 29. Single-Tone FFT with Input Frequency ( $f_{IN}$ ) = 10.3 MHz

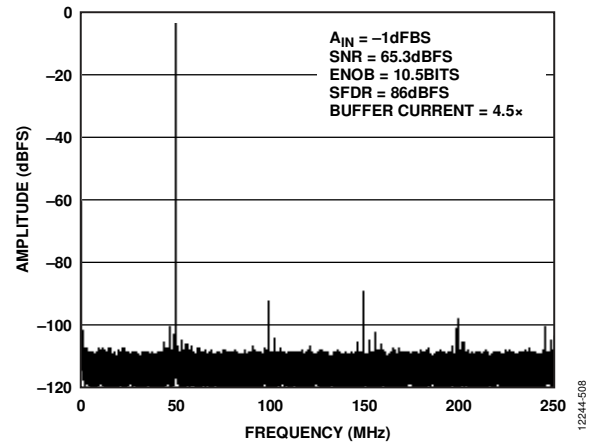


Figure 32. Single-Tone FFT with  $f_{IN} = 450.3$  MHz

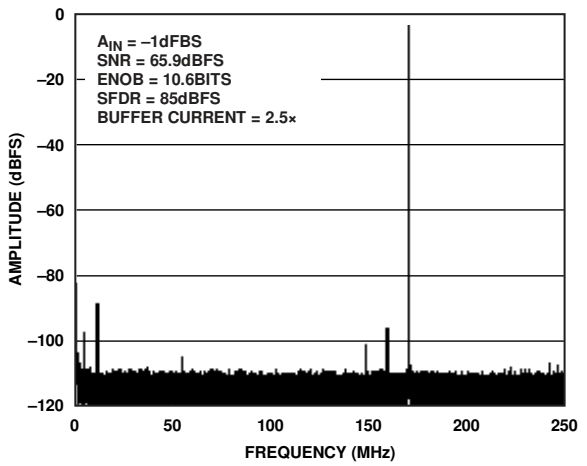


Figure 30. Single-Tone FFT with  $f_{IN} = 170.3$  MHz

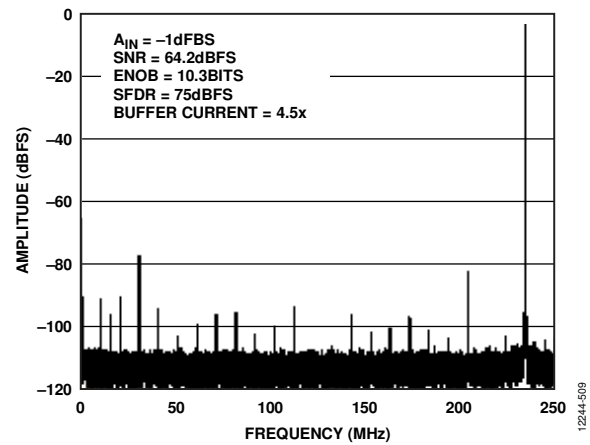


Figure 33. Single-Tone FFT with  $f_{IN} = 737.3$  MHz

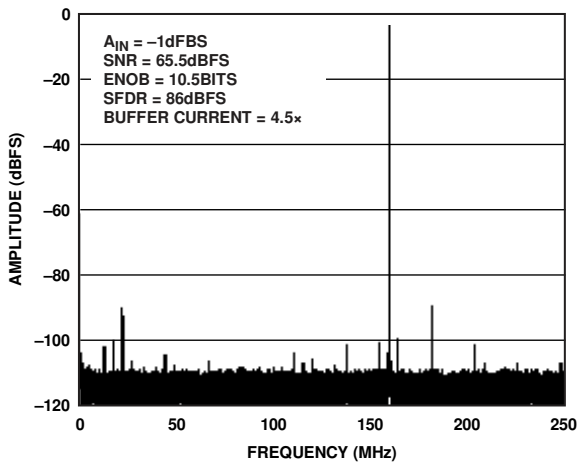


Figure 31. Single-Tone FFT with  $f_{IN} = 340.3$  MHz

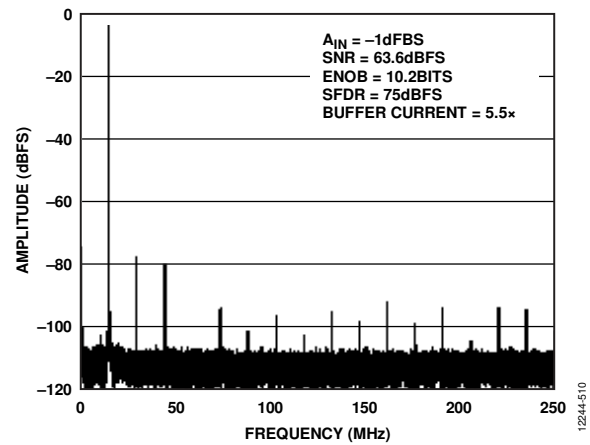


Figure 34. Single-Tone FFT with  $f_{IN} = 985.3$  MHz

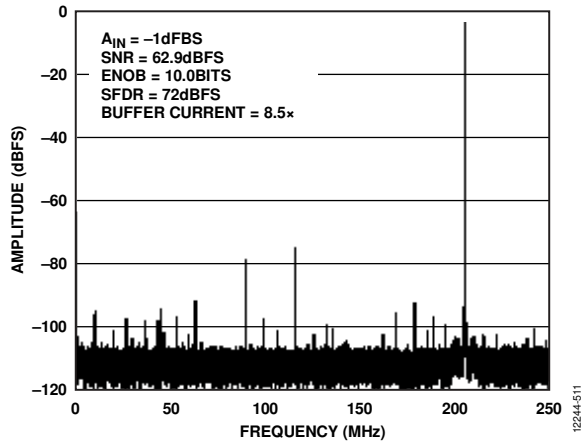


Figure 35. Single-Tone FFT with  $f_{IN} = 1213.3$  MHz

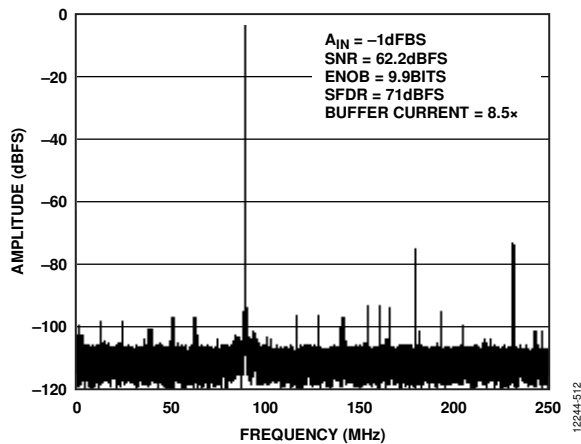


Figure 36. Single-Tone FFT with  $f_{IN} = 1413.3$  MHz

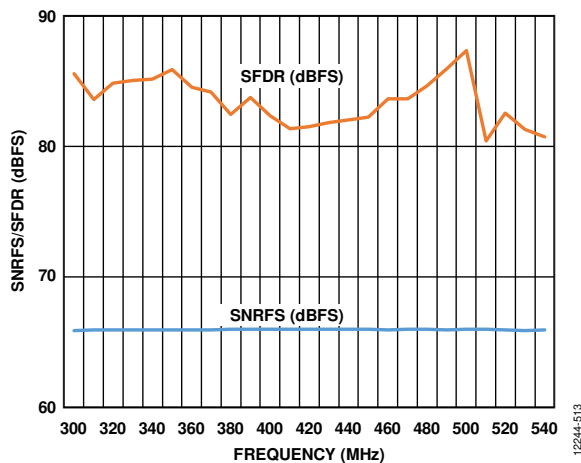


Figure 37. SNR/SFDR vs. Sample Rate ( $f_s$ ),  $f_{IN} = 170.3$  MHz; Buffer Current = 3.0x

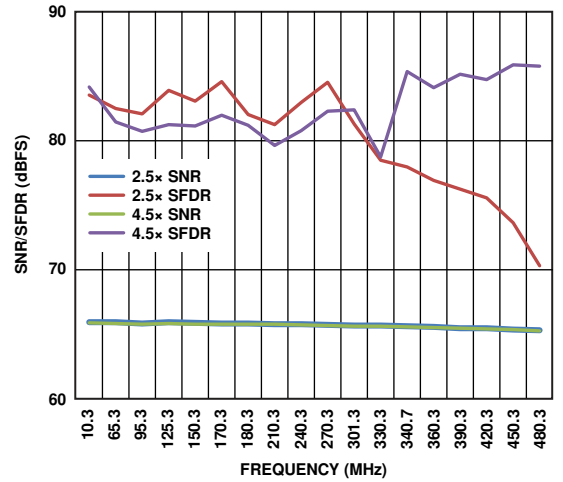


Figure 38. SNR/SFDR vs. Input Frequency;  $f_{IN} < 500$  MHz; Buffer Current = 2.5x and 4.5x (Uses Circuit Shown in Figure 63)

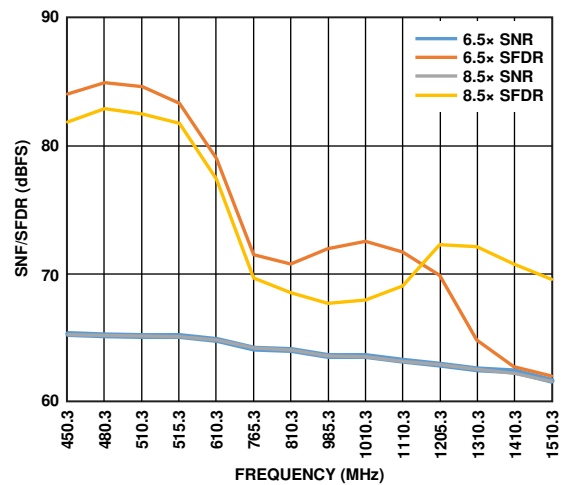


Figure 39. SNR/SFDR vs. Input Frequency;  $450$  MHz  $< f_{IN} < 1500$  MHz; Buffer Current = 6.5x and 8.5x (Uses Circuit Shown in Figure 64)

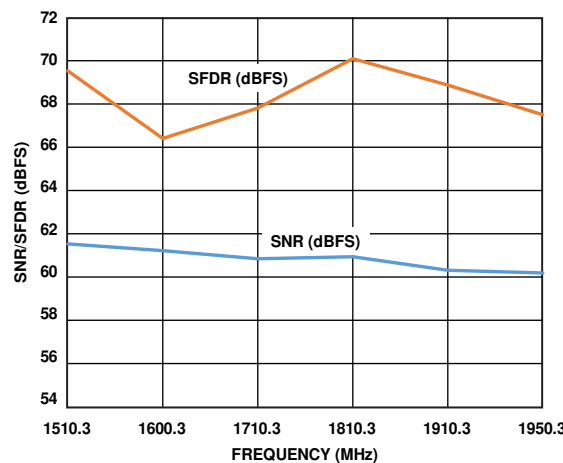


Figure 40. SNR/SFDR vs. Input Frequency;  $1500$  MHz  $< f_{IN} < 2000$  MHz; Buffer Current = 8.5x (Uses Circuit Shown in Figure 64)

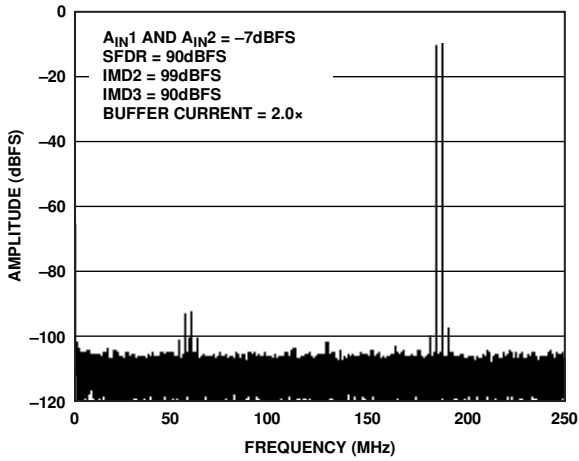


Figure 41. Two-Tone FFT;  $f_{IN1} = 184$  MHz,  $f_{IN2} = 187$  MHz

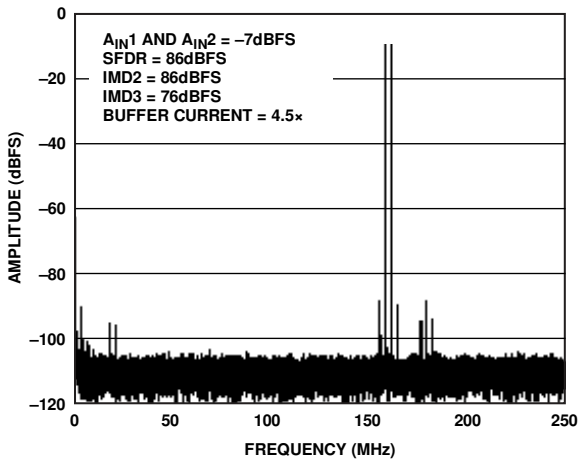


Figure 42. Two-Tone FFT;  $f_{IN1} = 338$  MHz,  $f_{IN2} = 341$  MHz

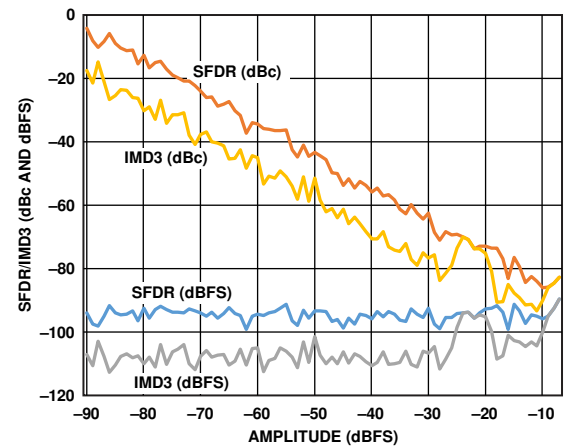


Figure 43. Two-Tone SFDR/IMD3 vs. Input Amplitude ( $A_{IN}$ ) with  $f_{IN1} = 184$  MHz and  $f_{IN2} = 187$  MHz

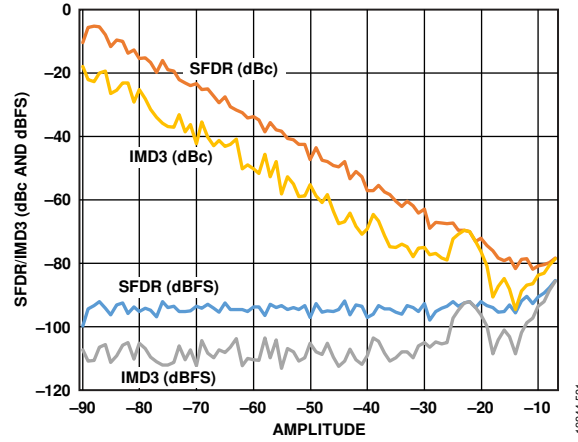


Figure 44. Two-Tone SFDR/IMD3 vs. Input Amplitude ( $A_{IN}$ ) with  $f_{IN1} = 338$  MHz and  $f_{IN2} = 341$  MHz

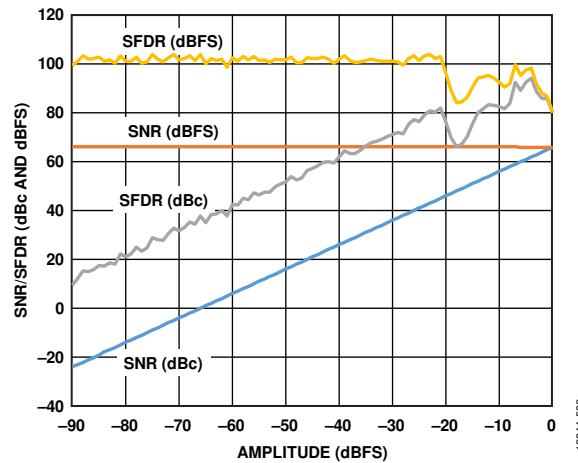


Figure 45. SNR/SFDR vs. Analog Input Level,  $f_{IN} = 10.3$  MHz; Buffer Current = 2.0x

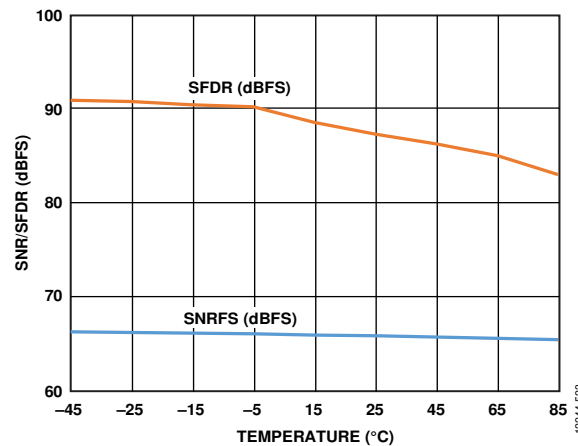


Figure 46. SNR/SFDR vs. Temperature,  $f_{IN} = 170.3$  MHz

12244-518

12244-519

12244-520

12244-521

12244-522

12244-523

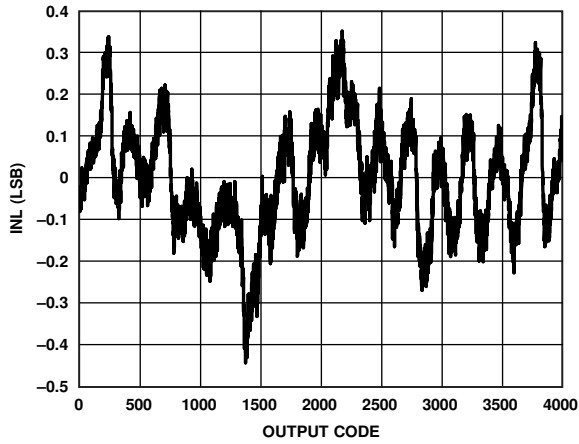


Figure 47. INL,  $f_{IN} = 10.3$  MHz

12244-524

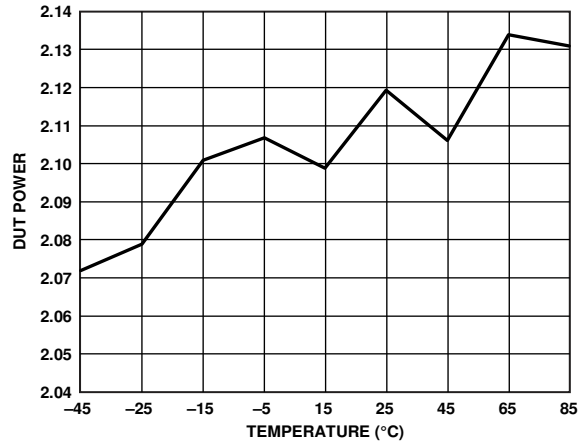


Figure 50. Power Dissipation vs. Temperature

12244-527

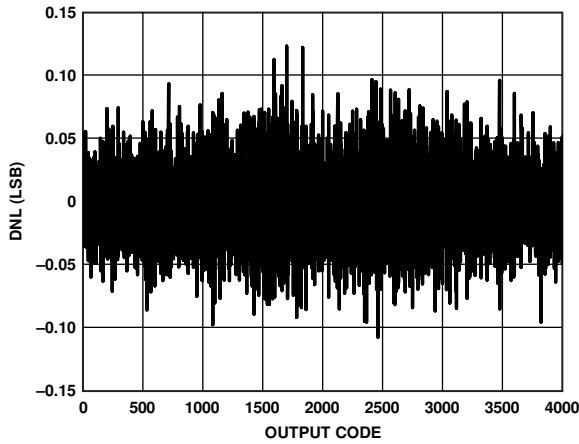


Figure 48. DNL,  $f_{IN} = 10$  MHz

12244-525

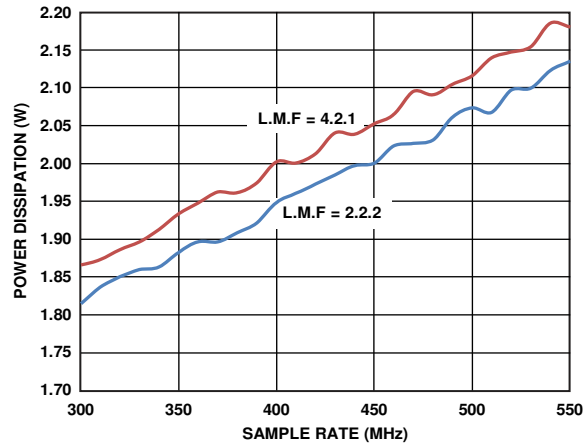


Figure 51. Power Dissipation vs. Sample Rate ( $f_s$ )

12244-528

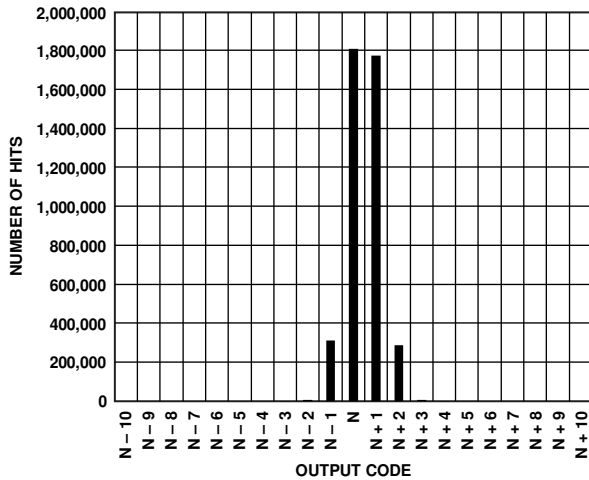


Figure 49. Input Referred Noise Histogram

12244-526



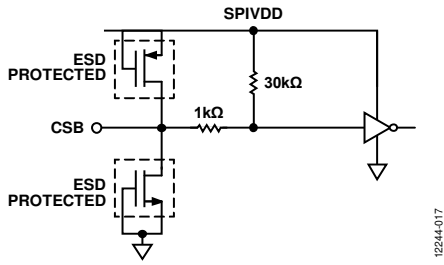


Figure 58. CSB Input

12244-017

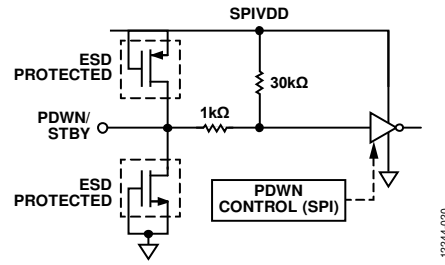


Figure 61. PDWN/STBY Input

12244-020

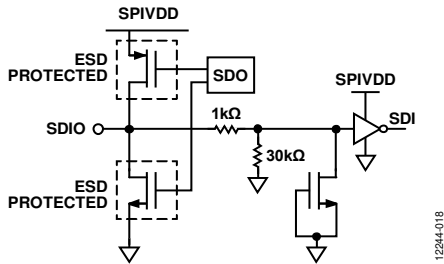


Figure 59. SDIO Input

12244-018

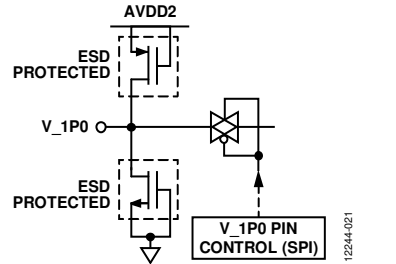


Figure 62. V\_1P0 Input

12244-021

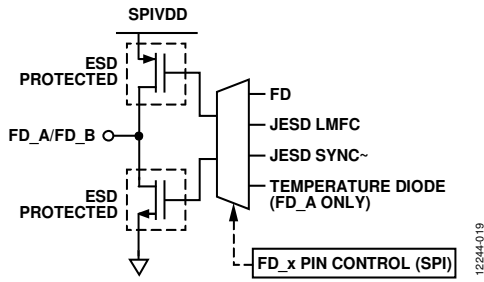


Figure 60. FD\_A/FD\_B Outputs

12244-019

## THEORY OF OPERATION

The AD9234 has two analog input channels and four JESD204B output lane pairs. The ADC is designed to sample wide bandwidth analog signals of up to 2 GHz. The AD9234 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The AD9234 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

The Subclass 1 JESD204B-based high speed serialized output data rate can be configured in one-lane ( $L = 1$ ), two-lane ( $L = 2$ ), and four-lane ( $L = 4$ ) configurations, depending on the sample rate and the decimation ratio. Multiple device synchronization is supported through the SYSREF $\pm$  and SYNCINB $\pm$  input pins.

### ADC ARCHITECTURE

The architecture of the AD9234 consists of an input buffered pipelined ADC. The input buffer is designed to provide a termination impedance to the analog input signal. This termination impedance can be changed using the SPI to meet the termination needs of the driver/amplifier. The default termination value is set to 400  $\Omega$ . The equivalent circuit diagram of the analog input termination is shown in Figure 52. The input buffer is optimized for high linearity, low noise, and low power.

The input buffer provides a linear high input impedance (for ease of drive) and reduces kickback from the ADC. The buffer is optimized for high linearity, low noise, and low power. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample; at the same time, the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

### ANALOG INPUT CONSIDERATIONS

The analog input to the AD9234 is a differential buffer. The internal common-mode voltage of the buffer is 2.05 V. The clock signal alternately switches the input circuit between sample mode and hold mode. When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, helps reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, thus, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input, which limits unwanted broadband noise. For more information, refer to the [AN-742 Application Note](#), the [AN-827 Application Note](#), and the Analog Dialogue article “*Transformer-Coupled Front-End for Wideband A/D Converters*” (Volume 39, April 2005). In general, the precise values depend on the application.

For best dynamic performance, the source impedances driving VIN+x and VIN-x must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9234, the available span is 1.34 V p-p differential for AD9234-1000 and 1.63 V p-p differential for AD9234-500.

#### Differential Input Configurations

There are several ways to drive the AD9234, either actively or passively. However, optimum performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 63 and Figure 64) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9234.

For low to midrange frequencies, a double balun or double transformer network (see Figure 63) is recommended for optimum performance of the AD9234. For higher frequencies in the second and third Nyquist zones, it is better to remove some of the front-end passive components to ensure wideband operation (see Figure 64).



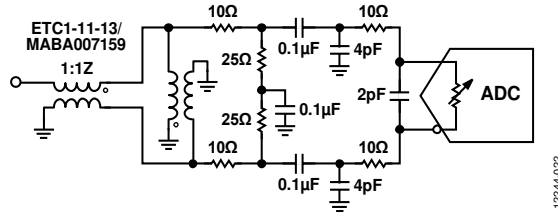


Figure 63. Differential Transformer-Coupled Configuration for Frequencies up to 500 MHz

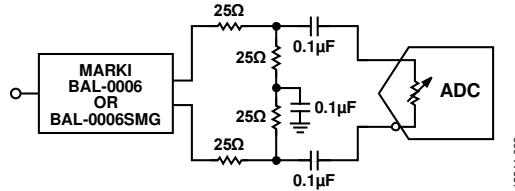


Figure 64. Differential Transformer-Coupled Configuration for Frequencies > 500 MHz

**Input Common Mode**

The analog inputs of the AD9234 are internally biased to the common mode as shown in Figure 65. The common-mode buffer has a limited range in that the performance suffers greatly if the common-mode voltage drops by more than 100 mV. Therefore, in dc-coupled applications, set the common-mode voltage to 2.05 V, ±100 mV to ensure proper ADC operation.

**Analog Input Controls and SFDR Optimization**

The AD9234 offers flexible controls for the analog inputs, such as input termination and buffer current. All of the available controls are shown in Figure 65.

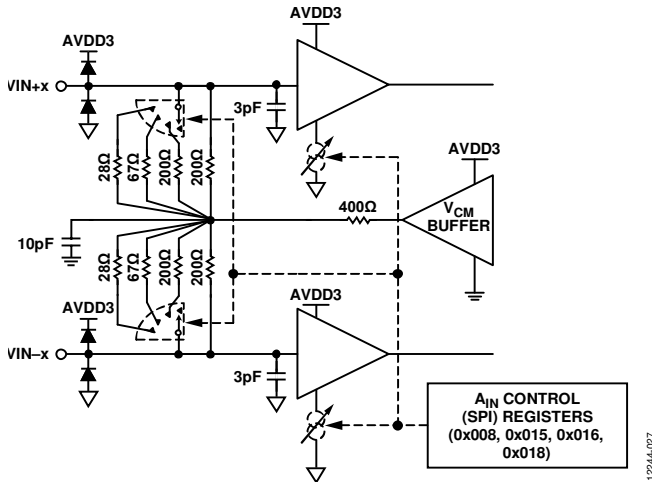


Figure 65. Analog Input Controls

Using Register 0x018, the buffer currents on each channel can be scaled to optimize the SFDR over various input frequencies and bandwidths of interest. As the input buffer currents are set, the amount of current required by the AVDD3 supply changes. This relationship is shown in Figure 66. For a complete list of buffer current settings, see Table 25.

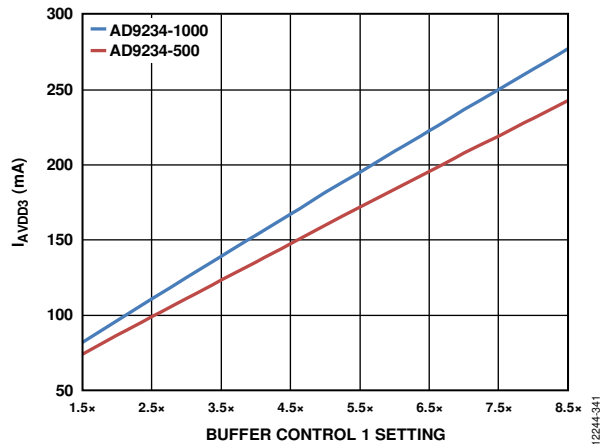


Figure 66. AVDD3 Power (I<sub>AVDD3</sub>) vs. Buffer Current Setting

Figure 67, Figure 68, and Figure 69 show how the SFDR for AD9234-1000 can be optimized using the buffer current setting in Register 0x018 for different Nyquist zones. Figure 70, Figure 71, and Figure 72 show how the SFDR for AD9234-500 can be optimized using the buffer current setting in Register 0x018 for different Nyquist zones. At frequencies greater than 1 GHz, it is better to run the ADC at input amplitudes less than  $-1$  dBFS ( $-3$  dBFS, for example). This greatly improves the linearity of the converted signal without sacrificing SNR performance.

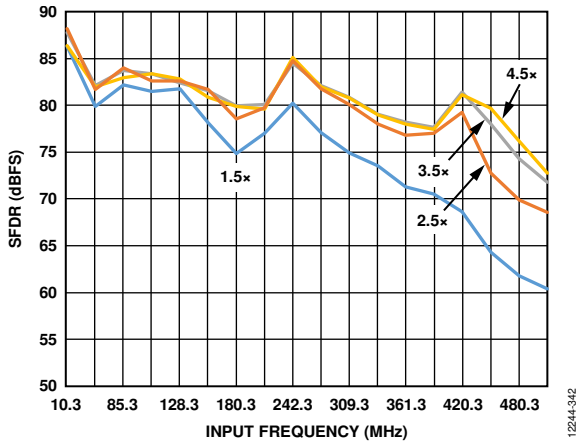


Figure 67. Buffer Current Sweeps, AD9234-1000; SFDR vs. Input Frequency ( $I_{BUFF}$ );  $f_{IN} < 500$  MHz

12244-342

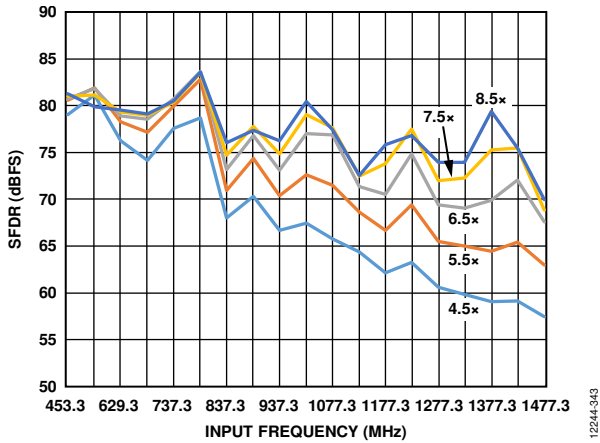


Figure 68. Buffer Current Sweeps, AD9234-1000; SFDR vs. Input Frequency ( $I_{BUFF}$ );  $500$  MHz  $< f_{IN} < 1500$  MHz

12244-343

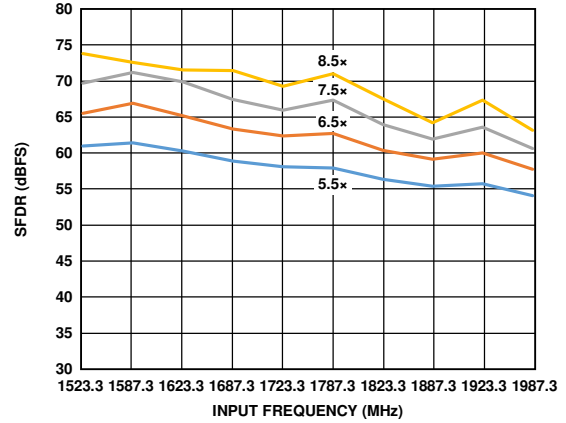


Figure 69. Buffer Current Sweeps, AD9234-1000; SFDR vs. Input Frequency ( $I_{BUFF}$ );  $1500$  MHz  $< f_{IN} < 2000$  MHz

12244-344

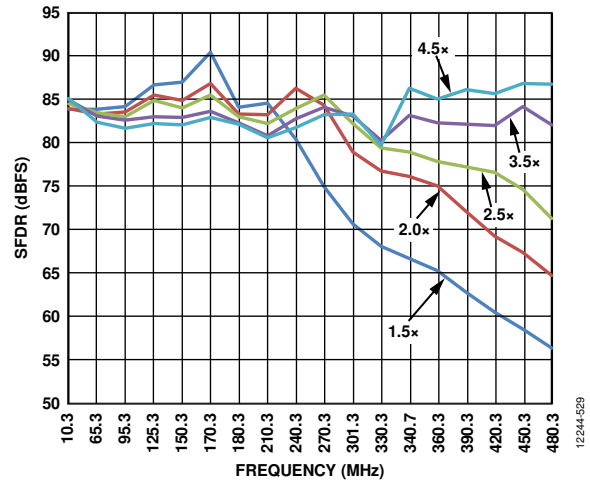


Figure 70. Buffer Current Sweeps, AD9234-500; SFDR vs. Input Frequency ( $I_{BUFF}$ );  $f_{IN} < 500$  MHz

12244-559

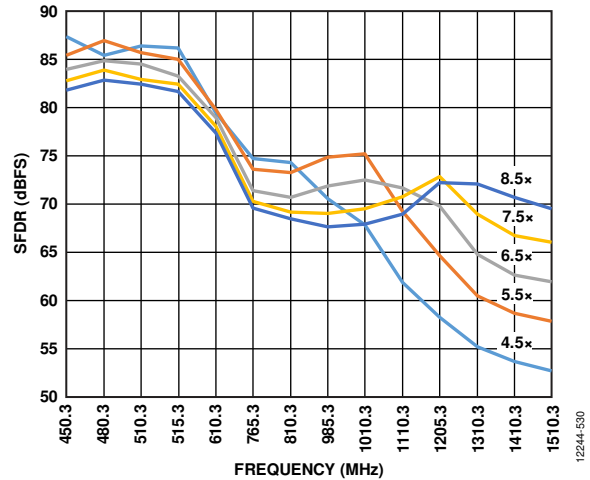


Figure 71. Buffer Current Sweeps, AD9234-500; SFDR vs. Input Frequency ( $I_{BUFF}$ );  $500$  MHz  $< f_{IN} < 1500$  MHz

12244-530

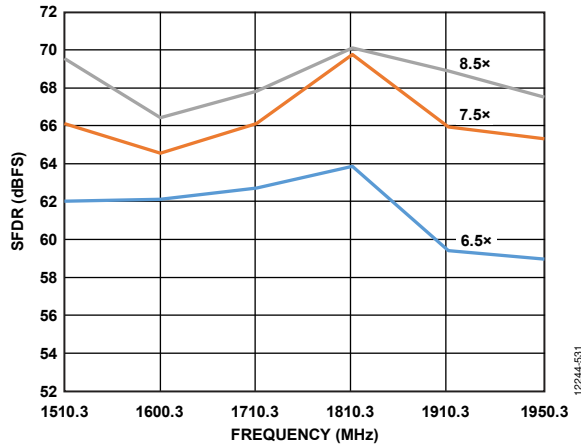


Figure 72. Buffer Current Sweeps, AD9234-500; SFDR vs. Input Frequency ( $I_{BUFF}$ );  $1500\text{ MHz} < f_{IN} < 2000\text{ MHz}$

Table 9 shows the recommended buffer current and full-scale voltage settings for the different analog input frequency ranges.

Table 9. SFDR Optimization for Analog Input Frequencies

| Input Frequency  | Input Buffer Current Control Setting, Register 0x018 |
|------------------|--|
| <400 MHz         | 2.5x or 3.0x   |
| 400 MHz to 1 GHz | 4.5x or 6.5x   |
| >1 GHz           | 6.5x or higher                                       |

**Absolute Maximum Input Swing**

The absolute maximum input swing allowed at the inputs of the AD9234 is 4.3 V p-p differential. Signals operating near or at this level can cause permanent damage to the ADC.

**VOLTAGE REFERENCE**

A stable and accurate 1.0 V voltage reference is built into the AD9234. This internal 1.0 V reference is used to set the full-scale input range of the ADC. For more information on adjusting the input swing, see Table 25. Figure 73 shows the block diagram of the internal 1.0 V reference controls.

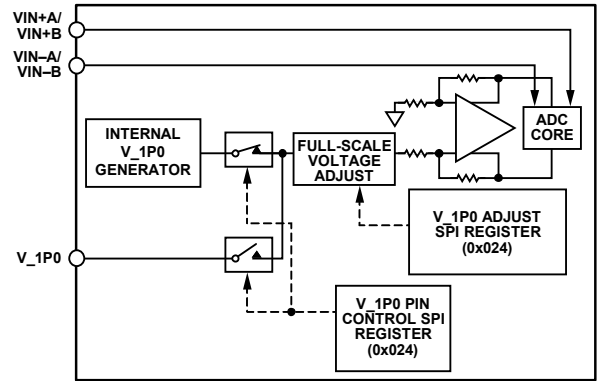


Figure 73. Internal Reference Configuration and Controls

The SPI Register 0x024 enables the user to either use this internal 1.0 V reference, or to provide an external 1.0 V reference. When using an external voltage reference, provide a 1.0 V reference.

The use of an external reference may be necessary, in some applications, to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 74 shows the typical drift characteristics of the internal 1.0 V reference.

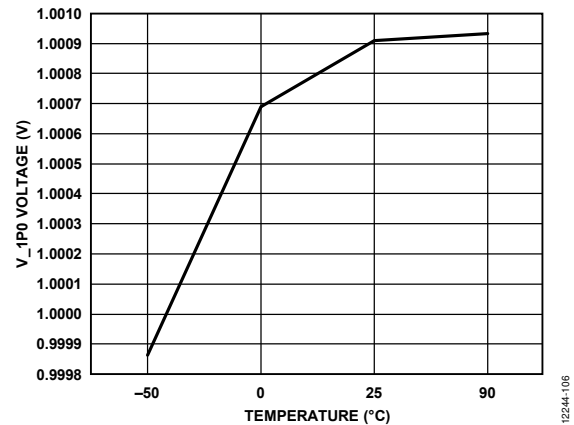


Figure 74. Typical V<sub>1P0</sub> Drift

The external reference must be a stable 1.0 V reference. The ADR130 is a good option for providing the 1.0 V reference. Figure 75 shows how the ADR130 can be used to provide the external 1.0 V reference to the AD9234. The grayed out areas show unused blocks within the AD9234 while using the ADR130 to provide the external reference.

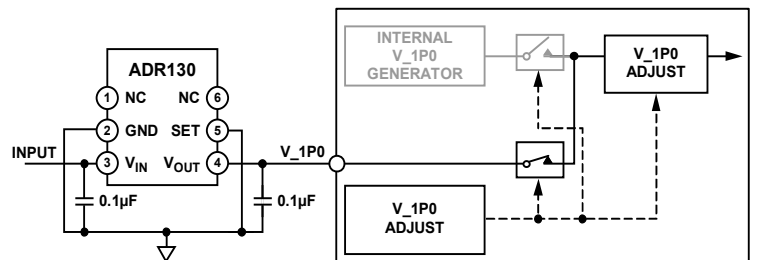


Figure 75. External Reference Using ADR130

**CLOCK INPUT CONSIDERATIONS**

For optimum performance, drive the AD9234 sample clock inputs (CLK+ and CLK-) with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK- pins via a transformer or clock drivers. These pins are biased internally and require no additional biasing.

Figure 76 shows a preferred method for clocking the AD9234. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer.

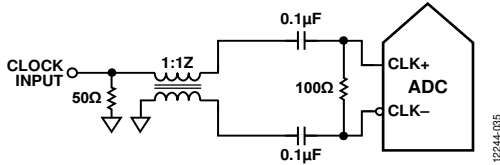


Figure 76. Transformer-Coupled Differential Clock

Another option is to ac couple a differential CML or LVDS signal to the sample clock input pins, as shown in Figure 77 and Figure 78.

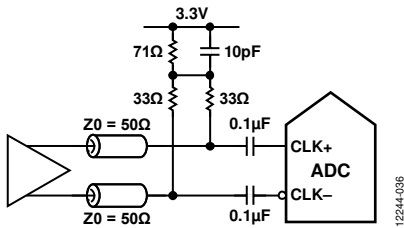
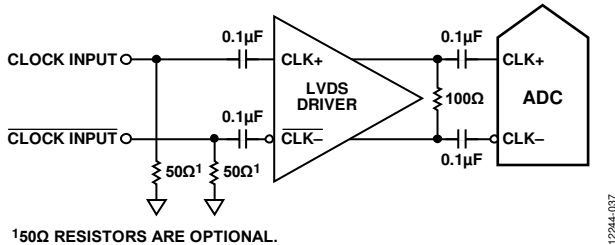


Figure 77. Differential CML Sample Clock



150Ω RESISTORS ARE OPTIONAL.

Figure 78. Differential LVDS Sample Clock

**Clock Duty Cycle Considerations**

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. In applications where the clock duty cycle cannot be guaranteed to be 50%, a higher multiple frequency clock can be supplied to the device. The AD9234 can be clocked at 2 GHz with the internal clock divider set to 2. The output of the divider offers a 50% duty cycle, high slew rate (fast edge) clock signal to the internal ADC. See the Memory Map section for more details on using this feature.

**Input Clock Divider**

The AD9234 contains an input clock divider with the ability to divide the Nyquist input clock by 1, 2, 4, and 8. The divider ratios can be selected using Register 0x10B. This is shown in Figure 79.

The maximum frequency at the CLK± inputs is 4 GHz. This is the limit of the divider. In applications where the clock input is a multiple of the sample clock, care must be taken to program the appropriate divider ratio into the clock divider before applying the clock signal. This ensures that the current transients during device startup are controlled.

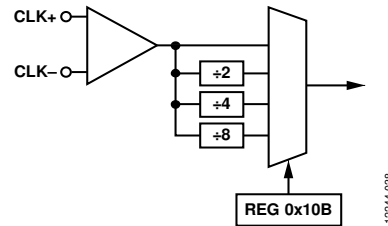


Figure 79. Clock Divider Circuit

The AD9234 clock divider can be synchronized using the external SYSREF± input. A valid SYSREF± causes the clock divider to reset to a programmable state. This feature is enabled by setting Bit 7 of Register 0x10D. This synchronization feature allows multiple devices to have their clock dividers aligned to guarantee simultaneous input sampling. See the Deterministic Latency section for more information

**Input Clock Divider 1/2 Period Delay Adjust**

The input clock divider inside the AD9234 provides phase delay in increments of 1/2 the input clock cycle. Register 0x10C can be programmed to enable this delay independently for each channel. Changing this register does not affect the stability of the JESD204B link.

**Clock Fine Delay Adjust**

The AD9234 sampling edge instant can be adjusted by writing to Register 0x117 and Register 0x118. Setting Bit 0 of Register 0x117 enables the feature, and Register 0x118, Bits[7:0] set the value of the delay. This value can be programmed individually for each channel. The clock delay can be adjusted from -151.7 ps to +150 ps in ~1.7 ps increments. The clock delay adjust takes effect immediately when it is enabled via SPI writes. Enabling the clock fine delay adjust in Register 0x117 causes a datapath reset. However, the contents of Register 0x118 can be changed without affecting the stability of the JESD204B link.

**CLOCK JITTER CONSIDERATIONS**

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency ( $f_A$ ) due only to aperture jitter ( $t_j$ ) can be calculated by

$$SNR = 20 \times \log_{10} (2 \times \pi \times f_A \times t_j)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 80).

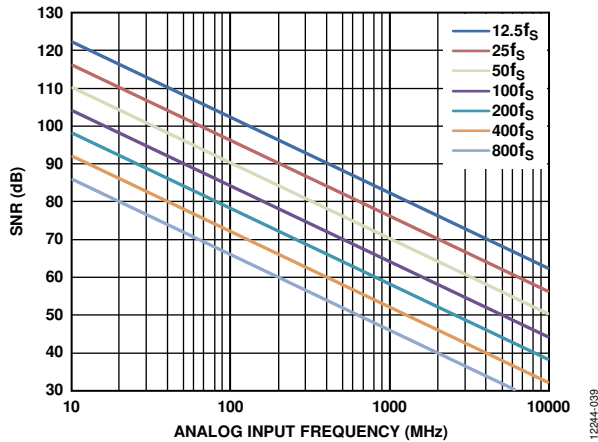


Figure 80. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9234. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by the original clock at the last step. Refer to the [AN-501 Application Note](#) and the [AN-756 Application Note](#) for more in-depth information about jitter performance as it relates to ADCs.

**POWER-DOWN/STANDBY MODE**

The AD9234 has a PDWN/STBY pin that can be used to configure the device in power-down or standby mode. The default operation is the PDWN function. The PDWN/STBY pin is a logic high pin. When in power-down mode, the JESD204B link is disrupted. The power-down option can also be set via Register 0x03F and Register 0x040.

In standby mode, the JESD204B link is not disrupted and transmits zeroes for all converter samples. This can be changed using Register 0x571, Bit 7 to select /K/ characters.

**TEMPERATURE DIODE**

The AD9234 contains a diode-based temperature sensor for measuring the temperature of the die. This diode can output a voltage and serve as a coarse temperature sensor to monitor the internal die temperature.

The temperature diode voltage can be output to the FD\_A pin using the SPI. Use Register 0x028, Bit 0 to enable or disable the diode. Register 0x028 is a local register. Channel A must be selected in the device index register (Register 0x008) to enable the temperature diode readout. Configure the FD\_A pin to output the diode voltage by programming Register 0x040[2:0]. See Table 25 for more information.

The voltage response of the temperature diode (SPIVDD = 1.8 V) is shown in Figure 81.

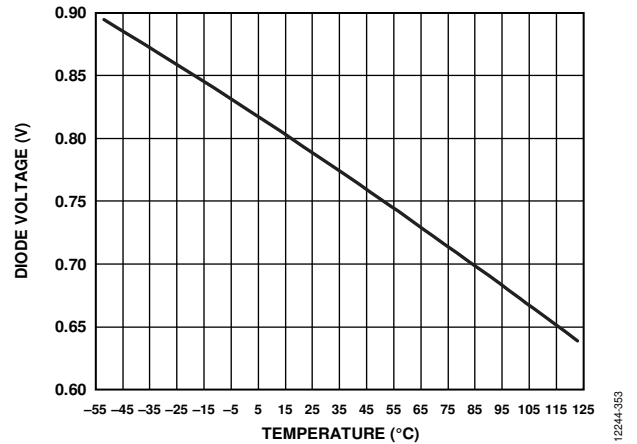


Figure 81. Diode Voltage vs. Temperature

## ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overrange bit in the JESD204B outputs provides information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD9234 contains fast detect circuitry for individual channels to monitor the threshold and assert the FD\_A and FD\_B pins.

### ADC OVERRANGE

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be embedded within the JESD204B link as a control bit (when CSB > 0). The latency of this overrange indicator matches the sample latency.

The AD9234 also records any overrange condition in any of the four virtual converters. For more information on the virtual converters, refer to Figure 87. The overrange status of each virtual converter is registered as a sticky bit in Register 0x563. The contents of Register 0x563 can be cleared using Register 0x562, by toggling the bits corresponding to the virtual converter to set and reset position.

### FAST THRESHOLD DETECTION (FD\_A AND FD\_B)

The FD bit (enabled via the control bits in Register 0x559 and Register 0x55A) is immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is only cleared when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bit from excessively toggling.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 82.

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located at Register 0x247 and Register 0x248. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 28 clock cycles (maximum). The approximate upper threshold magnitude is defined by

$$\text{Upper Threshold Magnitude (dBFS)} = 20 \log (\text{Threshold Magnitude}/2^{13})$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x249 and Register 0x24A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency, but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\text{Lower Threshold Magnitude (dBFS)} = 20 \log (\text{Threshold Magnitude}/2^{13})$$

For example, to set an upper threshold of -6 dBFS, write 0xFF to Register 0x247 and Register 0x248. To set a lower threshold of -10 dBFS, write 0xA1D to Register 0x249 and Register 0x24A.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located at Register 0x24B and Register 0x24C. See the Memory Map section (Register 0x040, and Register 0x245 to Register 0x24C in Table 25) for more details.

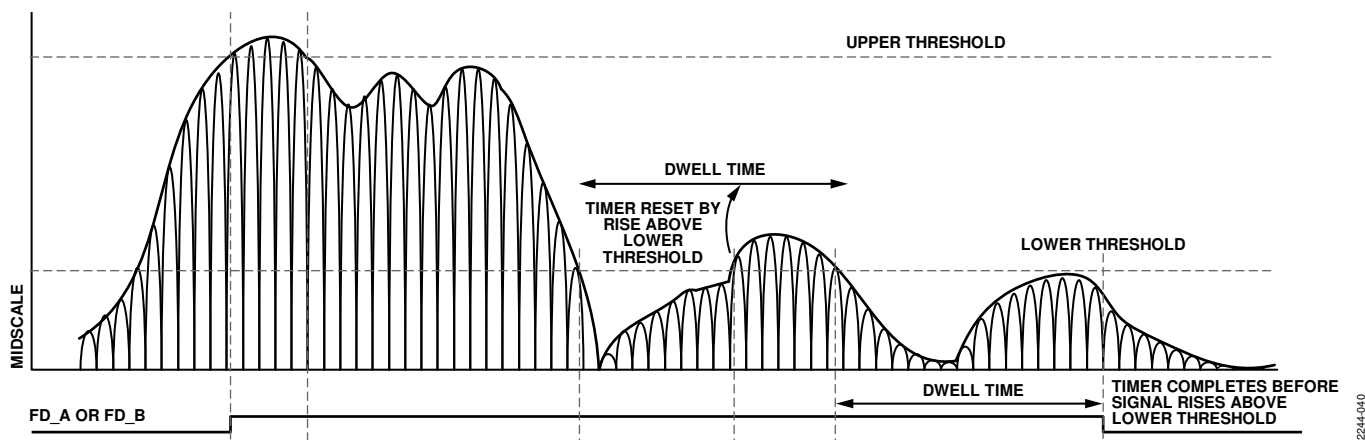


Figure 82. Threshold Settings for FD\_A and FD\_B Signals



## SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained either by reading back the internal values from the SPI port or by embedding the signal monitoring information into the JESD204B interface as special control bits. A global, 24-bit programmable period controls the duration of the measurement. Figure 83 shows the simplified block diagram of the signal monitor block.

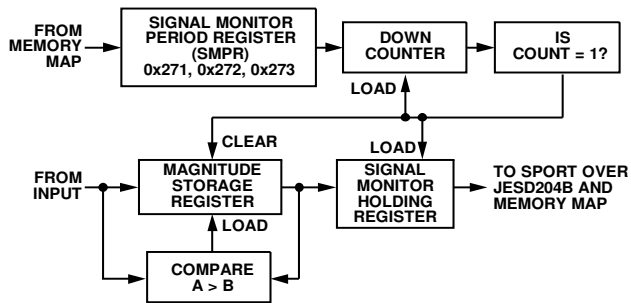


Figure 83. Signal Monitor Block

The peak detector captures the largest signal within the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is a 13-bit value and the observation period is 24 bits and represents converter output samples. The peak magnitude can be derived by using the following equation:

$$\text{Peak Magnitude (dBFS)} = 20 \log (\text{Peak Detector Value}/2^{13})$$

The magnitude of the input port signal is monitored over a programmable time period, which is determined by the signal monitor period register (SMPR). The peak detector function is enabled by setting Bit 1 of Register 0x270 in the signal monitor control register. The 24-bit SMPR must be programmed before activating this mode.

After enabling this mode, the value in the SMPR is loaded into a monitor period timer, which decrements at the decimated clock rate. The magnitude of the input signal is compared with the

value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map or output through the SPORT over the JESD204B interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. In addition, the magnitude of the first input sample is updated in the magnitude storage register, and the comparison and update procedure, as explained previously, continues.

### SPORT Over JESD204B

The signal monitor data can also be serialized and sent over the JESD204B interface as control bits. These control bits must be deserialized from the samples to reconstruct the statistical data. This function is enabled by setting Bit 1 and Bit 0 of Register 0x279 and Bit 1 of Register 0x27A. Figure 84 shows two different example configurations for the signal monitor control bit locations inside the JESD204B samples. There are a maximum of three control bits that can be inserted into the JESD204B samples; however, only one control bit is required for the signal monitor. Control bits are inserted from MSB to LSB. If only one control bit is to be inserted (CS = 1), then only the most significant control bit is used (see Example Configuration 1 and Example Configuration 2 in Figure 84). To select the SPORT over JESD204B option, program Register 0x559, Register 0x55A, and Register 0x58F. See Table 25 for more information on setting these bits.

Figure 85 shows the 25-bit frame data that encapsulates the peak detector value. The frame data is transmitted MSB first with five 5-bit subframes. Each subframe contains a start bit that can be used by a receiver to validate the deserialized data. Figure 86 shows the SPORT over JESD204B signal monitor data with a monitor period timer set to 80 samples.

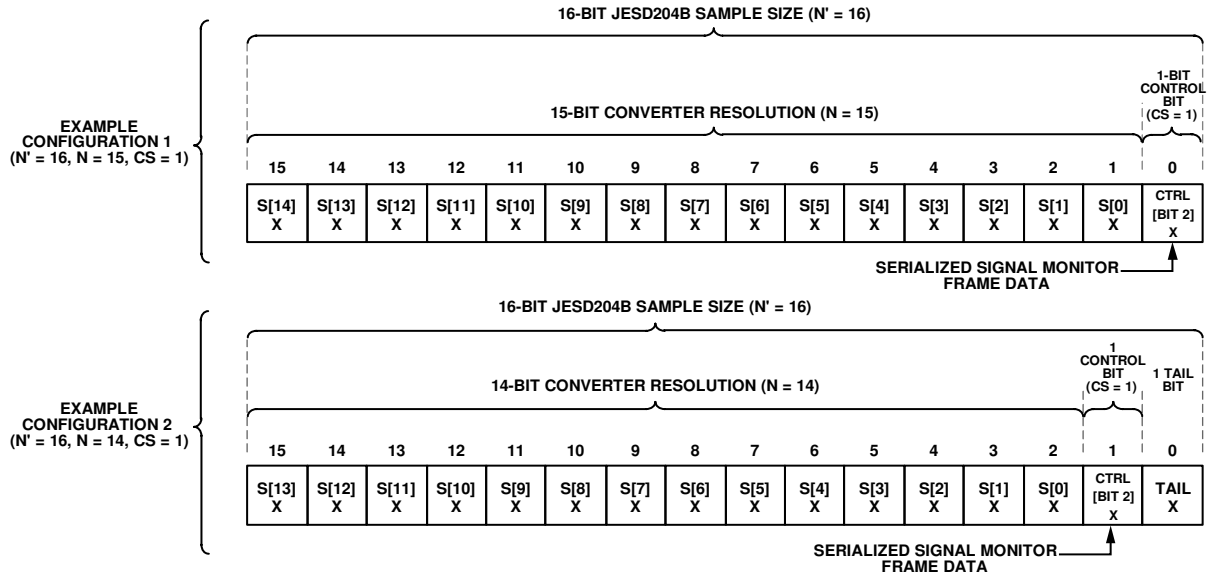


Figure 84. Signal Monitor Control Bit Locations

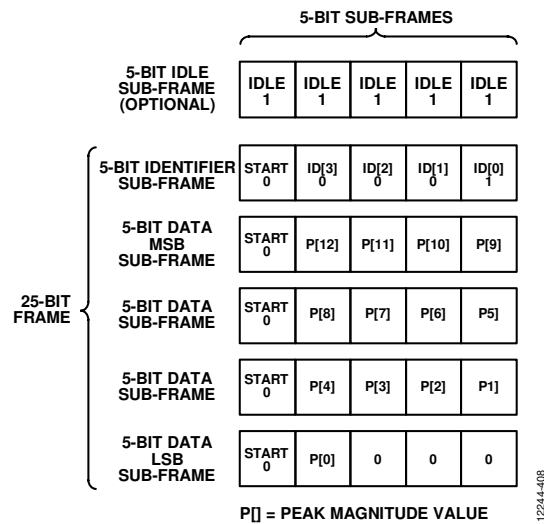
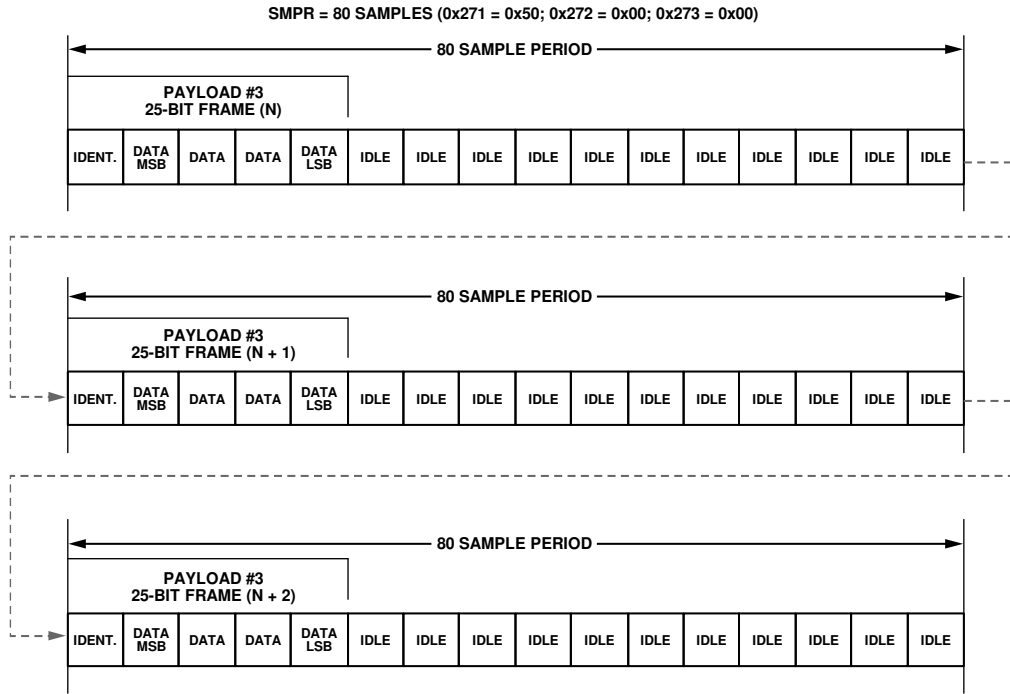


Figure 85. SPORT over JESD204B Signal Monitor Frame Data





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Figure 86. SPORT over JESD204B Signal Monitor Example with Period = 80 Samples

## DIGITAL DOWNCONVERTER (DDC)

The AD9234 includes two digital downconverters (DDC 0 and DDC 1) that provide filtering and reduce the output data rate. This digital processing section includes a half-band decimating filter, a gain stage, and a complex to real conversion stage. Each of these processing blocks has control lines that allow it to be independently enabled and disabled to provide the desired processing function. The digital downconverter can be configured to output either real data or complex output data.

### DDC GENERAL DESCRIPTION

The two DDC blocks are used to extract a portion of the full digital spectrum captured by the ADC(s). They are intended for IF sampling or oversampled baseband radios requiring wide bandwidth input signals.

Each DDC block contains a decimate by 2 digital processing block, as shown in Figure 87.

When DDCs have different decimation ratios, the chip decimation ratio (Register 0x201) must be set to the lowest decimation ratio of all the DDC blocks. In this scenario, samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate. Whenever the NCO frequency is set or changed, the DDC soft reset must be issued. If the DDC soft reset is not issued, the output may potentially show amplitude variations. The DDCs output a 16-bit stream. To enable this operation, the converter number of bits N is set to a default value of 16, even though the analog core only outputs 12 bits.

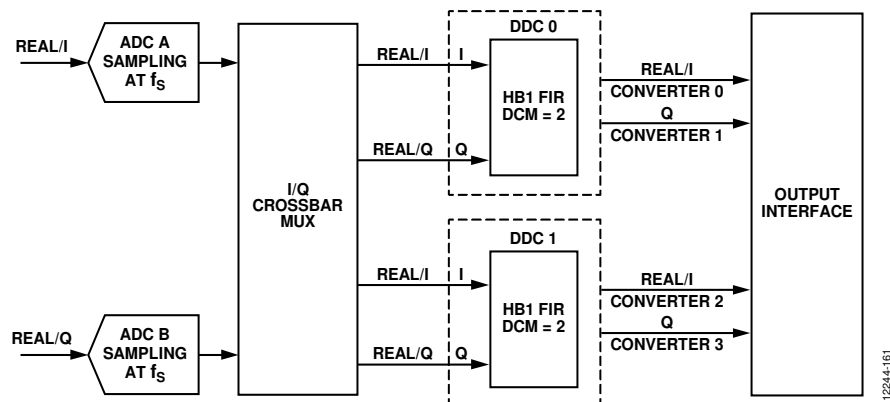


Figure 87. DDC Detailed Block Diagram

**HALF-BAND FILTER**

The AD9234 offers one half-band filter per DDC to enable digital signal processing of the ADC converted data.

The decimate by 2, half-band (HB), low-pass FIR filter uses a 55-tap, symmetrical, fixed coefficient filter implementation, optimized for low power consumption. The HB filter is enabled when the DDC is selected. Table 10 and Figure 88 show the coefficients and response of the HB1 filter.

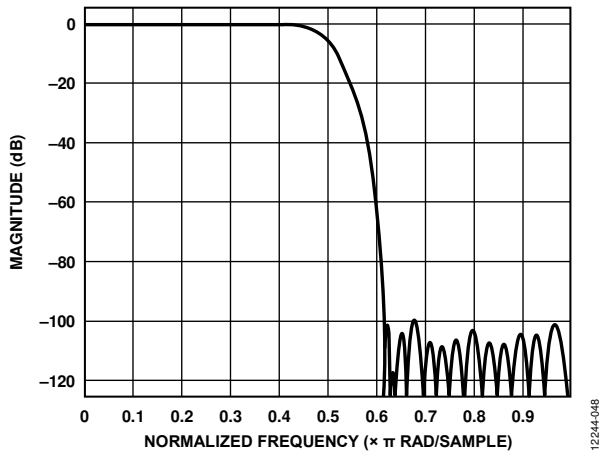


Figure 88. HB1 Filter Response

Table 10. Half-Band Filter Coefficients

| HB1 Coefficient Number | Normalized Coefficient | Decimal Coefficient (21-Bit) |
|------------------------|------------------------|------------------------------|
| C1, C55                | -0.000023              | -24                          |
| C2, C54                | 0                      | 0                            |
| C3, C53                | 0.000097               | 102                          |
| C4, C52                | 0                      | 0                            |
| C5, C51                | -0.000288              | -302                         |
| C6, C50                | 0                      | 0                            |
| C7, C49                | 0.000696               | 730                          |
| C8, C48                | 0                      | 0                            |
| C9, C47                | -0.0014725             | -1544                        |
| C10, C46               | 0                      | 0                            |
| C11, C45               | 0.002827               | 2964                         |
| C12, C44               | 0                      | 0                            |
| C13, C43               | -0.005039              | -5284                        |
| C14, C42               | 0                      | 0                            |
| C15, C41               | 0.008491               | 8903                         |
| C16, C40               | 0                      | 0                            |
| C17, C39               | -0.013717              | -14,383                      |
| C18, C38               | 0                      | 0                            |
| C19, C37               | 0.021591               | 22640                        |
| C20, C36               | 0                      | 0                            |
| C21, C35               | -0.033833              | -35476                       |
| C22, C34               | 0                      | 0                            |
| C23, C33               | 0.054806               | 57468                        |
| C24, C32               | 0                      | 0                            |
| C25, C31               | -0.100557              | -105442                      |
| C26, C30               | 0                      | 0                            |
| C27, C29               | 0.316421               | 331,792                      |
| C28                    | 0.500000               | 524,288                      |

## DDC GAIN STAGE

Each DDC contains an independently controlled gain stage. The gain is selectable as either 0 dB or 6 dB. When mixing a real input signal down to baseband, it is recommended that the user enable the 6 dB of gain to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the mixer has already recentered the dynamic range of the signal within the full scale of the output bits and no additional gain is necessary. However, the optional 6 dB gain can be used to compensate for low signal strengths. The downsample by 2 portion of the HB1 FIR filter is bypassed when using the complex to real conversion stage (see Figure 89).

## DDC COMPLEX TO REAL CONVERSION

Each DDC contains an independently controlled complex to real conversion block. The complex to real conversion block reuses the last filter (HB1 FIR) in the filtering stage, along with an  $f_s/4$  complex mixer, to upconvert the signal.

After upconverting the signal, the Q portion of the complex mixer is no longer needed and is dropped.

Figure 89 shows a simplified block diagram of the complex to real conversion.

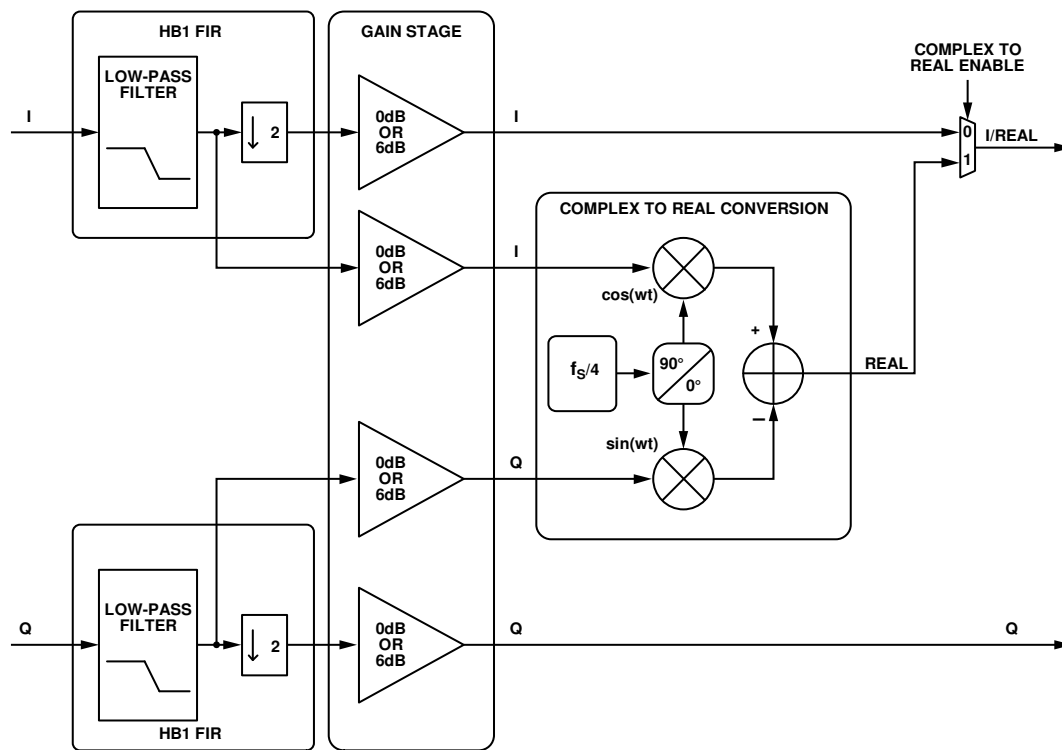


Figure 89. Complex to Real Conversion Block

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## DIGITAL OUTPUTS

### INTRODUCTION TO THE JESD204B INTERFACE

The AD9234 digital outputs are designed to the JEDEC standard JESD204B, serial interface for data converters. JESD204B is a protocol to link the AD9234 to a digital processing device over a serial interface with lane rates of up to 10 Gbps. The benefits of the JESD204B interface over LVDS include a reduction in required board area for data interface routing, and an ability to enable smaller packages for converter and logic devices.

### JESD204B OVERVIEW

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8B/10B encoding as well as optional scrambling to form serial output data. Lane synchronization is supported through the use of special control characters during the initial establishment of the link. Additional control characters are embedded in the data stream to maintain synchronization thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, users are encouraged to refer to the JESD204B standard.

The AD9234 JESD204B data transmit block maps up to two physical ADCs or up to eight virtual converters (when DDCs are enabled) over a link. A link can be configured to use one, two, or four JESD204B lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (the AD9234 output) and the JESD204B receiver (the logic device input).

The JESD204B link is described according to the following parameters:

- L = number of lanes/converter device (lanes/link) (AD9234 value = 1, 2, or 4)
- M = number of converters/converter device (virtual converters/link) (AD9234 value = 1, 2, 4, or 8)
- F = octets/frame (AD9234 value = 1, 2, 4, 8, or 16)
- N' = number of bits per sample (JESD204B word size) (AD9234 value = 8 or 16)
- N = converter resolution (AD9234 value = 7 to 16)
- CS = number of control bits/sample (AD9234 value = 0, 1, 2, or 3)

- K = number of frames per multiframe (AD9234 value = 4, 8, 12, 16, 20, 24, 28, or 32)
- S = samples transmitted/single converter/frame cycle (AD9234 value = set automatically based on L, M, F, and N')
- HD = high density mode (AD9234 = set automatically based on L, M, F, and N')
- CF = number of control words/frame clock cycle/converter device (AD9234 value = 0)

Figure 90 shows a simplified block diagram of the AD9234 JESD204B link. By default, the AD9234 is configured to use two converters and four lanes. Converter A data is output to SERDOUT0± and/or SERDOUT1±, and Converter B is output to SERDOUT2± and/or SERDOUT3±. The AD9234 allows other configurations such as combining the outputs of both converters onto a single lane, or changing the mapping of the A and B digital output paths. These modes are set up via a quick configuration register in the SPI register map, along with additional customizable options.

By default in the AD9234, the 12-bit converter word from each converter is broken into two octets (eight bits of data). Bit 13 (MSB) through Bit 6 are in the first octet. The second octet contains Bit 5 through Bit 0 (LSB) and two tail bits. The tail bits can be configured as zeros or a pseudorandom number (PN) sequence. The tail bits can also be replaced with control bits indicating overrange, SYSREF±, signal monitor, or fast detect output.

The two resulting octets can be scrambled. Scrambling is optional; however, it is recommended to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self-synchronizing, polynomial-based algorithm defined by the equation  $1 + x^{14} + x^{15}$ . The descrambler in the receiver is a self-synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8B/10B encoder. The 8B/10B encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 91 shows how the 12-bit data is taken from the ADC, the tail bits are added, the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 91 illustrates the default data format.

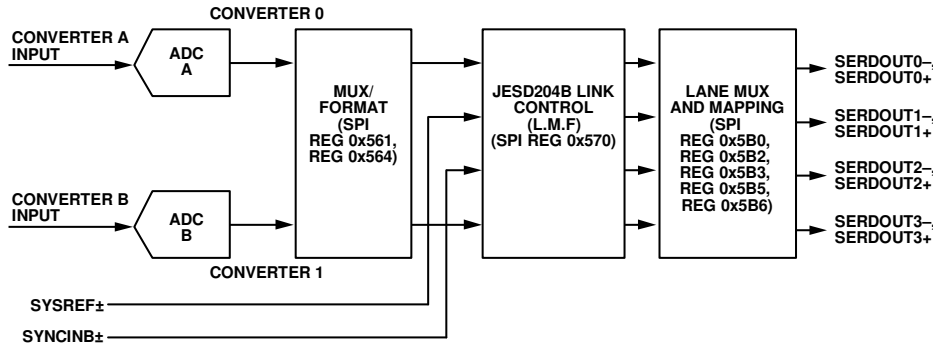


Figure 90. Transmit Link Simplified Block Diagram Showing Full Bandwidth Mode (Register 0x200 = 0x00)

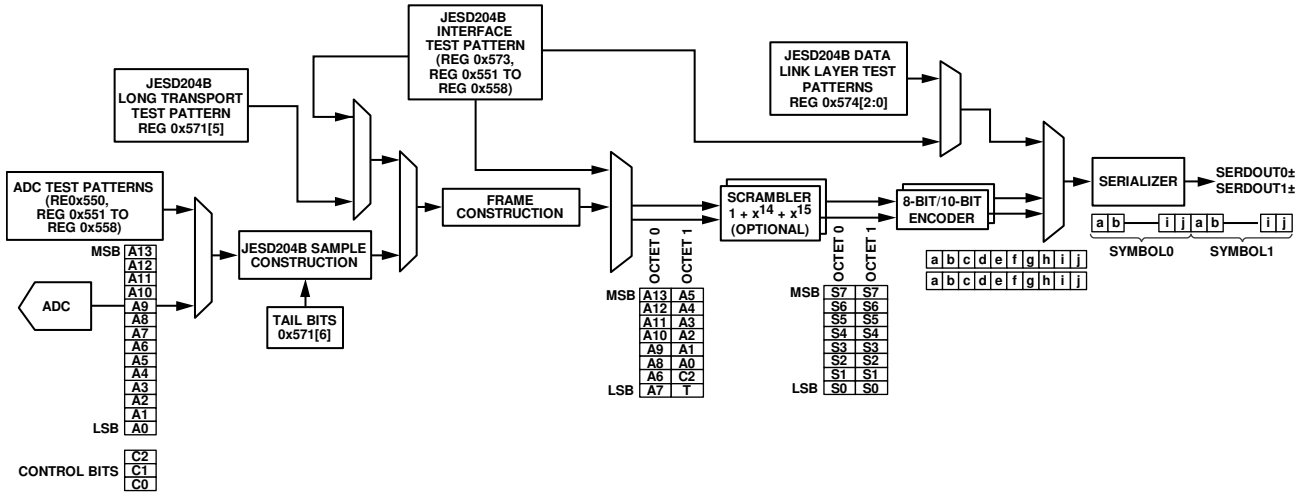


Figure 91. ADC Output Datapath Showing Data Framing

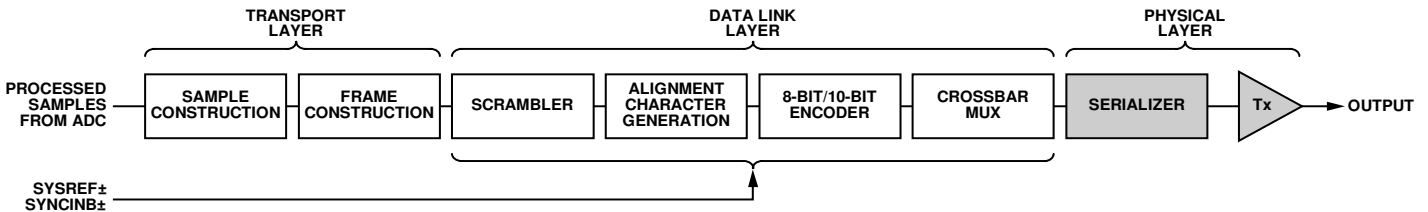


Figure 92. Data Flow

## FUNCTIONAL OVERVIEW

The block diagram in Figure 92 shows the flow of data through the JESD204B hardware from the sample input to the physical output. The processing can be divided into layers that are derived from the open-source initiative (OSI) model widely used to describe the abstraction layers of communications systems. These layers are the transport layer, data link layer, and physical layer (serializer and output driver).

### Transport Layer

The transport layer handles packing the data (consisting of samples and optional control bits) into JESD204B frames that are mapped to 8-bit octets. These octets are sent to the data link layer. The transport layer mapping is controlled by rules derived from the link parameters. Tail bits are added to fill gaps where required. The following equation can be used to determine the number of tail bits within a sample (JESD204B word):

$$T = N' - N - CS$$

### Data Link Layer

The data link layer is responsible for the low level functions of passing data across the link. These include optionally scrambling the data, inserting control characters for multichip synchronization/lane alignment/monitoring, and encoding 8-bit octets into 10-bit symbols. The data link layer is also responsible for sending the initial lane alignment sequence (ILAS), which contains the link configuration data used by the receiver to verify the settings in the transport layer.

### Physical Layer

The physical layer consists of the high speed circuitry clocked at the serial clock rate. In this layer, parallel data is converted into one, two, or four lanes of high speed differential serial data.

## JESD204B LINK ESTABLISHMENT

The AD9234 JESD204B transmitter (Tx) interface operates in Subclass 1 as defined in the JEDEC Standard JESD204B (July 2011 specification). The link establishment process is divided into the following steps: code group synchronization and SYNCINB±, initial lane alignment sequence, and user data and error correction.

### Code Group Synchronization (CGS) and SYNCINB±

The CGS is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver must locate /K28.5/ characters in its input data stream using clock and data recovery (CDR) techniques.

The receiver issues a synchronization request by asserting the SYNCINB± pin of the AD9234 low. The JESD204B Tx then begins sending /K/ characters. After the receiver has synchronized, it waits for the correct reception of at least four consecutive /K/ symbols. It then deasserts SYNCINB±. The AD9234 then transmits an ILAS on the following local multiframe clock (LMFC) boundary.

For more information on the code group synchronization phase, refer to the JEDEC Standard JESD204B, July 2011, Section 5.3.3.1.

The SYNCINB± pin operation can also be controlled by the SPI. The SYNCINB± signal is a differential dc-coupled LVDS mode signal by default, but it can also be driven single-ended. For more information on configuring the SYNCINB± pin operation, refer to Register 0x572.

### Initial Lane Alignment Sequence (ILAS)

The ILAS phase follows the CGS phase and begins on the next LMFC boundary. The ILAS consists of four multiframes, with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS begins by sending an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent, starting with the third character. The second character is a /Q/ character to confirm that the link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 93. The four multiframes include the following:

- Multiframe 1. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 2. Begins with an /R/ character followed by a /Q/ (/K28.4/) character, followed by link configuration parameters over 14 configuration octets (see Table 11) and ends with an /A/ character. Many of the parameter values are of the value - 1 notation.
- Multiframe 3. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 4. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

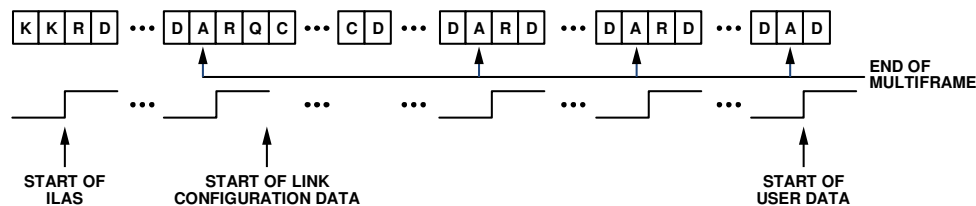


Figure 93. Initial Lane Alignment Sequence

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### User Data and Error Detection

After the initial lane alignment sequence is complete, the user data is sent. Normally, within a frame, all characters are considered user data. However, to monitor the frame clock and multiframe clock synchronization, there is a mechanism for replacing characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default, but it can be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/, and any 0x7C character at the end of a multiframe is replaced with an /A/. The JESD204B receiver (Rx) checks for /F/ and /A/ characters in the received data stream and verifies that they only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic realignment or asserting the SYNCINB± signal for more than four frames to initiate a resynchronization. For unscrambled data, if the final character of two subsequent frames is equal, the second character is replaced with an /F/ if it is at the end of a frame, and an /A/ if it is at the end of a multiframe.

Insertion of alignment characters can be modified using SPI. The frame alignment character insertion (FACI) is enabled by default. More information on the link controls is available in the Memory Map section, Register 0x571.

### 8B/10B Encoder

The 8B/10B encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 11. The 8B/10B encoding ensures that the signal is dc balanced by using the same number of ones and zeros across multiple symbols.

The 8B/10B interface has options that can be controlled via the SPI. These operations include bypass and invert. These options are intended to be troubleshooting tools for the verification of the digital front end (DFE). Refer to the Memory Map section, Register 0x572[2:1] for information on configuring the 8B/10B encoder.

**Table 11. AD9234 Control Characters Used in JESD204B**

| Abbreviation | Control Symbol | 8-Bit Value | 10-Bit Value, RD <sup>1</sup> = -1 | 10-Bit Value, RD <sup>1</sup> = +1 | Description                      |
|--------------|----------------|-------------|------------------------------------|------------------------------------|----------------------------------|
| /R/          | /K28.0/        | 000 11100   | 001111 0100                        | 110000 1011                        | Start of multiframe              |
| /A/          | /K28.3/        | 011 11100   | 001111 0011                        | 110000 1100                        | Lane alignment                   |
| /Q/          | /K28.4/        | 100 11100   | 001111 0010                        | 110000 1101                        | Start of link configuration data |
| /K/          | /K28.5/        | 101 11100   | 001111 1010                        | 110000 0101                        | Group synchronization            |
| /F/          | /K28.7/        | 111 11100   | 001111 1000                        | 110000 0111                        | Frame alignment                  |

<sup>1</sup> RD means running disparity.



**PHYSICAL LAYER (DRIVER) OUTPUTS**

**Digital Outputs, Timing, and Controls**

The AD9234 physical layer consists of drivers that are defined in the JEDEC Standard JESD204B, July 2011. The differential digital outputs are powered up by default. The drivers use a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver, which results in a nominal 300 mV p-p swing at the receiver (see Figure 94). It is recommended to use ac coupling to connect the AD9234 SERDES outputs to the receiver.

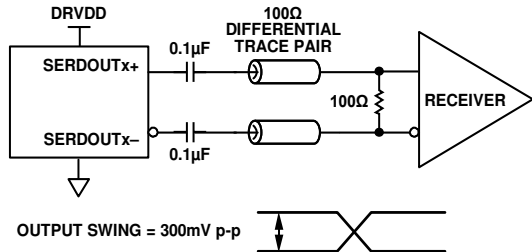


Figure 94. AC-Coupled Digital Output Termination Example

If there is no far-end receiver termination, or if there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and at equal lengths.

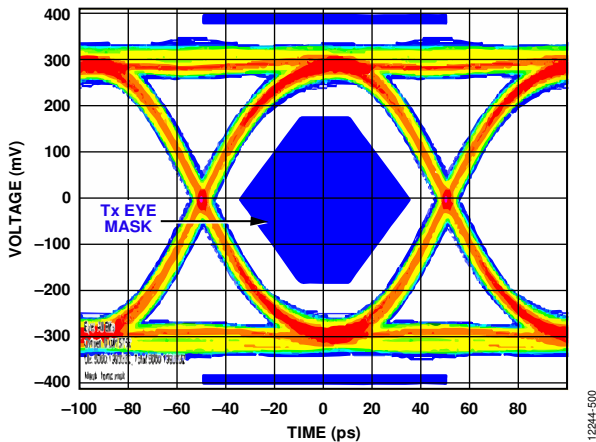


Figure 95. Digital Outputs Data Eye, External 100 Ω Terminations at 10 Gbps

Figure 95 to Figure 100 show examples of the digital output data eye, time interval error (TIE) jitter histogram, and bathtub curve for one AD9234 lane running at 10 Gbps and 6 Gbps, respectively. The format of the output data is twos complement by default. To change the output data format, see the Memory Map section (Register 0x561 in Table 25).

**De-Emphasis**

De-emphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. Use the de-emphasis feature only when the receiver is unable to recover the clock due to excessive insertion loss. Under normal conditions, it is disabled to conserve power. Additionally, enabling and setting too high a de-emphasis value on a short link may cause the receiver eye diagram to fail. Use the de-emphasis setting with caution because it may increase electromagnetic interference (EMI). See the Memory Map section (Register 0x5C1 to Register 0x5C5 in Table 25) for more details.

**Phase-Locked Loop**

The PLL is used to generate the serializer clock, which will operate at the JESD204B lane rate. The JESD204B lane rate Register 0x056E[4:3] must be set to correspond with the lane rate.

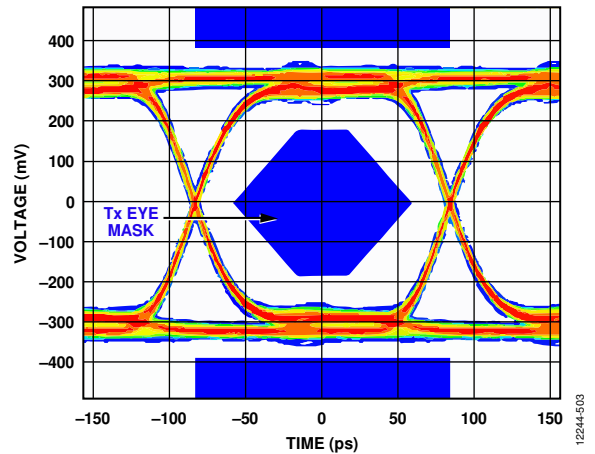


Figure 96. Digital Outputs Data Eye, External 100 Ω Terminations at 6 Gbps

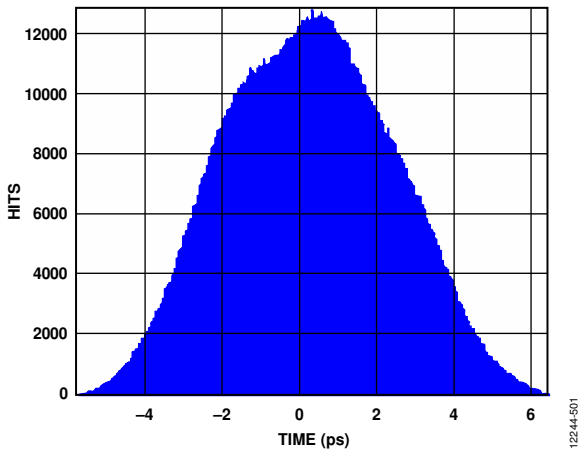


Figure 97. Digital Outputs Histogram, External 100Ω Terminations at 10 Gbps

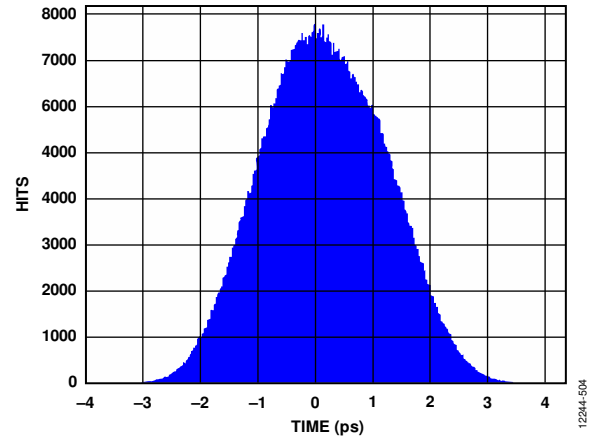


Figure 99. Digital Outputs Histogram, External 100Ω Terminations at 6 Gbps

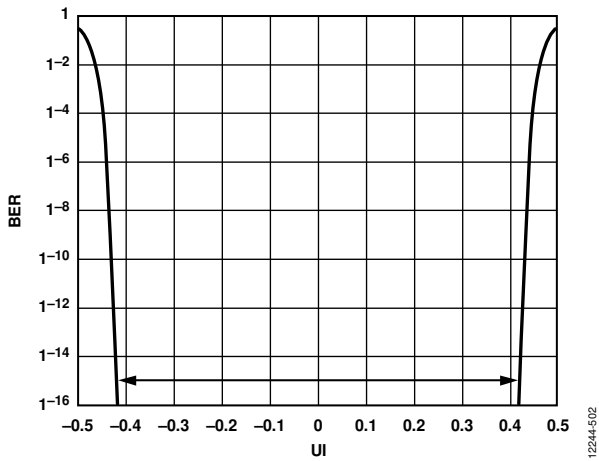


Figure 98. Digital Outputs Bathtub Curve, External 100Ω Terminations at 10 Gbps

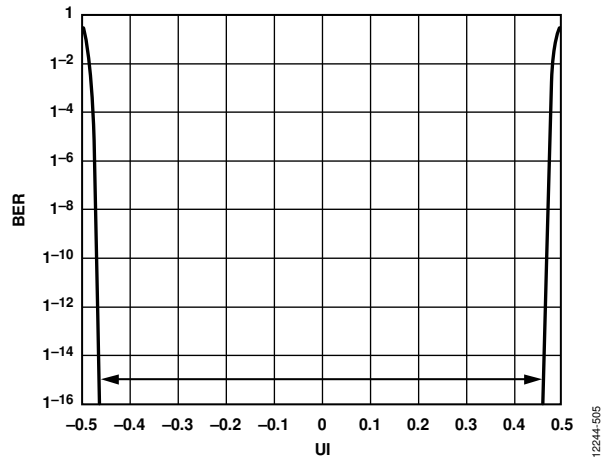


Figure 100. Digital Outputs Bathtub Curve, External 100Ω Terminations at 6 Gbps

**CONFIGURING THE JESD204B LINK**

The AD9234 has one JESD204B link. The device offers an easy way to set up the JESD204B link through the quick configuration register (Register 0x570). The serial outputs (SERDOUT0± to SERDOUT3±) are considered part of one JESD204B link. The basic parameters that determine the link setup are

- Number of lanes per link (L)
- Number of converters per link (M)
- Number of octets per frame (F)

The maximum lane rate allowed by the JESD204B specification is 12.5 Gbps. The lane line rate is related to the JESD204B parameters using the following equation:

$$\text{Lane Line Rate} = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L}$$

where  $f_{OUT} = f_{ADC\_CLOCK} / \text{decimation ratio}$ .

The following steps can be used to configure the output:

1. Power down the link.
2. Select quick configuration options.
3. Configure detailed options.
4. Set output lane mapping (optional).
5. Set additional driver configuration options (optional).
6. Power up the link.

If the lane line rate calculated is less than 6.25 Gbps, select the low line rate option. This is done by programming a value of 0x10 to Register 0x56E.

Table 12 and Table 13 show the JESD204B output configurations supported for both  $N' = 16$  and  $N' = 8$  for a given number of virtual converters. Care must be taken to ensure that the serial line rate for a given configuration is within the supported range of 3.125 Gbps to 12.5 Gbps.

**Table 12. JESD204B Output Configurations for  $N' = 16$**

| No. of Virtual Converters Supported (Same Value as M) | JESD204B Quick Configuration (0x570) | JESD204B Serial Line Rate <sup>1</sup> | JESD204B Transport Layer Settings <sup>2</sup> |   |   |   |    |         |    |        |   |
|---|--------------------------------------|--|--|---|---|---|----|---------|----|--------|---|
|   |                                      |  | L  | M | F | S | HD | N       | N' | CS     | K <sup>3</sup>  |
| 1   | 0x01                                 | $20 \times f_{OUT}$                    | 1  | 1 | 2 | 1 | 0  | 8 to 16 | 16 | 0 to 3 | Only valid K values that are divisible by 4 are supported |
|   | 0x40                                 | $10 \times f_{OUT}$                    | 2  | 1 | 1 | 1 | 1  | 8 to 16 | 16 | 0 to 3 |   |
|   | 0x41                                 | $10 \times f_{OUT}$                    | 2  | 1 | 2 | 2 | 0  | 8 to 16 | 16 | 0 to 3 |   |
|   | 0x80                                 | $5 \times f_{OUT}$                     | 4  | 1 | 1 | 2 | 1  | 8 to 16 | 16 | 0 to 3 |   |
|   | 0x81                                 | $5 \times f_{OUT}$                     | 4  | 1 | 2 | 4 | 0  | 8 to 16 | 16 | 0 to 3 |   |
| 2   | 0x0A                                 | $40 \times f_{OUT}$                    | 1  | 2 | 4 | 1 | 0  | 8 to 16 | 16 | 0 to 3 |   |
|   | 0x49                                 | $20 \times f_{OUT}$                    | 2  | 2 | 2 | 1 | 0  | 8 to 16 | 16 | 0 to 3 |   |
|   | 0x88                                 | $10 \times f_{OUT}$                    | 4  | 2 | 1 | 1 | 1  | 8 to 16 | 16 | 0 to 3 |   |
|   | 0x89                                 | $10 \times f_{OUT}$                    | 4  | 2 | 2 | 2 | 0  | 8 to 16 | 16 | 0 to 3 |   |
| 4   | 0x13                                 | $80 \times f_{OUT}$                    | 1  | 4 | 8 | 1 | 0  | 8 to 16 | 16 | 0 to 3 |   |
|   | 0x52                                 | $40 \times f_{OUT}$                    | 2  | 4 | 4 | 1 | 0  | 8 to 16 | 16 | 0 to 3 |   |
|   | 0x91                                 | $20 \times f_{OUT}$                    | 4  | 4 | 2 | 1 | 0  | 8 to 16 | 16 | 0 to 3 |   |

<sup>1</sup>  $f_{OUT}$  = output sample rate = ADC sample rate/chip decimation ratio. The JESD204B serial line rate must be  $\geq 3.125$  Gbps and  $\leq 12.5$  Gbps; when the serial line rate is  $\leq 12.5$  Gbps and  $\geq 6.25$  Gbps, the low line rate mode must be disabled (set Bit 4 to 0x0 in 0x56E). When the serial line rate is  $< 6.25$  Gbps and  $\geq 3.125$  Gbps, the low line rate mode must be enabled (set Bit 4 to 0x1 in Register 0x56E).

<sup>2</sup> JESD204B transport layer descriptions are as described in the JESD204B Overview section.

<sup>3</sup> For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

Table 13. JESD204B Output Configurations for N' = 8

| No. of Virtual Converters Supported (Same Value as M) | JESD204B Quick Configuration (0x570) | Serial Line Rate <sup>1</sup> | JESD204B Transport Layer Settings <sup>2</sup> |   |   |   |    |        |    |        |  |
|---|--------------------------------------|-------------------------------|--|---|---|---|----|--------|----|--------|--|
|   |                                      |                               | L  | M | F | S | HD | N      | N' | CS     | K <sup>3</sup>   |
| 1   | 0x00                                 | 10 × f <sub>OUT</sub>         | 1  | 1 | 1 | 1 | 0  | 7 to 8 | 8  | 0 to 1 | Only valid K values which are divisible by 4 are supported |
|   | 0x01                                 | 10 × f <sub>OUT</sub>         | 1  | 1 | 2 | 2 | 0  | 7 to 8 | 8  | 0 to 1 |  |
|   | 0x40                                 | 5 × f <sub>OUT</sub>          | 2  | 1 | 1 | 2 | 0  | 7 to 8 | 8  | 0 to 1 |  |
|   | 0x41                                 | 5 × f <sub>OUT</sub>          | 2  | 1 | 2 | 4 | 0  | 7 to 8 | 8  | 0 to 1 |  |
|   | 0x42                                 | 5 × f <sub>OUT</sub>          | 2  | 1 | 4 | 8 | 0  | 7 to 8 | 8  | 0 to 1 |  |
|   | 0x80                                 | 2.5 × f <sub>OUT</sub>        | 4  | 1 | 1 | 4 | 0  | 7 to 8 | 8  | 0 to 1 |  |
| 2   | 0x81                                 | 2.5 × f <sub>OUT</sub>        | 4  | 1 | 2 | 8 | 0  | 7 to 8 | 8  | 0 to 1 |  |
|   | 0x09                                 | 20 × f <sub>OUT</sub>         | 1  | 2 | 2 | 1 | 0  | 7 to 8 | 8  | 0 to 1 |  |
|   | 0x48                                 | 10 × f <sub>OUT</sub>         | 2  | 2 | 1 | 1 | 0  | 7 to 8 | 8  | 0 to 1 |  |
|   | 0x49                                 | 10 × f <sub>OUT</sub>         | 2  | 2 | 2 | 2 | 0  | 7 to 8 | 8  | 0 to 1 |  |
|   | 0x88                                 | 5 × f <sub>OUT</sub>          | 4  | 2 | 1 | 2 | 0  | 7 to 8 | 8  | 0 to 1 |  |
|   | 0x89                                 | 5 × f <sub>OUT</sub>          | 4  | 2 | 2 | 4 | 0  | 7 to 8 | 8  | 0 to 1 |  |
|   | 0x8A                                 | 5 × f <sub>OUT</sub>          | 4  | 2 | 4 | 8 | 0  | 7 to 8 | 8  | 0 to 1 |  |

<sup>1</sup> f<sub>OUT</sub> = output sample rate = ADC sample rate/chip decimation ratio. The JESD204B serial line rate must be ≥3125 Mbps and ≤12,500 Mbps; when the serial line rate is ≤12.5 Gbps and ≥6.25 Gbps, the low line rate mode must be disabled (set Bit 4 to 0x0 in Register 0x56E). When the serial line rate is <6.25 Gbps and ≥3.125 Gbps, the low line rate mode must be enabled (set Bit 4 to 0x1 in Register 0x56E).

<sup>2</sup> JESD204B transport layer descriptions are as described in the JESD204B Overview section.

<sup>3</sup> For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

See the Example 1: Full Bandwidth Mode section, the Example 2: Full Bandwidth Mode at 500 MSPS section, and the Example 3: ADC with DDC Option (Two ADCs Plus Two DDCs) section for examples describing which JESD204B transport layer settings are valid for a given chip mode.

**Example 1: Full Bandwidth Mode at 1 GSPS**

Chip application mode is full bandwidth mode (see Figure 101).

- Two 12-bit converters at 1000 MSPS
- Full bandwidth application layer mode
- No decimation

JESD204B output configuration includes the following:

- Two virtual converters required (see Table 12)
- Output sample rate (f<sub>OUT</sub>) = 1000/1 = 1000 MSPS

JESD204B supported output configurations (see Table 12) include

- N' = 16 bits
- N = 12 bits
- L = 4, M = 2, and F = 1, or L = 4, M = 2, and F = 2 (quick configuration = 0x88 or 0x89)
- CS = 0 to 2
- K = 32
- Output serial line rate = 10 Gbps per lane, low line rate mode disabled

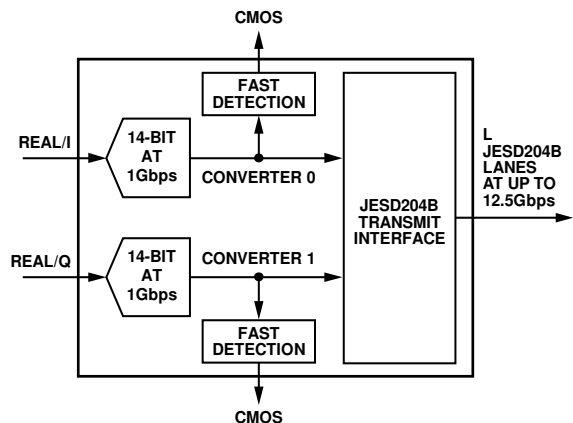


Figure 101. Full Bandwidth Mode

**Example 2: Full Bandwidth Mode at 500 MSPS**

Chip application mode is full bandwidth mode (see Figure 101).

- Two 12-bit converters at 500 MSPS
- Full bandwidth application layer mode
- No decimation

JESD204B output configuration includes the following:

- Two virtual converters required (see Table 12)
- Output sample rate (f<sub>OUT</sub>) = 500/1 = 500 MSPS

JESD204B supported output configurations (see Table 12) include

- $N' = 16$  bits
- $N = 12$  bits
- $L = 4, M = 2,$  and  $F = 1,$  or  $L = 2, M = 2,$  and  $F = 2$  (quick configuration = 0x88 or 0x49)
- $CS = 0$  to 2
- $K = 32$
- Output serial line rate
  - 5 Gbps per lane for L.M.F = 4.2.1, low line rate mode enabled (0x56E = 0x00)
  - 10 Gbps per lane for L.M.F = 2.2.2, low line rate mode disabled (0x56E = 0x00)

**Example 3: ADC with DDC Option (Two ADCs Plus Two DDCs)**

Chip application mode is two-DDC mode. (see Figure 102).

- Two 12-bit converters at 1 MSPS
- Two DDC application layer mode with complex outputs (I/Q)
- Chip decimation ratio = 2
- DDC decimation ratio = 2 (see Table 25)

JESD204B output configuration includes the following:

- Virtual converters required = 4 (see Table 12)
- Output sample rate ( $f_{OUT}$ ) = 1000/2 = 500 MSPS

JESD204B supported output configurations include (see Table 12)

- $N' = 16$  bits
- $N = 12$  bits
- $L = 4, M = 4,$  and  $F = 2$  (quick configuration = 0x91)
- $CS = 0$  to 1
- $K = 32$
- Output serial line rate = 10 Gbps per lane ( $L = 4$ )
- Low line rate mode is disabled (0x56E = 0x00).

Example 2 shows the flexibility in the digital and lane configurations for the AD9234. The sample rate is 1 GSPS, but the outputs are all combined in either one or two lanes, depending on the I/O speed capability of the receiving device.

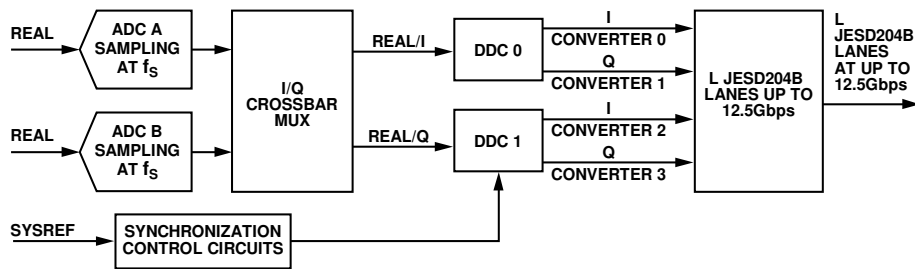


Figure 102. Two-ADC Plus Two DDC Mode

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## DETERMINISTIC LATENCY

Both ends of the JESD204B link contain various clock domains distributed throughout the transmit and receive systems. Data traversing from one clock domain to another clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to nonrepeatable latencies across the JESD204B link from one power cycle or link reset to the next. The JESD204B specification addresses deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

The AD9234 supports JESD204B Subclass 0 and Subclass 1 operation. Register 0x0590, Bit 5 sets the subclass mode for the AD9234; the default mode is the Subclass 1 operating mode (Register 0x590, Bit 5 = 1). If deterministic latency is not a system requirement, Subclass 0 operation is recommended and the SYSREF± signal may not be required. Even in Subclass 0 mode, the SYSREF± signal can be required in an application where multiple AD9234 devices must be synchronized with each other (see the Timestamp Mode section).

### SUBCLASS 0 OPERATION

If there is no requirement for multichip synchronization while operating in Subclass 0 mode (Register 0x590, Bit 5 = 0), the SYSREF± input can be left disconnected. In this mode, the relationship of the JESD204B clocks between the JESD204B transmitter and receiver are arbitrary but does not affect the ability of the receiver to capture and align the lanes within the link.

### SUBCLASS 1 OPERATION

The JESD204B protocol organizes data samples into octets, frames, and multiframe as described in the Transport Layer Sample Test Mode section. The LMFC is synchronous with the starts of these multiframe. In Subclass 1 operation, the SYSREF± signal synchronizes the LMFCs for an individual link or across multiple links (within the AD9234, SYSREF± also synchronizes the internal sample dividers), as shown in Figure 103.

The JESD204B receiver uses the multiframe boundaries and buffering to achieve consistent latency across lanes (or even multiple devices), and also to achieve a fixed latency between power cycles and link reset conditions.

### Deterministic Latency Requirements

Several key factors are required for achieving deterministic latency in a JESD204B Subclass 1 system.

- SYSREF± signal distribution skew within the system must be less than the desired uncertainty for the system.
- SYSREF± setup and hold time requirements must be met for each device in the system.
- The total latency variation across all lanes, links, and devices must be  $\leq 1$  LMFC period (see Figure 103). This includes both variable delays and the variation in fixed delays from lane to lane, link to link and device to device in the system.

### Setting Deterministic Latency Registers

The JESD204B receive buffer in the logic device buffers data starting on the LMFC boundary. If the total link latency in the system is near an integer multiple of the LMFC period, it is possible that from one power cycle to the next the data arrival time at the receive buffer can straddle an LMFC boundary. To ensure deterministic latency in this case, perform a phase adjustment of the LMFC at either the transmitter or receiver. Typically, adjustments to accommodate the receive buffer are made to the LMFC of the receiver. In the AD9234, this adjustment can be made using the LMFC offset bits (Register 0x578, Bits[4:0]). These bits delay the LMFC in frame clock increments, depending on the F parameter, which is the number of octets per lane per frame. When  $F = 1$ , every fourth setting (0, 4, 8, ..., for example) results in a one frame clock shift. When  $F = 2$ , every other setting (0, 2, 4, ..., for example) results in a one frame clock shift. For all other values of F, each setting results in a one frame clock shift.

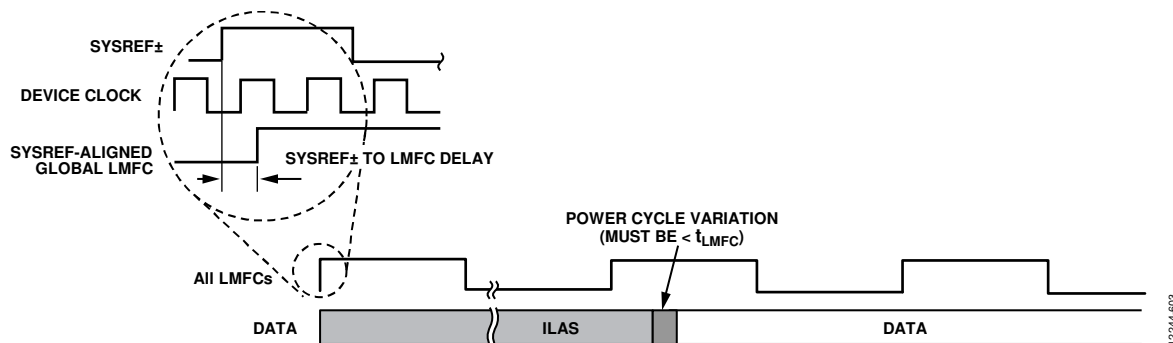


Figure 103. SYSREF± and LMFC

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Figure 104 shows that, in the case where the link latency is near an LMFC boundary, the local LMFC of the AD9234 can be delayed to delay the data arrival time at the receiver. Figure 105 shows how the LMFC of the receiver is delayed to accommodate the receive buffer timing. Refer to the applicable ASIC or FPGA JESD204B receiver user guide for details on accommodating the receiver buffer timing. If the total latency in the system is not near an integer multiple of the LMFC period, or if the appropriate adjustments are not applied to the LMFC phase at the clock source, it is still possible to have variable latency from one power cycle to the next. In this case, check if the setup and hold time requirements for the SYSREF± signal are being met. Perform this check by reading the SYSREF± setup and hold

monitor register (Register 0x128). This function is described in the SYSREF± Setup/Hold Window Monitor section.

If reading Register 0x128 indicates a timing problem, there are adjustments that can be made in the AD9234. Changing the SYSREF± level used for alignment is possible using the SYSREF± transition select bit (Register 0x120, Bit 4). Also, changing which edge of the clock captures SYSREF± can be performed using the clock edge select bit (Register 0x120, Bit 3). Both of these options are described in the SYSREF± Control Features section. If neither of these measures help achieve an acceptable setup and hold time, adjusting the phase of SYSREF± and/or the device clock (CLK±) may be required.

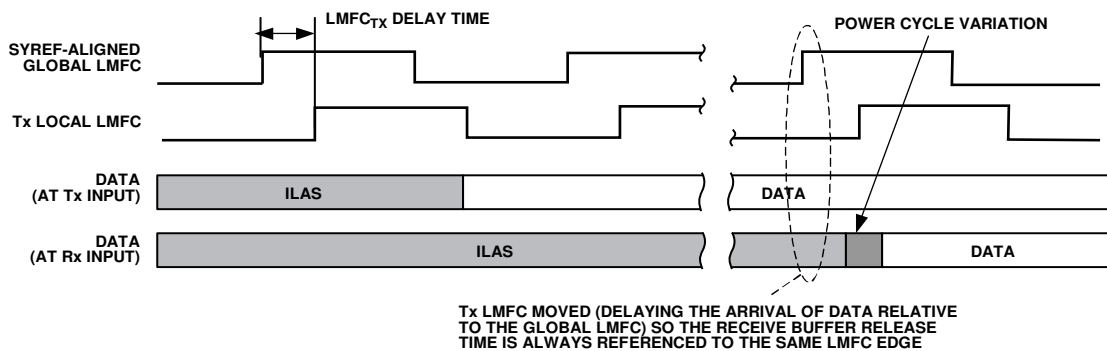


Figure 104. Adjusting the JESD204B Tx LMFC in the AD9234

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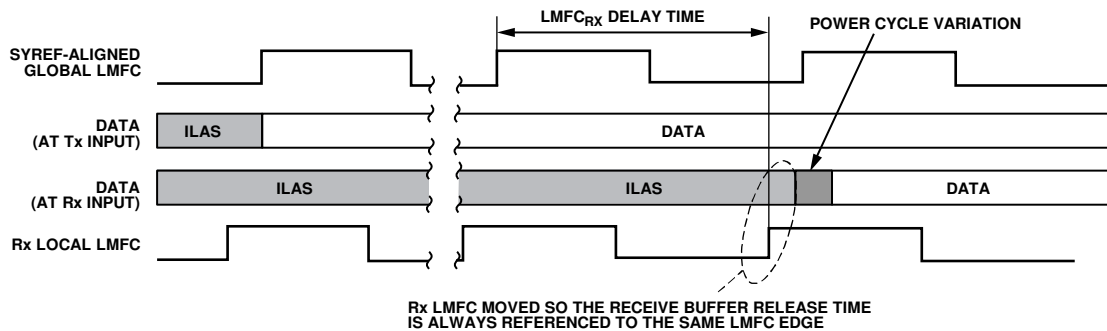


Figure 105. Adjusting the JESD204B Rx LMFC in the Logic Device

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## MULTICHIP SYNCHRONIZATION

The flowchart shown in Figure 107 describes the internal mechanism for multichip synchronization in the AD9234. There are two methods by which multichip synchronization can take place, as determined by the chip synchronization mode bit (Register 0x1FF, Bit 0). Both methods involve different SYSREF± signal applications.

### NORMAL MODE

The default state of the chip synchronization mode bit is 0, which configures the AD9234 for normal chip synchronization. The JESD204B standard specifies the use of SYSREF± to provide deterministic latency within a single link. This same concept, when applied to a system with multiple converters and logic devices, can also provide multichip synchronization. In Figure 107, this is referred to as normal mode. Following the process outlined in Figure 107 ensures the AD9234 is configured appropriately. Consult the respective ASIC or FPGA user intellectual property (IP) guide to ensure the JESD204B receivers are configured appropriately.

### TIMESTAMP MODE

For all AD9234 full bandwidth operating modes, the SYSREF input can also timestamp samples, which is another method in which multiple channels and multiple devices can achieve synchronization. This feature is especially effective when synchronizing multiple devices to one or more logic devices. The logic devices buffer the data streams, identify the time stamped samples, and align them.

When the chip synchronization mode bit (0x1FF, Bit 0) is set to 1, the timestamp method synchronizes multiple channels and/or devices. In timestamp mode, the clocks do not reset, but the coinciding sample is time stamped using the JESD204B control bits of that sample. To operate in timestamp mode, these additional settings are necessary:

- Continuous or N shot SYSREF± enabled (0x120[2:1] = 1 or 2)
- At least one control bit must be enabled (CS > 0, Register 0x58F, Bits[7:6] = 1, 2, or 3)
- Set the function for one of the control bits to SYSREF
  - Register 0x559, Bits[2:0] = 5 if using Control Bit 0
  - Register 0x559, Bits[6:4] = 5 if using Control Bit 1
  - Register 0x55A, Bits[2:0] = 5 if using Control Bit 2

Control bits must be enabled MSB first. In other words, if only using one control bit (CS = 1), Control Bit 2 must be enabled. If two control bits are used, Control Bits[2:1] must be enabled. Figure 106 shows how the input sample coincident with SYSREF± is time stamped, and ultimately, the output of the ADC. In this example, there are two control bits and Control Bit 1 is the bit indicating which sample was coincident with the SYSREF± rising edge. Note that the pipeline latencies for each channel are identical. If so desired, the SYSREF± timestamp delay register (Register 0x123) can be used to adjust the timing of which sample is time stamped.

Note that time stamping is not supported by any AD9234 operating modes that use decimation.

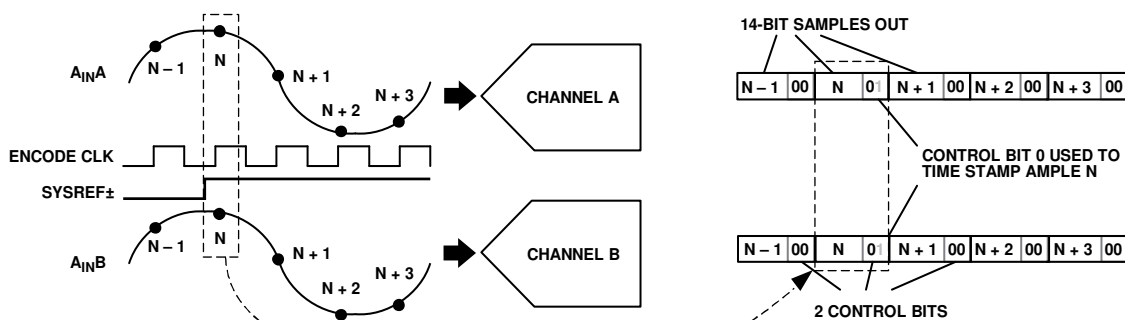


Figure 106. AD9234 Timestamping—CS = 2 (Register 0x58F, Bits[7:6] = 2), Control Bit 1 is SYSREF± (Register 0x559, Bits[6:4] = 5)

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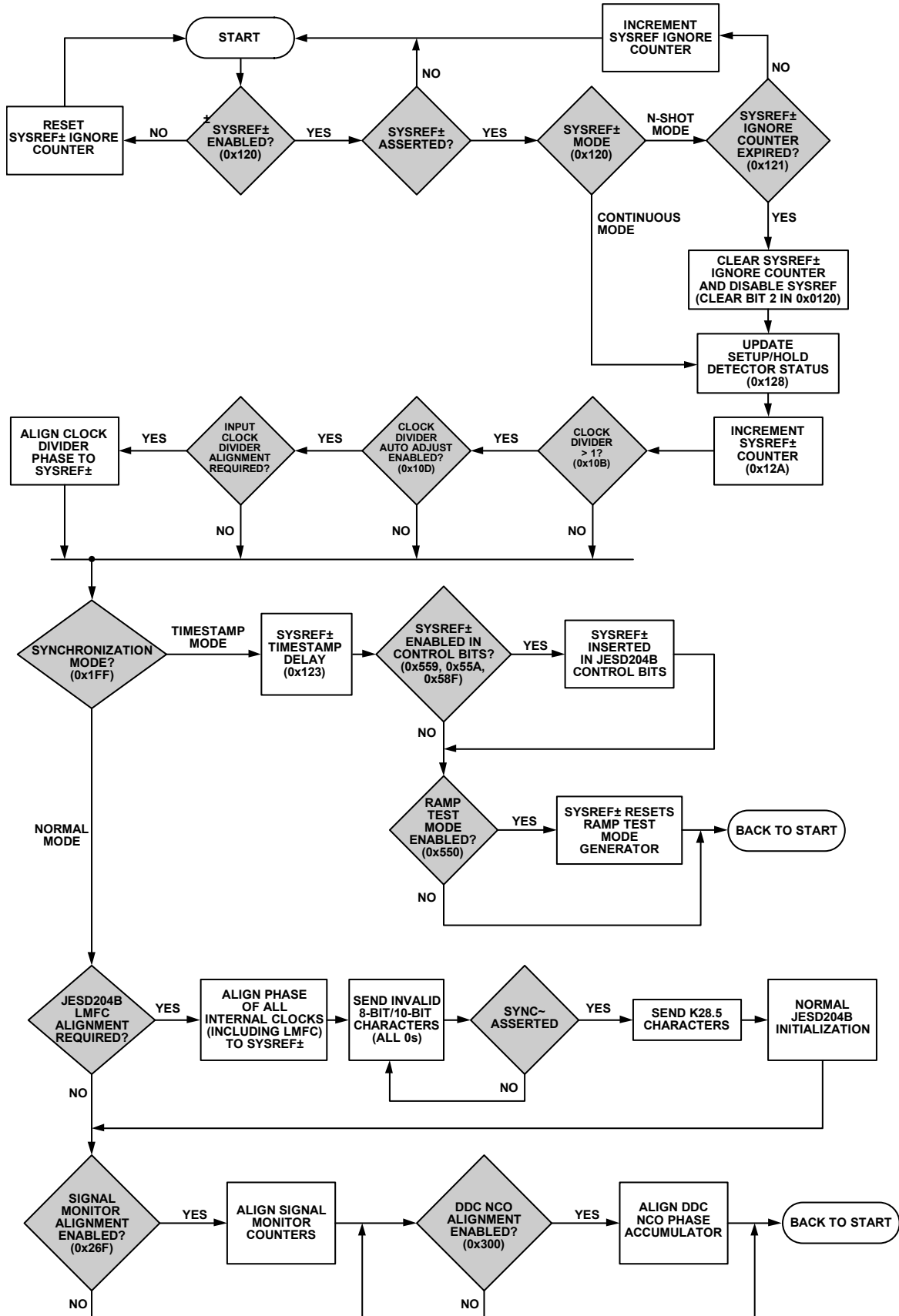


Figure 107. SYSREF± Capture Scenarios and Multichip Synchronization

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## SYSREF± INPUT

The SYSREF± input signal is used as a high accuracy system reference for deterministic latency and multichip synchronization. The AD9234 accepts a single shot or periodic input signal. The SYSREF± mode select bits (Register 0x120, Bits[2:1]) select the input signal type and also arm the SYSREF± state machine when set. If in single (or N) shot mode (Register 0x120, Bits[2:1] = 2), the SYSREF± mode select bit self clears after detecting the appropriate SYSREF± transition. The pulse width must have a minimum width of two CLK± periods. If the clock divider (Register 0x10B, Bits[2:0]) is set to a value other than divide by 1, then multiply this minimum pulse width requirement by the divide ratio (for example, if set to divide by 8, the minimum pulse width is 16 CLK± cycles). When using a continuous SYSREF± signal (Register 0x120, Bits[2:1] = 1), the period of the SYSREF± signal must be an integer multiple of the LMFC. Derive the LMFC using the following formula:

$$LMFC = ADC\ Clock/S \times K$$

where:

S is the JESD204B parameter for number of samples per converter.

K is JESD204B parameter for number of frames per multiframe.

The input clock divider, DDCs, signal monitor block, and JESD204B link are all synchronized using the SYSREF± input when in normal synchronization mode (Register 0x1FF, Bits[1:0] = 0). The SYSREF± input can also time stamp an ADC sample to provide a mechanism for synchronizing multiple AD9234 devices in a system. For the highest level of timing accuracy, SYSREF± must meet the setup and hold requirements relative to the CLK± input. There are several features in the AD9234 to ensure these requirements are met (see the SYSREF± Control Features section).

### SYSREF± Control Features

SYSREF± and the input clock (CLK±) are part of a source synchronous timing interface that requires setup and hold timing requirements of 117 ps and -96 ps, relative to the input clock (see Figure 108).

The AD9234 has several features to meet these requirements. First, the SYSREF± sample event can be defined as either a synchronous low to high transition or synchronous high to low transition. Second, the AD9234 allows the SYSREF± signal to be sampled using either the rising edge or falling edge of the input clock. Figure 108, Figure 109, Figure 110, and Figure 111 show all four possible combinations.

The third SYSREF± related feature available is the ability to ignore a programmable number (up to 16) of SYSREF± events. The SYSREF± ignore feature is enabled by setting the SYSREF± mode

register (Register 0x120, Bits[2:1]) to 10, which is labeled as N shot mode. The AD9234 can ignore N SYSREF± events, which can handle periodic SYSREF± signals that require time to settle after startup. Ignoring SYSREF± until the clocks in the system settle avoids an inaccurate SYSREF± trigger. Figure 112 shows an example of the SYSREF± ignore feature when ignoring three SYSREF± events.

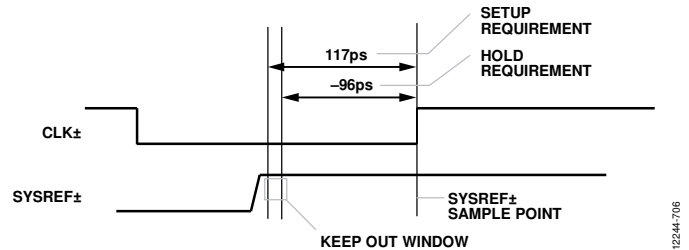


Figure 108. SYSREF± Setup and Hold Time Requirements; SYSREF± Low to High Transition Using the Rising Edge Clock (Default)

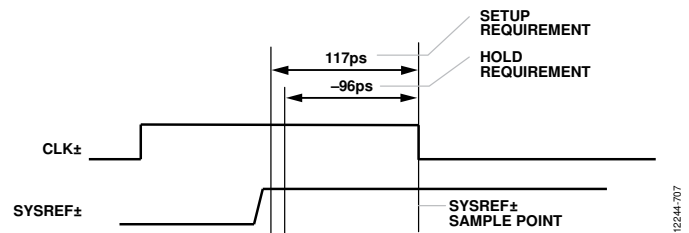


Figure 109. SYSREF± Low to High Transition Using Falling Edge Clock Capture (Register 0x120, Bit 4 = 0 and Register 0x120, Bit 3 = 1)

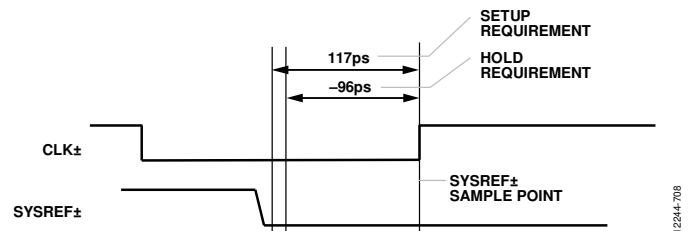


Figure 110. SYSREF± High to Low Transition Using Rising Edge Clock Capture (Register 0x120, Bit 4 = 1 and Register 0x120, Bit 3 = 0)

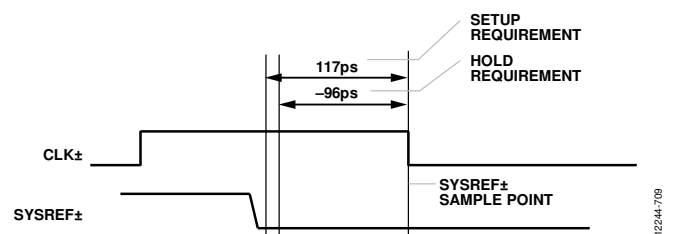


Figure 111. SYSREF± High to Low Transition Using Falling Edge Clock Capture (Register 0x120, Bit 4 = 1 and Register 0x120, Bit 3 = 1)

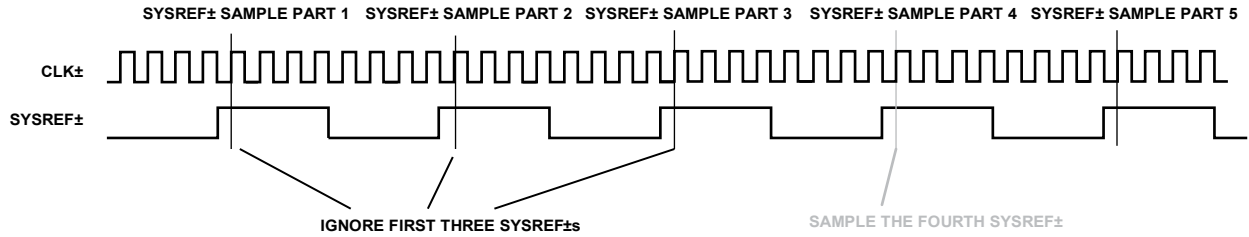


Figure 112. SYSREF± Ignore Example; SYSREF± Ignore Count Bits (Register 0x121, Bits[3:0]) = 3

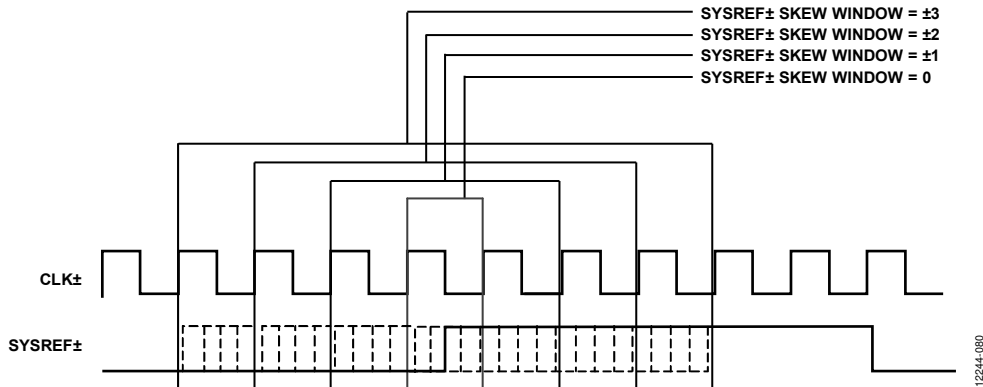


Figure 113. SYSREF± Skew Window

When in continuous SYSREF± mode (Register 0x120, Bits[2:1] = 1), the AD9234 monitors the placement of the SYSREF± leading edge compared to the internal LMFC. If the SYSREF± edge is captured with a clock edge other than the one that is aligned with LMFC, the AD9234 initiates a resynchronization of the link.

Because the input clock rates for the AD9234 can range up to 4 GHz, the AD9234 provides another SYSREF± related feature that makes it possible to accommodate periodic SYSREF± signals where cycle accurate capture is not feasible or is not required. For these scenarios, the AD9234 has a programmable SYSREF± skew window that allows the internal dividers to remain undisturbed, unless SYSREF± occurs outside the skew window. The resolution of the SYSREF± skew window is set in sample clock cycles.

If the SYSREF± negative skew window is 1 and the positive skew window is 1, the total skew window is ±1 sample clock cycles, meaning that, as long as SYSREF± is captured within ±1 sample clock cycle of the clock that is aligned with the LMFC, the link continues to operate normally. If the SYSREF± has jitter, which can cause a misalignment between SYSREF± and the LMFC, the system continues to run without a resynchronization, while still allowing the device to monitor for larger errors not caused by jitter. For the AD9234, the positive and negative skew window is controlled by the SYSREF± window negative bits (Register 0x122, Bits[3:2]) and the SYSREF± window positive bits (Register 0x122, Bits[1:0]). Figure 113 shows the location of the skew window settings relative to Phase 0 of the internal dividers. Negative skew is defined as occurring before the internal dividers reach Phase 0 and positive skew is defined after the internal dividers reach Phase 0.

**SYSREF± SETUP/HOLD WINDOW MONITOR**

To ensure a valid SYSREF± signal capture, the AD9234 has a SYSREF± setup and hold window monitor. This feature allows the system designer to determine the location of the SYSREF± signals relative to the CLK± signals by reading back the amount of setup and hold margin on the interface through the memory map. Figure 114 and Figure 115 show the setup and hold status values for different phases of SYSREF±. The setup detector

returns the status of the SYSREF± signal before the CLK± edge, and the hold detector returns the status of the SYSREF signal after the CLK± edge. Register 0x128 stores the status of SYSREF± and lets the user know if the SYSREF± signal is captured by the ADC.

Table 14 describes the contents of Register 0x128 and how to interpret them.

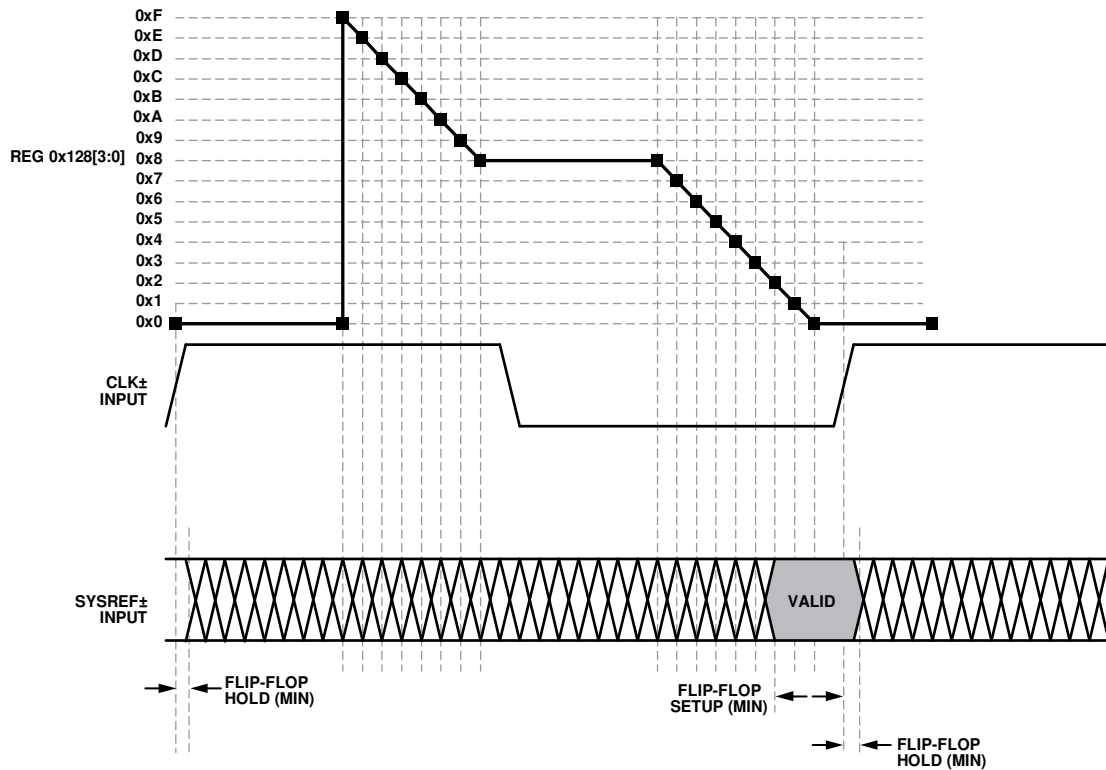


Figure 114. SYSREF± Setup Detector

12244-113

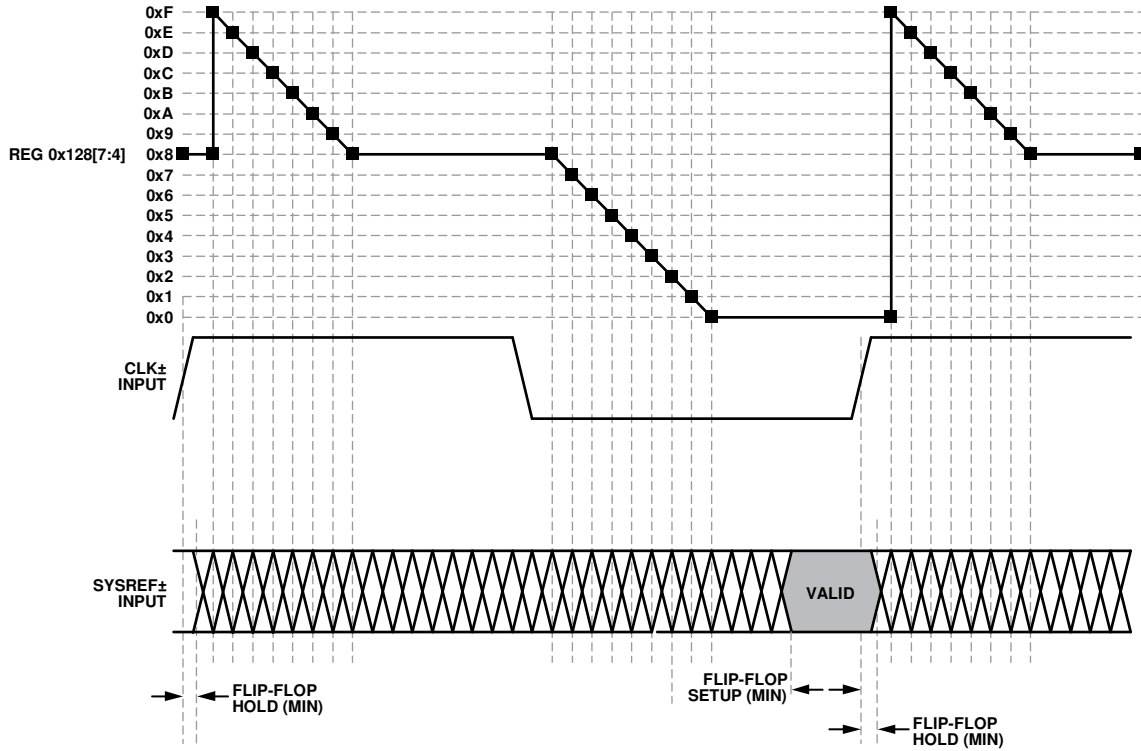


Figure 115. SYSREF± Hold Detector

12244-114

Table 14. SYSREF± Setup/Hold Monitor, Register 0x128

| Register 0x128, Bits[7:4], Hold Status | Register 0x128, Bits[3:0], Setup Status | Description  |
|--|---|--|
| 0x0                                    | 0x0 to 0x7                              | Possible setup error. The smaller this number, the smaller the setup margin. |
| 0x0 to 0x8                             | 0x8                                     | No setup or hold error (best hold margin).                                   |
| 0x8                                    | 0x9 to 0xF                              | No setup or hold error (best setup and hold margin).                         |
| 0x8                                    | 0x0                                     | No setup or hold error (best setup margin).                                  |
| 0x9 to 0xF                             | 0x0                                     | Possible hold error. The larger this number, the smaller the hold margin.    |
| 0x0                                    | 0x0                                     | Possible setup or hold error.  |

## LATENCY

### END TO END TOTAL LATENCY

Total latency in the AD9234 is dependent on the various digital signal processing (DSP) and JESD204B configuration modes. Latency is fixed at 26 encode clocks through the ADC itself; however, the latency through the DSP and JESD204B blocks can vary greatly depending on the configuration. Therefore, total latency must be calculated based on the DSP options selected and the JESD204B configuration.

Table 15 shows the combined latency through the ADC and DSP blocks (including data formatting) for the different application modes supported by the AD9234. Table 16 shows the latency through the JESD204B block for each JESD204B configuration and the various decimation modes supported for those modes. For Table 15 and Table 16, latency is in units of the number of encode clocks. Latency through the JESD204B clock can also be affected by the decimation ratio in some JESD204B configurations. Table 17 shows the latency for these modes for each of the possible decimation ratios.

Table 15. Latency Through the ADC and DSP Blocks

| ADC Application Mode                 | Latency (Number of Encode Clocks), ADC + DSP Total |
|--------------------------------------|--|
| Full Bandwidth                       | 29   |
| DDC (HB1), no mixer, complex outputs | 78   |

### EXAMPLE LATENCY CALCULATION

For a configuration where the ADC application mode is full bandwidth, the decimation ratio = 2, L = 4, M = 2, F = 1, and S = 1 (JESD204B mode):

$$\text{Latency} = 29 + 30 = 59 \text{ Encode Clocks}$$

Table 16. Latency Through JESD204B Block—Full Bandwidth Modes

| JESD204B Quick Configuration (Register 0x570) | Decimation Ratio | JESD204B Transport Layer Settings |   |   |   |    |         |    | Latency (Encode Clock) |
|---|------------------|-----------------------------------|---|---|---|----|---------|----|------------------------|
|   |                  | L                                 | M | F | S | HD | N       | N' |                        |
| 0x01  | 1                | 1                                 | 1 | 2 | 1 | 0  | 8 to 16 | 16 | 13                     |
| 0x40  | 1                | 2                                 | 1 | 1 | 1 | 1  | 8 to 16 | 16 | 28                     |
| 0x41  | 1                | 2                                 | 1 | 2 | 2 | 0  | 8 to 16 | 16 | 28                     |
| 0x80  | 1                | 4                                 | 1 | 1 | 2 | 1  | 8 to 16 | 16 | 53                     |
| 0x81  | 1                | 4                                 | 1 | 2 | 4 | 0  | 8 to 16 | 16 | 53                     |
| 0x0A  | 1                | 1                                 | 2 | 4 | 1 | 0  | 8 to 16 | 16 | 7                      |
| 0x49  | 1                | 2                                 | 2 | 2 | 1 | 0  | 8 to 16 | 16 | 13                     |
| 0x88  | 1                | 4                                 | 2 | 1 | 1 | 1  | 8 to 16 | 16 | 28                     |
| 0x89  | 1                | 4                                 | 2 | 2 | 2 | 0  | 8 to 16 | 16 | 28                     |

Table 17. Latency Through JESD204B Block with Decimation

| JESD204B Quick Configuration (Register 0x570) | Decimation Ratio | JESD204B Transport Layer Settings |   |    |   |    |         |    | Latency (Encode CLK) |
|---|------------------|-----------------------------------|---|----|---|----|---------|----|----------------------|
|   |                  | L                                 | M | F  | S | HD | N       | N' |                      |
| 0x88  | 2                | 4                                 | 2 | 1  | 1 | 1  | 8 to 16 | 16 | 30                   |
| 0x89  | 2                | 4                                 | 2 | 2  | 2 | 0  | 8 to 16 | 16 | 30                   |
| 0x13 <sup>1</sup>                             | 2, 4, 8, 16      | 1                                 | 4 | 8  | 1 | 0  | 8 to 16 | 16 | 4                    |
| 0x52 <sup>1</sup>                             | 2, 4, 8, 16      | 2                                 | 4 | 4  | 1 | 0  | 8 to 16 | 16 | 7                    |
| 0x91 <sup>1</sup>                             | 2, 4, 8, 16      | 4                                 | 4 | 2  | 1 | 0  | 8 to 16 | 16 | 13                   |
| 0x1C <sup>1</sup>                             | 4, 8, 16         | 1                                 | 8 | 16 | 1 | 0  | 8 to 16 | 16 | 2                    |
| 0x5B <sup>1</sup>                             | 4, 8, 16         | 2                                 | 8 | 8  | 1 | 0  | 8 to 16 | 16 | 4                    |
| 0x9A <sup>1</sup>                             | 4, 8, 16         | 4                                 | 8 | 4  | 1 | 0  | 8 to 16 | 16 | 7                    |

<sup>1</sup> For these modes, changing decimation does not affect latency.

# TEST MODES

## ADC TEST MODES

The AD9234 has various test options that aid in system level implementation. The AD9234 has ADC test modes that are available in Register 0x550. These test modes are described in Table 18. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back end blocks, and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x550.

These tests can be performed with or without an analog signal (if present, the analog signal is ignored); however, they do require an encode clock.

If the application mode is set to select a DDC mode of operation, the test modes must be enabled for each DDC enabled. The test patterns can be enabled via Bit 2 and Bit 0 of Register 0x327 and Register 0x347 depending on which DDCs are selected. The I data uses the test patterns selected for Channel A, and the Q data uses the test patterns selected for Channel B. For more information, see the [AN-877 Application Note, Interfacing to High Speed ADCs via SPI](#).

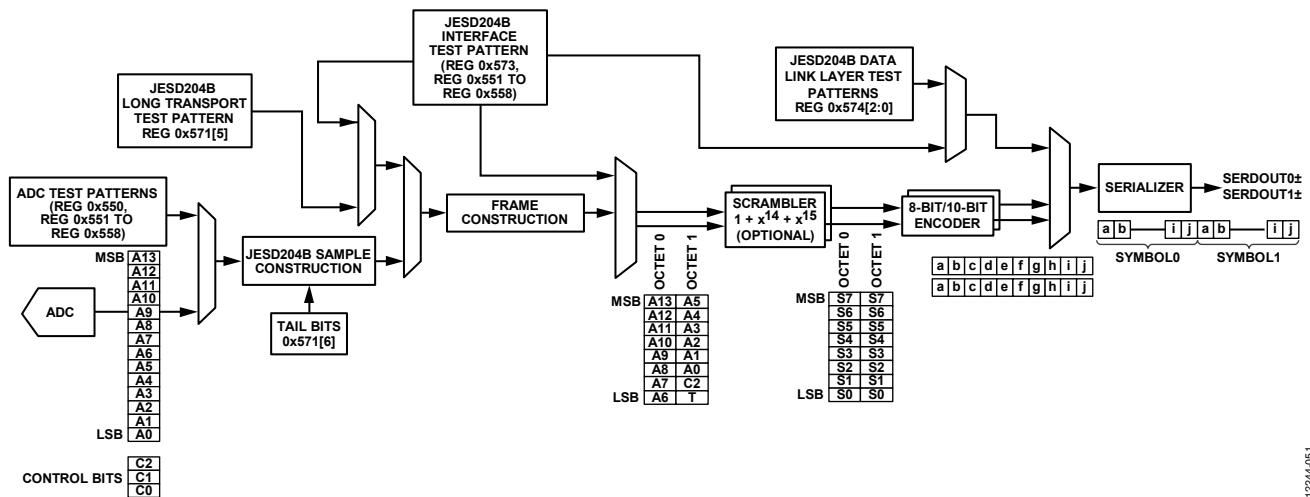


Figure 116. ADC Output Datapath Showing Data Framing

Table 18. ADC Test Modes

| Output Test Mode Bit Sequence | Pattern Name              | Expression                       | Default/Seed Value | Sample (N, N + 1, N + 2, ...)  |
|-------------------------------|---------------------------|----------------------------------|--------------------|--|
| 0000                          | Off (default)             | Not applicable                   | Not applicable     | Not applicable   |
| 0001                          | Midscale short            | 0000 0000 0000                   | Not applicable     | Not applicable   |
| 0010                          | Positive full-scale short | 01 1111 1111 1111                | Not applicable     | Not applicable   |
| 0011                          | Negative full-scale short | 10 0000 0000 0000                | Not applicable     | Not applicable   |
| 0100                          | Checkerboard              | 10 1010 1010 1010                | Not applicable     | 0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555   |
| 0101                          | PN sequence long          | $x^{23} + x^{18} + 1$            | 0x3AFF             | 0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6   |
| 0110                          | PN sequence short         | $x^9 + x^5 + 1$                  | 0x0092             | 0x125B, 0x3C9A, 0x2660, 0x0c65, 0x0697   |
| 0111                          | One-/zero-word toggle     | 11 1111 1111 1111                | Not applicable     | 0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000   |
| 1000                          | User input                | Register 0x551 to Register 0x558 | Not applicable     | User Pattern 1, Bits[15:2], User Pattern 2, Bits[15:2], User Pattern 3, Bits[15:2], User Pattern 4, Bits[15:2], User Pattern 1, Bits[15:2] ... for repeat mode.<br>User Pattern 1, Bits[15:2], User Pattern 2, Bits[15:2], User Pattern 3, Bits[15:2], User Pattern 4, Bits[15:2], 0x0000 ... for single mode. |
| 1111                          | Ramp Output               | $(x) \% 2^{14}$                  | Not applicable     | $(x) \% 2^{14}, (x + 1) \% 2^{14}, (x + 2) \% 2^{14}, (x + 3) \% 2^{14}$   |

## JESD204B BLOCK TEST MODES

In addition to the ADC pipeline test modes, the AD9234 also has flexible test modes in the JESD204B block. These test modes are listed in Register 0x573 and Register 0x574. These test patterns can be injected at various points along the output datapath.

These test injection points are shown in Figure 116. Table 19 describes the various test modes available in the JESD204B block. For the AD9234, a transition from test modes (Register 0x573  $\neq$  0x00) to normal mode (Register 0x573 = 0x00) requires an SPI soft reset, which is done by writing 0x81 to Register 0x000 (self cleared).

### Transport Layer Sample Test Mode

The transport layer samples are implemented in the AD9234 as defined by Section 5.1.6.3 in the JEDEC JESD204B specification. These tests are shown in Register 0x571, Bit 5. The test pattern is equivalent to the raw samples from the ADC.

## Interface Test Modes

The interface test modes are described in Register 0x573, Bits[3:0]. These test modes are also explained in Table 19. The interface tests can be injected at various points along the data. See Figure 91 for more information on the test injection points. Register 0x573, Bits[5:4] show where these tests are injected.

Table 20, Table 21, and Table 22 show examples of some of the test modes when injected at the JESD204B sample input, PHY 10-bit input, and scrambler 8-bit input. UPx in the Table 20, Table 21, and Table 22 represent the user pattern control bits from the memory map.

### Data Link Layer Test Modes

The data link layer test modes are implemented in the AD9234, defined by Section 5.3.3.8.2 in the JEDEC JESD204B specification. These tests are shown in Register 0x574, Bits[2:0]. Test patterns inserted at this point are useful for verifying the functionality of the data link layer. When the data link layer test modes are enabled, disable SYNCINB $\pm$  by writing 0xC0 to Register 0x572.

Table 19. JESD204B Interface Test Modes

| Output Test Mode Bit Sequence | Pattern Name                | Expression                       | Default                                       |
|-------------------------------|-----------------------------|----------------------------------|---|
| 0000                          | Off (default)               | Not applicable                   | Not applicable                                |
| 0001                          | Alternating checker board   | 0x5555, 0xAAAA, 0x5555, ...      | Not applicable                                |
| 0010                          | 1/0 word toggle             | 0x0000, 0xFFFF, 0x0000, ...      | Not applicable                                |
| 0011                          | 31-bit PN sequence          | $x^{31} + x^{28} + 1$            | 0x0003AFFF                                    |
| 0100                          | 23-bit PN sequence          | $x^{23} + x^{18} + 1$            | 0x003AFF                                      |
| 0101                          | 15-bit PN sequence          | $x^{15} + x^{14} + 1$            | 0x03AF  |
| 0110                          | 9-bit PN sequence           | $x^9 + x^5 + 1$                  | 0x092   |
| 0111                          | 7-bit PN sequence           | $x^7 + x^6 + 1$                  | 0x07  |
| 1000                          | Ramp output                 | $(x) \% 2^{16}$                  | Ramp size depends on test injection point     |
| 1110                          | Continuous/repeat user test | Register 0x551 to Register 0x558 | User Pattern 1 to User Pattern 4, then repeat |
| 1111                          | Single user test            | Register 0x551 to Register 0x558 | User Pattern 1 to User Pattern 4, then zeros  |

Table 20. JESD204B Sample Input for M = 2, S = 2, N' = 16 (Register 0x573, Bits[5:4] = 0)

| Frame No. | Converter No. | Sample No. | Alternating Checkerboard | 1/0 Word Toggle | Ramp                | PN9    | PN23   | User Repeat | User Single |
|-----------|---------------|------------|--------------------------|-----------------|---------------------|--------|--------|-------------|-------------|
| 0         | 0             | 0          | 0x5555                   | 0x0000          | $(x) \% 2^{16}$     | 0x496F | 0xFF5C | UP1[15:0]   | UP1[15:0]   |
| 0         | 0             | 1          | 0x5555                   | 0x0000          | $(x) \% 2^{16}$     | 0x496F | 0xFF5C | UP1[15:0]   | UP1[15:0]   |
| 0         | 1             | 0          | 0x5555                   | 0x0000          | $(x) \% 2^{16}$     | 0x496F | 0xFF5C | UP1[15:0]   | UP1[15:0]   |
| 0         | 1             | 1          | 0x5555                   | 0x0000          | $(x) \% 2^{16}$     | 0x496F | 0xFF5C | UP1[15:0]   | UP1[15:0]   |
| 1         | 0             | 0          | 0xAAAA                   | 0xFFFF          | $(x + 1) \% 2^{16}$ | 0xC9A9 | 0x0029 | UP2[15:0]   | UP2[15:0]   |
| 1         | 0             | 1          | 0xAAAA                   | 0xFFFF          | $(x + 1) \% 2^{16}$ | 0xC9A9 | 0x0029 | UP2[15:0]   | UP2[15:0]   |
| 1         | 1             | 0          | 0xAAAA                   | 0xFFFF          | $(x + 1) \% 2^{16}$ | 0xC9A9 | 0x0029 | UP2[15:0]   | UP2[15:0]   |
| 1         | 1             | 1          | 0xAAAA                   | 0xFFFF          | $(x + 1) \% 2^{16}$ | 0xC9A9 | 0x0029 | UP2[15:0]   | UP2[15:0]   |
| 2         | 0             | 0          | 0x5555                   | 0x0000          | $(x + 2) \% 2^{16}$ | 0x980C | 0xB80A | UP3[15:0]   | UP3[15:0]   |
| 2         | 0             | 1          | 0x5555                   | 0x0000          | $(x + 2) \% 2^{16}$ | 0x980C | 0xB80A | UP3[15:0]   | UP3[15:0]   |
| 2         | 1             | 0          | 0x5555                   | 0x0000          | $(x + 2) \% 2^{16}$ | 0x980C | 0xB80A | UP3[15:0]   | UP3[15:0]   |
| 2         | 1             | 1          | 0x5555                   | 0x0000          | $(x + 2) \% 2^{16}$ | 0x980C | 0xB80A | UP3[15:0]   | UP3[15:0]   |
| 3         | 0             | 0          | 0xAAAA                   | 0xFFFF          | $(x + 3) \% 2^{16}$ | 0x651A | 0x3D72 | UP4[15:0]   | UP4[15:0]   |
| 3         | 0             | 1          | 0xAAAA                   | 0xFFFF          | $(x + 3) \% 2^{16}$ | 0x651A | 0x3D72 | UP4[15:0]   | UP4[15:0]   |
| 3         | 1             | 0          | 0xAAAA                   | 0xFFFF          | $(x + 3) \% 2^{16}$ | 0x651A | 0x3D72 | UP4[15:0]   | UP4[15:0]   |
| 3         | 1             | 1          | 0xAAAA                   | 0xFFFF          | $(x + 3) \% 2^{16}$ | 0x651A | 0x3D72 | UP4[15:0]   | UP4[15:0]   |



| Frame No. | Converter No. | Sample No. | Alternating Checkerboard | 1/0 Word Toggle | Ramp                | PN9    | PN23   | User Repeat | User Single |
|-----------|---------------|------------|--------------------------|-----------------|---------------------|--------|--------|-------------|-------------|
| 4         | 0             | 0          | 0x5555                   | 0x0000          | $(x + 4) \% 2^{16}$ | 0x5FD1 | 0x9B26 | UP1[15:0]   | 0x0000      |
| 4         | 0             | 1          | 0x5555                   | 0x0000          | $(x + 4) \% 2^{16}$ | 0x5FD1 | 0x9B26 | UP1[15:0]   | 0x0000      |
| 4         | 1             | 0          | 0x5555                   | 0x0000          | $(x + 4) \% 2^{16}$ | 0x5FD1 | 0x9B26 | UP1[15:0]   | 0x0000      |
| 4         | 1             | 1          | 0x5555                   | 0x0000          | $(x + 4) \% 2^{16}$ | 0x5FD1 | 0x9B26 | UP1[15:0]   | 0x0000      |

Table 21. Physical Layer 10-Bit Input (Register 0x573, Bits[5:4] = 1)

| 10-Bit Symbol No. | Alternating Checkerboard | 1/0 Word Toggle | Ramp                 | PN9   | PN23  | User Repeat | User Single |
|-------------------|--------------------------|-----------------|----------------------|-------|-------|-------------|-------------|
| 0                 | 0x155                    | 0x000           | $(x) \% 2^{10}$      | 0x125 | 0x3FD | UP1[15:6]   | UP1[15:6]   |
| 1                 | 0x2AA                    | 0x3FF           | $(x + 1) \% 2^{10}$  | 0x2FC | 0x1C0 | UP2[15:6]   | UP2[15:6]   |
| 2                 | 0x155                    | 0x000           | $(x + 2) \% 2^{10}$  | 0x26A | 0x00A | UP3[15:6]   | UP3[15:6]   |
| 3                 | 0x2AA                    | 0x3FF           | $(x + 3) \% 2^{10}$  | 0x198 | 0x1B8 | UP4[15:6]   | UP4[15:6]   |
| 4                 | 0x155                    | 0x000           | $(x + 4) \% 2^{10}$  | 0x031 | 0x028 | UP1[15:6]   | 0x000       |
| 5                 | 0x2AA                    | 0x3FF           | $(x + 5) \% 2^{10}$  | 0x251 | 0x3D7 | UP2[15:6]   | 0x000       |
| 6                 | 0x155                    | 0x000           | $(x + 6) \% 2^{10}$  | 0x297 | 0x0A6 | UP3[15:6]   | 0x000       |
| 7                 | 0x2AA                    | 0x3FF           | $(x + 7) \% 2^{10}$  | 0x3D1 | 0x326 | UP4[15:6]   | 0x000       |
| 8                 | 0x155                    | 0x000           | $(x + 8) \% 2^{10}$  | 0x18E | 0x10F | UP1[15:6]   | 0x000       |
| 9                 | 0x2AA                    | 0x3FF           | $(x + 9) \% 2^{10}$  | 0x2CB | 0x3FD | UP2[15:6]   | 0x000       |
| 10                | 0x155                    | 0x000           | $(x + 10) \% 2^{10}$ | 0x0F1 | 0x31E | UP3[15:6]   | 0x000       |
| 11                | 0x2AA                    | 0x3FF           | $(x + 11) \% 2^{10}$ | 0x3DD | 0x008 | UP4[15:6]   | 0x000       |

Table 22. Scrambler 8-Bit Input (Register 0x573, Bits[5:4] = 0)

| 8-Bit Octet No. | Alternating Checkerboard | 1/0 Word Toggle | Ramp              | PN9  | PN23 | User Repeat | User Single |
|-----------------|--------------------------|-----------------|-------------------|------|------|-------------|-------------|
| 0               | 0x55                     | 0x00            | $(x) \% 2^8$      | 0x49 | 0xFF | UP1[15:9]   | UP1[15:9]   |
| 1               | 0xAA                     | 0xFF            | $(x + 1) \% 2^8$  | 0x6F | 0x5C | UP2[15:9]   | UP2[15:9]   |
| 2               | 0x55                     | 0x00            | $(x + 2) \% 2^8$  | 0xC9 | 0x00 | UP3[15:9]   | UP3[15:9]   |
| 3               | 0xAA                     | 0xFF            | $(x + 3) \% 2^8$  | 0xA9 | 0x29 | UP4[15:9]   | UP4[15:9]   |
| 4               | 0x55                     | 0x00            | $(x + 4) \% 2^8$  | 0x98 | 0xB8 | UP1[15:9]   | 0x00        |
| 5               | 0xAA                     | 0xFF            | $(x + 5) \% 2^8$  | 0x0C | 0x0A | UP2[15:9]   | 0x00        |
| 6               | 0x55                     | 0x00            | $(x + 6) \% 2^8$  | 0x65 | 0x3D | UP3[15:9]   | 0x00        |
| 7               | 0xAA                     | 0xFF            | $(x + 7) \% 2^8$  | 0x1A | 0x72 | UP4[15:9]   | 0x00        |
| 8               | 0x55                     | 0x00            | $(x + 8) \% 2^8$  | 0x5F | 0x9B | UP1[15:9]   | 0x00        |
| 9               | 0xAA                     | 0xFF            | $(x + 9) \% 2^8$  | 0xD1 | 0x26 | UP2[15:9]   | 0x00        |
| 10              | 0x55                     | 0x00            | $(x + 10) \% 2^8$ | 0x63 | 0x43 | UP3[15:9]   | 0x00        |
| 11              | 0xAA                     | 0xFF            | $(x + 11) \% 2^8$ | 0xAC | 0xFF | UP4[15:9]   | 0x00        |

## SERIAL PORT INTERFACE

The AD9234 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the [Serial Control Interface Standard \(Rev. 1.0\)](#).

### CONFIGURATION USING THE SPI

Three pins define the SPI of the AD9234 ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 23). The SCLK pin synchronizes the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

**Table 23. Serial Port Interface Pins**

| Pin  | Function  |
|------|---|
| SCLK | Serial clock. The serial shift clock input that synchronizes serial interface, reads, and writes.   |
| SDIO | Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame. |
| CSB  | Chip select bar. An active low control that gates the read and write cycles.  |

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 3 and Table 5.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB pin can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or

write command is issued, allowing the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the [Serial Control Interface Standard \(Rev. 1.0\)](#).

### HARDWARE INTERFACE

The pins described in Table 23 comprise the physical interface between the user programming device and the serial port of the AD9234. The SCLK pin and the CSB pin function as inputs when using the SPI. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the [AN-812 Application Note, Microcontroller-Based Serial Port Interface \(SPI\) Boot Circuit](#).

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9234 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

### SPI ACCESSIBLE FEATURES

Table 24 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the [Serial Control Interface Standard \(Rev. 1.0\)](#). The AD9234 device-specific features are described in the Memory Map section.

**Table 24. Features Accessible Using the SPI**

| Feature Name        | Description  |
|---------------------|--|
| Mode                | Allows the user to set either power-down mode or standby mode.           |
| Clock               | Allows the user to access the clock divider via the SPI.                 |
| DDC                 | Allows the user to set up decimation filters for different applications. |
| Test Input/Output   | Allows the user to set test modes to have known data on output bits.     |
| Output Mode         | Allows the user to set up outputs.                                       |
| SERDES Output Setup | Allows the user to vary SERDES settings such as swing and emphasis.      |

## MEMORY MAP

### READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is divided into four sections: the Analog Devices SPI registers (Register 0x000 to Register 0x00D), the ADC function registers (Register 0x015 to Register 0x27A), The DDC function registers (Register 0x300 to Register 0x347), and the digital outputs and test modes registers (Register 0x550 to Register 0x5C5).

Table 25 (see the Memory Map section) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x561, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see the Table 25.

### Open and Reserved Locations

All address and bit locations that are not included in Table 25 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned (for example, Address 0x561). If the entire address location is open (for example, Address 0x013), do not write to this address location.

### Default Values

After the AD9234 is reset, critical registers are loaded with default values. The default values for the registers are given in Table 25.

### Logic Levels

An explanation of logic level terminology follows:

- “Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.”
- “Clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”
- X denotes a don't care bit.

### Channel-Specific Registers

Some channel setup functions, such as the input termination (Register 0x016), can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 25 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x008. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, set only Channel A or Channel B to read one of the two registers. If both bits are set during an SPI read cycle, the device returns the value for Channel A. Registers and bits designated as global in Table 25 affect the entire device and the channel features for which independent settings are not allowed between channels. The settings in Register 0x005 do not affect the global registers and bits.

### SPI Soft Reset

After issuing a soft reset by programming 0x81 to Register 0x000, the AD9234 requires 5 ms to recover. When programming the AD9234 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

## MEMORY MAP REGISTER TABLE

All address locations that are not included in Table 25 are not currently supported for this device and must not be written.

Table 25. Memory Map Registers

| Reg Addr (Hex)               | Register Name                        | Bit 7 (MSB)   | Bit 6                           | Bit 5             | Bit 4 | Bit 3                                   | Bit 2             | Bit 1  | Bit 0 (LSB)   | Default | Notes  |           |
|------------------------------|--------------------------------------|---|---------------------------------|-------------------|-------|---|-------------------|--|---|---------|--|-----------|
| Analog Devices SPI Registers |                                      |   |                                 |                   |       |   |                   |  |   |         |  |           |
| 0x000                        | INTERFACE_CONFIG_A                   | Soft reset (self clearing)  | LSB first<br>0 = MSB<br>1 = LSB | Address ascension | 0     | 0                                       | Address ascension | LSB first<br>0 = MSB<br>1 = LSB                          | Soft reset (self clearing)                                  | 0x00    |  |           |
| 0x001                        | INTERFACE_CONFIG_B                   | Single instruction  | 0                               | 0                 | 0     | 0                                       | 0                 | Datapath soft reset (self clearing)                      | 0   | 0x00    |  |           |
| 0x002                        | DEVICE_CONFIG (local)                | 0   | 0                               | 0                 | 0     | 0                                       | 0                 | 00 = normal operation<br>10 = standby<br>11 = power-down |   | 0x00    |  |           |
| 0x003                        | CHIP_TYPE                            | 0   | 0                               | 0                 | 0     | 011 = high speed ADC                    |                   |  |   | 0x03    | Read only                                    |           |
| 0x004                        | CHIP_ID (low byte)                   | 1   | 1                               | 0                 | 0     | 1                                       | 1                 | 1  | 0   | 0xCE    | Read only                                    |           |
| 0x005                        | CHIP_ID (high byte)                  | 0   | 0                               | 0                 | 0     | 0                                       | 0                 | 0  | 0   | 0x00    | Read only                                    |           |
| 0x006                        | CHIP_GRADE                           | 1010 = 1000 MSPS<br>0101 = 500 MSPS   |                                 |                   |       | X                                       | X                 | X  | X   |         | 0xA for AD9234-1000<br>0x5 for AD9234-500    | Read only |
| 0x008                        | Device index                         | 0   | 0                               | 0                 | 0     | 0                                       | 0                 | Channel B  | Channel A   | 0x03    |  |           |
| 0x00A                        | Scratch pad                          | 0   | 0                               | 0                 | 0     | 0                                       | 0                 | 0  | 0   | 0x00    |  |           |
| 0x00B                        | SPI revision                         | 0   | 0                               | 0                 | 0     | 0                                       | 0                 | 0  | 1   | 0x01    |  |           |
| 0x00C                        | Vendor ID (low byte)                 | 0   | 1                               | 0                 | 1     | 0                                       | 1                 | 1  | 0   | 0x56    | Read only                                    |           |
| 0x00D                        | Vendor ID (high byte)                | 0   | 0                               | 0                 | 0     | 0                                       | 1                 | 0  | 0   | 0x04    | Read only                                    |           |
| ADC Function Registers       |                                      |   |                                 |                   |       |   |                   |  |   |         |  |           |
| 0x015                        | Analog Input (local)                 | 0   | 0                               | 0                 | 0     | 0                                       | 0                 | 0  | Input disable<br>0 = normal operation<br>1 = input disabled | 0x00    |  |           |
| 0x016                        | Input termination (local)            | Analog input differential termination<br>0000 = 400 Ω<br>0001 = 200 Ω<br>0010 = 100 Ω<br>0110 = 50 Ω  |                                 |                   |       | 0011 = AD9234-1000<br>0001 = AD9234-500 |                   |  |   |         | 0x03 for AD9234-1000;<br>0x01 for AD9234-500 |           |
| 0x018                        | Input buffer current control (local) | 0000 = 1.0× buffer current<br>0001 = 1.5× buffer current<br>0010 = 2.0× buffer current<br>0011 = 2.5× buffer current<br>0100 = 3.0× buffer current<br>0101 = 3.5× buffer current<br>...<br>1111 = 8.5× buffer current |                                 |                   |       | 0                                       | 0                 | 0  | 0   |         | 0x30 for AD9234-1000;<br>0x20 for AD9234-500 |           |
| 0x024                        | V_1P0 control                        | 0   | 0                               | 0                 | 0     | 0                                       | 0                 | 0  | 1.0 V reference select<br>0 = internal<br>1 = external      | 0x00    |  |           |

| Reg Addr (Hex) | Register Name                    | Bit 7 (MSB)   | Bit 6 | Bit 5 | Bit 4  | Bit 3  | Bit 2  | Bit 1   | Bit 0 (LSB)  | Default   | Notes  |  |
|----------------|----------------------------------|---|-------|-------|--|--|--|---|--|-----------|--|--|
| 0x028          | Temperature diode (local)        | 0   | 0     | 0     | 0  | 0  | 0  | 0   | Diode selection<br>0 = no diode selected<br>1 = temperature diode selected | 0x00      | Used in conjunction with Reg. 0x040                          |  |
| 0x03F          | PDWN/STBY pin control (local)    | 0 = PDWN/STBY enabled<br>1 = disabled   | 0     | 0     | 0  | 0  | 0  | 0   | 0  | 0x00      | Used in conjunction with Reg. 0x040                          |  |
| 0x040          | Chip pin control                 | PDWN/STBY function<br>00 = power down<br>01 = standby<br>10 = disabled  |       |       | Fast Detect B (FD_B)<br>000 = Fast Detect B output<br>001 = JESD204B LMFC output<br>010 = JESD204B internal SYNC~ output<br>111 = disabled |  |  | Fast Detect A (FD_A)<br>000 = Fast Detect A output<br>001 = JESD204B LMFC output<br>010 = JESD204B internal SYNC~ output<br>011 = temperature diode<br>111 = disabled                 |  |           | 0x3F   |  |
| 0x10B          | Clock divider                    | 0   | 0     | 0     | 0  | 0  | 000 = divide by 1<br>001 = divide by 2<br>011 = divide by 4<br>111 = divide by 8 |   |  | 0x00      |  |  |
| 0x10C          | Clock divider phase (local)      | 0   | 0     | 0     | 0  | Independently controls Channel A and Channel B clock divider phase offset<br>0000 = 0 input clock cycles delayed<br>0001 = ½ input clock cycles delayed<br>0010 = 1 input clock cycles delayed<br>0011 = 1½ input clock cycles delayed<br>0100 = 2 input clock cycles delayed<br>0101 = 2½ input clock cycles delayed<br>...<br>1111 = 7½ input clock cycles delayed |  |   |  | 0x00      |  |  |
| 0x10D          | Clock divider and SYSREF control | Clock divider auto phase adjust<br>0 = disabled<br>1 = enabled  | 0     | 0     | 0  | Clock divider negative skew window<br>00 = no negative skew<br>01 = 1 device clock of negative skew<br>10 = 2 device clocks of negative skew<br>11 = 3 device clocks of negative skew  |  | Clock divider positive skew window<br>00 = no positive skew<br>01 = 1 device clock of positive skew<br>10 = 2 device clocks of positive skew<br>11 = 3 device clocks of positive skew |  | 0x00      | Clock divider must be >1                                     |  |
| 0x117          | Clock delay control              | 0   | 0     | 0     | 0  | 0  | 0  | 0   | Clock fine delay adjust enable<br>0 = disabled<br>1 = enabled              | 0x00      | Enabling the clock fine delay adjust causes a datapath reset |  |
| 0x118          | Clock fine delay (local)         | Clock fine delay adjust[7:0],<br>twos complement coded control to adjust the fine sample clock skew in ~1.7 ps steps<br>≤ -88 = -151.7 ps skew<br>-87 = -150 ps skew<br>...<br>0 = 0 ps skew<br>...<br>≥ +87 = +150 ps skew |       |       |  |  |  |   |  | 0x00      | Used in conjunction with Reg. 0x0117                         |  |
| 0x11C          | Clock status                     | 0   | 0     | 0     | 0  | 0  | 0  | 0   | 0 = no input clock detected<br>1 = input clock detected                    | Read only |  |  |

| Reg Addr (Hex) | Register Name                    | Bit 7 (MSB)   | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1  | Bit 0 (LSB) | Default  | Notes |
|----------------|----------------------------------|---|---|---|---|---|---|--|-------------|--|-------|
| 0x120          | SYSREF± Control 1                | 0   | SYSREF± flag reset<br>0 = normal operation<br>1 = flags held in reset   | 0   | SYSREF± transition select<br>0 = low to high<br>1 = high to low | CLK± edge select<br>0 = rising<br>1 = falling   | SYSREF± mode select<br>00 = disabled<br>01 = continuous<br>10 = N shot  |  | 0           | 0x00   |       |
| 0x121          | SYSREF± Control 2                | 0   | 0   | 0   | 0   | SYSREF± N-shot ignore counter select<br>0000 = next SYSREF± Only<br>0001 = ignore the first SYSREF± transitions<br>0010 = ignore the first two SYSREF± transitions<br>...<br>1111 = ignore the first 16 SYSREF± transitions   |   |  | 0x00        | Mode select, Reg. 0x120, Bits[2:1], must be N shot |       |
| 0x122          | SYSREF± Control 3                | 0   | 0   | 0   | 0   | Negative skew window (measured in sample clocks); number of clock cycles before the sample clock by which captured SYSREF± transitions are ignored<br>00 = no negative skew – SYSREF± must be captured accurately<br>01 = 1 sample clock of negative skew<br>10 = 2 sample clocks of negative skew<br>11 = 3 sample clocks of negative skew | Positive skew window (measured in sample clocks); number of clock cycles before the sample clock by which captured SYSREF± transitions are ignored<br>00 = no positive skew – SYSREF± must be captured accurately<br>01 = 1 sample clock of positive skew<br>10 = 2 sample clocks of positive skew<br>11 = 3 sample clocks of positive skew |  | 0x00        |  |       |
| 0x123          | SYSREF± timestamp delay control  | 0   | SYSREF± timestamp delay, Bits[6:0]<br>0x00 = no delay<br>0x01 = 1 clock delay<br>...<br>0x7F = 127 clocks delay |   |   |   |   |  | 0x00        | Ignored when Reg. 0x01FF = 0x00                    |       |
| 0x128          | SYSREF± Status 1                 | SYSREF± hold status, Register 0x128[7:4], refer to Table 14             |   |   |   | SYSREF± setup status, Register 0x128[3:0], refer to Table 14  |   |  |             | Read only  |       |
| 0x129          | SYSREF± and clock divider status | 0   | 0   | 0   | 0   | Clock divider phase when SYSREF± was captured<br>0000 = in-phase<br>0001 = SYSREF± is ½ cycle delayed from clock<br>0010 = SYSREF± is 1 cycle delayed from clock<br>0011 = 1½ input clock cycles delayed<br>0100 = 2 input clock cycles delayed<br>0101 = 2½ input clock cycles delayed<br>...<br>1111 = 7½ input clock cycles delayed      |   |  | Read only   |  |       |
| 0x12A          | SYSREF± counter                  | SYSREF± counter, Bits[7:0] increments when a SYSREF± signal is captured |   |   |   |   |   |  |             | Read only  |       |
| 0x1FF          | Chip sync mode                   | 0   | 0   | 0   | 0   | 0   | 0   | Synchronization mode<br>00 = normal<br>01 = timestamp                                    | 0x00        |  |       |
| 0x200          | Chip application mode            | 0   | 0   | Chip Q ignore<br>0 = normal (I/Q)<br>1 = ignore (I- only) | 0   | 0   | 0   | Chip operating mode<br>00 = full bandwidth mode<br>01 = DDC 0 on<br>10 = DDC 0 and DDC 1 | 0x00        |  |       |
| 0x201          | Chip decimation ratio            | 0   | 0   | 0   | 0   | 0   | Chip decimation ratio select<br>000 = full sample rate (decimate = 1)<br>001 = decimate by 2  |  | 0x00        |  |       |
| 0x228          | Customer offset                  | Offset adjust in LSBs from +127 to –128 (twos complement format)        |   |   |   |   |   |  |             | 0x00   |       |

| Reg Addr (Hex) | Register Name                            | Bit 7 (MSB)  | Bit 6 | Bit 5 | Bit 4  | Bit 3  | Bit 2   | Bit 1   | Bit 0 (LSB)   | Default   | Notes                               |
|----------------|--|--|-------|-------|--|--|---|---|---|-----------|-------------------------------------|
| 0x245          | Fast detect (FD) control (local)         | 0  | 0     | 0     | 0  | Force FD_A/ FD_B pins; 0 = normal function; 1 = force to value | Force value of FD_A/ FD_B pins if force pins is true, this value is output on FD pins | 0   | Enable fast detect output                             | 0x00      |                                     |
| 0x247          | FD upper threshold LSB (local)           | Fast detect upper threshold, Bits[7:0]   |       |       |  |  |   |   |   | 0x00      |                                     |
| 0x248          | FD upper threshold MSB (local)           | 0  | 0     | 0     | Fast detect upper threshold, Bits[12:8]          |  |   |   |   | 0x00      |                                     |
| 0x249          | FD lower threshold LSB (local)           | Fast detect lower threshold, Bits[7:0]   |       |       |  |  |   |   |   | 0x00      |                                     |
| 0x24A          | FD lower threshold MSB (local)           | 0  | 0     | 0     | Fast detect lower threshold, Bits[12:8]          |  |   |   |   | 0x00      |                                     |
| 0x24B          | FD dwell time LSB (local)                | Fast detect dwell time, Bits[7:0]  |       |       |  |  |   |   |   | 0x00      |                                     |
| 0x24C          | FD dwell time MSB (local)                | Fast detect dwell time, Bits[15:8]   |       |       |  |  |   |   |   | 0x00      |                                     |
| 0x26F          | Signal monitor synchronization control   | 0  | 0     | 0     | 0  | 0  | 0   | Synchronization mode<br>00 = disabled<br>01 = continuous<br>11 = one shot |   | 0x00      | Refer to the Signal Monitor section |
| 0x270          | Signal monitor control (local)           | 0  | 0     | 0     | 0  | 0  | 0   | Peak detector<br>0 = disabled<br>1 = enabled                              | 0   | 0x00      |                                     |
| 0x271          | Signal Monitor Period Register 0 (local) | Signal monitor period, Bits[7:0]   |       |       |  |  |   |   |   | 0x80      | In decimated output clock cycles    |
| 0x272          | Signal Monitor Period Register 1 (local) | Signal monitor period, Bits[15:8]  |       |       |  |  |   |   |   | 0x00      | In decimated output clock cycles    |
| 0x273          | Signal Monitor Period Register 2 (local) | Signal monitor period, Bits[23:16]   |       |       |  |  |   |   |   | 0x00      | In decimated output clock cycles    |
| 0x274          | Signal monitor result control (local)    | 0  | 0     | 0     | Result update<br>1 = update results (self clear) | 0  | 0   | 0   | Result selection<br>0 = reserved<br>1 = peak detector | 0x01      |                                     |
| 0x275          | Signal Monitor Result Register 0 (local) | Signal monitor result, Bits[7:0]<br>When Register 0x0274[0] = 1, result bits [19:7] = peak detector absolute value [12:0]; result bits [6:0] = 0 |       |       |  |  |   |   |   | Read only | Updated based on Reg. 0x274[4]      |
| 0x276          | Signal Monitor Result Register 1 (local) | Signal monitor result, Bits[15:8]  |       |       |  |  |   |   |   | Read only | Updated based on Reg. 0x274[4]      |

| Reg Addr (Hex) | Register Name                                      | Bit 7 (MSB)                    | Bit 6 | Bit 5 | Bit 4 | Bit 3                              | Bit 2 | Bit 1  | Bit 0 (LSB) | Default   | Notes                          |
|----------------|--|--------------------------------|-------|-------|-------|------------------------------------|-------|--|-------------|-----------|--------------------------------|
| 0x277          | Signal Monitor Result Register 1 (local)           | 0                              | 0     | 0     | 0     | Signal monitor result, Bits[19:16] |       |  |             | Read only | Updated based on Reg. 0x274[4] |
| 0x278          | Signal monitor period counter result (local)       | Period count result, Bits[7:0] |       |       |       |                                    |       |  |             | Read only | Updated based on Reg. 0x274[4] |
| 0x279          | Signal monitor SPORT over JESD204B control (local) | 0                              | 0     | 0     | 0     | 0                                  | 0     | 00 = reserved<br>11 = enable                 |             | 0x00      |                                |
| 0x27A          | SPORT over JESD204B input selection (local)        | 0                              | 0     | 0     | 0     | 0                                  | 0     | Peak detector<br>0 = disabled<br>1 = enabled | 0           | 0x00      |                                |

## DDC Function Registers (See the Digital Downconverter (DDC) Section)

|       |                                  |   |   |  |   |  |  |   |  |      |      |  |
|-------|----------------------------------|---|---|--|---|--|--|---|--|------|------|--|
| 0x300 | DDC synchron control             | 0   | 0   | 0  | DDC NCO soft reset<br>0 = normal operation<br>1 = reset | 0  | 0  | Synchronization mode (triggered by SYSREF±)<br>00 = disabled<br>01 = continuous<br>11 = 1-shot                          |  |      |      |  |
| 0x310 | DDC 0 control                    | Mixer select<br>0 = real mixer<br>1 = complex mixer   | Gain select<br>0 = 0 dB gain<br>1 = 6 dB gain | IF (intermediate frequency) mode<br>00 = variable IF mode (mixers and NCO enabled)<br>01 = 0 Hz IF mode (mixer bypassed, NCO disabled)<br>10 = $f_{ADC}/4$ Hz IF mode ( $f_{ADC}/4$ downmixing mode)<br>11 = test mode (mixer inputs forced to +FS, NCO enabled) |   | Complex to real enable<br>0 = disabled<br>1 = enabled  | 0  | Decimation rate select (complex to real disabled)<br>11 = decimate by 2 (complex to real enabled)<br>11 = decimate by 1 |  | 0x00 |      |  |
| 0x311 | DDC 0 input selection            | 0   | 0   | 0  | 0   | 0  | Q input select<br>0 = Ch A<br>1 = Ch B                             | 0   | I input select<br>0 = Ch A<br>1 = Ch B                             | 0x00 |      |  |
| 0x314 | DDC 0 frequency LSB              | DDC 0 NCO frequency value, Bits[7:0], twos complement |   |  |   |  |  |   |  | 0x00 |      |  |
| 0x315 | DDC0 frequency MSB               | X   | X   | X  | X   | DDC 0 NCO frequency value, Bits[11:8], twos complement |  |   |  |      | 0x00 |  |
| 0x320 | DDC 0 phase LSB                  | DDC 0 NCO phase value, Bits[7:0], twos complement     |   |  |   |  |  |   |  | 0x00 |      |  |
| 0x321 | DDC 0 phase MSB                  | X   | X   | X  | X   | DDC 0 NCO phase value, Bits[11:8], twos complement     |  |   |  |      | 0x00 |  |
| 0x327 | DDC 0 output test mode selection | 0   | 0   | 0  | 0   | 0  | Q output test mode enable<br>0 = disabled<br>1 = enabled from Ch B | 0   | I output test mode enable<br>0 = disabled<br>1 = enabled from Ch A | 0x00 |      |  |



| Reg Addr (Hex)                 | Register Name                    | Bit 7 (MSB)   | Bit 6   | Bit 5  | Bit 4   | Bit 3  | Bit 2  | Bit 1   | Bit 0 (LSB)  | Default | Notes                               |
|--------------------------------|----------------------------------|---|---|--|---|--|--|---|--|---------|-------------------------------------|
| 0x330                          | DDC 1 control                    | Mixer select<br>0 = real mixer<br>1 = complex mixer                   | Gain select<br>0 = 0 dB gain<br>1 = 6 dB gain | IF (intermediate frequency) mode<br>00 = variable IF mode (mixers and NCO enabled)<br>01 = 0 Hz IF mode (mixer bypassed, NCO disabled)<br>10 = $f_{ADC}/4$ Hz IF mode ( $f_{ADC}/4$ downmixing mode)<br>11 = test mode (mixer inputs forced to +FS, NCO enabled) |   | Complex to real enable<br>0 = disabled<br>1 = enabled  | 0  | Decimation rate select (complex to real disabled)<br>11 = decimate by 2 (complex to real enabled)<br>11 = decimate by 1 |  | 0x00    |                                     |
| 0x331                          | DDC 1 input selection            | 0   | 0   | 0  | 0   | 0  | Q input select<br>0 = Ch A<br>1 = Ch B                             | 0   | I input select<br>0 = Ch A<br>1 = Ch B                             | 0x00    |                                     |
| 0x334                          | DDC 1 frequency LSB              | DDC 1 NCO frequency value, Bits[7:0], twos complement                 |   |  |   |  |  |   |  | 0x00    |                                     |
| 0x335                          | DDC 1 frequency MSB              | X   | X   | X  | X   | DDC 1 NCO frequency value, Bits[11:8], twos complement   |  |   | 0x00   |         |                                     |
| 0x340                          | DDC 1 phase LSB                  | DDC 1 NCO phase value, Bits[7:0], twos complement                     |   |  |   |  |  |   |  | 0x00    |                                     |
| 0x341                          | DDC 1 phase MSB                  | X   | X   | X  | X   | DDC 1 NCO phase value, Bits[11:8], twos complement   |  |   | 0x00   |         |                                     |
| 0x347                          | DDC 1 output test mode selection | 0   | 0   | 0  | 0   | 0  | Q output test mode enable<br>0 = disabled<br>1 = enabled from Ch B | 0   | I output test mode enable<br>0 = disabled<br>1 = enabled from Ch A | 0x00    |                                     |
| Digital Outputs and Test Modes |                                  |   |   |  |   |  |  |   |  |         |                                     |
| 0x550                          | ADC test modes (local)           | User pattern selection<br>0 = continuous repeat<br>1 = single pattern | 0   | Reset PN long gen<br>0 = long PN enable<br>1 = long PN reset   | Reset PN short gen<br>0 = short PN enable<br>1 = short PN reset | Test mode selection<br>0000 = off, normal operation<br>0001 = midscale short<br>0010 = positive full scale<br>0011 = negative full scale<br>0100 = alternating checker board<br>0101 = PN sequence, long<br>0110 = PN sequence, short<br>0111 = 1/0 word toggle<br>1000 = the user pattern test mode (used with Register 0x550, Bit 7 and user pattern (1, 2, 3, 4) registers), 1111 = ramp output |  |   | 0x00   |         |                                     |
| 0x551                          | User Pattern 1 LSB               | 0   | 0   | 0  | 0   | 0  | 0  | 0   | 0  | 0x00    | Used with Reg. 0x550 and Reg. 0x573 |
| 0x552                          | User Pattern 1 MSB               | 0   | 0   | 0  | 0   | 0  | 0  | 0   | 0  | 0x00    | Used with Reg. 0x550 and Reg. 0x573 |
| 0x553                          | User Pattern 2 LSB               | 0   | 0   | 0  | 0   | 0  | 0  | 0   | 0  | 0x00    | Used with Reg. 0x550 and Reg. 0x573 |

| Reg Addr (Hex) | Register Name               | Bit 7 (MSB)   | Bit 6  | Bit 5   | Bit 4   | Bit 3   | Bit 2  | Bit 1   | Bit 0 (LSB)   | Default | Notes                               |
|----------------|-----------------------------|---|--|---|---|---|--|---|---|---------|-------------------------------------|
| 0x554          | User Pattern 2 MSB          | 0   | 0  | 0   | 0   | 0   | 0  | 0   | 0   | 0x00    | Used with Reg. 0x550 and Reg. 0x573 |
| 0x555          | User Pattern 3 LSB          | 0   | 0  | 0   | 0   | 0   | 0  | 0   | 0   | 0x00    | Used with Reg. 0x550 and Reg. 0x573 |
| 0x556          | User Pattern 3 MSB          | 0   | 0  | 0   | 0   | 0   | 0  | 0   | 0   | 0x00    | Used with Reg. 0x550 and Reg. 0x573 |
| 0x557          | User Pattern 4 LSB          | 0   | 0  | 0   | 0   | 0   | 0  | 0   | 0   | 0x00    | Used with Reg. 0x550 and Reg. 0x573 |
| 0x558          | User Pattern 4 MSB          | 0   | 0  | 0   | 0   | 0   | 0  | 0   | 0   | 0x00    | Used with Reg. 0x550 and Reg. 0x573 |
| 0x559          | Output Mode Control 1       | 0   | Converter control Bit 1 selection<br>000 = tie low (1'b0)<br>001 = overrange bit<br>010 = signal monitor bit<br>011 = fast detect (FD) bit<br>101 = SYSREF±<br>Only used when CS (Register 0x58F) = 2 or 3 |   |   | 0   | Converter control Bit 0 selection<br>000 = tie low (1'b0)<br>001 = overrange bit<br>010 = signal monitor bit<br>011 = fast detect (FD) bit<br>101 = SYSREF±<br>Only used when CS (Register 0x58F) = 3    |   |   | 0x00    |                                     |
| 0x55A          | Output Mode Control 2       | 0   | 0  | 0   | 0   | 0   | Converter control Bit 2 selection<br>000 = tie low (1'b0)<br>001 = overrange bit<br>010 = signal monitor bit<br>011 = fast detect (FD) bit<br>101 = SYSREF<br>Used when CS (Register 0x58F) = 1, 2, or 3 |   |   | 0x01    |                                     |
| 0x561          | Output mode                 | 0   | 0  | 0   | 0   | 0   | Sample invert<br>0 = normal<br>1 = sample invert   | Data format select<br>00 = offset binary<br>01 = twos complement      |   | 0x01    |                                     |
| 0x562          | Output overrange (OR) clear | Virtual Converter 7<br>OR<br>0 = OR bit enabled<br>1 = OR bit cleared | Virtual Converter 6<br>OR<br>0 = OR bit enabled<br>1 = OR bit cleared  | Virtual Converter 5<br>OR<br>0 = OR bit enabled<br>1 = OR bit cleared | Virtual Converter 4<br>OR<br>0 = OR bit enabled<br>1 = OR bit cleared | Virtual Converter 3<br>OR<br>0 = OR bit enabled<br>1 = OR bit cleared | Virtual Converter 2<br>OR<br>0 = OR bit enabled<br>1 = OR bit cleared  | Virtual Converter 1<br>OR<br>0 = OR bit enabled<br>1 = OR bit cleared | Virtual Converter 0<br>OR<br>0 = OR bit enabled<br>1 = OR bit cleared | 0x00    |                                     |
| 0x563          | Output OR status            | Virtual Converter 7<br>OR<br>0 = no OR<br>1 = OR occurred             | Virtual Converter 6<br>OR<br>0 = no OR<br>1 = OR occurred  | Virtual Converter 5<br>OR<br>0 = no OR<br>1 = OR occurred             | Virtual Converter 4<br>OR<br>0 = no OR<br>1 = OR occurred             | Virtual Converter 3<br>OR<br>0 = no OR<br>1 = OR occurred             | Virtual Converter 2<br>OR<br>0 = no OR<br>1 = OR occurred  | Virtual Converter 1<br>OR<br>0 = no OR<br>1 = OR occurred             | Virtual Converter 0<br>OR<br>0 = no OR<br>1 = OR occurred             | 0x00    | Read only                           |

| Reg Addr (Hex) | Register Name                | Bit 7 (MSB)   | Bit 6   | Bit 5   | Bit 4  | Bit 3  | Bit 2   | Bit 1   | Bit 0 (LSB)   | Default                                      | Notes                          |
|----------------|------------------------------|---|---|---|--|--|---|---|---|--|--------------------------------|
| 0x564          | Output channel select        | 0   | 0   | 0   | 0  | 0  | 0   | 0   | Converter channel swap<br>0 = normal channel ordering<br>1 = channel swap enabled | 0x00   |                                |
| 0x56E          | JESD204B lane rate control   | 0   | 0   | 0   | 0 = serial lane rate $\geq$ 6.25 Gbps and $\leq$ 12.5 Gbps<br>1 = serial lane rate must be $\geq$ 3.125 Gbps and $\leq$ 6.25 Gbps  | 0  | 0   | 0   | 0   | 0x00 for AD9234-1000;<br>0x10 for AD9234-500 |                                |
| 0x56F          | JESD204B PLL lock status     | PLL lock<br>0 = not locked<br>1 = locked  | 0   | 0   | 0  | 0  | 0   | 0   | 0   | 0x00   | Read only                      |
| 0x570          | JESD204B quick configuration | JESD204B quick configuration<br>$L = \text{number of lanes} = 2^{\text{Register 0x570, Bits[7:6]}}$<br>$M = \text{number of converters} = 2^{\text{Register 0x570, Bits[5:3]}}$<br>$F = \text{number of octets/frame} = 2^{\text{Register 0x570, Bits[2:0]}}$ |   |   |  |  |   |   |   | 0x88   | Refer to Table 12 and Table 13 |
| 0x571          | JESD204B Link Mode Control 1 | Standby mode<br>0 = all converter outputs 0<br>1 = CGS (/K28.5/)  | Tail bit (t) PN<br>0 = disable<br>1 = enable<br>$T = N' - N - CS$ | Long transport layer test<br>0 = disable<br>1 = enable  | Lane synchronization<br>0 = disable<br>FACI uses /K28.7/<br>1 = enable<br>FACI uses /K28.3/ and /K28.7/  | ILAS sequence mode<br>00 = ILAS disabled<br>01 = ILAS enabled<br>11 = ILAS always on test mode | FACI<br>0 = enabled<br>1 = disabled   | Link control<br>0 = active<br>1 = power down                    | 0x14  |  |                                |
| 0x572          | JESD204B Link Mode Control 2 | SYNCSINB± pin control<br>00 = normal<br>10 = ignore SYNCSINB± (force CGS)<br>11 = ignore SYNCSINB± (force ILAS/user data)   |   | SYNCSINB± pin invert<br>0 = active low<br>1 = active high   | SYNCSINB± pin type<br>0 = differential<br>1 = cmos   | 0  | 8B/10B bypass<br>0 = normal<br>1 = bypass   | 8B/10B bit invert<br>0 = normal<br>1 = invert the a...j symbols | 0   | 0x00   |                                |
| 0x573          | JESD204B Link Mode Control 3 | CHKSUM mode<br>00 = sum of all 8-bit link config registers<br>01 = sum of individual link config fields<br>10 = checksum set to zero  |   | Test injection point<br>00 = N' sample input<br>01 = 10-bit data at 8B/10B output (for PHY testing)<br>10 = 8-bit data at scrambler input | JESD204B test mode patterns<br>0000 = normal operation (test mode disabled)<br>0001 = alternating checker board<br>0010 = 1/0 word toggle<br>0011 = 31-bit PN sequence— $X^{31} + X^{28} + 1$<br>0100 = 23-bit PN sequence— $X^{23} + X^{18} + 1$<br>0101 = 15-bit PN sequence— $X^{15} + X^{14} + 1$<br>0110 = 9-bit PN sequence— $X^9 + X^5 + 1$<br>0111 = 7-bit PN sequence— $X^7 + X^6 + 1$<br>1000 = ramp output<br>1110 = continuous/repeat user test<br>1111 = single user test |  |   |   | 0x00  |  |                                |
| 0x574          | JESD204B Link Mode Control 4 | ILAS delay<br>0000 = transmit ILAS on first LMFC after SYNCSINB± deasserted<br>0001 = transmit ILAS on second LMFC after SYNCSINB± deasserted<br>...<br>1111 = transmit ILAS on 16 <sup>th</sup> LMFC after SYNCSINB± deasserted                              |   |   |  | 0  | Link layer test mode<br>000 = normal operation (link layer test mode disabled)<br>001 = continuous sequence of /D21.5/ characters<br>100 = modified RPAT test sequence<br>101 = JSPAT test sequence<br>110 = JTSPAT test sequence |   |   | 0x00   |                                |
| 0x578          | JESD204B LMFC offset         | 0   | 0   | 0   | LMFC phase offset value, Bits[4:0]   |  |   |   | 0x00  |  |                                |

| Reg Addr (Hex) | Register Name                    | Bit 7 (MSB)  | Bit 6 | Bit 5   | Bit 4   | Bit 3                            | Bit 2 | Bit 1  | Bit 0 (LSB)    | Default | Notes                     |
|----------------|----------------------------------|--|-------|---|---|----------------------------------|-------|--|----------------|---------|---------------------------|
| 0x580          | JESD204B DID config              | JESD204B Tx DID value, Bits[7:0]   |       |   |   |                                  |       |  |                | 0x00    |                           |
| 0x581          | JESD204B BID config              | 0  | 0     | 0   | 0   | JESD204B Tx BID value, Bits[7:0] |       |  | 0x00           |         |                           |
| 0x583          | JESD204B LID Config 1            | 0  | 0     | 0   | Lane 0 LID value, Bits[4:0]   |                                  |       | 0x00   |                |         |                           |
| 0x584          | JESD204B LID Config 2            | 0  | 0     | 0   | Lane 1 LID value, Bits[4:0]   |                                  |       | 0x01   |                |         |                           |
| 0x585          | JESD204B LID Config 3            | 0  | 0     | 0   | Lane 2 LID value, Bits[4:0]   |                                  |       | 0x01   |                |         |                           |
| 0x586          | JESD204B LID Config 4            | 0  | 0     | 0   | Lane 3 LID value, Bits[4:0]   |                                  |       | 0x03   |                |         |                           |
| 0x58B          | JESD204B parameters SCR/L        | JESD204B scrambling (SCR)<br>0 = disabled<br>1 = enabled   | 0     | 0   | 0   | 0                                | 0     | JESD204B lanes (L)<br>00 = 1 lane<br>01 = 2 lanes<br>11 = 4 lanes<br>Read only, see Register 0x570 |                | 0x8X    |                           |
| 0x58C          | JESD204B F config                | Number of octets per frame, F = Register 0x58C, Bits[7:0] + 1  |       |   |   |                                  |       |  |                | 0x88    | Read only, see Reg. 0x570 |
| 0x58D          | JESD204B K config                | 0  | 0     | 0   | Number of frames per multiframe, K = Register 0x58D, Bits[4:0] + 1<br>Only values where (F × K) mod 4 = 0 are supported |                                  |       | 0x1F   | See Reg. 0x570 |         |                           |
| 0x58E          | JESD204B M config                | Number of converters per link, Bits[7:0]<br>0x00 = link connected to one virtual converter (M = 1)<br>0x01 = link connected to two virtual converters (M = 2)<br>0x03 = link connected to four virtual converters (M = 4)<br>0x07 = link connected to eight virtual converters (M = 8) |       |   |   |                                  |       |  |                |         | Read only                 |
| 0x58F          | JESD204B CS/N config             | Number of control bits (CS) per sample<br>00 = no control bits (CS = 0)<br>01 = 1 control bit (CS = 1); Control Bit 2 only<br>10 = 2 control bits (CS = 2); Control Bit 2 and Control Bit 1 only<br>11 = 3 control bits (CS = 3); all control bits (2, 1, 0)                           | 0     | ADC converter resolution (N)<br>0x06 = 7-bit resolution<br>0x07 = 8-bit resolution<br>0x08 = 9-bit resolution<br>0x09 = 10-bit resolution<br>0x0A = 11-bit resolution<br>0x0B = 12-bit resolution<br>0x0C = 13-bit resolution<br>0x0D = 14-bit resolution<br>0x0E = 15-bit resolution<br>0x0F = 16-bit resolution |   |                                  | 0x0F  |  |                |         |                           |
| 0x590          | JESD204B N' config               | Subclass support (Subclass version)<br>000 = Subclass 0 (no deterministic latency)<br>001 = Subclass 1   |       |   | ADC number of bits per sample (N')<br>0x7 = 8 bits<br>0xF = 16 bits   |                                  |       | 0x2F   |                |         |                           |
| 0x591          | JESD204B S config                | 0  | 0     | 1   | Samples per converter frame cycle (S)<br>S value = Register 0x591 [4:0] + 1   |                                  |       |  | Read only      |         |                           |
| 0x592          | JESD204B HD and CF configuration | HD value<br>0 = disabled<br>1 = enabled  | 0     | 0   | Control words per frame clock cycle per link (CF)<br>CF value = Register 0x592, Bits[4:0]                               |                                  |       | 0x80   | Read only      |         |                           |
| 0x5A0          | JESD204B CHKSUM 0                | CHKSUM value for SERDOUT0±, Bits[7:0]  |       |   |   |                                  |       |  |                | 0x81    | Read only                 |
| 0x5A1          | JESD204B CHKSUM 1                | CHKSUM value for SERDOUT1±, Bits[7:0]  |       |   |   |                                  |       |  |                | 0x82    | Read only                 |
| 0x5A2          | JESD204B CHKSUM 2                | CHKSUM value for SERDOUT2±, Bits[7:0]  |       |   |   |                                  |       |  |                | 0x82    | Read only                 |
| 0x5A3          | JESD204B CHKSUM 3                | CHKSUM value for SERDOUT3±, Bits[7:0]  |       |   |   |                                  |       |  |                | 0x84    | Read only                 |

| Reg Addr (Hex) | Register Name                     | Bit 7 (MSB) | Bit 6                                   | Bit 5 | Bit 4                                   | Bit 3   | Bit 2   | Bit 1 | Bit 0 (LSB)                            | Default | Notes |
|----------------|-----------------------------------|-------------|---|-------|---|---|---|-------|--|---------|-------|
| 0x5B0          | JESD204B lane power-down          | 1           | SERD-OUT3±<br>0 = on<br>1 = off         | 1     | SERD-OUT2±<br>0 = on<br>1 = off         | 1   | SERD-OUT1±<br>0 = on<br>1 = off   | 1     | SERDOUT0±<br>0 = on<br>1 = off         | 0xAA    |       |
| 0x5B2          | JESD204B lane SERDOUT0± assign    | X           | X                                       | X     | X                                       | 0   | SERDOUT0± lane assignment<br>000 = Logical Lane 0<br>001 = Logical Lane 1<br>010 = Logical Lane 2<br>011 = Logical Lane 3 |       |  | 0x00    |       |
| 0x5B3          | JESD204B lane SERDOUT1± assign    | X           | X                                       | X     | X                                       | 0   | SERDOUT1± lane assignment<br>000 = Logical Lane 0<br>001 = Logical Lane 1<br>010 = Logical Lane 2<br>011 = Logical Lane 3 |       |  | 0x11    |       |
| 0x5B5          | JESD204B lane SERDOUT2± assign    | X           | X                                       | X     | X                                       | 0   | SERDOUT2± lane assignment<br>000 = Logical Lane 0<br>001 = Logical Lane 1<br>010 = Logical Lane 2<br>011 = Logical Lane 3 |       |  | 0x22    |       |
| 0x5B6          | JESD204B lane SERDOUT3± assign    | X           | X                                       | X     | X                                       | 0   | SERDOUT3± lane assignment<br>000 = Logical Lane 0<br>001 = Logical Lane 1<br>010 = Logical Lane 2<br>011 = Logical Lane 3 |       |  | 0x33    |       |
| 0x5BF          | JESD serializer drive adjust      | 0           | 0                                       | 0     | 0                                       | Swing voltage<br>0000 = 237.5 mV<br>0001 = 250 mV<br>0010 = 262.5 mV<br>0011 = 275 mV<br>0100 = 287.5 mV<br>0101 = 300 mV (default)<br>0110 = 312.5 mV<br>0111 = 325 mV<br>1000 = 337.5 mV<br>1001 = 350 mV<br>1010 = 362.5 mV<br>1011 = 375 mV<br>1100 = 387.5 mV<br>1101 = 400 mV<br>1110 = 412.5 mV<br>1111 = 425 mV |   |       |  | 0x05    |       |
| 0x5C1          | De-emphasis select                | 0           | SERD-OUT3±<br>0 = disable<br>1 = enable | 0     | SERD-OUT2±<br>0 = disable<br>1 = enable | 0   | SERD-OUT1±<br>0 = disable<br>1 = enable   | 0     | SERDOUT0±<br>0 = disable<br>1 = enable | 0x00    |       |
| 0x5C2          | De-emphasis setting for SERDOUT0± | 0           | 0                                       | 0     | 0                                       | SERDOUT0± de-emphasis settings:<br>0000 = 0 dB<br>0001 = 0.3 dB<br>0010 = 0.8 dB<br>0011 = 1.4 dB<br>0100 = 2.2 dB<br>0101 = 3.0 dB<br>0110 = 4.0 dB<br>0111 = 5.0 dB   |   |       |  | 0x00    |       |
| 0x5C3          | De-emphasis setting for SERDOUT1± | 0           | 0                                       | 0     | 0                                       | SERDOUT1± de-emphasis settings:<br>0000 = 0 dB<br>0001 = 0.3 dB<br>0010 = 0.8 dB<br>0011 = 1.4 dB<br>0100 = 2.2 dB<br>0101 = 3.0 dB<br>0110 = 4.0 dB<br>0111 = 5.0 dB   |   |       |  | 0x00    |       |

| Reg Addr (Hex) | Register Name                     | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3   | Bit 2 | Bit 1 | Bit 0 (LSB) | Default | Notes |
|----------------|-----------------------------------|-------------|-------|-------|-------|---|-------|-------|-------------|---------|-------|
| 0x5C4          | De-emphasis setting for SERDOUT2± | 0           | 0     | 0     | 0     | SERDOUT2± de-emphasis settings:<br>0000 = 0 dB<br>0001 = 0.3 dB<br>0010 = 0.8 dB<br>0011 = 1.4 dB<br>0100 = 2.2 dB<br>0101 = 3.0 dB<br>0110 = 4.0 dB<br>0111 = 5.0 dB |       |       |             | 0x00    |       |
| 0x5C5          | De-emphasis setting for SERDOUT3± | 0           | 0     | 0     | 0     | SERDOUT3± de-emphasis settings:<br>0000 = 0 dB<br>0001 = 0.3 dB<br>0010 = 0.8 dB<br>0011 = 1.4 dB<br>0100 = 2.2 dB<br>0101 = 3.0 dB<br>0110 = 4.0 dB<br>0111 = 5.0 dB |       |       |             | 0x00    |       |

## APPLICATIONS INFORMATION

### POWER SUPPLY RECOMMENDATIONS

The AD9234 must be powered by the following seven supplies: AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1\_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, and SPIVDD = 1.8 V. For applications requiring an optimal high power efficiency and low noise performance, it is recommended that the [ADP2164](#) and [ADP2370](#) switching regulators be used to convert the 3.3 V, 5.0 V, or 12 V input rails to an intermediate rail (1.8 V and 3.8 V). These intermediate rails are then postregulated by very low noise, low dropout (LDO) regulators ([ADP1741](#), [ADM7172](#), and [ADP125](#)). Figure 117 shows the recommended power supply scheme for AD9234.

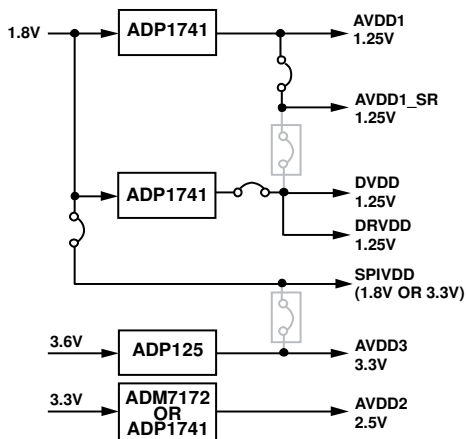


Figure 117. High Efficiency, Low Noise Power Solution for the AD9234

It is not necessary to split all of these power domains in all cases. The recommended solution shown in Figure 117 provides the lowest noise, highest efficiency power delivery system for the AD9234. If only one 1.25 V supply is available, route to AVDD1 first and then tap it off and isolate it with a ferrite bead or a filter choke, preceded by decoupling capacitors for AVDD1\_SR, SPIVDD, DVDD, and DRVDD, in that order. The user can employ several different decoupling capacitors to cover both high and low frequencies. These must be located close to the point of entry at the PCB level and close to the devices, with minimal trace lengths.

### EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADC be connected to ground to achieve the best electrical and thermal performance of the AD9234. Connect an exposed continuous copper plane on the PCB to the AD9234 exposed pad, Pin 0. The copper plane must have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias must be solder filled or plugged. The number of vias and the fill determine the resultant  $\theta_{JA}$  measured on the board, which is shown in Table 7.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions only guarantees one tie point. See Figure 118 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the [AN-772 Application Note, A Design and Manufacturing Guide for the Lead Frame Chip Scale Package \(LFCSP\)](#).

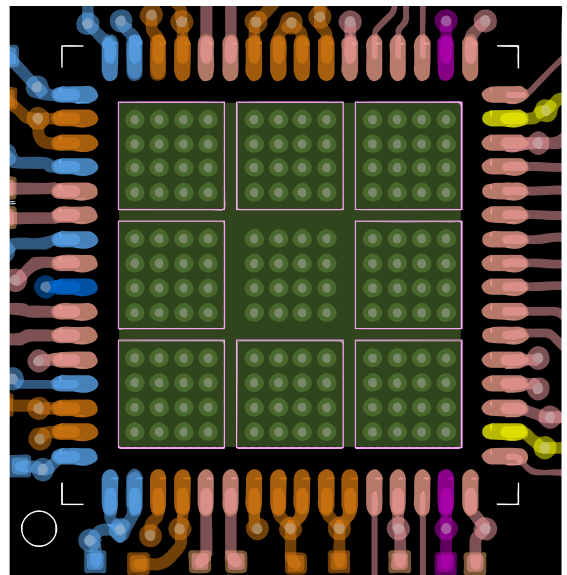
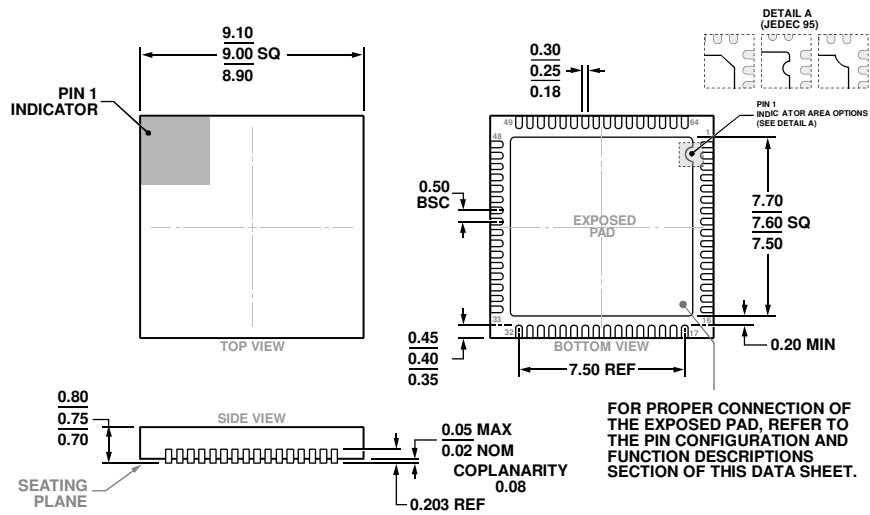


Figure 118. Recommended PCB Layout of Exposed Pad for the AD9234

### AVDD1\_SR (PIN 57) AND AGND (PIN 56 AND PIN 60)

AVDD1\_SR (Pin 57) and AGND (Pin 56 and Pin 60) can be used to provide a separate power supply node to the SYSREF± circuits of AD9234. If running in Subclass 1, the AD9234 can support periodic one shot or gapped signals. To minimize the coupling of this supply into the AVDD1 supply node, adequate supply bypassing is needed.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WMMD

Figure 119. 64-Lead Lead Frame Chip Scale Package [LFCSP]  
9 mm × 9 mm Body and 0.75 Package Height  
(CP-64-15)  
Dimensions shown in millimeters

ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description  | Package Option |
|--------------------|-------------------|--|----------------|
| AD9234BCPZ-500     | -40°C to +85°C    | 64-Lead Lead Frame Chip Scale Package [LFCSP]                                      | CP-64-15       |
| AD9234BCPZRL7-500  | -40°C to +85°C    | 64-Lead Lead Frame Chip Scale Package [LFCSP]                                      | CP-64-15       |
| AD9234BCPZ-1000    | -40°C to +85°C    | 64-Lead Lead Frame Chip Scale Package [LFCSP]                                      | CP-64-15       |
| AD9234BCPZRL7-1000 | -40°C to +85°C    | 64-Lead Lead Frame Chip Scale Package [LFCSP]                                      | CP-64-15       |
| AD9234-500EBZ      |                   | Evaluation Board for AD9234-500 (Optimized for Full Analog Input Frequency Range)  |                |
| AD9234-1000EBZ     |                   | Evaluation Board for AD9234-1000 (Optimized for Full Analog Input Frequency Range) |                |
| AD9234-LF500EBZ    |                   | Evaluation Board for AD9234-500 with 1 GHz Bandwidth                               |                |
| AD9234-LF1000EBZ   |                   | Evaluation Board for AD9234-1000 with 1 GHz Bandwidth                              |                |

<sup>1</sup> Z = RoHS Compliant Part.