The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

For More Information

Please contact your local sales office for additional information about Cypress products and solutions.

About Cypress

Cypress is the leader in advanced embedded system solutions for the world's most innovative automotive, industrial, smart home appliances, consumer electronics and medical products. Cypress' microcontrollers, analog ICs, wireless and USB-based connectivity solutions and reliable, high-performance memories help engineers design differentiated products and get them to market first. Cypress is committed to providing customers with the best support and development resources on the planet enabling them to disrupt markets by creating new product categories in record time. To learn more, go to www.cypress.com.

MB91550 Series

MB91F552, FR Family FR81S, 32-bit Microcontroller

The MB91550 series is a Cypress 32-bit microcontroller designed for automotive devices. This series contains the FR81S CPU which is compatible with the FR family.

Note: FR is a line of products of Cypress

Features

FR81S CPU Core

- 32-bit RISC, load/store architecture, 5-stage pipeline
- Maximum operating frequency: 80 MHz (Source oscillation = 4.0 MHz and 20 multiplied (PLL clock multiplication system))
- General-purpose register : 32 bits × 16 sets
- 16-bit fixed length instructions (basic instruction), 1 instruction per cycle
- Instructions appropriate to embedded applications
  - Memory-to-memory transfer instruction
  - Bit processing instruction
  - Barrel shift order etc.
- High-level language support instructions
- Function entry/exit instructions
- Register content multi-load and store instructions
- Bit search instructions

  Logical 1 detection, 0 detection, and change-point detection
- Branch instructions with delay slot

  Decrease overhead during branch process
- Register interlock function

  Easy assembler writing
- Built-in multiplier and instruction level support

  Signed 32-bit multiplication: 5 cycles

  Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS saving) 6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR Family
- Built-in memory protection function (MPU)
  - Eight protection areas can be specified commonly for instructions and the data.
  - Control access privilege in both privilege mode and user mode.
- Built-in FPU (floating point arithmetic)
  - IEEE754 compliant
  - Floating-point register 32-bit × 16 sets

Peripheral functions

- CPU function for clock generation (with SSCG function)
  - Main oscillation (4MHz to 16MHz)
  - PLL multiplication rate (1 to 20 times)
- PWM function for clock generation
  - Main oscillation (4 MHz to 16 MHz)
  - PLL multiplication rate (1 to 50 times)
- Built-in program flash memory capacity MB91F552:128+64KB
- Built-in data flash (WorkFlash) 64KB
- Built-in RAM capacity
  - Main RAM MB91F552:24KB
- General-purpose ports: MB91F552: 30sets

DMA Controller

- Up to 8 channels can be started simultaneously.
- 2 transfer factors (Internal peripheral request and software)
- A/D converter 1 (successive approximation type)
  - 12-bit resolution : 8 channels × 1 unit
  - Conversion time : 1µs
- A/D converter 2 (successive approximation type simultaneous sampling of 4-channel input)
  - 12-bit resolution: Max. 4 channels × 1 unit
  - Conversion time :
    - For 1-channel conversion: Min. 0.7 µs
    - For 4-channel conversion: Min. 1.75 µs
- External interrupt input: 4 channels
  - Level ("H"/"L"), or edge detection (rising or falling) supported
- Multi-function serial communication (built-in transmission/reception FIFO memory) :3 channels
  - 5V tolerant input: 3 channels (ch.0, ch.1, ch.2) CMOS hysteresis input

< UART (Asynchronous serial interface) >

- Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
- Parity or no parity is selectable.
- Built-in dedicated baud rate generator
- The external clock can be used as the transfer clock.
- Parity, frame, and overrun error detection functions are provided
- DMA transfer support

<CSIO (Synchronous serial interface) >

- Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
- SPI supported; master and slave systems supported; 5-bit to 16-bit, 20-bit, 24-bit, 32-bit data length can be set.
- Built-in dedicated baud rate generator (Master operation)
- The external clock can be entered (Slave operation).
- Overrun error detection function is provided
- DMA transfer support
- Serial chip select SPI function

<LIN (Asynchronous Serial Interface for LIN) >

- Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
- LIN protocol revision 2.1 supported
- Master and slave systems supported
- Framing error and overrun error detection
- LIN synch break generation and detection; LIN synch delimiter generation
- Built-in dedicated baud rate generator
- The external clock can be adjusted by the reload counter
- DMA transfer support
- Hard assist function

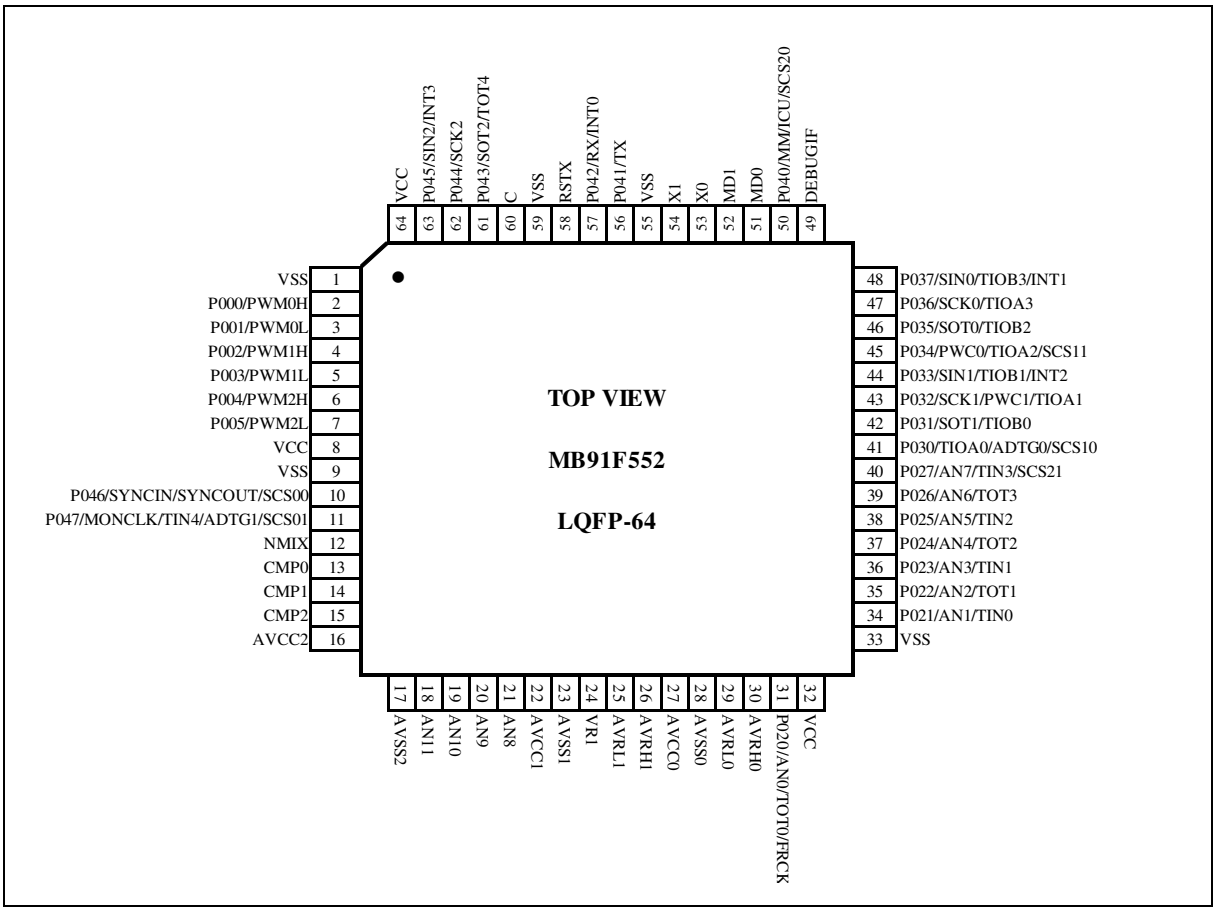
- CAN Controller (CAN) : 1 channel
  - Transfer speed : Up to 1Mbps
  - 64-transmission/reception message buffering: 1 channel
- Reload timer: 16-bit × 5 channels
- Free-run timer: 16-bit × 1 channel
- Input capture: 16-bit × 1 channel (linked with the free-run timer)
- PWC: 2 channels
  - Max. 80 MHz operation
- PWM: 6 channels (2 channels × 3 pairs)
  - Max. 200 MHz operation
- Clock supervisor
  - Monitoring abnormality (by damaged quartz, etc.) of external main oscillation (4 MHz)
  - When abnormality is detected, it switches to the CR clock.
- Base timer : Max.4 channels
  - 16-bit timer
  - The timer mode is selected from PWM/PPG/PWC/reload.
  - A 32-bit timer can be used in 2 channels of cascade mode for the reload timer/PWC function.
- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog (An effective range of a clear counter can be set.)
- Slope compensation (constant current unit): 1 channel
- Comparator: 3 channels
- NMI (non-maskable interrupt)
- Interrupt controller
- Interrupt request batch read
  - Multiple interrupts from peripherals can be read by a series of registers.
- Low-power consumption mode
  - Sleep / Stop / Watch mode
- Power-on reset
- Low-voltage detection reset (external power supply and internal power supply are independently observed.)
- Device Package : LQFP-64
- CMOS 90nm Technology
- Power supply
  - 5V Power supply
  - The internal 1.2V is generated from 5V with the voltage step-down circuit.

Contents

1. Product Lineup

Parameter \ Part number	MB91F552
System Clock	On chip PLL Clock multiple method
Minimum instruction execution time	12.5ns(80MHz)
Flash Capacity (Program)	128 + 64KB
Flash Capacity (Data)	64KB
RAM Capacity	24KB
DMA Transfer	8 channels
16-bit Base Timer	4 channels
Free-run Timer	16bit×1 channel
Input capture	16bit×1 channel
16-bit Reload Timer	5 channels
Clock Supervisor	Yes
External Interrupt	4 channels
A/D converter	12 bit×8 channels (1 unit) Simultaneous sampling of 12 bit×4 channels input (1 unit)
Multi-Function Serial Interface	3 channels
CAN	64 msg×1 channel
Hardware Watchdog Timer	Yes
CRC Formation	Yes
Low-voltage detection reset	Yes
Flash Security	Yes
ECC Flash/WorkFlash	Yes
ECC RAM	Yes
Memory Protection Function (MPU)	Yes
Floating point arithmetic (FPU)	Yes
General-purpose port (#GPIOs)	30 ports
SSCG	Yes
CR oscillator	Yes
OCD (On Chip Debug)	Yes
TPU (Timing Protection Unit)	Yes
Key code register	Yes
Comparator	3 channels
Slope compensation (constant current unit)	1 channel
PWC	2 channels
PWM	2 channels×3pairs
NMI request function	Yes
Operation guaranteed temperature (T_A)	-40°C to+125°C
Power supply	4.5V to 5.5V
Package	LQFP-64

2. Pin Assignment



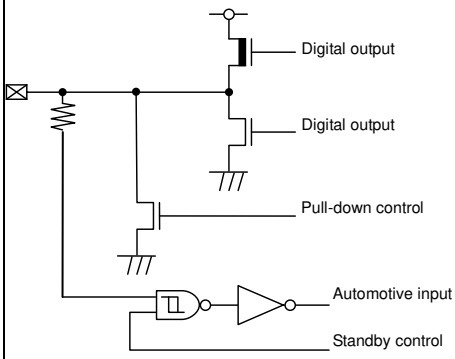
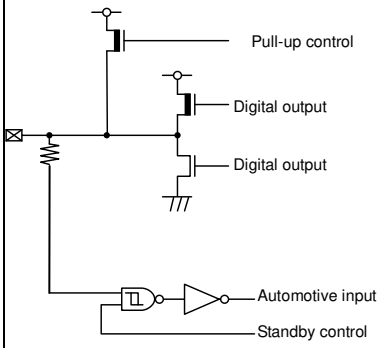
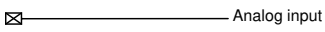
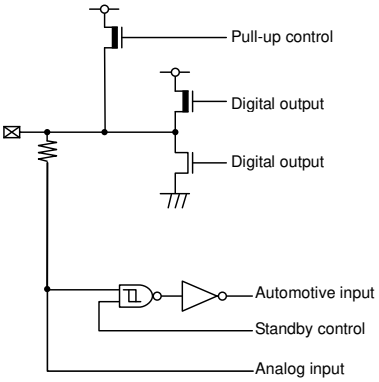
3. Pin Description

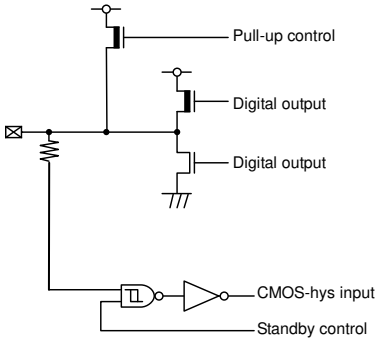
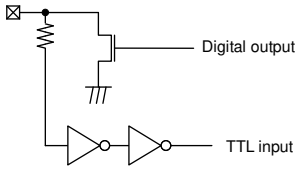
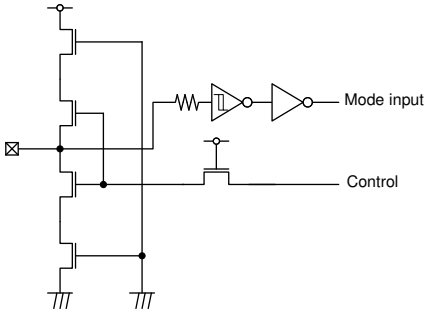
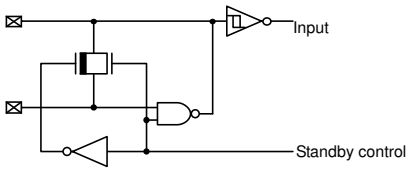
Pin no.	Pin Name	Polarity	I/O circuit types	Function
2	P000 PWM0H	- -	A	General-purpose I/O port PWM ch.0-H
3	P001 PWM0L	- -	A	General-purpose I/O port PWM ch.0-L
4	P002 PWM1H	- -	A	General-purpose I/O port PWM ch.1-H
5	P003 PWM1L	- -	A	General-purpose I/O port PWM ch.1-L
6	P004 PWM2H	- -	A	General-purpose I/O port PWM ch.2-H
7	P005 PWM2L	- -	A	General-purpose I/O port PWM ch.2-L
10	P046 SYNCIN SYNCOUT SCS00	- - - -	B	General-purpose I/O port Master/Slave input pin for PWM parallel operation drive Master/Slave output pin for PWM parallel operation drive Multi-function serial ch.0 serial chip select 00 I/O pin
11	P047 MONCLK TIN4 ADTG1 SCS01	- - - - -	B	General-purpose I/O port Clock monitor output pin Reload timer ch.4 event input pin A/D converter ch.8-ch.11 external trigger input pin Multi-function serial ch.0 serial chip select 01 output pin
12	NMIX	N	L	Interrupt input pin without mask
13	CMP0	-	C	Comparator ch.0 input pin
14	CMP1	-	C	Comparator ch.1 input pin
15	CMP2	-	C	Comparator ch.2 input pin
18	AN11	-	C	A/D converter ch.11 analog input pin (Simultaneous sampling possible with ch.8, ch.9, ch.10, and ch.11)
19	AN10	-	C	A/D converter ch.10 analog input pin (Simultaneous sampling possible with ch.8, ch.9, ch.10, and ch.11)
20	AN9	-	C	A/D converter ch.9 analog input pin (Simultaneous sampling possible with ch.8, ch.9, ch.10, and ch.11)
21	AN8	-	C	A/D converter ch.8 analog input pin (Simultaneous sampling possible with ch.8, ch.9, ch.10, and ch.11)
31	P020 AN0 TOT0 FRCK	- - - -	D	General-purpose I/O port A/D converter ch.0 analog input pin Reload timer ch.0 output pin Free-run timer clock input pin
34	P021 AN1 TIN0	- - -	D	General-purpose I/O port A/D converter ch.1 analog input pin Reload timer ch.0 event input pin
35	P022 AN2 TOT1	- - -	D	General-purpose I/O port A/D converter ch.2 analog input pin Reload timer ch.1 output pin

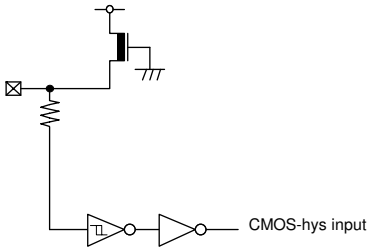
Pin no.	Pin Name	Polarity	I/O circuit types	Function
36	P023 AN3 TIN1	- - -	D	General-purpose I/O port A/D converter ch.3 analog input pin Reload timer ch.1 event input pin
37	P024 AN4 TOT2	- - -	D	General-purpose I/O port A/D converter ch.4 analog input pin Reload timer ch.2 output pin
38	P025 AN5 TIN2	- - -	D	General-purpose I/O port A/D converter ch.5 analog input pin Reload timer ch.2 event input pin
39	P026 AN6 TOT3	- - -	D	General-purpose I/O port A/D converter ch.6 analog input pin Reload timer ch.3 output pin
40	P027 AN7 TIN3 SCS21	- - - -	D	General-purpose I/O port A/D converter ch.7 analog input pin Reload timer ch.3 event input pin Multi-function serial ch.2 serial chip select 21 output pin
41	P030 TIOA0 ADTG0 SCS10	- - - -	B	General-purpose I/O port Base timer ch.0 TIOA output pin A/D converter ch.0-ch.7 external trigger input pin Multi-function serial ch.1 serial chip select 10 I/O pin
42	P031 SOT1 TIOB0	- - -	B	General-purpose I/O port Multi-function serial ch.1 serial data output pin Base timer ch.0 TIOB input pin
43	P032 SCK1 PWC1 TIOA1	- - - -	E	General-purpose I/O port Multi-function serial ch.1 clock I/O pin PWC ch.1 input pin Base timer ch.1 TIOA I/O pin
44	P033 SIN1 TIOB1 INT2	- - - -	E	General-purpose I/O port Multi-function serial ch.1 serial data input pin Base timer ch.1 TIOB input pin INT2 external interrupt input pin
45	P034 PWC0 TIOA2 SCS11	- - - -	B	General-purpose I/O port PWC ch.0 input pin Base timer ch.2 TIOA output pin Multi-function serial ch.1 serial chip select 11 output pin
46	P035 SOT0 TIOB2	- - -	B	General-purpose I/O port Multi-function serial ch.0 serial data output pin Base timer ch.2 TIOB input pin
47	P036 SCK0 TIOA3	- - -	E	General-purpose I/O port Multi-function serial ch.0 clock I/O pin Base timer ch.3 TIOA I/O pin
48	P037 SIN0 TIOB3 INT1	- - - -	E	General-purpose I/O port Multi-function serial ch.0 serial data input pin Base timer ch.3 TIOB input pin INT1 external interrupt input pin
49	DEBUGIF	-	F	MDI I/O pin for debug (OCD)
50	P040 MM ICU SCS20	- - - -	B	General-purpose I/O port Clock supervisor main clock stop detection output pin Input capture input pin Multi-function serial ch.2 serial chip select 20 I/O pin
51	MD0	-	G	Mode pin 0
52	MD1	-	G	Mode pin 1
53	X0	-	H	Main clock oscillation input pin
54	X1	-	H	Main clock oscillation output pin

Pin no.	Pin Name	Polarity	I/O circuit types	Function
56	P041 TX	- -	B	General-purpose I/O port CAN transmission data output pin
57	P042 RX INT0	- - -	E	General-purpose I/O port CAN reception data input pin INT0 external interrupt input pin
58	RSTX	N	L	External reset input pin
61	P043 SOT2 TOT4	- - -	B	General-purpose I/O port Multi-function serial ch.2 serial data output pin Reload timer ch.4 output pin
62	P044 SCK2	- -	E	General-purpose I/O port Multi-function serial ch.2 clock I/O pin
63	P045 SIN2 INT3	- - -	E	General-purpose I/O port Multi-function serial ch.2 serial data input pin INT3 external interrupt input pin
16	AVCC2	-	-	Analog power supply pin for comparator and slope compensation circuit
22	AVCC1	-	-	Analog power supply pin for A/D converter, with 4ch. simultaneous sampling/hold function
27	AVCC0	-	-	A/D converter analog power supply pin
26	AVRH1	-	-	Upper limit reference voltage pin for A/D converter, with 4ch. simultaneous sampling/hold function
30	AVRH0	-	-	A/D converter upper limit reference voltage pin
17	AVSS2	-	-	GND pin for comparator and slope compensation circuit
23	AVSS1	-	-	GND pin for A/D converter, with 4ch. simultaneous sampling/hold function
25	AVRL1	-	-	Lower limit reference voltage pin for A/D converter, with 4ch. simultaneous sampling/hold function
24	VR1	-	-	Intermediate reference voltage pin for A/D converter, with 4ch. simultaneous sampling/hold function
28	AVSS0	-	-	A/D converter GND pin
29	AVRL0	-	-	A/D converter lower limit reference voltage pin
60	C	-	-	External capacity connection output pin
8 32 64	VCC	-	-	+5.0 V power supply pin
1 9 33 55 59	VSS	-	-	GND

4. I/O Circuit Type

Type	Circuit	Remarks
A		■ General-purpose I/O port ■ Output 8mA ■ Pull-down resistor control 50kΩ ■ Automotive input
B		■ General-purpose I/O port ■ Output 4mA ■ Pull-up resistor control 50kΩ ■ Automotive input
C		■ Analog input
D		■ Analog input, General-purpose I/O port ■ Output 4mA ■ Pull-up resistor control 50kΩ ■ Automotive input

Type	Circuit	Remarks
E		■ General-purpose I/O port ■ Output 4mA ■ Pull-up resistor control 50kΩ ■ CMOS hysteresis input
F		■ Open-drain I/O ■ Output 25mA (Nch open drain) ■ TTL input
G		■ Mode I/O ■ CMOS hysteresis input
H		■ Main oscillation I/O

Type	Circuit	Remarks
L		■ CMOS hysteresis input ■ Pull-up resistor 50kΩ

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

5.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION:

The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. *Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.*
2. *Be sure that abnormal current flows do not occur during the power-on sequence.*

- Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION:

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

5.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress recommended conditions. For detailed information about mount conditions, contact your sales representative.

- Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

- Lead-Free Packaging

CAUTION:

When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

5.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

CAUTION:

Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

This section explains the latch-up prevention and pin processing.

6.1 For Latch-up Prevention

If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC and VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supply (AVCC, AVRH) and analog input must not be exceed the digital power supply (VCC) when the power supply to the analog system is turned on or off.

In the correct power-on sequence of the microcontroller, turn on the digital power supply (VCC) and analog power supplies (AVCC, AVRH) simultaneously. Or, turn on the digital power supply (VCC), and then turn on analog power supplies (AVCC, AVRH).

6.2 Treatment of Unused Pins

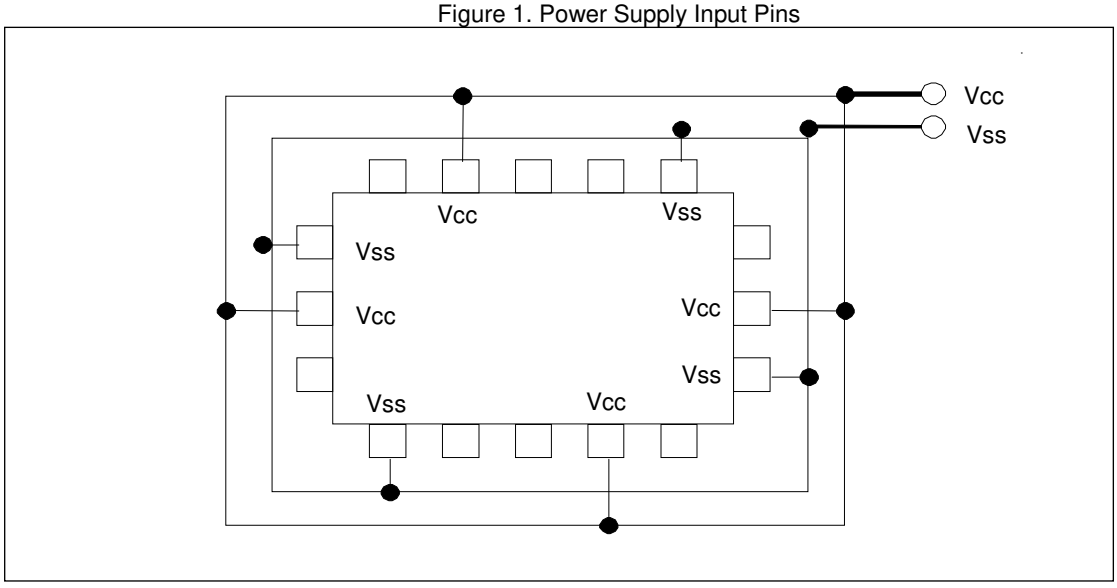
If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect at least a 2kΩ resistor to each of the unused pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

6.3 Power Supply Pins

The device is designed to ensure that if the device contains multiple VCC or VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in figure 1, all Vss power supply pins must be treated in the similar way. If multiple Vcc or Vss systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Figure 1. Power Supply Input Pins



The power supply pins should be connected to VCC and VSS pins of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC and VSS pins.

6.4 Crystal Oscillation Circuit

An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

6.5 Mode Pins (MD1, MD0)

Connect the MD1 and MD0 mode pins to the VCC or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and VCC or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

6.6 During Power-on

To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on.

6.7 Notes during PLL clock Operation

When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self-oscillator circuit built in the PLL clock. This operation is not guaranteed.

6.8 Treatment of A/D Converter Power Supply Pins

Connect the pins to have AVCC=AVRH=VCC and AVSS/AVRL=VSS even if the A/D converter is not used.

6.9 External clock is not Supported

None of the external direct clock input can be used.

6.10 Power-on Sequence of A/D Converter Power Supplies and Analog Inputs

Be sure to turn on the digital power supply (Vcc) first, and then turn on the A/D converter power supplies (AVcc, AVRH, AVRL) and analog inputs (AN0 to AN7, AN8 to AN11). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (Vcc). When the AVRH pin voltage is turned on or off, it must not exceed AVCC. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVcc. (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

6.11 Power-on Sequence of Comparator and Slope Compensation Power Supply and Analog Inputs

Be sure to turn on the digital power supply (Vcc) first, and then turn on the comparator and slope compensation power supply (AVcc) and analog inputs (CMP0 to CMP2). Also, turn off the comparator and slope compensation power supply and analog inputs first, and then turn off the digital power supply (Vcc). (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

6.12 Treatment of C Pin

This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

Note: Please see the latest data sheet for a detailed specification of the operation voltage.

6.13 Function Switching of a Multiplexed Port

To switch between the port function and the multiplexed pin function, use the PFR (port function register). However, if a pin is also used for an external bus, its function is switched by the external bus setting. For details, see "I/O PORTS" in the hardware manual.

6.14 Low-Power Consumption Mode

To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in "Activating the sleep mode, watch mode, or stop mode" or "Activating the watch mode (power-off) or stop mode(power-off)" of " POWER CONSUMPTION CONTROL" in the hardware manual.

Take the following notes when using a monitor debugger.

Do not set a break point for the low-power consumption transition program.

Do not execute an operation step for the low-power consumption transition program.

6.15 Notes when Writing Data in a Register having the Status Flag

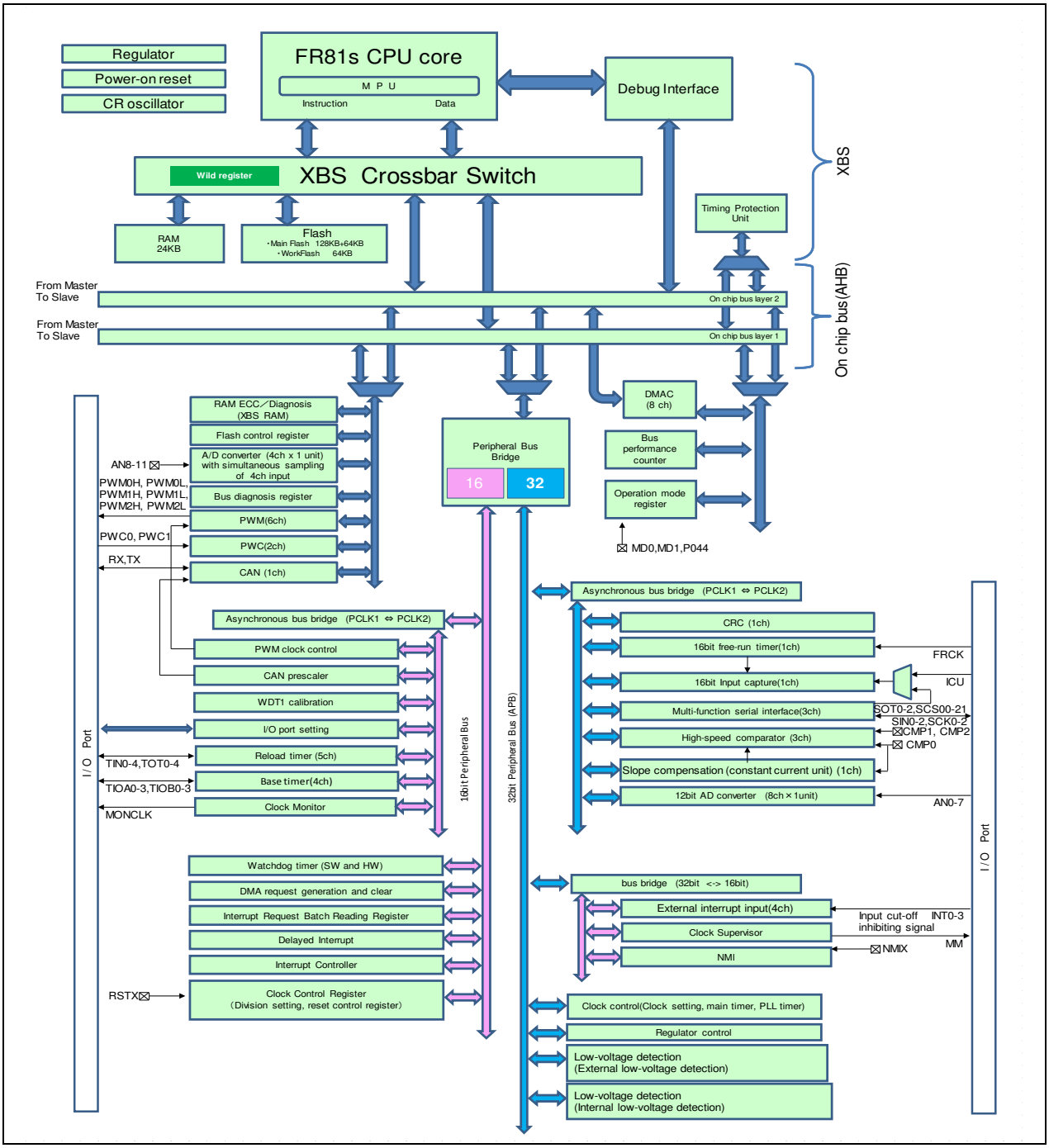
When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

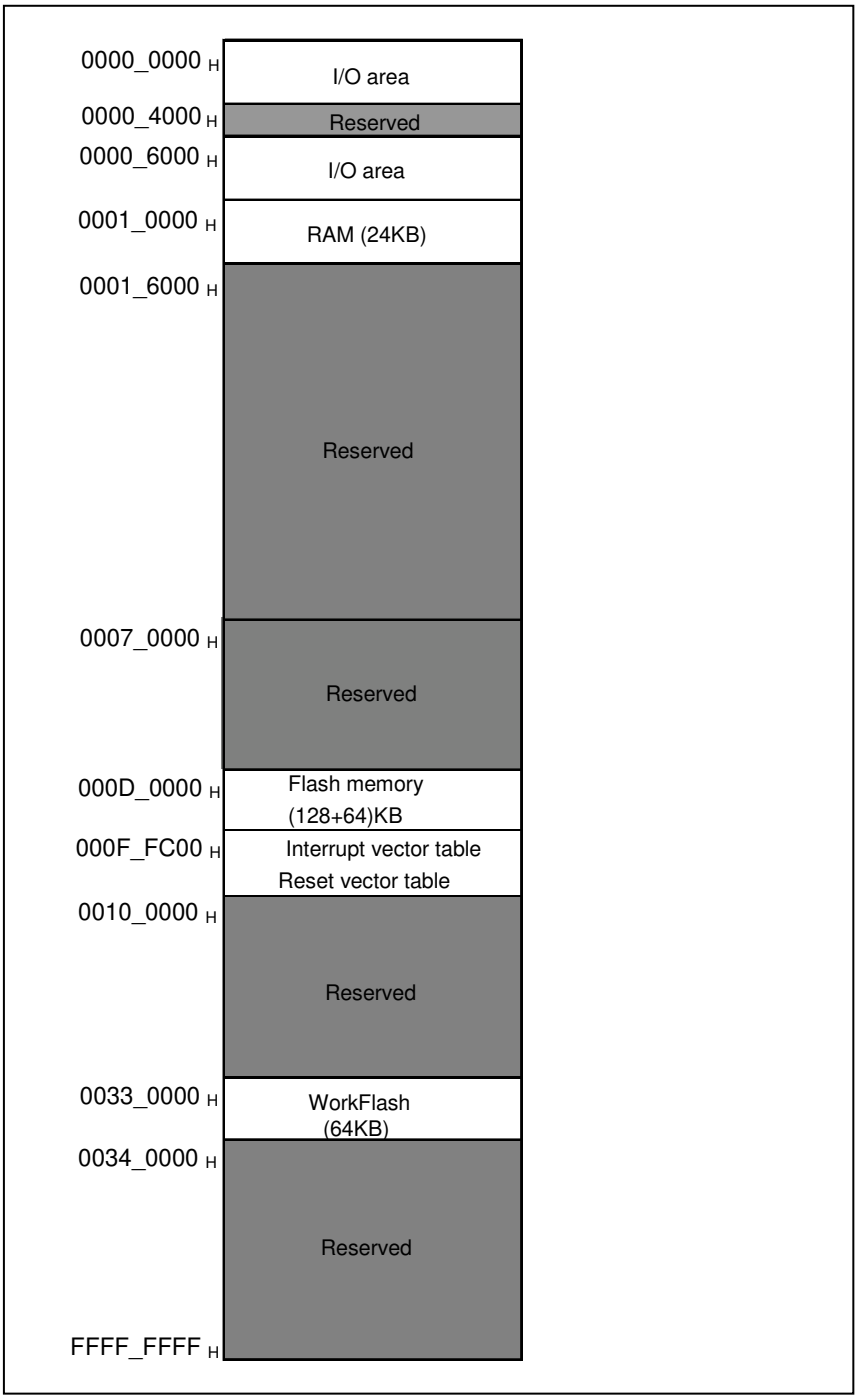
Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

Note: These points can be ignored because the bit instructions are already taken the points into consideration.

7. Block Diagram



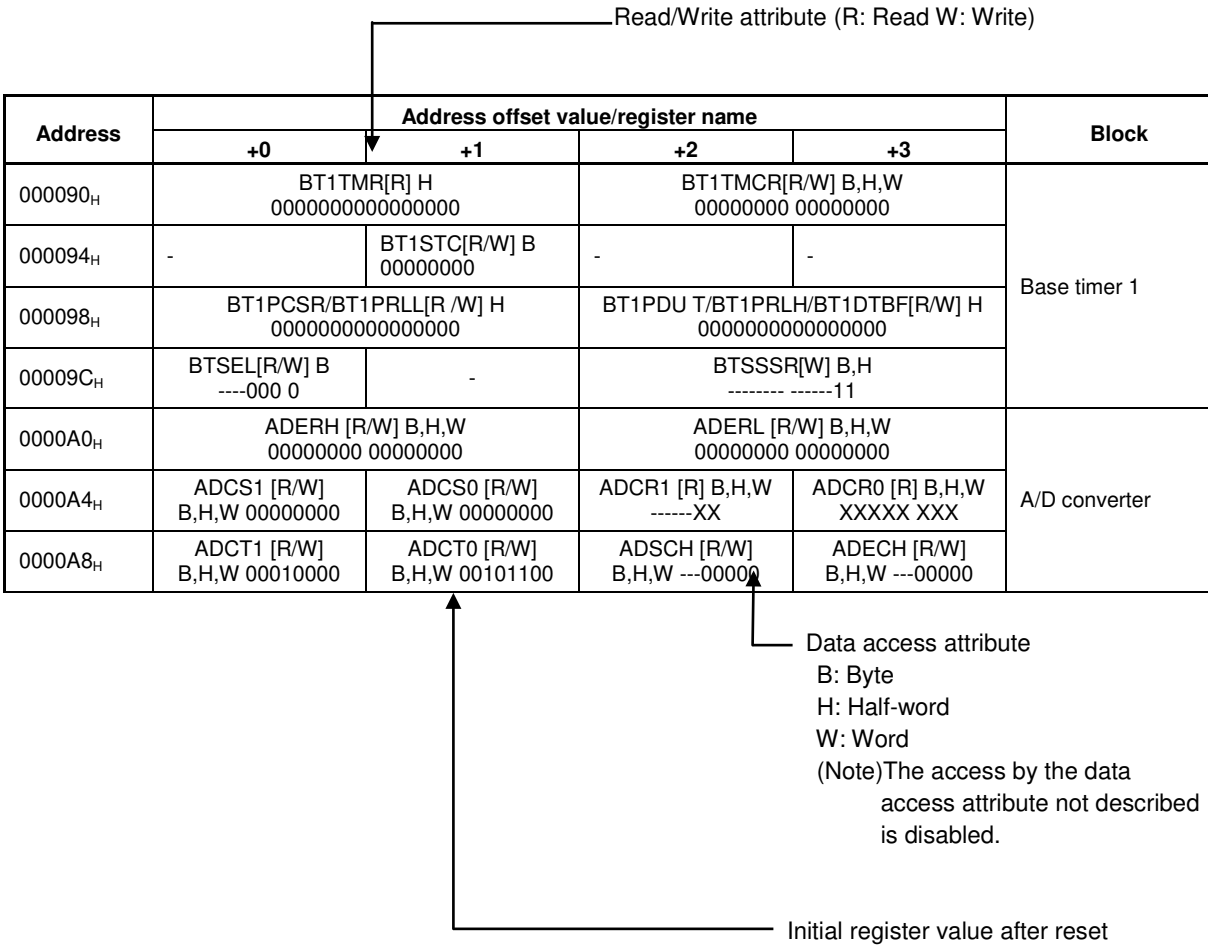
8. Memory Map


0000_0000 H
I/O area
0000_4000 H
Reserved
0000_6000 H
I/O area
0001_0000 H
RAM (24KB)
0001_6000 H
Reserved
0007_0000 H
Reserved
000D_0000 H
Flash memory
(128+64)KB
000F_FC00 H
Interrupt vector table
Reset vector table
0010_0000 H
Reserved
0033_0000 H
WorkFlash
(64KB)
0034_0000 H
Reserved
FFFF_FFFF H

9. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map



Address	Address offset value/register name				Block
	+0	+1	+2	+3	
000090_H	BT1TMR[R] H 0000000000000000		BT1TMCR[R/W] B,H,W 00000000 00000000		Base timer 1
000094_H	-	BT1STC[R/W] B 00000000	-	-	
000098_H	BT1PCSR/BT1PRLL[R /W] H 0000000000000000		BT1PDU T/BT1PRLH/BT1DTBF[R/W] H 0000000000000000		
$00009C_H$	BTSEL[R/W] B ----000 0	-	BTSSSR[W] B,H -------- ------11		
$0000A0_H$	ADERH [R/W] B,H,W 00000000 00000000		ADERL [R/W] B,H,W 00000000 00000000		A/D converter
$0000A4_H$	ADCS1 [R/W] B,H,W 00000000	ADCS0 [R/W] B,H,W 00000000	ADCR1 [R] B,H,W ------XX	ADCR0 [R] B,H,W XXXXX XXX	
$0000A8_H$	ADCT1 [R/W] B,H,W 00010000	ADCT0 [R/W] B,H,W 00101100	ADSCH [R/W] B,H,W ---00000	ADECH [R/W] B,H,W ---00000	

The initial register value after reset indicates as follows:

"1": Initial value "1"

"0": Initial value "0"

"X": Initial value undefined

"-": Reserved bit/Undefined bit

"*": Initial value "0" or "1" according to the setting

Note: The access to addresses not described is disabled.

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
000000_H	PDR00 [R/W] B,H,W --XXXXXX	—	PDR02 [R/W] B,H,W XXXXXXXX	PDR03 [R/W] B,H,W XXXXXXXX	Port Data Register
000004_H	PDR04 [R/W] B,H,W XXXXXXXX	—	—	—	
000008_H to 000034_H	—	—	—	—	Reserved
000038_H	WDTECR0 [R/W] B,H,W ---00000	—	—	—	Watchdog Timer [S]
$00003C_H$	WDTCR0 [R/W] B,H,W -0--0000	WDTCPR0 [W] B,H,W 00000000	WDTCR1 [R] B,H,W ----0110	WDTCPR1 [W] B,H,W 00000000	
000040_H	—	—	—	—	Reserved
000044_H	DICR [R/W] B ---0	—	—	—	Delayed Interrupt
000048_H to $00005C_H$	—	—	—	—	Reserved
000060_H	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		Reload Timer 0
000064_H	TMRLRB0 [R/W] H XXXXXXXX XXXXXXXX		TMCSR0 [R/W] B,H,W 00000000 0-000000		
000068_H to $00007C_H$	—	—	—	—	Reserved
000080_H	BT0TMR [R] H 00000000 00000000		BT0TMCR [R/W] H -000--00 -000-000		Base Timer 0
000084_H	BT0TMCR2 [R/W] B -------0	BT0STC [R/W] B -0-0-0-0	—	—	
000088_H	BT0PCSR/BT0PRLL [R/W] H XXXXXXXX XXXXXXXX		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H XXXXXXXX XXXXXXXX		
$00008C_H$	—	—	—	—	Reserved
000090_H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] H -000--00 -000-000		Base Timer 1
000094_H	BT1TMCR2 [R/W] B ----0	BT1STC [R/W] B -0-0-0-0	—	—	
000098_H	BT1PCSR/BT1PRLL [R/W] H XXXXXXXX XXXXXXXX		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H XXXXXXXX XXXXXXXX		
$00009C_H$	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -------- ------11		Base Timer 0,1

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
0000A0$_H$ to 0000FC$_H$	—	—	—	—	Reserved
000100$_H$	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload Timer 1
000104$_H$	TMRLRB1 [R/W] H XXXXXXXX XXXXXXXX		TMCSR1 [R/W] B, H,W 00000000 0-000000		
000108$_H$	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload Timer 2
00010C$_H$	TMRLRB2 [R/W] H XXXXXXXX XXXXXXXX		TMCSR2 [R/W] B,H,W 00000000 0-000000		
000110$_H$	TMRLRA3 [R/W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload Timer 3
000114$_H$	TMRLRB3 [R/W] H XXXXXXXX XXXXXXXX		TMCSR3 [R/W] B,H,W 00000000 0-000000		
000118$_H$	BT2TMR [R] H 00000000 00000000		BT2TMCR [R/W] H -000--00 -000-000		Base Timer 2
00011C$_H$	BT2TMCR2 [R/W] B -------0	BT2STC [R/W] B -0-0-0-0	—	—	
000120$_H$	BT2PCSR/BT2PRLL [R/W] H XXXXXXXX XXXXXXXX		BT2PDUT/BT2PRLH/BT2DTBF [R/W] H XXXXXXXX XXXXXXXX		
000124$_H$	BT3TMR [R] H 00000000 00000000		BT3TMCR [R/W] H -000--00 -000-000		Base Timer 3
000128$_H$	BT3TMCR2 [R/W] B -------0	BT3STC [R/W] B -0-0-0-0	—	—	
00012C$_H$	BT3PCSR/BT3PRLL [R/W] H XXXXXXXX XXXXXXXX		BT3PDUT/BT3PRLH/BT3DTBF [R/W] H XXXXXXXX XXXXXXXX		
000130$_H$	BTSEL23 [R/W] B ----0000	—	BTSSSRA [W] B,H -------- ------11		Base Timer 2,3
000134$_H$ to 0001B4$_H$	—	—	—	—	Reserved
0001B8$_H$	—	EPFR65 [R/W] B,H,W --000000	—	—	Extended port function register
0001BC$_H$ to 0001C8$_H$	—	—	—	—	Reserved
0001CC$_H$	—	—	EPFR86 [R/W] B,H,W -----0--	—	Extended port function register
0001D0$_H$	EPFR88 [R/W] B,H,W -------0	—	—	—	
0001D4$_H$	—	—	—	—	Reserved
0001D8$_H$	TMRLRA4 [R/W] H XXXXXXXX XXXXXXXX		TMR4 [R] H XXXXXXXX XXXXXXXX		Reload Timer 4
0001DC$_H$	TMRLRB4 [R/W] H XXXXXXXX XXXXXXXX		TMCSR4 [R/W] B,H,W 00000000 0-000000		
0001E0$_H$ to 00030C$_H$	—	—	—	—	Reserved

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
000310_H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only CPU core can access this area)
000314_H	—	—	—	—	
000318_H	—				
$00031C_H$	—	—	—	—	
000320_H	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	—	—	DPVSR [R/W] H -------- 00000--0		
000328_H	DEAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	—	—	DESR [R/W] H -------- 00000--0		
000330_H	PABR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	—	—	PACR0 [R/W] H 000000-0 00000--0		
000338_H	PABR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	—	—	PACR1 [R/W] H 000000-0 00000--0		
000340_H	PABR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344_H	—	—	PACR2 [R/W] H 000000-0 00000--0		
000348_H	PABR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00034C_H$	—	—	PACR3 [R/W] H 000000-0 00000--0		
000350_H	PABR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000354_H	—	—	PACR4 [R/W] H 000000-0 00000--0		
000358H	PABR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	—	—	PACR5 [R/W] H 000000-0 00000--0		
000360_H	PABR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	—	—	PACR6 [R/W] H 000000-0 00000--0		
000368_H	PABR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00036C_H$	—	—	PACR7 [R/W] H 000000-0 00000--0		
000370_H to $0003FC_H$	—	—	—	—	Reserved [S]

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
000400_H	ICSEL0 [R/W] B,H,W -----000	—	ICSEL2 [R/W] B,H,W ------00	ICSEL3 [R/W] B,H,W -------0	DMA request generation and clear
000404_H	—	ICSEL5 [R/W] B,H,W -----000	—	—	
000408_H	—	—	—	ICSEL11 [R/W] B,H,W -----000	
$00040C_H$	—	ICSEL13 [R/W] B,H,W ------00	ICSEL14 [R/W] B,H,W ------00	ICSEL15 [R/W] B,H,W ----0000	
000410_H	ICSEL16 [R/W] B,H,W ------00	ICSEL17 [R/W] B,H,W ----0000	ICSEL18 [R/W] B,H,W ------00	ICSEL19 [R/W] B,H,W -------0	
000414_H	ICSEL20 [R/W] B,H,W -------0	ICSEL21 [R/W] B,H,W ------00	ICSEL22 [R/W] B,H,W ------00	ICSEL23 [R/W] B,H,W ------00	
000418_H	IRPR0H [R] B,H,W 000-----	IRPR0L [R] B,H,W 00------	IRPR1H [R] B,H,W 00------	IRPR1L [R] B,H,W 00------	Interrupt Request Batch Reading Register
$00041C_H$	IRPR2H [R] B,H,W 00------	IRPR2L [R] B,H,W 00------	IRPR3H [R] B,H,W 00------	IRPR3L [R] B,H,W 00------	
000420_H	IRPR4H [R] B,H,W 0000----	IRPR4L [R] B,H,W 0000----	IRPR5H [R] B,H,W 0000----	IRPR5L [R] B,H,W 00------	
000424_H	IRPR6H [R] B,H,W -0------	IRPR6L [R] B,H,W 0-0-----	IRPR7H [R] B,H,W 0000----	IRPR7L [R] B,H,W 00000000	
000428_H	IRPR8H [R] B,H,W 000-----	IRPR8L [R] B,H,W 0000----	IRPR9H [R] B,H,W 00000000	IRPR9L [R] B,H,W 00000000	
$00042C_H$	IRPR10H [R] B,H,W 00000000	IRPR10L [R] B,H,W 00000000	IRPR11H [R] B,H,W 0000----	IRPR11L [R] B,H,W 0000----	
000430_H	IRPR12H [R] B,H,W 00------	IRPR12L [R] B,H,W 00------	IRPR13H [R] B,H,W 00------	IRPR13L [R] B,H,W 00------	
000434_H	IRPR14H [R] B,H,W 00000000	—	IRPR15H [R] B,H,W 0000----	IRPR15L [R] B,H,W -000----	
000438_H	—	ICSEL25 [R/W] B,H,W ---00000	—	—	DMA request generation and clear
$00043C_H$	—	—	—	—	Reserved [S]

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] B,H,W ---11111	ICR01 [R/W] B,H,W ---11111	ICR02 [R/W] B,H,W ---11111	ICR03 [R/W] B,H,W ---11111	Interrupt Controller [S]
000444_H	ICR04 [R/W] B,H,W ---11111	ICR05 [R/W] B,H,W ---11111	ICR06 [R/W] B,H,W ---11111	ICR07 [R/W] B,H,W ---11111	
000448_H	ICR08 [R/W] B,H,W ---11111	ICR09 [R/W] B,H,W ---11111	ICR10 [R/W] B,H,W ---11111	ICR11 [R/W] B,H,W ---11111	
$00044C_H$	ICR12 [R/W] B,H,W ---11111	ICR13 [R/W] B,H,W ---11111	ICR14 [R/W] B,H,W ---11111	ICR15 [R/W] B,H,W ---11111	
000450_H	ICR16 [R/W] B,H,W ---11111	ICR17 [R/W] B,H,W ---11111	ICR18 [R/W] B,H,W ---11111	ICR19 [R/W] B,H,W ---11111	
000454_H	ICR20 [R/W] B,H,W ---11111	ICR21 [R/W] B,H,W ---11111	ICR22 [R/W] B,H,W ---11111	ICR23 [R/W] B,H,W ---11111	
000458_H	ICR24 [R/W] B,H,W ---11111	ICR25 [R/W] B,H,W ---11111	ICR26 [R/W] B,H,W ---11111	ICR27 [R/W] B,H,W ---11111	
$00045C_H$	ICR28 [R/W] B,H,W ---11111	ICR29 [R/W] B,H,W ---11111	ICR30 [R/W] B,H,W ---11111	ICR31 [R/W] B,H,W ---11111	
000460_H	ICR32 [R/W] B,H,W ---11111	ICR33 [R/W] B,H,W ---11111	ICR34 [R/W] B,H,W ---11111	ICR35 [R/W] B,H,W ---11111	
000464_H	ICR36 [R/W] B,H,W ---11111	ICR37 [R/W] B,H,W ---11111	ICR38 [R/W] B,H,W ---11111	ICR39 [R/W] B,H,W ---11111	
000468_H	ICR40 [R/W] B,H,W ---11111	ICR41 [R/W] B,H,W ---11111	ICR42 [R/W] B,H,W ---11111	ICR43 [R/W] B,H,W ---11111	
$00046C_H$	ICR44 [R/W] B,H,W ---11111	ICR45 [R/W] B,H,W ---11111	ICR46 [R/W] B,H,W ---11111	ICR47 [R/W] B,H,W ---11111	
000470_H to $00047C_H$	—	—	—	—	Reserved[S]
000480_H	RSTRR [R] B,H,W XXXX--XX	RSTCR [R/W] B,H,W 111----0	STBCR [R/W] B,H,W * 000---11	—	Reset Control [S] Power Control [S] *: Writing STBCR by DMA is forbidden
000484_H	—	—	—	—	Reserved [S]
000488_H	DIVR0 [R/W] B,H,W 000-----	—	DIVR2 [R/W] B,H,W 0011----	—	Clock Control [S]
$00048C_H$	—	—	—	—	Reserved [S]

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
000490_H	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	DMA request by peripheral[S]
000494_H	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
000498_H	—	—	—	—	
$00049C_H$	—	—	—	—	
$0004A0_H$	—	—	—	—	Reserved
$0004A4_H$	CANPRE [R/W] B,H,W ---00000	—	—	—	CAN prescaler
$0004A8_H$	—	—	CSCFG[R/W]B,H,W ---0----	CMCFG[R/W]B,H,W 00000000	Clock monitor control register
$0004AC_H$	—	—	ADERL0[R/W] B,H -------- 11111111		Analog input control register
$0004B0_H$ to $0004C0_H$	—	—	—	—	Reserved
$0004C4_H$	CUCR1 [R/W] B,H,W -------- ---0--00		CUTD1 [R/W] B,H,W 11000011 01010000		WDT1 calibration
$0004C8_H$	CUTR1 [R] B,H,W -------- 00000000 00000000 00000000				
$0004CC_H$ to $0004E4_H$	—	—	—	—	Reserved
$0004E8_H$	PLL2DIVM [R/W] B,H,W ----0000	PLL2DIVN [R/W] B,H,W -0000000	—	—	PWM Clock control
$0004EC_H$	—	PLL2DIVK [R/W] B,H,W -------0	CLKR2 [R/W] B,H,W 000--000	—	
$0004F0_H$	—	PWMCGRCR0 [R/W] B,H,W 00----00	PWMCGRCR1 [R/W] B,H,W 00000000	PWMCGRCR2 [R/W] B,H,W 00000000	
$0004F4_H$ to $00050C_H$	—	—	—	—	Reserved
000510_H	CSELR [R/W] B,H,W -01---00	CMONR [R] B,H,W -01---00	MTMCR [R/W] B,H,W 00001111	—	Clock Control[S]
000514_H	PLLCR [R/W] B,H,W -------- 11110000		CSTBR [R/W] B,H,W ----0000	PTMCR [R/W] B,H,W 00------	
000518_H	—	—	CPUAR [R/W] B,H,W 0----XXX	—	Reset clock[S]
$00051C_H$	—	—	—	—	Reserved[S]

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
000520_H	CCPSSELR [R/W] B,H,W -------0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock Control 2[S]
000524_H	—	CCPLLFBR [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000	
000528_H	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1 [R/W] H,W 000----- --------		
$00052C_H$	—	CCCGRCR0 [R/W] B,H,W 00----00	CCCGRCR1 [R/W] B,H,W 00000000	CCCGRCR2 [R/W] B,H,W 00000000	
000530_H to $00053C_H$	—	—	—	—	
000540_H to $00054C_H$	—	—	—	—	Reserved
000550_H	EIRR0 [R/W] B,H,W ----XXXX	ENIR0 [R/W] B,H,W ----0000	ELVR0 [R/W] B,H,W -------- 00000000		External Interrupt (INT0 to 3)
000554_H to 000568_H	—	—	—	—	Reserved
$00056C_H$	—	CSVCR [R/W] B -0-11--0	—	—	Clock Supervisor
000570_H to $00057C_H$	—	—	—	—	Reserved
000580_H	REGSEL [R/W] B,H,W 01------	—	—	—	Regulator Control / Low Voltage Detection
000584_H	LVD5R [R/W] B,H,W -------1	LVD5F [R/W] B,H,W 00110001	LVD [R/W] B,H,W 01000--0	—	
000588_H to $00059C_H$	—	—	—	—	Reserved

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
$0005A0_H$	SLPCNT [R/W] B,H,W ------00	—	—	—	Slope Compensation Control
$0005A4_H$	SLPEDGESEL1 [R/W] B,H,W ---0-000 ---0-000		SLPEDGESEL2 [R/W] B,H,W ---0-000 ---0-000		
$0005A8_H$	SLPSWA [R/W] B,H,W -----100	SLPSWB [R/W] B,H,W -----100	SLPSWC [R/W] B,H,W -----100	—	
$0005AC_H$	SLP1A [R/W] H,W 00000000 00000000		SLP1B [R/W] H,W 00000000 00000000		
$0005B0_H$	SLP1C [R/W] H,W 00000000 00000000		SLP3 [R/W] H,W 00000000 00000000		
$0005B4_H$	SLP2A [R/W] H,W 00000000 00000000		SLP2B [R/W] H,W 00000000 00000000		
$0005B8_H$	SLP2C [R/W] H,W 00000000 00000000		SLP4 [R/W] H,W 00000000 00000000		
$0005BC_H$	—	—	SLPDADR [R/W] H,W ------00 00000000		
$0005C0_H$	SLPSTMSEL1 [R/W] B,H,W -000-000 -----000		SLPSTMSEL2 [R/W] B,H,W -000-000 --------		
$0005C4_H$	SLPCVE [R] H,W ------XX XXXXXXXX		—	—	
$0005C8_H$ to $0005DC_H$	—	—	—	—	Reserved
$0005E0_H$	CMPCTL0 [R/W] B,H,W --001000	CMPCTL1 [R/W] B,H,W --001000	CMPCTL2 [R/W] B,H,W --001000	CMPDIV [R/W] B,H,W ------00	Comparator Control
$0005E4_H$	CMPDACR0 [R/W] B,H,W -------0	—	CMPDADR0 [R/W] H,W ------00 00000000		
$0005E8_H$	CMPDACR1 [R/W] B,H,W -------0	—	CMPDADR1 [R/W] H,W ------00 00000000		
$0005EC_H$	CMPDACR2 [R/W] B,H,W -------0	—	CMPDADR2 [R/W] H,W ------00 00000000		
$0005F0_H$	CMPINT [R/W] B,H,W -----000	—	—	—	
$0005F4_H$	CMPST [R] B,H,W -----XXX	—	—	—	
$0005F8_H$ to $0005FC_H$	—	—	—	—	Reserved

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
000600_H to $0006FC_H$	—	—	—	—	Reserved[S]
000700_H to $00070C_H$	—	—	—	—	Reserved
000710_H	BPCCRA [R/W] B 00000000	BPCCRB [R/W] B 00000000	BPCCRC [R/W] B 00000000	—	Bus Performance Counter
000714_H	BPCTRA [R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB [R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC [R/W] W 00000000 00000000 00000000 00000000				
000720_H to $0007F8_H$	—	—	—	—	Reserved
$0007FC_H$	BMODR [R] B, H, W XXXXXXXX	—	—	—	Operation Mode
000800_H to $00083C_H$	—	—	—	—	Reserved[S]
000840_H	FCTLR [R/W] H -0--1000 0--0----		—	FSTR [R/W] B -----001	Flash Memory Register [S]
000844_H to 000854_H	—	—	—	—	Reserved[S]
000858_H	—	—	WREN [R/W] H 00000000 00000000		Wild Register [S]
$00085C_H$ to $00087C_H$	—	—	—	—	Reserved[S]
000880_H	WRAR00 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
000884_H	WRDR00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888_H	WRAR01 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00088C_H$	WRDR01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890_H	WRAR02 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
000894_H	WRDR02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898_H	WRAR03 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
00089C$_H$	WRDR03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild Register [S]
0008A0$_H$	WRAR04 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008A4$_H$	WRDR04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008A8$_H$	WRAR05 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008AC$_H$	WRDR05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B0$_H$	WRAR06 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008B4$_H$	WRDR06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B8$_H$	WRAR07 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008BC$_H$	WRDR07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C0$_H$	WRAR08 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008C4$_H$	WRDR08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C8$_H$	WRAR09 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008CC$_H$	WRDR09 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D0$_H$	WRAR10 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008D4$_H$	WRDR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D8$_H$	WRAR11 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008DC$_H$	WRDR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E0$_H$	WRAR12 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008E4$_H$	WRDR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
$0008E8_H$	WRAR13 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
$0008EC_H$	WRDR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F0_H$	WRAR14 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008F4_H$	WRDR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F8_H$	WRAR15 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008FC_H$	WRDR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000900_H	TPUUNLOCK [R/W] W 00000000 00000000 00000000 00000000				Time Protection Unit[S]
000904_H	TPULST [R] B,H,W -------0	—	TPUVST [R/W] B,H,W -----000	—	
000908_H	TPUCFG [R/W] B,H,W -------0 0-000000 -------- -------0				
$00090C_H$	TPUTIR [R] B,H,W 00000000	—	—	—	
000910_H	TPUTST [R] B,H,W 00000000	—	—	—	
000914_H	TPUTIE [R/W] B,H,W 00000000	—	—	—	
000918_H	TPUTMID [R] B,H,W 00000000 00000000 00000000 00000000				
$00091C_H$ to $00092C_H$	—	—	—	—	
000930_H	TPUTCN00 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000934_H	TPUTCN01 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000938_H	TPUTCN02 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
$00093C_H$	TPUTCN03 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000940_H	TPUTCN04 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000944_H	TPUTCN05 [R/W] B,H,W 000000-- 00000000 00000000 00000000				

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
000948_H	TPUTCN06 [R/W] B,H,W 000000-- 00000000 00000000 00000000				Time Protection Unit[S]
$00094C_H$	TPUTCN07 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000950_H	TPUTCN10 [R/W] B,H,W ---00000	—	—	—	
000954_H	TPUTCN11 [R/W] B,H,W ---00000	—	—	—	
000958_H	TPUTCN12 [R/W] B,H,W ---00000	—	—	—	
$00095C_H$	TPUTCN13 [R/W] B,H,W ---00000	—	—	—	
000960_H	TPUTCN14 [R/W] B,H,W ---00000	—	—	—	
000964_H	TPUTCN15 [R/W] B,H,W ---00000	—	—	—	
000968_H	TPUTCN16 [R/W] B,H,W ---00000	—	—	—	
$00096C_H$	TPUTCN17 [R/W] B,H,W ---00000	—	—	—	
000970_H	TPUTCC0 [R] B,H,W -------- 00000000 00000000 00000000				
000974_H	TPUTCC1 [R] B,H,W -------- 00000000 00000000 00000000				
000978_H	TPUTCC2 [R] B,H,W -------- 00000000 00000000 00000000				
$00097C_H$	TPUTCC3 [R] B,H,W -------- 00000000 00000000 00000000				
000980_H	TPUTCC4 [R] B,H,W -------- 00000000 00000000 00000000				
000984_H	TPUTCC5 [R] B,H,W -------- 00000000 00000000 00000000				
000988_H	TPUTCC6 [R] B,H,W -------- 00000000 00000000 00000000				
$00098C_H$	TPUTCC7 [R] B,H,W -------- 00000000 00000000 00000000				
000990_H to $0009FC_H$	—	—	—	—	
$000A00_H$ to $000BEC_H$	—	—	—	—	Reserved

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
$000BF0_H$	HSCFR [R/W] B,H,W -------- ------00 00000000 00000000				OCDU
$000BF4_H$	—	—	—	—	
$000BF8_H$	—	—	MBR [R/W] B,H,W 00------ XXXXXXXX		OCDU
$000BFC_H$	—	—	UER [W] B,H,W -------- -------X		
$000C00_H$	DCCR0 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller[S]
$000C04_H$	DCSR0 [R/W] H 0------- -----000		DTCR0 [R/W] H 00000000 00000000		
$000C08_H$	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C0C_H$	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C10_H$	DCCR1 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C14_H$	DCSR1 [R/W] H 0------- -----000		DTCR1 [R/W] H 00000000 00000000		
$000C18_H$	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C1C_H$	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C20_H$	DCCR2 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C24_H$	DCSR2 [R/W] H 0------- -----000		DTCR2 [R/W] H 00000000 00000000		
$000C28_H$	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C2C_H$	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C30_H$	DCCR3 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C34_H$	DCSR3 [R/W] H 0------- -----000		DTCR3 [R/W] H 00000000 00000000		
$000C38_H$	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C3C_H$	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
$000C40_H$	DCCR4 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller[S]
$000C44_H$	DCSR4 [R/W] H 0------- -----000		DTCR4 [R/W] H 00000000 00000000		
$000C48_H$	DSAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C4C_H$	DDAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C50_H$	DCCR5 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C54_H$	DCSR5 [R/W] H 0------- -----000		DTCR5 [R/W] H 00000000 00000000		
$000C58_H$	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C5C_H$	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C60_H$	DCCR6 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C64_H$	DCSR6 [R/W] H 0------- -----000		DTCR6 [R/W] H 00000000 00000000		
$000C68_H$	DSAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C6C_H$	DDAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C70_H$	DCCR7 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C74_H$	DCSR7 [R/W] H 0------- -----000		DTCR7 [R/W] H 00000000 00000000		
$000C78_H$	DSAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C7C_H$	DDAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C80_H$ to $000DF0_H$	—	—	—	—	Reserved[S]
$000DF4_H$	—	—	DNMIR [R/W] B 0------0	DILVR [R/W] B ---11111	DMA Controller[S]
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	—	—	—	—	Reserved[S]

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
$000E00_H$	—	—	DDR02 [R/W] B,H,W 00000000	DDR03 [R/W] B,H,W 00000000	Data Direction Register
$000E04_H$	DDR04 [R/W] B,H,W 00000000	—	—	—	
$000E08_H$ to $000E1C_H$	—	—	—	—	Reserved
$000E20_H$	PFR00 [R/W] B,H,W --000000	—	PFR02 [R/W] B,H,W 00000000	PFR03 [R/W] B,H,W 00000000	Port Function Register
$000E24_H$	PFR04 [R/W] B,H,W 00000000	—	—	—	
$000E28_H$ to $000E3C_H$	—	—	—	—	Reserved
$000E40_H$	PDDR00 [R] B,H,W --XXXXXX	—	PDDR02 [R] B,H,W XXXXXXXX	PDDR03 [R] B,H,W XXXXXXXX	Port Direct Read Register
$000E44_H$	PDDR04 [R] B,H,W XXXXXXXX	—	—	—	
$000E48_H$to $000E5C_H$	—	—	—	—	Reserved
$000E60_H$	—	—	EPFR02 [R/W] B,H,W ---00000	—	Extended Port Function Register
$000E64_H$ to $000E68_H$	—	—	—	—	
$000E70_H$	EPFR16 [R/W] B,H,W -------0	—	—	—	
$000E74_H$	—	—	—	—	
$000E78_H$	—	—	EPFR26 [R/W] B,H,W -0-0-0-0	—	
$000E7C_H$	—	—	—	—	
$000E80_H$	—	—	—	EPFR35 [R/W] B,H,W --000000	
$000E84_H$ to $000EBC_H$	—	—	—	—	Reserved
$000EC0_H$	PPER00 [R/W] B,H,W --000000	—	PPER02 [R/W] B,H,W 00000000	PPER03 [R/W] B,H,W 00000000	Port Pull-up/down Enable Register
$000EC4_H$	PPER04 [R/W] B,H,W 00000000	—	—	—	
$000EC8_H$ to $000F3C_H$	—	—	—	—	Reserved

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
$000F40_H$	PORTEN [R/W] B,H,W -------0	—	—	—	Port Enable Register
$000F44_H$	KEYCDR [R/W] H 00000000 00000000		—	—	Key Code Register
$000F48_H$ to $000FFC_H$	—	—	—	—	Reserved
001000_H	SACR [R/W] B,H,W -------0	PICD [R/W] B,H,W ----0011	—	—	Clock Control
001004_H to $00112C_H$	—	—	—	—	Reserved
001130_H	—	—	—	CRCCR [R/W] B,H,W -0000000	CRC calculation unit
001134_H	CRCINIT [R/W] B,H,W 11111111 11111111 11111111 11111111				
001138_H	CRCIN [R/W] B,H,W 00000000 00000000 00000000 00000000				
$00113C_H$	CRCR [R] B,H,W 11111111 11111111 11111111 11111111				
001140_H to 001200_H	—	—	—	—	Reserved
001204_H	CPCLRB0/CPCLR0 [W] H,W 11111111 11111111		TCDT0 [R/W] H,W 00000000 00000000		Free-run Timer 0 (16bit)
001208_H	TCCS0 [R/W] B,H,W 00000000 01000000 ----0000 --------				
$00120C_H$ to 001278_H	—	—	—	—	Reserved
$00127C_H$	IPCP0 [R] H,W 00000000 00000000		—	—	Input Capture 0 (16bit)
001280_H	ICS01 [R/W] B,H,W -------0 -0-0--00		—	LSYNS [R/W] B,H,W -----000	
001284_H to 001300_H	—	—	—	—	Reserved

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
001304$_H$	ADTSS0[R/W]B,H ,W-------0	—	—	—	12 bit A/D converter
001308$_H$	ADTSE0[R/W] B,H,W -------- -------- -------- 00000000				
00130C$_H$	—		—		
001310$_H$	—		—		
001314$_H$	—		—		
001318$_H$	—		—		
00131C$_H$ to 001348$_H$	—	—	—	—	
00134C$_H$	ADTCS0[R/W] B,H,W 00000000 --------		ADTCS1[R/W] B,H,W 00000000 --------		
001350$_H$	ADTCS2[R/W] B,H,W 00000000 --------		ADTCS3[R/W] B,H,W 00000000 --------		
001354$_H$	ADTCS4[R/W] B,H,W 00000000 --------		ADTCS5[R/W] B,H,W 00000000 --------		
001358$_H$	ADTCS6[R/W] B,H,W 00000000 --------		ADTCS7[R/W] B,H,W 00000000 --------		
00135C$_H$ to 001388$_H$	—	—	—	—	
00138C$_H$	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001390$_H$	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		
001394$_H$	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		
001398$_H$	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
00139C$_H$ to 0013C8$_H$	—	—	—	—	
0013CC$_H$	ADTECS0[R/W] B,H,W -------0 ---00000		ADTECS1[R/W] B,H,W -------0 ---00000		
0013D0$_H$	ADTECS2[R/W] B,H,W -------0 ---00000		ADTECS3[R/W] B,H,W -------0 ---00000		
0013D4$_H$	ADTECS4[R/W] B,H,W -------0 ---00000		ADTECS5[R/W] B,H,W -------0 ---00000		
0013D8$_H$	ADTECS6[R/W] B,H,W -------0 ---00000		ADTECS7[R/W] B,H,W -------0 ---00000		
0013DC$_H$ to 001454$_H$	—	—	—	—	
001458$_H$	ADPRTF0[R] B,H,W -------- -------- -------- 00000000				
00145C$_H$	—				
001460$_H$	ADCS0[R] B,H,W 0------- --------		ADCH0[R] B,H,W ---00000	ADMD0[R/W] B,H,W 0---0000	
001464$_H$	ADSTPCS0[R/W] B,H,W 00000000	ADSTPCS1[R/W] B,H,W 00000000	—	—	
001468$_H$	—	—	—	—	
00146C$_H$	EADTCS0 [R/W] B,H,W ----0000	EADTCS1 [R/W] B,H,W ----0000	EADTCS2 [R/W] B,H,W ----0000	EADTCS3 [R/W] B,H,W ----0000	
001470$_H$	EADTCS4 [R/W] B,H,W ----0000	EADTCS5 [R/W] B,H,W ----0000	EADTCS6 [R/W] B,H,W ----0000	EADTCS7 [R/W] B,H,W ----0000	

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
001474_H to $00174C_H$	—	—	—	—	Reserved
001750_H	SCR0[R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0[R/W] B,H,W 00000000	Multi-UART0 [1]: Byte access is possible only for access to lower 8 bits. [2]: Reserved because CSIO mode is not set immediately after reset. [3]: Reserved because LIN2.1 mode is not set immediately after reset. [4]: Byte access in CSIO mode is prohibited.
001754_H	— /(RDR10/(TDR10))[R/W] H,W -------- --------[2]		RDR00/(TDR00)[R/W] B,H,W[4] -------0 00000000[1]		
001758_H	SACSR0[R/W] B,H,W 00-----0 0--00000		STMR0[R] B,H,W 00000000 00000000		
$00175C_H$	STMCR0[R/W] B,H,W 00000000 00000000		— /(SCSCR0/SFUR0)[R/W] B,H,W -------- --------[2] [3]		
001760_H	— /(SCSTR30)/ (LAMSR0) [R/W] B,H,W--------[2]	— /(SCSTR20)/ (LAMCR0) [R/W] B,H,W--------[2]	— /(SCSTR10) /(SFLR10) [R/W] B,H,W--------[2]	— /(SCSTR00)/ (SFLR00) [R/W] B,H,W--------[2]	
001764_H	—	—	—	— /(SCSFR00) [R/W] B,H,W--------[2]	
001768_H	—/(LAMESR0) [R/W] B,H,W --------[2]	—/(LAMERT0) [R/W] B,H,W --------[2]	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W --------[2]	TBYTE00/(LAMRID0)/ (LAMTID0) [R/W] B,H,W 00000000	
$00176C_H$	BGR0[R/W] H, W 00000000 00000000		—	—	
001770_H	FCR10[R/W] B,H,W ---00100	FCR00[R/W] B,H,W -0000000	FBYTE0[R/W] B,H,W 00000000 00000000		
001774_H	FTICR0[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset Value/Register name				Blocks
	+0	+1	+2	+3	
001778_H	SCR1[R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000-00-0	SSR1[R/W] B,H,W 0-000011	ESCR1[R/W] B,H,W 00000000	Multi-UART1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because CSIO mode is not set immediately after reset. [3]: Reserved because LIN2.1 mode is not set immediately after reset. [4]: Byte access in CSIO mode is prohibited.
$00177C_H$	— /(RDR11/(TDR11))[R/W] H,W -------- --------[2]		RDR01/(TDR01)[R/W] B,H,W [4] -------0 00000000[1]		
001780_H	SACSR1[R/W] B,H,W 00-----0 0--00000		STMR1[R] B,H,W 00000000 00000000		
001784_H	STMCR1[R/W] B,H,W 00000000 00000000		— /(SCSCR1/SFUR1)[R/W] B,H,W -------- -------- [2] [3]		
001788_H	— /(SCSTR31)/ (LAMSR1) [R/W] B,H,W --------[2]	— /(SCSTR21)/ (LAMCR1) [R/W] B,H,W --------[2]	— /(SCSTR11)/ (SFLR11) [R/W] B,H,W --------[2]	— /(SCSTR01)/ (SFLR01) [R/W] B,H,W --------[2]	
$00178C_H$	—	—	—	— /(SCSFR01) [R/W] B,H,W --------[2]	
001790_H	—/(LAMESR1) [R/W] B,H,W --------[2]	—/(LAMERT1) [R/W] B,H,W --------[2]	—/(TBYTE11)/ (LAMIER1) [R/W] B,H,W --------[2]	TBYTE01/(LAMRID1)/ (LAMTID1) [R/W] B,H,W 00000000	
001794_H	BGR1[R/W] H,W 00000000 00000000		—	—	
001798_H	FCR11[R/W] B,H,W ---00100	FCR01[R/W] B,H,W -0000000	FBYTE1[R/W] B,H,W 00000000 00000000		
$00179C_H$	FTICR1[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset Value/Register name				Blocks
	+0	+1	+2	+3	
0017A0$_H$	SCR2[R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000-00-0	SSR2[R/W] B,H,W 0-000011	ESCR2[R/W] B,H,W 00000000	Multi-UART2 [1]: Byte access is possible only for access to lower 8 bits. [2]: Reserved because CSIO mode is not set immediately after reset. [3]: Reserved because LIN2.1 mode is not set immediately after reset. [4]: Byte access in CSIO mode is prohibited.
0017A0$_H$	SCR2[R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000-00-0	SSR2[R/W] B,H,W 0-000011	ESCR2[R/W] B,H,W 00000000	
0017A4$_H$	— /(RDR12/(TDR12))[R/W] H,W -------- -------- [2]		RDR02/(TDR02)[R/W] B,H,W[4] -------0 00000000[1]		
0017A8$_H$	SACSR2[R/W] B,H,W 00-----0 0--00000		STMR2[R] B,H,W 00000000 00000000		
0017AC$_H$	STMCR2[R/W] B,H,W 00000000 00000000		— /(SCSCR2/SFUR2)[R/W] B,H,W -------- -------- [2] [3]		
0017B0$_H$	— /(SCSTR32)/ (LAMSR2) [R/W] B,H,W -------- [2]	— /(SCSTR22)/ (LAMCR2) [R/W] B,H,W -------- [2]	— /(SCSTR12)/ (SFLR12) [R/W] B,H,W -------- [2]	— /(SCSTR02)/ (SFLR02) [R/W] B,H,W -------- [2]	
0017B4$_H$	—	—	—	— /(SCSFR02) [R/W] B,H,W -------- [2]	
0017B8$_H$	—/(LAMESR2) [R/W] B,H,W --------[2]	—/(LAMERT2) [R/W] B,H,W --------[2]	—/(TBYTE12)/ (LAMIER2) [R/W] B,H,W --------[2]	TBYTE02/(LAMRID2)/ (LAMTID2) [R/W] B,H,W 00000000	
0017BC$_H$	BGR2[R/W] H, W 00000000 00000000		—	—	
0017C0$_H$	FCR12[R/W] B,H,W ---00100	FCR02[R/W] B,H,W -0000000	FBYTE2[R/W] B,H,W 00000000 00000000		
0017C4$_H$	FTICR2[R/W] B,H,W 00000000 00000000		—	—	
0017C8$_H$ to 0020FC$_H$	—	—	—	—	Reserved

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
002100_H	CTRLR1 [R/W] B,H,W -------- 000-0001		STATR1 [R/W] B,H,W -------- 00000000		CAN (64msb)
002104_H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001		
002108_H	INTR1 [R] H,W 00000000 00000000		TESTR1 [R/W] B,H,W -------- X00000--		
$00210C_H$	BRPER1 [R/W] B,H,W -------- ----0000		—	—	
002110_H	IF1CREQ1 [R/W] B,H,W 0------- 00000001		IF1CMSK1 [R/W] B,H,W -------- 00000000		
002114_H	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118_H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
$00211C_H$	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002120_H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124_H	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128_H	—	—	—	—	
$00212C_H$	—	—	—	—	
002130_H, 002134_H	Reserved (IF1 data mirror)				
002138_H	—	—	—	—	
$00213C_H$	—	—	—	—	
002140_H	IF2CREQ1 [R/W] B,H,W 0------- 00000001		IF2CMSK1 [R/W] B,H,W -------- 00000000		
002144_H	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148_H	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
$00214C_H$	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002150_H	IF2DTA11 [R/W] B,H,W 00000000 00000000		IF2DTA21 [R/W] B,H,W 00000000 00000000		

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
002154_H	IF2DTB11 [R/W] B,H,W 00000000 00000000		IF2DTB21 [R/W] B,H,W 00000000 00000000		CAN (64msb)
002158_H	—	—	—	—	
$00215C_H$	—	—	—	—	
002160_H, 002164_H	Reserved (IF2 data mirror)				
002168_H To $00217C_H$	—				
002180_H	TREQR21 [R] B,H,W 00000000 00000000		TREQR11 [R] B,H,W 00000000 00000000		
002184_H	TREQR41 [R] B,H,W 00000000 00000000		TREQR31 [R] B,H,W 00000000 00000000		
002188_H	—	—	—	—	
$00218C_H$	—	—	—	—	
002190_H	NEWDT21 [R] B,H,W 00000000 00000000		NEWDT11 [R] B,H,W 00000000 00000000		
002194_H	NEWDT41 [R] B,H,W 00000000 00000000		NEWDT31 [R] B,H,W 00000000 00000000		
002198_H	—	—	—	—	
$00219C_H$	—	—	—	—	
$0021A0_H$	INTPND21 [R] B,H,W 00000000 00000000		INTPND11 [R] B,H,W 00000000 00000000		
$0021A4_H$	INTPND41 [R] B,H,W 00000000 00000000		INTPND31 [R] B,H,W 00000000 00000000		
$0021A8_H$	—	—	—	—	
$0021AC_H$	—	—	—	—	
$0021B0_H$	MSGVAL21 [R] B,H,W 00000000 00000000		MSGVAL11 [R] B,H,W 00000000 00000000		
$0021B4_H$	MSGVAL41 [R] B,H,W 00000000 00000000		MSGVAL31 [R] B,H,W 00000000 00000000		
$0021B8_H$	—	—	—	—	
$0021BC_H$	—	—	—	—	
$0021C0_H$ to $0022FC_H$	—				Reserved

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
002300_H	DFCTLR [R/W] B,H,W -0------ --------		—	DFSTR [R/W] B,H,W -----001	WorkFlash
002304_H	—	—	—	—	
002308_H	FLIFCTLR [R/W] B,H,W ---0--00	—	FLIFFER1 [R/W] B,H,W --------	FLIFFER2 [R/W] B,H,W --------	Flash / WorkFlash
$00230C_H$ to $0023FC_H$	—				Reserved
002400_H	SEEARX [R] B,H,W -0000000 00000000		DEEARX [R] B,H,W -0000000 00000000		XBS RAM ECC control
002404_H	EECSRX [R/W] B,H,W ----00-0	—	EFEARX [R/W] B,H,W -0000000 00000000		
002408_H	—	EFECRX [R/W] B,H,W -------0 00000000 00000000			
$00240C_H$ to 003008_H	—				Reserved
$00300C_H$	TEAR0X[R] B,H,W 000----- -------- -0000000 00000000				RAM diagnosis XBS RAM
003010_H	TEAR1X[R] B,H,W 000----- -------- -0000000 00000000				
003014_H	TEAR2X[R] B,H,W 000----- -------- -0000000 00000000				
003018_H	TAEARX [R/W] B,H,W -1111111 11111111		TASARX [R/W] B,H,W -0000000 00000000		
$00301C_H$	TFECRX [R/W] B,H,W ----0000	TICRX [R/W] B,H,W ----0000	TTCRX [R/W] B,H,W ------00 00001100		
003020_H	TSRCRX [W] B,H,W 0-------	—	—	TKCCRX [R/W] B,H,W 00----00	
$003024_H$to $0030FC_H$	—				Reserved

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		Bus diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0 [R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1 [R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2 [R] W 00000000 00000000 00000000 00000000				
003114_H	—	—	BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--000- 00000000		
$00311C_H$	—	—	—	—	
003120_H	BUSADR3 [R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4 [R] W 00000000 00000000 00000000 00000000				
003128_H to $00313C_H$	—				Reserved
003140_H	PWCINIT0 [R/W] B,H,W -------0	PWCC0 [R/W] B,H,W ---00000	—	—	PWC 0ch
003144_H	PWCCPCLRB00/PWCCPCLR00 [W] H,W 11111111 11111111		PWCTCDT00 [R/W] H,W 00000000 00000000		
003148_H	PWCTCCS00 [R/W] B,H,W -0000000 0--0-000		—	—	
$00314C_H$	PWCCPCLRB10/PWCCPCLR10 [W] H,W 11111111 11111111		PWCTCDT10 [R/W] H,W 00000000 00000000		
003150_H	PWCTCCS10 [R/W] B,H,W -0000000 0--0----		—	—	
003154_H	PWCDBR00 [R] H,W 00000000 00000000		PWCDBR10 [R] H,W 00000000 00000000		
003158_H	PWCDBR20 [R] H,W 00000000 00000000		PWCDBR30 [R] H,W 00000000 00000000		
$00315C_H$	PWCDBS0 [R] B,H,W -000-000 -000-000		—	—	
003160_H	PWCBFIRQF0 [R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
003164_H	PWCBFIRQC0 [R/W] B,H,W 00000000 00000000 00000000			—	PWC 0ch
003168_H	PWCCUC00 [R/W] H,W 00000000 00000000		PWCCLC00 [R/W] H,W 00000000 00000000		
$00316C_H$	PWCCUC10 [R/W] H,W 00000000 00000000		PWCCLC10 [R/W] H,W 00000000 00000000		
003170_H	PWCCUC20 [R/W] H,W 00000000 00000000		PWCCLC20 [R/W] H,W 00000000 00000000		
003174_H	PWCCUC30 [R/W] H,W 00000000 00000000		PWCCLC30 [R/W] H,W 00000000 00000000		
003178_H	PWCINIT1 [R/W] B,H,W -------0	PWCC1 [R/W] B,H,W ---00000	—	—	PWC 1ch
$00317C_H$	PWCCPCLRB01/PWCCPCLR01 [W] H,W 11111111 11111111		PWCTCDT01 [R/W] H,W 00000000 00000000		
003180_H	PWCTCCS01 [R/W] B,H,W -0000000 0--0-000		—	—	
003184_H	PWCCPCLRB11/PWCCPCLR11 [W] H,W 11111111 11111111		PWCTCDT11 [R/W] H,W 00000000 00000000		
003188_H	PWCTCCS11 [R/W] B,H,W -0000000 0--0----		—	—	
$00318C_H$	PWCDBR01 [R] H,W 00000000 00000000		PWCDBR11 [R] H,W 00000000 00000000		
003190_H	PWCDBR21 [R] H,W 00000000 00000000		PWCDBR31 [R] H,W 00000000 00000000		
003194_H	PWCDBS1 [R] B,H,W -000-000 -000-000		—	—	
003198_H	PWCBFIRQF1 [R/W] B,H,W 00000000 00000000		—	—	
$00319C_H$	PWCBFIRQC1 [R/W] B,H,W 00000000 00000000 00000000			—	
$0031A0_H$	PWCCUC01 [R/W] H,W 00000000 00000000		PWCCLC01 [R/W] H,W 00000000 00000000		
$0031A4_H$	PWCCUC11 [R/W] H,W 00000000 00000000		PWCCLC11 [R/W] H,W 00000000 00000000		
$0031A8_H$	PWCCUC21 [R/W] H,W 00000000 00000000		PWCCLC21 [R/W] H,W 00000000 00000000		
$0031AC_H$	PWCCUC31 [R/W] H,W 00000000 00000000		PWCCLC31 [R/W] H,W 00000000 00000000		

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
$0031B0_H$ to $0031BC_H$	—		—		Reserved
$0031C0_H$	PWMTCGS [R/W] B,H,W ------00	—	—	PWMTCGSE [R/W] B,H,W ------00	PWM master clock generation
$0031C4_H$	PWMCPCLRB0/PWMCPCLR0 [W] H,W 11111111 11111111		PWMTCDT0 [R/W] H,W 00000000 00000000		
$0031C8_H$	PWMTCCS0 [R/W] B,H,W -0000000 0100-000 ----0000			—	
$0031CC_H$	PWMCPCLRB1/PWMCPCLR1 [W] H,W 11111111 11111111		PWMTCDT1 [R/W] H,W 00000000 00000000		
$0031D0_H$	PWMTCCS1 [R/W] B,H,W -0000000 0100---- ----0000			—	
$0031D4_H$	PWMTRC [R/W] B,H,W -0000000 -000-000 -----000			—	
$0031D8_H$	PWMSYNCP0 [R/W] H,W 00000000 00000000		PWMSYNCP1 [R/W] H,W 00000000 00000000		
$0031DC_H$	PWMSEVCON [R/W] B,H,W ---00000 ---00000		—	—	
$0031E0_H$	PWMSEVST [R/W] B,H,W ------00	—	—	—	
$0031E4_H$	PWMSEVCP0 [R/W] H,W 00000000 00000000		PWMSEVCP1 [R/W] H,W 00000000 00000000		
$0031E8_H$	PWMMCD0B [R/W] H,W 00000000 00000000		PWMMCD1B [R/W] H,W 00000000 00000000		
$0031EC_H$	PWMST0 [R/W] B,H,W ----0000	PWMST1 [R/W] B,H,W ----0000	PWMST2 [R/W] B,H,W ----0000	PWMFLTST [R] B,H,W --XXXXXX	
$0031F0_H$	PWMCMD [R/W] H,W 00000000 00000000		PWMPCGS [R/W] B,H,W -----000	—	PWM PWM generation
$0031F4_H$	PWMPCN01 [R/W] B,H,W 00000000 ------00		—	—	
$0031F8_H$	PWMCC0B [R/W] H,W 00000000 00000000		PWMCP0B [R/W] H,W 00000000 00000000		
$0031FC_H$	PWMCD0B [R/W] H,W 00000000 00000000		PWMPTMR0 [R] H,W 00000000 00000000		
003200_H	PWMCC1B [R/W] H,W 00000000 00000000		PWMCP1B [R/W] H,W 00000000 00000000		

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
003204_H	PWMCD1B [R/W] H,W 00000000 00000000		PWMPTMR1 [R] H,W 00000000 00000000		PWM PWM generation
003208_H	PWMPCN23 [R/W] B,H,W 00000000 ------00		—	—	
$00320C_H$	PWMCC2B [R/W] H,W 00000000 00000000		PWMCP2B [R/W] H,W 00000000 00000000		
003210_H	PWMCD2B [R/W] H,W 00000000 00000000		PWMPTMR2 [R] H,W 00000000 00000000		
003214_H	PWMCC3B [R/W] H,W 00000000 00000000		PWMCP3B [R/W] H,W 00000000 00000000		
003218_H	PWMCD3B [R/W] H,W 00000000 00000000		PWMPTMR3 [R] H,W 00000000 00000000		
$00321C_H$	PWMPCN45 [R/W] B,H,W 00000000 ------00		—	—	
003220_H	PWMCC4B [R/W] H,W 00000000 00000000		PWMCP4B [R/W] H,W 00000000 00000000		
003224_H	PWMCD4B [R/W] H,W 00000000 00000000		PWMPTMR4 [R] H,W 00000000 00000000		
003228_H	PWMCC5B [R/W] H,W 00000000 00000000		PWMCP5B [R/W] H,W 00000000 00000000		
$00322C_H$	PWMCD5B [R/W] H,W 00000000 00000000		PWMPTMR5 [R] H,W 00000000 00000000		
003230_H	PWMFLTCON00 [R/W] B,H,W 00000000 -0000-00		PWMFLTCON01 [R/W] B,H,W 00000000 -0000-00		PWM fault
003234_H	PWMFLTRCON0 [R/W] B,H,W -000-000 -000-000		PWMFLTCAPCON0 [R/W] B,H,W --00--00 -0000000		
003238_H	PWMFLTSR0 [R/W] B,H,W -------0 -------0		—	—	
$00323C_H$	PWMCAPITH0 [R/W] H,W 00000000 00000000		—	—	
003240_H	PWMFLTRDCON00 [R/W] H,W 00000000 00000000 00000000 00000000				
003244_H	PWMFLTRDCON01 [R/W] H,W 00000000 00000000 00000000 00000000				
003248_H	PWMFLTCAPRDCON0 [R/W] H,W 00000000 00000000 00000000 00000000				
$00324C_H$	PWMFLTCAPD0 [R] H,W 00000000 00000000 00000000 00000000				

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
003250_H	PWMFLTCON10 [R/W] B,H,W 00000000 -0000-00		PWMFLTCON11 [R/W] B,H,W 00000000 -0000-00		PWM fault
003254_H	PWMFLTRCON1 [R/W] B,H,W -000-000 -000-000		PWMFLTCAPCON1 [R/W] B,H,W --00--00 -0000000		
003258_H	PWMFLTSR1 [R/W] B,H,W -------0 -------0		—	—	
$00325C_H$	PWMCAPITH1 [R/W] H,W 00000000 00000000		—	—	
003260_H	PWMFLTRDCON10 [R/W] H,W 00000000 00000000 00000000 00000000				
003264_H	PWMFLTRDCON11 [R/W] H,W 00000000 00000000 00000000 00000000				
003268_H	PWMFLTCAPRDCON1 [R/W] H,W 00000000 00000000 00000000 00000000				
$00326C_H$	PWMFLTCAPD1 [R] H,W 00000000 00000000 00000000 00000000				
003270_H	PWMFLTCON20 [R/W] B,H,W 00000000 -0000-00		PWMFLTCON21 [R/W] B,H,W 00000000 -0000-00		
003274_H	PWMFLTRCON2 [R/W] B,H,W -000-000 -000-000		PWMFLTCAPCON2 [R/W] B,H,W --00--00 -0000000		
003278_H	PWMFLTSR2 [R/W] B,H,W -------0 -------0		—	—	
$00327C_H$	PWMCAPITH2 [R/W] H,W 00000000 00000000		—	—	
003280_H	PWMFLTRDCON20 [R/W] H,W 00000000 00000000 00000000 00000000				
003284_H	PWMFLTRDCON21 [R/W] H,W 00000000 00000000 00000000 00000000				
003288_H	PWMFLTCAPRDCON2 [R/W] H,W 00000000 00000000 00000000 00000000				
$00328C_H$	PWMFLTCAPD2 [R] H,W 00000000 00000000 00000000 00000000				

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
003290_H	PWMSOWCON0 [R/W] B,H,W 00000000 -------0 00000000 00000000				PWM soft overwrite control
003294_H	PWMSOWCON1 [R/W] B,H,W 00000000 -------0 00000000 00000000				
003298_H	PWMSOWCON2 [R/W] B,H,W 00000000 -------0 00000000 00000000				
$00329C_H$	PWMDMOD [R/W] B,H,W--000000	—	—	—	PWM dead time
$0032A0_H$	PWMHRTMRR0 [R/W] H,W 00000000 00000000		PWMHFTMRR0 [R/W] H,W 00000000 00000000		
$0032A4_H$	PWMLRTMRR0 [R/W] H,W 00000000 00000000		PWMLFTMRR0 [R/W] H,W 00000000 00000000		
$0032A8_H$	PWMHRTMRR1 [R/W] H,W 00000000 00000000		PWMHFTMRR1 [R/W] H,W 00000000 00000000		
$0032AC_H$	PWMLRTMRR1 [R/W] H,W 00000000 00000000		PWMLFTMRR1 [R/W] H,W 00000000 00000000		
$0032B0_H$	PWMHRTMRR2 [R/W] H,W 00000000 00000000		PWMHFTMRR2 [R/W] H,W 00000000 00000000		
$0032B4_H$	PWMLRTMRR2 [R/W] H,W 00000000 00000000		PWMLFTMRR2 [R/W] H,W 00000000 00000000		
$0032B8_H$	PWMLEBCON0 [R/W] B,H,W -000-000 -000-000 ----0000			—	PWM Blanking
$0032BC_H$	PWMLEBSDCON00 [R/W] H,W 00000000 00000000		PWMLEBSDCON01 [R/W] H,W 00000000 00000000		
$0032C0_H$	PWMLEBSDCON02 [R/W] H,W 00000000 00000000		PWMLEBSDCON03 [R/W] H,W 00000000 00000000		
$0032C4_H$	PWMLEBTCON00 [R/W] H,W 00000000 00000000 00000000 00000000				
$0032C8_H$	PWMLEBTCON01 [R/W] H,W 00000000 00000000 00000000 00000000				
$0032CC_H$	PWMLEBCON1 [R/W] B,H,W -000-000 -000-000 ----0000			—	
$0032D0_H$	PWMLEBSDCON10 [R/W] H,W 00000000 00000000		PWMLEBSDCON11 [R/W] H,W 00000000 00000000		
$0032D4_H$	PWMLEBSDCON12 [R/W] H,W 00000000 00000000		PWMLEBSDCON13 [R/W] H,W 00000000 00000000		
$0032D8_H$	PWMLEBTCON10 [R/W] H,W 00000000 00000000 00000000 00000000				

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
0032DC$_H$	PWMLEBTCON11 [R/W] H,W 00000000 00000000 00000000 00000000				PWM Blanking
0032E0$_H$	PWMLEBCON2 [R/W] B,H,W -000-000 -000-000 ----0000			—	
0032E4$_H$	PWMLEBSDCON20 [R/W] H,W 00000000 00000000		PWMLEBSDCON21 [R/W] H,W 00000000 00000000		
0032E8$_H$	PWMLEBSDCON22 [R/W] H,W 00000000 00000000		PWMLEBSDCON23 [R/W] H,W 00000000 00000000		
0032EC$_H$	PWMLEBTCON20 [R/W] H,W 00000000 00000000 00000000 00000000				
0032F0$_H$	PWMLEBTCON21 [R/W] H,W 00000000 00000000 00000000 00000000				
0032F4$_H$	PWMADTCON [R/W] B,H,W 00000000 00000000 --000000 ----0000				PWM trigger
0032F8$_H$	PWMADTST [R/W] B,H,W ----0000	—	—	—	
0032FC$_H$	PWMADTDCON0 [R/W] H,W 00000000 00000000		PWMADTDCON1 [R/W] H,W 00000000 00000000		
003300$_H$	PWMADTDCON2 [R/W] H,W 00000000 00000000		PWMADTDCON3 [R/W] H,W 00000000 00000000		
003304$_H$ to 00331C$_H$	—				Reserved
003320$_H$	AD4EN [R/W] B,H,W -------0	—	—	—	12 bit 4ch A/D converter
003324$_H$	AD4TSS [R/W] B,H,W -------0	—	—	—	
003328$_H$	AD4TSE [R/W] B,H,W -------- -------- -------- 00000000				
00332C$_H$	AD4TCS0 [R/W] B,H,W ---00--- --------		AD4TCS1 [R/W] B,H,W ---00--- --------		
003330$_H$	AD4TCS2 [R/W] B,H,W ---00--- --------		AD4TCS3 [R/W] B,H,W ---00--- --------		
003334$_H$	AD4TCS4 [R/W] B,H,W ---00--- --------		AD4TCS5 [R/W] B,H,W ---00--- --------		
003338$_H$	AD4TCS6 [R/W] B,H,W ---00--- --------		AD4TCS7 [R/W] B,H,W ---00--- --------		

Address	Address offset Value/Register name				Block
	+0	+1	+2	+3	
00333C$_H$	AD4TBUSY [R/W] B,H,W -------- -------- -------- 00000000				12 bit 4ch A/D converter
003340$_H$	AD4TECS0 [R/W] B,H,W 00--0000 0000----		AD4TECS1 [R/W] B,H,W 00--0000 0000----		
003344$_H$	AD4TECS2 [R/W] B,H,W 00--0000 0000----		AD4TECS3 [R/W] B,H,W 00--0000 0000----		
003348$_H$	AD4TECS4 [R/W] B,H,W 00--0000 0000----		AD4TECS5 [R/W] B,H,W 00--0000 0000----		
00334C$_H$	AD4TECS6 [R/W] B,H,W 00--0000 0000----		AD4TECS7 [R/W] B,H,W 00--0000 0000----		
003350$_H$	AD4PTC8 [R/W] B,H,W 0000----	AD4PTC9 [R/W] B,H,W 0000----	AD4PTC10 [R/W] B,H,W 0000----	AD4PTC11 [R/W] B,H,W 0000----	
003354$_H$	AD4TCD8 [R] B,H,W 10--0000 00000000		AD4TCD9 [R] B,H,W 10--0000 00000000		
003358$_H$	AD4TCD10 [R] B,H,W 10--0000 00000000		AD4TCD11 [R] B,H,W 10--0000 00000000		
00335C$_H$	AD4CS [R/W] B,H,W 00------ 00------		—	AD4MD [R/W] B,H,W ----0000	
003360$_H$	AD4PRTF [R] B,H,W -------- -------- -------- ----0000				
003364$_H$ to 00EFFC$_H$	—				Reserved
00F000$_H$ to 00FEFC$_H$	—	—	—	—	Reserved[S]

Address	Address offset Value/Register name				Blocks
	+0	+1	+2	+3	
$00FF00_H$	DSUCR [R/W] B,H,W -------- -------0		—	—	OCDU [S]
$00FF04_H$ to $00FF0C_H$	—				
$00FF10_H$	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00FF14_H$	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00FF18_H$ to $00FFF4_H$	—				
$00FFF8_H$	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00FFFC_H$	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

10. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

10.1 Interrupt vector

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN*
	Decimal	Hexadecimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request	15	0F	$15(F_H)$ Fixed	$3C0_H$	$000FFFC0_H$	-
Error generation during internal bus diagnosis						
XBS RAM double-bit error generation						
TPU violation						
External interrupt 0-3	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	-
Reload timer 0/1/4	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2
Reload timer 2/3	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4[1]
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5[1]
Multi-function serial interface ch.1 (reception completed)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6[1]
Multi-function serial interface ch.1(status)						
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7[1]
Multi-function serial interface ch.2 (reception completed)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8[1]
Multi-function serial interface ch.2(status)						
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9[1]
-	26	1A	ICR10	394_H	$000FFF94_H$	-

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN*
	Decimal	Hexadecimal				
-	27	1B	ICR11	390_H	$000FFF90_H$	-
-	28	1C	ICR12	$38C_H$	$000FFF8C_H$	-
-	29	1D	ICR13	388_H	$000FFF88_H$	-
-	30	1E	ICR14	384_H	$000FFF84_H$	-
-	31	1F	ICR15	380_H	$000FFF80_H$	-
-	32	20	ICR16	$37C_H$	$000FFF7C_H$	-
-	33	21	ICR17	378_H	$000FFF78_H$	-
CAN	34	22	ICR18	374_H	$000FFF74_H$	-
RAM diagnosis end RAM initialization completion Error generation during RAM diagnosis	35	23	ICR19	370_H	$000FFF70_H$	-
4ch A/D converter irregular activation interrupt/insufficient sampling time interrupt	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
-	37	25	ICR21	368_H	$000FFF68_H$	-
PWM special event interrupt 0/1	38	26	ICR22	364_H	$000FFF64_H$	-
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
PWM 0 detection interrupt 0, compare clear interrupt 0	40	28	ICR24	$35C_H$	$000FFF5C_H$	-
PWM 0 detection interrupt 1, compare clear interrupt 1	41	29	ICR25	358_H	$000FFF58_H$	-
PWM SOW interrupt 0, fault interrupt 0/1, capture interrupt 0	42	2A	ICR26	354_H	$000FFF54_H$	-
PWM SOW interrupt 1, fault interrupt 2/3, capture interrupt 1	43	2B	ICR27	350_H	$000FFF50_H$	-
PWM SOW interrupt 2, fault interrupt 4/5, capture interrupt 2	44	2C	ICR28	$34C_H$	$000FFF4C_H$	-
16bit ICU 0 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29
Main timer PLL timer	46	2E	ICR30	344_H	$000FFF44_H$	30
PWM trigger interrupt 0/1/2/3	47	2F	ICR31	340_H	$000FFF40_H$	-
A/D converter 0/1/2/3/4/5/6/7	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation)	49	31	ICR33	338_H	$000FFF38_H$	-
PLL alarm interrupt for PWM	50	32	ICR34	334_H	$000FFF34_H$	-
reserved	51	33	ICR35	330_H	$000FFF30_H$	-
Comparator output detection interrupt 0/1/2	52	34	ICR36	$32C_H$	$000FFF2C_H$	36
PWC0 0 detection interrupt 00/10, compare clear interrupt 00/10	53	35	ICR37	328_H	$000FFF28_H$	- [2]
PWC0 capture data upper limit interrupt 00/10/20/30, PWC0 capture data lower limit interrupt 00/10/20/30, PWC0 data buffer interrupt 00/10/20/30, PWC0 buffer overrun interrupt 00/10/20/30	54	36	ICR38	324_H	$000FFF24_H$	- [2]
PWC1 0 detection interrupt 01/11, compare clear interrupt 01/11	55	37	ICR39	320_H	$000FFF20_H$	- [2]

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN*
	Decimal	Hexadecimal				
PWC1 capture data upper limit interrupt 01/11/21/31, PWC1 capture data lower limit interrupt 01/11/21/31, PWC1 data buffer interrupt 01/11/21/31, PWC1 buffer overrun interrupt 01/11/21/31	56	38	ICR40	$31C_H$	$000FFF1C_H$	- [2]
A/D converter 8/9/10/11	57	39	ICR41	318_H	$000FFF18_H$	- [2]
Base Timer 2 IRQ0 Base Timer 2 IRQ1	58	3A	ICR42	314_H	$000FFF14_H$	42
Base Timer 3 IRQ0 Base Timer 3 IRQ1	59	3B	ICR43	310_H	$000FFF10_H$	43
Base Timer 0 IRQ0 Base Timer 0 IRQ1	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44
Base Timer 1 IRQ0 Base Timer 1 IRQ1	61	3D	ICR45	308_H	$000FFF08_H$	45
DMAC0/1/2/3/4/5/6/7	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS™[3])	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

*: DMA transfer request by interrupt from peripherals without an assigned RN number is not supported.

[1]: DMA transfer by the multi-function serial interface status is not supported.

[2]: DMA transfer request by on-chip bus IP interrupt is supported.

[3]: REALOS is a trademark of Cypress.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage [1] [2]	V_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	
Analog power supply voltage [1] [2]	AV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	AVRH ≤ AV_{CC} ≤V_{CC}
Analog reference voltage [1]	AVRH	V_{SS}-0.3	V_{SS}+6.0	V	AVRH ≤ AV_{CC}
Input voltage[1]	V_I	V_{SS}-0.3	V_{CC}+0.3	V	
Analog pin input voltage [1]	V_{IA5}	V_{SS}-0.3	V_{CC}+0.3	V	
Output voltage [1]	V_O	V_{SS}-0.3	V_{CC}+0.3	V	
Maximum clamp current	I_{CLAMP}	-	4.0	mA	[6]
Total maximum clamp current	$\Sigma\|I_{CLAMP}\|$	-	20	mA	[6]
"L" level maximum output current [3]	I_{OL1}	-	15	mA	
	I_{OL2}	-	30	mA	[8]
"L" level average output current [4]	I_{OLAV1}	-	4	mA	
	I_{OLAV2}	-	8	mA	[8]
"L" level total output current [5]	ΣI_{OL1}	-	50	mA	
	ΣI_{OL2}	-	60	mA	[8]
"H" level maximum output current [3]	I_{OH1}	-	-15	mA	
	I_{OH2}	-	-30	mA	[8]
"H" level average output current [4]	I_{OHAV1}	-	-4	mA	
	I_{OHAV2}	-	-8	mA	[8]
"H" level total output current [5]	ΣI_{OH1}	-	-50	mA	
	ΣI_{OH2}	-	-60	mA	[8]
Power consumption	P_D	-	690	mW	
Operating temperature	T_A	-40	+125	°C	[7]
Storage temperature	Tstg	-55	+150	°C	

[1]: These parameters are based on the condition that V_{SS}=AV_{SS}=0.0V

[2]: Caution must be taken that AV_{CC}, AVRH do not exceed V_{CC} upon power-on and under other circumstances.

[3]: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

[4]: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

[5]: The total output current is defined as the maximum current value flowing through all of corresponding pins.

[6]:

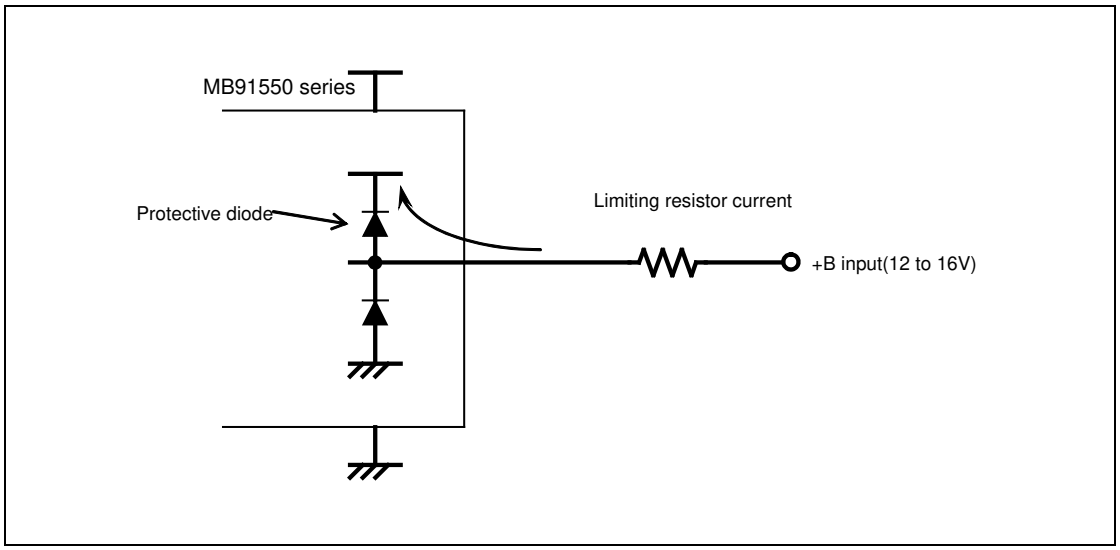
- Corresponding pins: all general-purpose ports.
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.

- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

[7]: When you use this product at TA = 125°C, it is necessary to built-in multi-layer substrate at least four -layer or more. If you use a 2-layer substrate, change the operating conditions (such as operating frequency, power supply voltage) , you will need to either you use the power consumption PD = 400mW or less, or use the operating temperature TA = 105°C or less.

[8]: Corresponding pins:PWM0H, PWM0L, PWM1H, PWM1L, PWM2H, PWM2L

Sample recommended circuit



WARNING

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

11.2 Recommended operating conditions

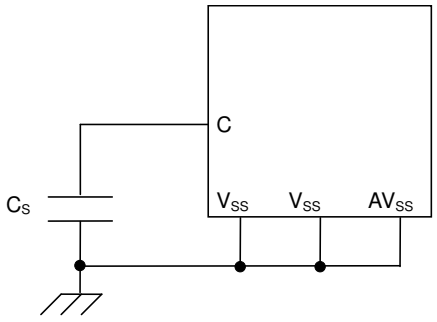
(V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	4.5	5.5	V	Recommended operation guarantee range
		3.4	5.5	V	Operation guarantee range[1]
	AVcc0 AVcc1	4.5	5.5	V	Operation guarantee range[1]
	AVcc2	4.925	5.075	V	Operation guarantee range[1]
Smoothing capacitor [2]	C_S	4.7 (tolerance within ±50%)		µF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+125	°C	

[1]: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset.

[2]: See the following diagram for details on the connection of smoothing capacitor C_S.

■ C Pin Connection Diagram



WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions. Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

11.3 DC characteristics

(T_A:-40°C to +125°C, Vcc=AVcc=4.5V to 5.5V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions		Value			Unit	Remarks
					Min	Typ	Max		
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP}=80MHz, Fcpp=40MHz Fcpwm=200MHz, at normal operation		-	60	98	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz Fcpwm=200MHz, at Flash write		-	72	112	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz Fcpwm=200MHz, at Flash erase		-	72	112	mA	
	$I_{CCS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, Fcpwm=200MHz at CPU sleep mode		-	33	66	mA	
	$I_{CCBS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, Fcpwm=200MHz at bus sleep mode		-	26	56	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4MHz T_A=+25°C	-	1320	2600	µA	
	$I_{CCH}5$		Stop mode	T_A=+25°C	-	190	1370	µA	

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	All input pins	V_{CC}=AV_{CC}=5.5V V_{SS}<V_I<V_{CC}	-5	-	5	µA	
Input capacitance 1	C_{IN1}	Other than VCC,VSS, AVCC, AVSS, C	-	-	5	15	pF	
Pull-up resistance	R_{UP1}	RSTX, NMIX	-	25	-	100	kΩ	
	R_{UP2}	Port pin other than P000 to P005	-	25	-	100	kΩ	
Pull-down resistance	R_{DOWN}	P000 to P005	-	25	-	100	kΩ	
"H" level output voltage	V_{OH1}	Normal output pin	Vcc=4.5V I_{OH}=-4.0mA	V_{CC}-0.5	-	V_{CC}	V	
	V_{OH2}	P000 to P005	Vcc=4.5V I_{OH}=-8.0mA	V_{CC}-0.5	-	V_{CC}	V	PWM pin output
"L" level output voltage	V_{OL1}	Normal output pin	Vcc=4.5V I_{OL}=4.0mA	0	-	0.4	V	
	V_{OL2}	P000 to P005	Vcc=4.5V I_{OL}=8.0mA	0	-	0.4	V	PWM pin output
"H" level input voltage	V_{IH1}	P032,P033, P036,P037 P042, P044,P045	CMOS hysteresis input level	0.7× V_{CC}	-	V_{CC}	V	
	V_{IH3}	Port other than V_{IH1}	Automotive input level	0.8× V_{CC}	-	V_{CC}	V	
	V_{IH5}	RSTX, NMIX, MD0, MD1	CMOS hysteresis input level	0.8× V_{CC}	-	V_{CC}	V	
	V_{IHT}	DEBUGIF	TTL input level	2	-	V_{CC}	V	
"L" level input voltage	V_{IL1}	P032, P033, P036, P037 P042, P044, P045	CMOS hysteresis input level	Vss	-	0.3× V_{CC}	V	
	V_{IL3}	Port other than V_{IH1}	Automotive input level	Vss	-	0.5× V_{CC}	V	
	V_{IL5}	RSTX, NMIX, MD0, MD1	CMOS hysteresis input level	Vss	-	0.2× V_{CC}	V	
	V_{ILT}	DEBUGIF	TTL input level	Vss	-	0.8	V	

11.4 AC Characteristics

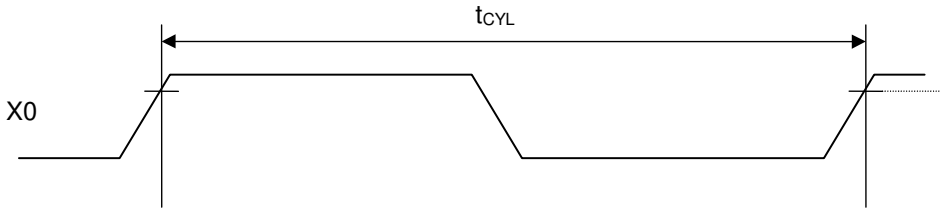
11.4.1 Main Clock Timing

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	-	4	-	16	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1		62.5	-	250	ns	
Internal operating clock frequency [1]	F_{CP}	-		2	-	80	MHz	CPU clock
	F_{CPP}			1		40		Peripheral bus clock
	F_{CPWM}			2		200		PWM clock
	F_{CPWMD}			2		200		PWM division clock
	F_{CCMP}			2		50		Comparator clock
Internal operating clock cycle time [1]	t_{CP}	-		12.5	-	500	ns	CPU clock
	t_{CPP}			25		1000		Peripheral bus clock
	t_{CPWM}			5		500		PWM clock
	t_{CPWMD}			5		500		PWM division clock
	t_{CCMP}			20		500		Comparator clock
CAN PLL jitter (during lock)	t_{PJ}	-		-10	-	10	ns	F_{CP}=80MHz (4MHz×Multiplied by 20)
Built-in CR oscillation frequency	F_{CCR}	-		50	100	150	kHz	

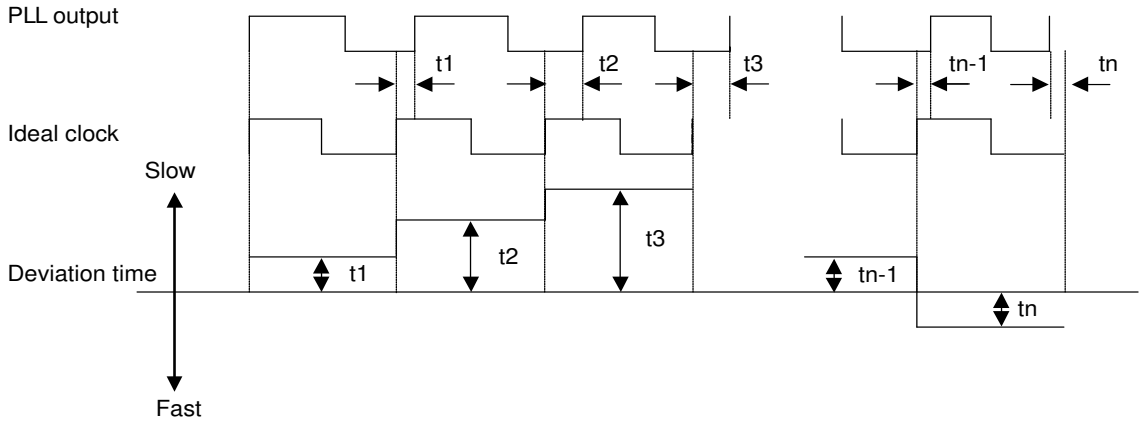
[1]: The maximum / minimum value is defined when using the main clock and PLL clock.

X0,X1 clock timing



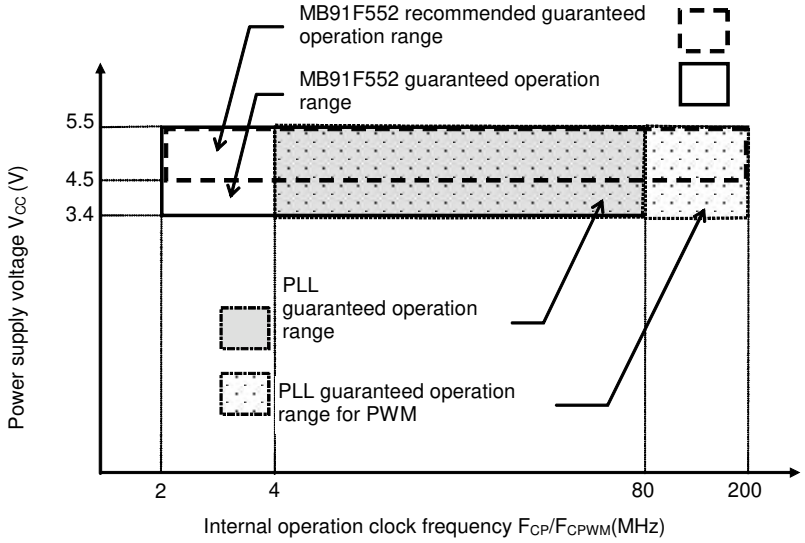
CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.



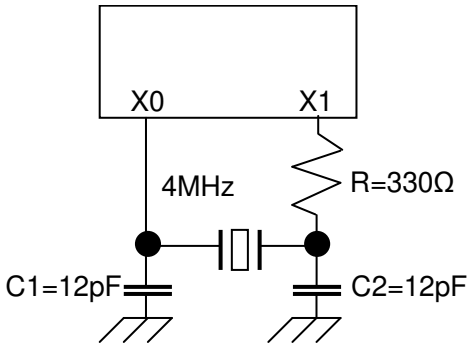
Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage



Note: The power supply voltage, which is the low-voltage detection setting voltage or lower, is in the reset state.

Example of oscillation circuit



Note:

As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.
Design your print circuit board so that the oscillator can start oscillation within 20ms. Moreover, it is recommended to be designed after the match evaluation of the circuit is requested to the departure pendulum maker when the oscillation circuit is composed.

11.4.2 The using condition of PLL

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS} =AV_{SS}=0.0V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
PLL Oscillation stabilization waiting time (LOCK UP time)	t_{LOCK}	-	-	-	100	µs	Time until the oscillation of PLL is stabilized
PLL input clock frequency	f_{PLLI}	-	4	-	16	MHz	
PLL multiplication rate	-	-	13	-	100	multiplication	
PLL Macro oscillation clock frequency	f_{PLLO}		200	-	400	MHz	

AC characteristics are specified by the following measurement reference voltage values.

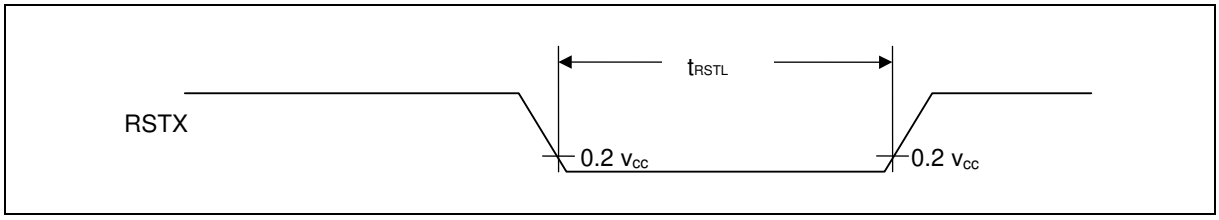
Input Signal Waveform	Output Signal Waveform
Hysteresis Input Pin (Automotive) 0.8Vcc 0.5Vcc	Output Pin 2.4V 0.8V
Hysteresis Input Pin (CMOS schmitt) 0.7Vcc 0.3Vcc	

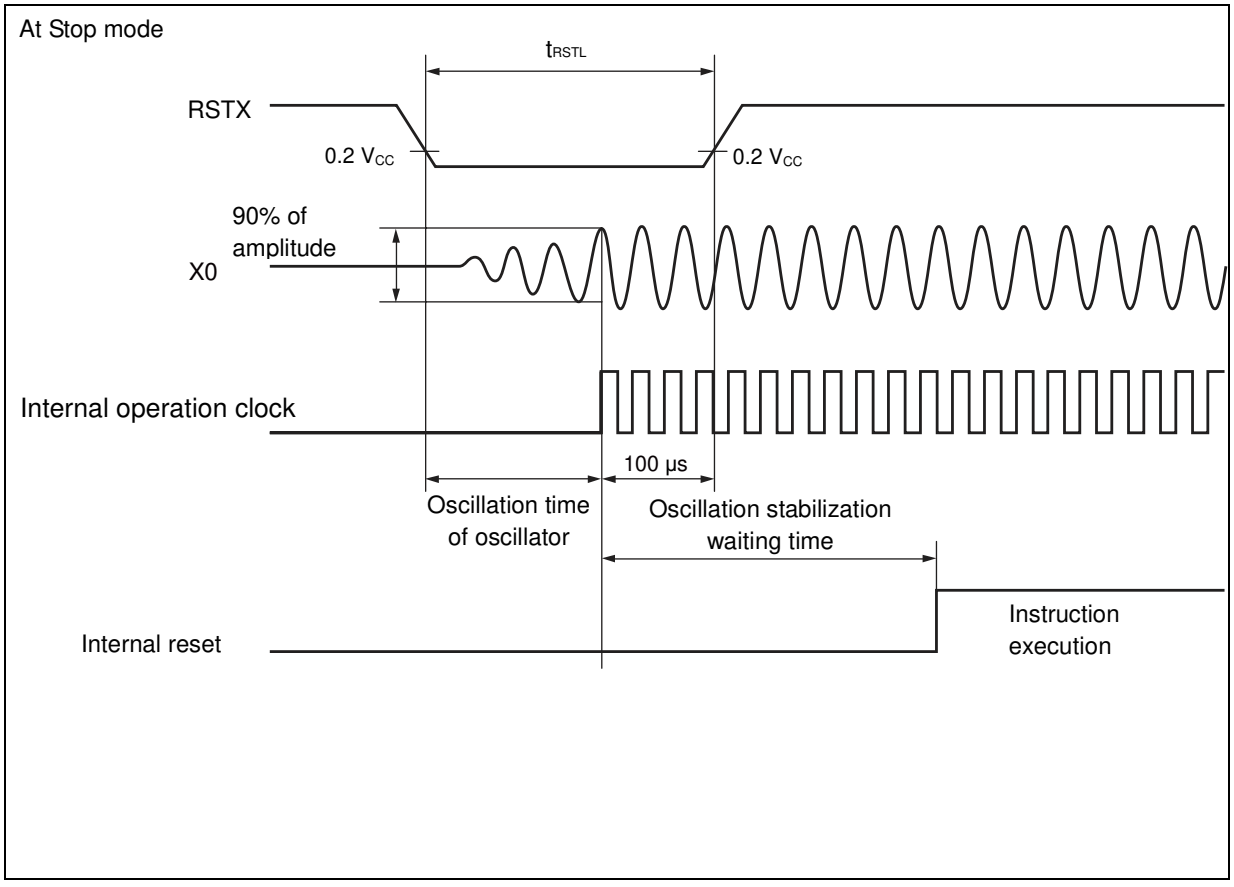
11.4.3 Reset Input

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	-	10	-	µs	When normal operation
				Oscillation time of oscillator[1]+100	-	µs	At Stop mode
				100	-	µs	At Watch mode
Width for reset input removal				1	-	µs	

[1]: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms.





11.4.4 Power-on Conditions

(T_A:-40°C to +125°C, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC	-	2.1	2.3	2.5	V	
Level detection hysteresis width	-	VCC	-	-	100	-	mV	
Level detection time	-	-	-	-	-	30	µs	[1]
Slope detection undetected standard	-	VCC	V_{CC} = at level detection release level time	-	-	4	mV/µs	[2]
Power off time	t_{OFF}	VCC	-	50	-	-	ms	[3]

[1]: If the fluctuation of the power supply is faster than the low-voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

[2]: When setting the power supply fluctuation to this standard or less, it is possible to suppress the slope detection. This is the standard when the power supply fluctuation is stable.

[3]: This time is to start the slope detection at next power on after power down and internal charge loss.

11.4.5 Multi-function Serial

11.4.5.1 CSIO timing

11.4.5.1.1 Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=0, SCR: SPI=0

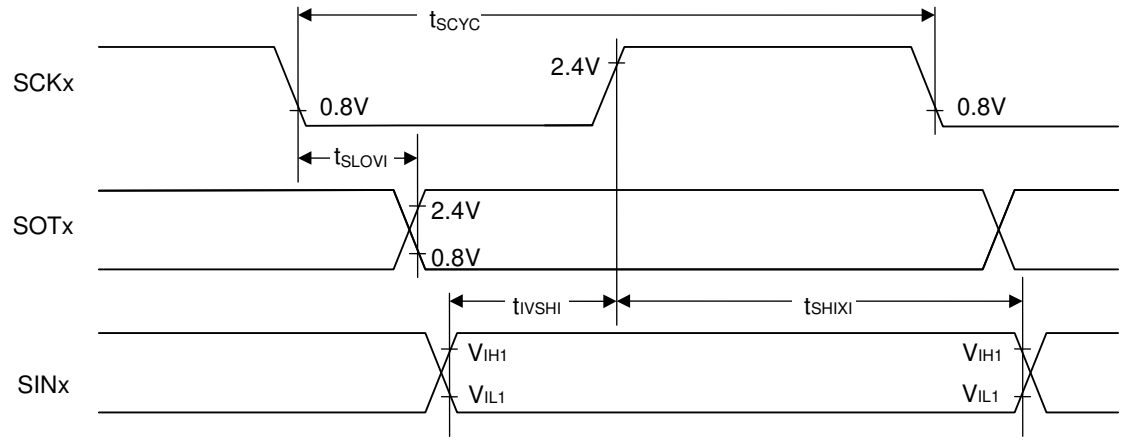
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : CL=50pF
SCK ↓ ⟶ SOT delay time	t_{SLOVI}	SCK0 to SCK2 SOT0 to SOT2		-30	30	ns	
Valid SIN ⟶ SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK2 SIN0 to SIN2		34	-	ns	
SCK ↑ ⟶ Valid SIN hold time	t_{SHIXI}			0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK2	-	t_{CPP}+10	-	ns	External shift clock mode output pin: CL=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ ⟶ SOT delay time	t_{SLOVE}	SCK0 to SCK2 SOT0 to SOT2		-	33	ns	
Valid SIN ⟶ SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK2 SIN0 to SIN2		10	-	ns	
SCK ↑ ⟶ Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK2		-	5	ns	
SCK rise time	t_R	SCK0 to SCK2		-	5	ns	

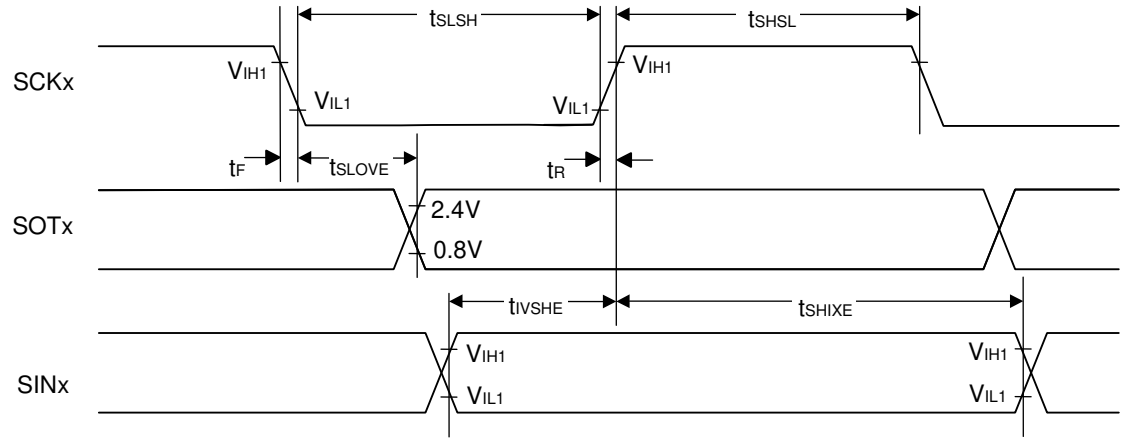
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum bard rate is limited by internal operation clock used and other parameters. See Hardware Manual for details.

Internal shift clock mode



External shift clock mode



11.4.5.1.2 Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=1, SCR: SPI=0

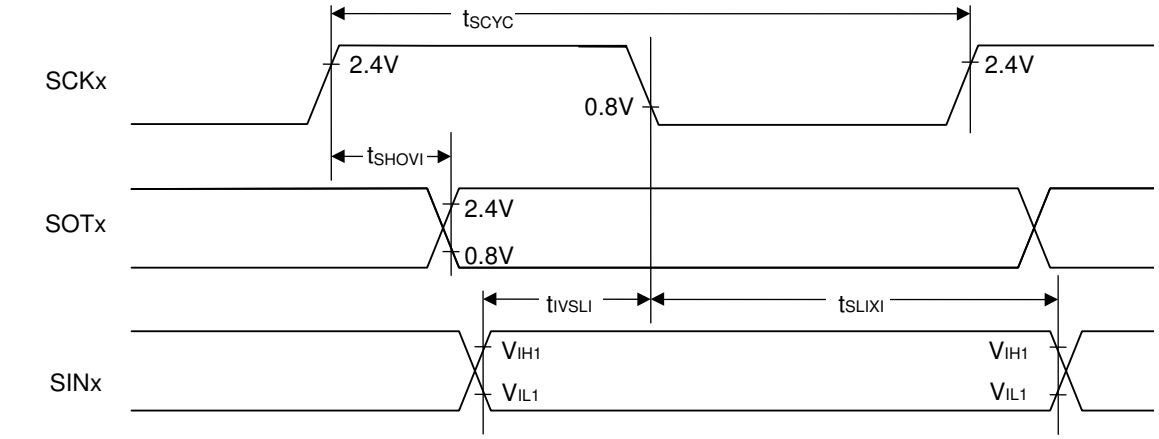
(T_A:-40°C to 125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : CL=50pF
SCK ↑ ⟶ SOT delay time	t_{SHOVI}	SCK0 to SCK2 SOT0 to SOT2		-30	30	ns	
Valid SIN ⟶ SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK2 SIN0 to SIN2		34	-	ns	
SCK ↓ ⟶ Valid SIN hold time	t_{SLIXI}			0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK2	-	t_{CPP}+10	-	ns	External shift clock mode output pin: CL=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ ⟶ SOT delay time	t_{SHOVE}	SCK0 to SCK2 SOT0 to SOT2		-	33	ns	
Valid SIN ⟶ SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK2 SIN0 to SIN2		10	-	ns	
SCK ↓ ⟶ Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK2		-	5	ns	
SCK rise time	t_R	SCK0 to SCK2		-	5	ns	

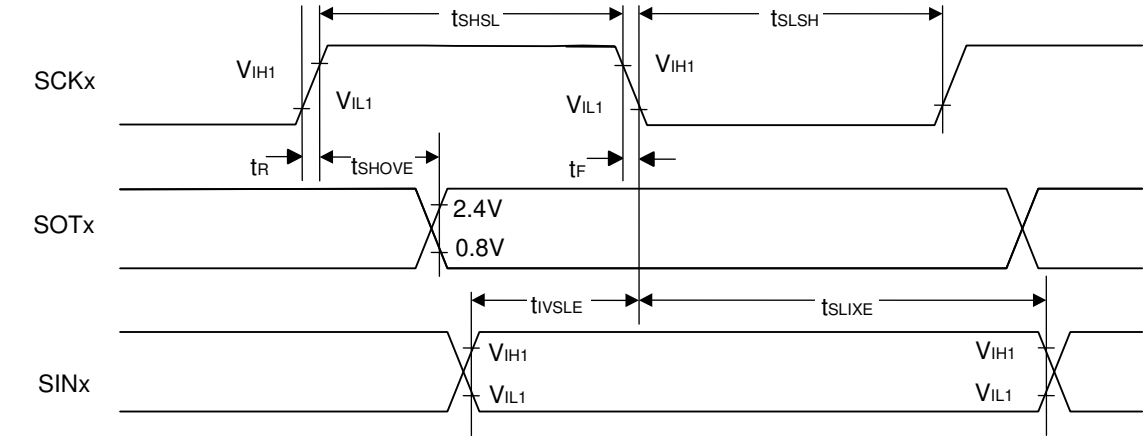
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum bard rate is limited by internal operation clock used and other parameters. See Hardware Manual for details.

Internal shift clock mode



External shift clock mode



11.4.5.1.3 Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=0, SCR: SPI=1

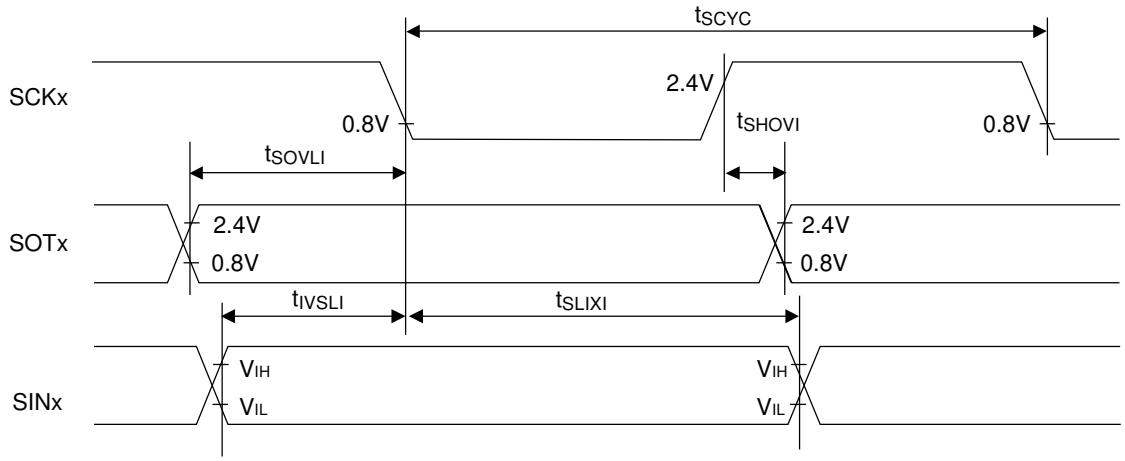
(T_A:-40°C +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : CL=50pF
SCK ↑ ⟶ SOT delay time	t_{SHOVI}	SCK0 to SCK2 SOT0 to SOT2		-30	30	ns	
Valid SIN ⟶ SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK2 SIN0 to SIN2		34	-	ns	
SCK ↓ ⟶ Valid SIN hold time	t_{SLIXI}			0	-	ns	
SOT⟶SCK↓ delay time	t_{SOVLI}	SCK0 to SCK2 SOT0 to SOT2		$2t_{CPP}$-30	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK2	-	t_{CPP}+10	-	ns	External shift clock mode output pin: CL=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ ⟶ SOT delay time	t_{SHOVE}	SCK0 to SCK2 SOT0 to SOT2		-	33	ns	
Valid SIN ⟶ SCK ↓ setup time	t_{IVSHE}	SCK0 to SCK2 SIN0 to SIN2		10	-	ns	
SCK ↓ ⟶ Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK2		-	5	ns	
SCK rise time	t_R	SCK0 to SCK2		-	5	ns	

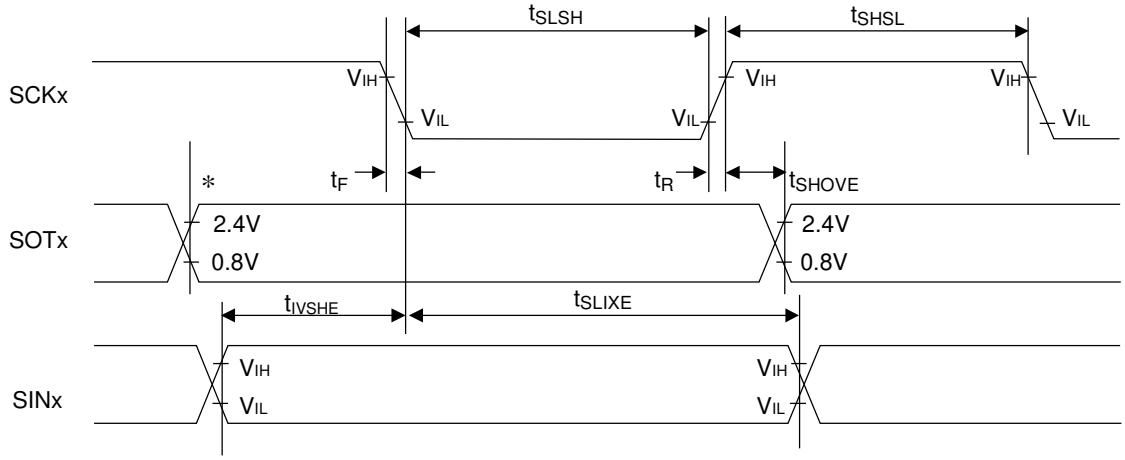
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum bard rate is limited by internal operation clock used and other parameters. See Hardware Manual for details.

Internal shift clock mode



External shift clock mode



*: It writes in the TDR register and, then, it changes.

11.4.5.1.4 Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=1, SCR: SPI=1

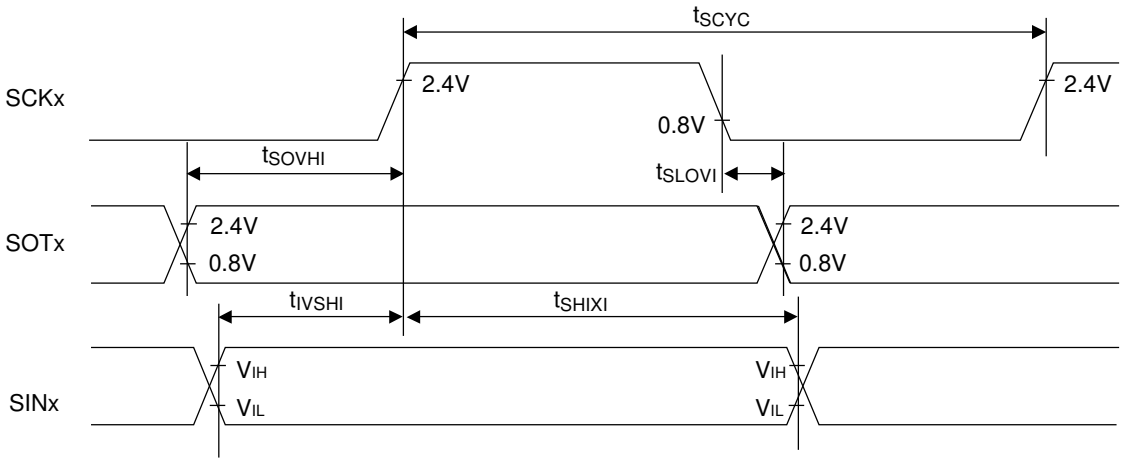
(T_A:-40°C + 125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2		$4t_{CPP}$	-	ns	
SCK↓⟶ SOT delay time	t_{SLOVI}	SCK0 to SCK2 SOT0 to SOT2		-30	30	ns	
Valid SIN ⟶ SCK↑setup time	t_{IVSHI}	SCK0 to SCK2 SIN0 to SIN2	-	34	-	ns	Internal shift clock mode output pin : CL=50pF
SCK↑⟶ Valid SIN hold time	t_{SHIXI}			0	-	ns	
SOT⟶SCK↑ delay time	t_{SOVHI}	SCK0 to SCK2 SOT0 to SOT2		$2t_{CPP}$-30	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK2		t_{CPP}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK↓⟶ SOT delay time	t_{SLOVE}	SCK0 to SCK2 SOT0 to SOT2		-	33	ns	
Valid SIN ⟶ SCK↑setup time	t_{IVSHE}	SCK0 to SCK2 SIN0 to SIN2	-	10	-	ns	External shift clock mode output pin: CL=50pF
SCK↑⟶ Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK2		-	5	ns	
SCK rise time	t_R	SCK0 to SCK2		-	5	ns	

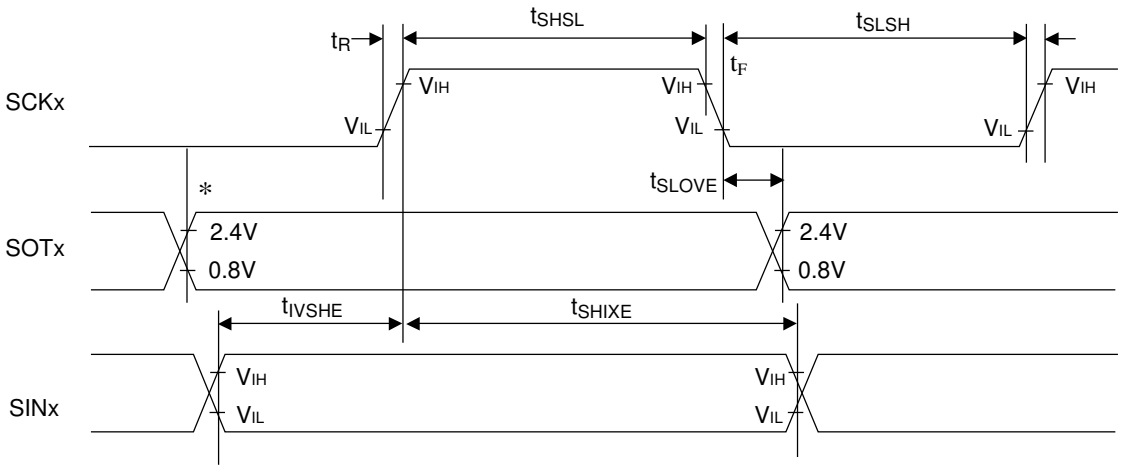
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum bard rate is limited by internal operation clock used and other parameters. See Hardware Manual for details.

Internal shift clock mode



External shift clock mode



*: It writes in the TDR register and, then, it changes.

11.4.5.1.5 Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,

When Serial chip select is used : SCSCR:CSEN=1,

Serial clock output mark level "H" : SMR, SCSFR:SCINV=0,

Serial chip select Inactive level "H" : SCSCR, SCSFR:CSLVL=1

(T_A:-40°C to + 125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

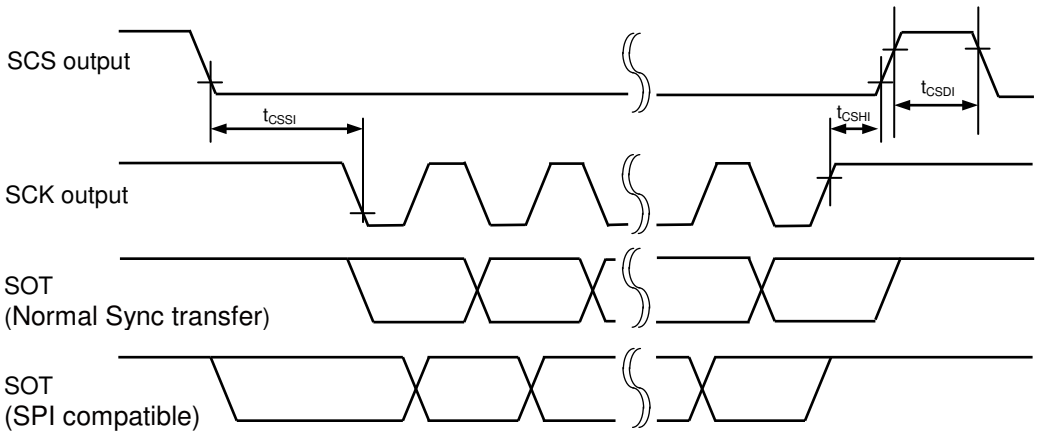
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓⟶SCK↓ setup time	t_{CSSI}	SCK0 to SCK2, SCS00, SCS01, SCS10, SCS11, SCS20, SCS21	-	t_{CSSU}[1]+0	t_{CSSU}[1]+50	ns	Internal shift clock mode output pin : C_L=50pF
SCK↑⟶SCS↑ hold time	t_{CSHI}			t_{CSHD}[2]-50	t_{CSHD}[2]+0	ns	
SCS deselect time	t_{CSDI}	SCS00, SCS01, SCS10, SCS11, SCS20, SCS21		t_{CSDS}[3]-50	t_{CSDS}[3]+50	ns	
SCS↓⟶SCK↓ setup time	t_{CSSE}	SCK0 to SCK2, SCS00, SCS01, SCS10, SCS11, SCS20, SCS21	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↑⟶SCS↑ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS00, SCS01, SCS10, SCS11, SCS20, SCS21		$3t_{CPP}$+30	-	ns	
SCS↓⟶SOT delay time	t_{DSE}	SCS00, SCS01, SCS10, SCS11, SCS20, SCS21, SOT0 to SOT2		-	40	ns	
SCS↑⟶SOT delay time	t_{DEE}			+0	-	ns	
SCK↓⟶SCS↓ clock switch time	t_{SCC}	SCK0 to SCK2, SCS00, SCS01, SCS10, SCS11, SCS20, SCS21	-	$3t_{CPP}$+0	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF

[1]: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock

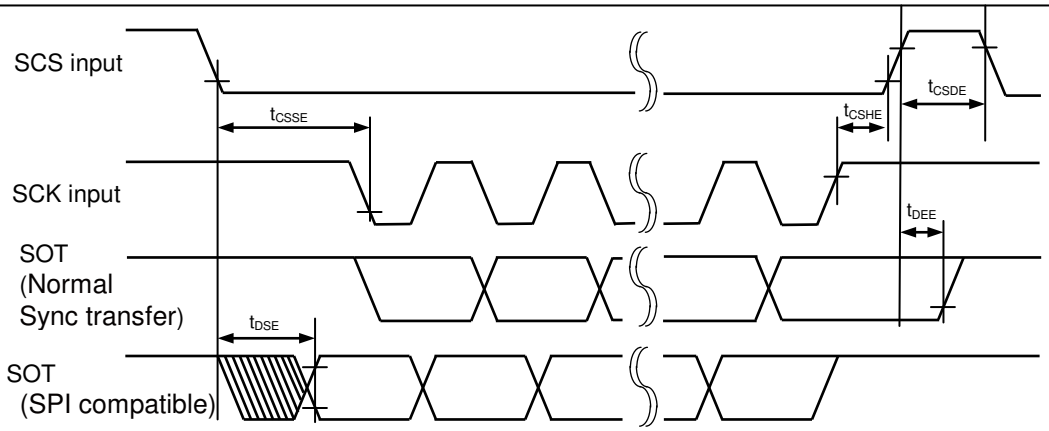
[2]: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock

[3]: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock

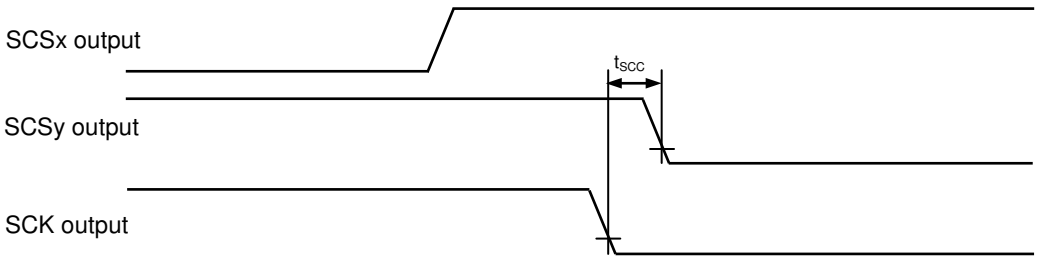
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again. Please see the hardware manual for details of above-mentioned[1], [2] and [3].



When Serial chip select is used, Serial clock output mark level "H", Serial chip select Inactive level "H"
Internal shift clock mode



When Serial chip select is used, Serial clock output mark level "H", Serial chip select Inactive level "H"
External shift clock mode



When Serial chip select is used, Serial clock output mark level "H",
Serial chip select Inactive level "H"
Internal shift clock mode, Example of switching clock by round operation (x,y=0, 1, 2, 3)

11.4.5.1.6 Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,

When Serial chip select is used : SCSCR:CSEN=1,

Serial clock output mark level "L" : SMR, SCSFR:SCINV=1,

Serial chip select Inactive level "H" : SCSCR, SCSFR:CSLVL=1

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↑ setup time	t_{CSSI}	SCK0 to SCK2, SCS00, SCS01, SCS10, SCS11, SCS20, SCS21	-	t_{CSSU}+0 [1]	t_{CSSU}+50 [1]	ns	Internal shift clock mode output pin : C_L=50pF
SCK↓→SCS↑ hold time	t_{CSHI}			t_{CSHD}-50 [2]	t_{CSHD}+0 [2]	ns	
SCS deselect time	t_{CSDI}	SCS00, SCS01, SCS10, SCS11, SCS20, SCS21		t_{CSDS}-50 [3]	t_{CSDS}+50 [3]	ns	
SCS↓→SCK↑ setup time	t_{CSSE}	SCK0 to SCK2, SCS00, SCS01, SCS10, SCS11, SCS20, SCS21	-	3t_{CPP}+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↓→SCS↑ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS00, SCS01, SCS10, SCS11, SCS20, SCS21		3t_{CPP}+30	-	ns	
SCS↓→SOT delay time	t_{DSE}	SCS00, SCS01, SCS10, SCS11, SCS20, SCS21, SOT0 to SOT2		-	40	ns	
SCS↑→SOT delay time	t_{DEE}			+0	-	ns	
SCK↑→SCS↓ clock switch time	t_{SCC}	SCK0 to SCK2, SCS00, SCS01, SCS10, SCS11, SCS20, SCS21	-	3t_{CPP}+0	3t_{CPP}+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF

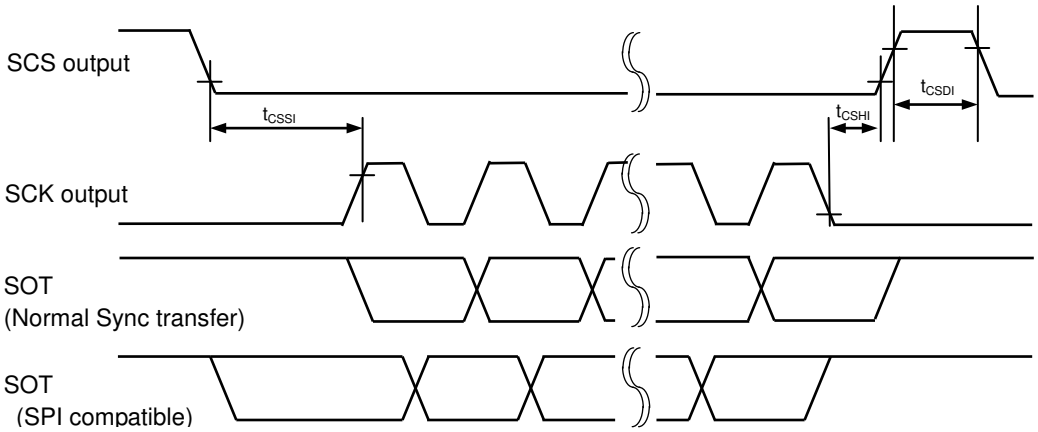
[1]: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock

[2]: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock

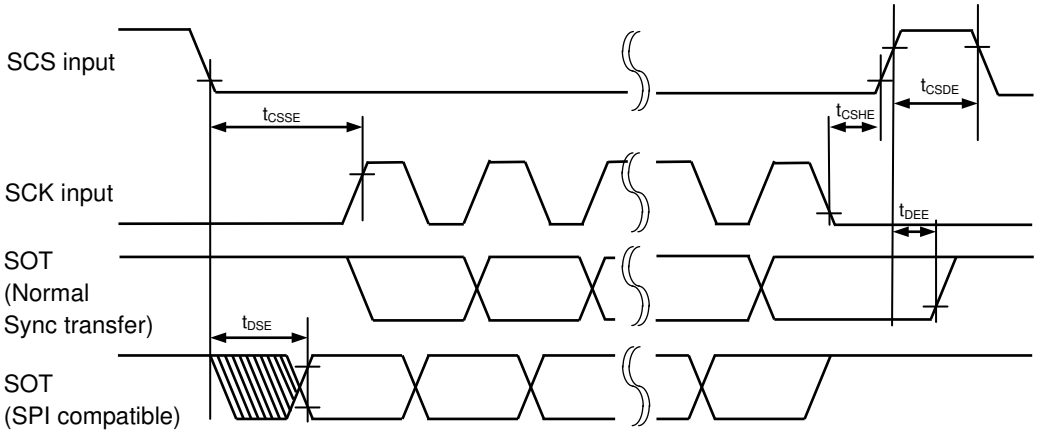
[3]: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

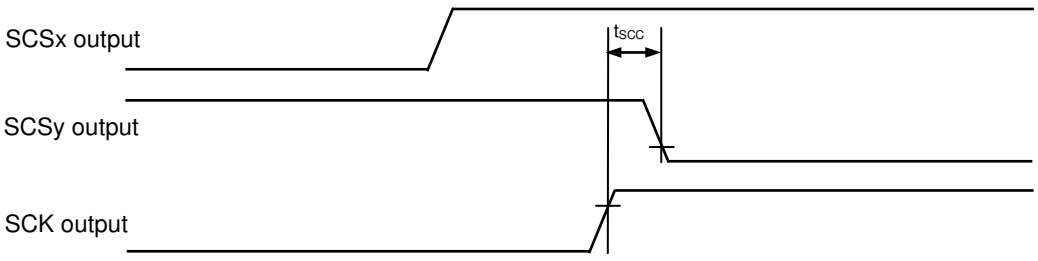
Please see the hardware manual for details of above-mentioned [1], [2], [3]



When Serial chip select is used, Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode



When Serial chip select is used, Serial clock output mark level "L",
Serial chip select Inactive level "H"
External shift clock mode



When Serial chip select is used, Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

11.4.5.1.7 Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,

When Serial chip select is used : SCSCR:CSEN=1,

Serial clock output mark level "H" : SMR, SCSFR:SCINV=0,

Serial chip select Inactive level "L" : SCSCR, SCSFR:CSLVL=0

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↓ setup time	t_{CSSI}	SCK0 to SCK2, SCS00, SCS01, SCS10, SCS11, SCS20, SCS21	-	t_{CSSU}+0 [1]	t_{CSSU}+50 [1]	ns	Internal shift clock mode output pin : C_L=50pF
SCK↑→SCS↓ hold time	t_{CSHI}			t_{CSHD}-50 [2]	t_{CSHD}+0 [2]	ns	
SCS deselect time	t_{CSDI}	SCS00, SCS01, SCS10, SCS11, SCS20, SCS21		t_{CSDS}-50 [3]	t_{CSDS}+50 [3]	ns	
SCS↑→SCK↓ setup time	t_{CSSE}	SCK0 to SCK2, SCS00, SCS01, SCS10, SCS11, SCS20, SCS21	-	3t_{CPP}+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↑→SCS↓ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS00, SCS01, SCS10, SCS11, SCS20, SCS21		3t_{CPP}+30	-	ns	
SCS↑→SOT delay time	t_{DSE}	SCS00, SCS01, SCS10, SCS11, SCS20, SCS21, SOT0 to SOT2		-	40	ns	
SCS↓→SOT delay time	t_{DEE}			+0	-	ns	
SCK↓→SCS↑ clock switch time	t_{SCC}	SCK0 to SCK2, SCS00, SCS01, SCS10, SCS11, SCS20, SCS21	-	3t_{CPP}+0	3t_{CPP}+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF

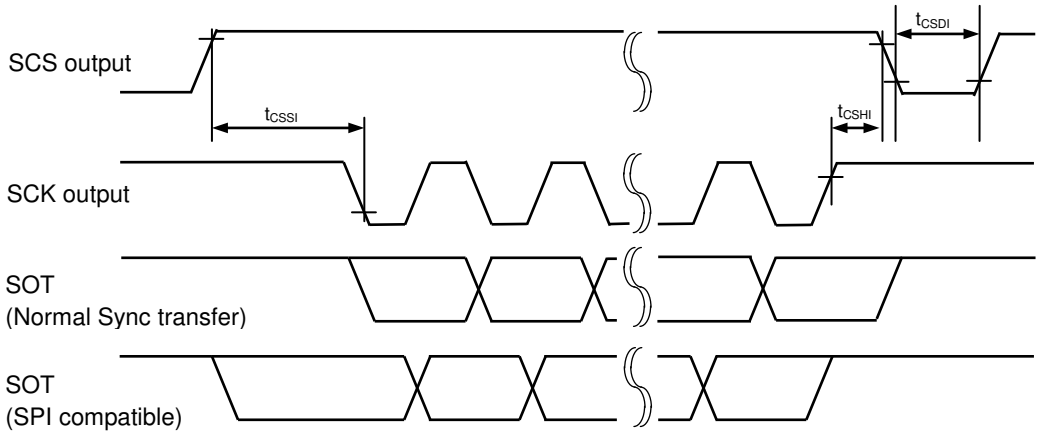
[1]: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock

[2]: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock

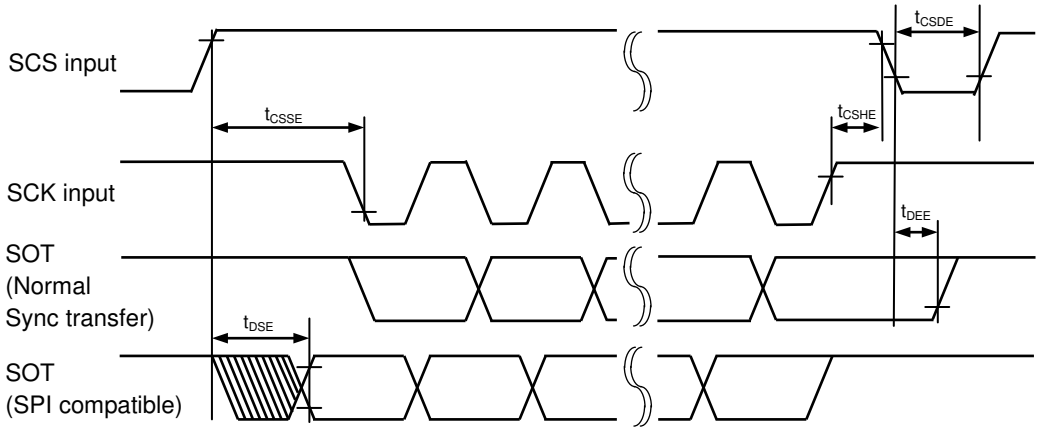
[3]: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

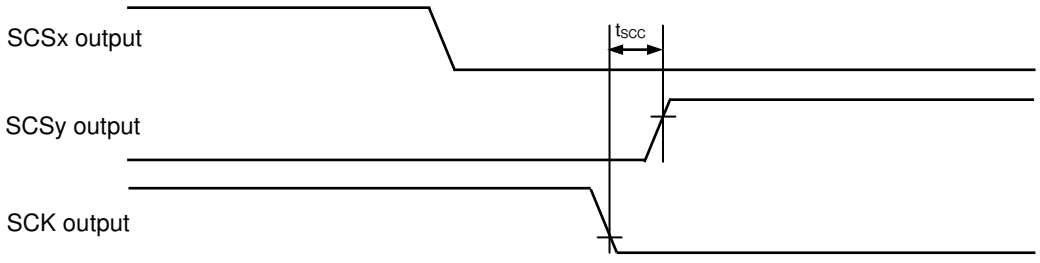
Please see the hardware manual for details of above-mentioned [1], [2] and [3]



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
External shift clock mode



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode , Example of switching clock by round operation (x, y=0, 1, 2, 3)

11.4.5.1.8 Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,

When Serial chip select is used: SCSCR: CSEN=1,

Serial clock output mark level "L" : SMR, SCSFR:SCINV=1,

Serial chip select Inactive level "L" : SCSCR, SCSFR:CSLVL=0

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↑ setup time	t_{CSSI}	SCK0 to SCK2, SCS00, SCS01, SCS10, SCS11, SCS20, SCS21	-	t_{CSSU}+0 [1]	t_{CSSU}+50 [1]	ns	Internal shift clock mode output pin : C_L=50pF
SCK↓→SCS↓ hold time	t_{CSHI}			t_{CSHD}-50 [2]	t_{CSHD}+0 [2]	ns	
SCS deselect time	t_{CSDI}	SCS00, SCS01, SCS10, SCS11, SCS20, SCS21		t_{CSDS}-50 [3]	t_{CSDS}+50 [3]	ns	
SCS↑→SCK↑ setup time	t_{CSSE}	SCK0 to SCK2, SCS00, SCS01, SCS10, SCS11, SCS20, SCS21	-	3t_{CPP}+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↓→SCS↓ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS00, SCS01, SCS10, SCS11, SCS20, SCS21		3t_{CPP}+30	-	ns	
SCS↑→SOT delay time	t_{DSE}	SCS00, SCS01, SCS10, SCS11, SCS20, SCS21, SOT0 to SOT2		-	40	ns	
SCS↓→SOT delay time	t_{DEE}			+0	-	ns	
SCK↑→SCS↑ clock switch time	t_{SCC}	SCK0 to SCK2, SCS00, SCS01, SCS10, SCS11, SCS20, SCS21	-	3t_{CPP}+0	3t_{CPP}+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF

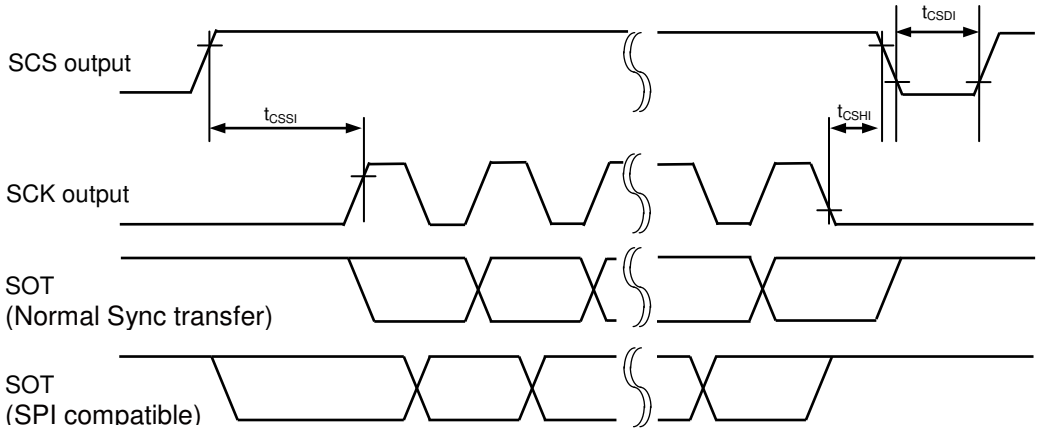
[1]: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock

[2]: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock

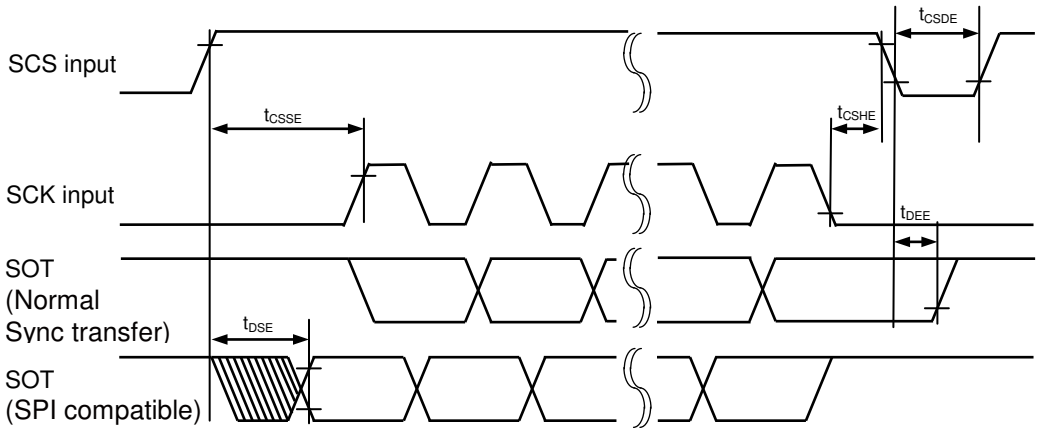
[3]: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

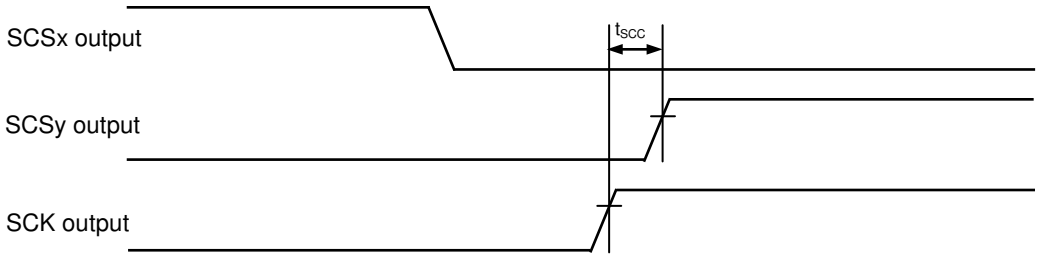
Please see the hardware manual for details of above-mentioned [1], [2], and [3].



When Serial chip select is used, Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode



When Serial chip select is used, Serial clock output mark level "L",
Serial chip select Inactive level "L"
Slave mode



When Serial chip select is used, Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode. Example of switching clock by round operation (x, y=0, 1, 2, 3)

11.4.5.2 UART (Asynchronous serial interface) timing

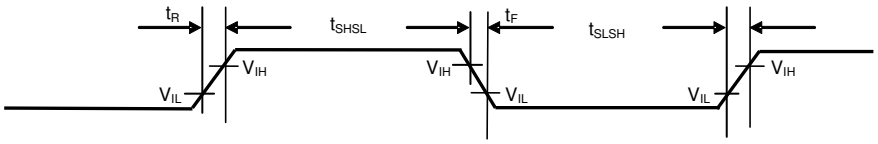
Bit setting: SMR : MD2=0, SMR:MD1=0, SMR : MD0=0

Bit setting: SMR : MD2=0, SMR:MD1=0, SMR : MD0=1

When external clock is selected (BGR: EXT=1)

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK2	-	t_{CPP}+10	-	ns	output pin: C_L=50pF
Serial clock "H"pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



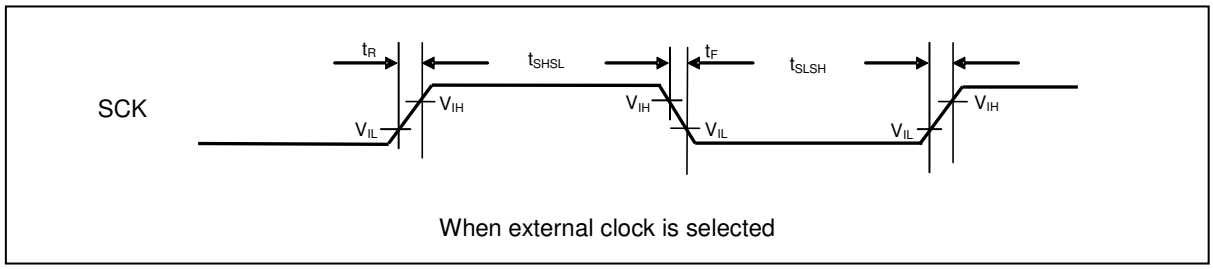
When external clock is selected

11.4.5.3 LIN Interface (v2.1) (Asynchronous Serial Interface for LIN (v2.1)) timing

Bit setting: SMR: MD2=0, SMR:MD1=1, SMR : MD0=1

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK2	-	t_{CPP}+10	-	ns	output pin: C_L=50pF
Serial clock "H"pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



When external clock is selected

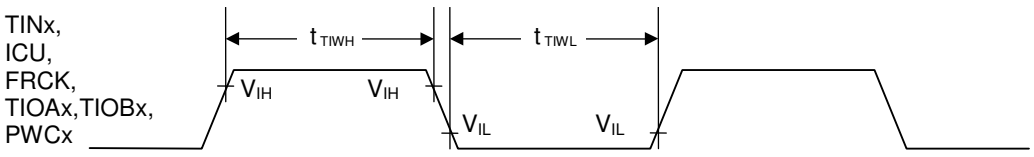
11.4.6 Timer input timing

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIN0 to TIN4, ICU, FRCK, TIOA0 to TIOA3, TIOB0 to TIOB3,	-	$4t_{CPP}$	-	ns	
		PWC0, PWC1	-	$4t_{CP}$[1]	-	ns	

[1]: In the case of digital LPF of PWC with buffers is setting as through.

Timer input timing

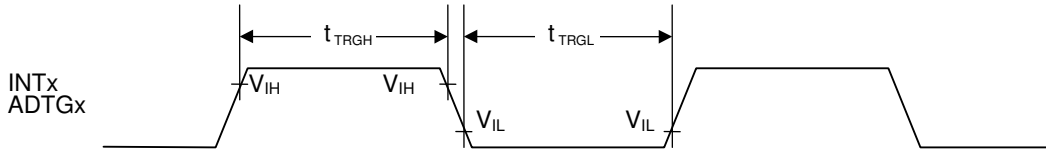


11.4.7 Trigger input timing

(T_A:-40°C + 125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT3	-	$5t_{CPP}$	-	ns	
				1	-	µs	At stop mode
		ADTG0	-	$5t_{CPP}$	-	ns	
		ADTG1	-	$5t_{CP}$	-	ns	

Trigger input timing

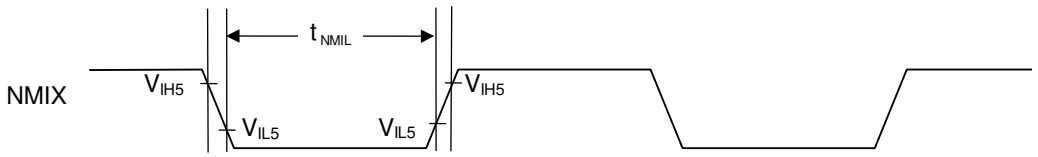


11.4.8 NMI input timing

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	-	$4t_{CPP}$	-	ns	

NMIX input timing



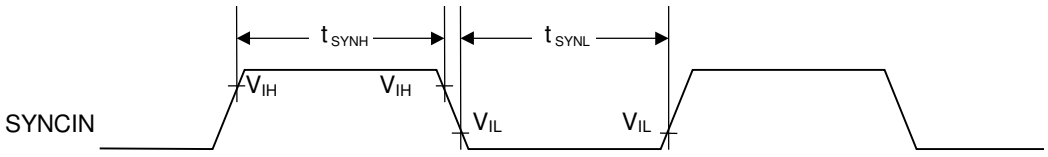
11.4.9 PWM

11.4.9.1 SYNCIN input timing

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{SYNH}, t_{SYNL}	SYNCIN	-	16 t_{CPWMD}	-	ns	[1]

SYNCIN input timing



[1]: In the case of digital LPF of SYNCIN pin is setting as through.

11.4.9.2 PWM output

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
CMPn⇒ PWMnH/PWMnL Delay time	t_{CPD}	CMP0 to CMP2 PWM0H to PWM2H PWM0L to PWM2L		-	100	ns	n=0, 1, 2 [1]
Min pulse width	tpw	PWM0H to PWM2H PWM0L to PWM2L		40	-	ns	[1]

[1]: In the case of PWM division clock is 200MHz

11.4.10 Low voltage detection (External low-voltage detection)

(T_A:-40°C to +125°C, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{DP5}	VCC	-	3.7	-	5.5	V	
Detection voltage	V_{DL}		[1]	-8%	3.9	+8%	V	When power-supply voltage falls and detection level is set initially
Hysteresis width	V_{HYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	Td	-		-	-	30	µs	
Power supply voltage regulation	-	VCC	-	-2	-	2	V/ms	[2]

[1]: If the fluctuation of the power supply is faster than the low-voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

[2]: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low-voltage detection by detecting voltage (V_{DL}).

11.4.11 Low voltage detection (Internal low-voltage detection)

(T_A:-40°C to +125°C, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	-	-	0.6	-	1.4	V	
Detection voltage	V_{RDL}		[1]	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V_{RHYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	-	-		-	-	30	µs	

[1]: If the fluctuation of the power supply is faster than the low-voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

11.5 A/D Converter

11.5.1 12-bit A/D Converter Electrical Characteristics

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total error	-	-	-	-	±6.0	LSB	
Linearity error	-	-	-	-	±4.0	LSB	
Differential linearity error	-	-	-	-	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL+0.5LSB -8mV	-	AVRL+0.5LSB +8mV	V	1LSB= (V_{FST}-V_{OT})/ 4094
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVRH-1.5LSB -8mV	-	AVRH-1.5LSB +8mV	V	
Sampling time	t_{SMP}	-	0.3	-	-	µs	[1] [3]
Compare time	t_{CMP}	-	0.7	-	28	µs	[1]
A/D conversion time	t_{CNV}	-	1.0	-	-	µs	[1]
Analog port input current	I_{AIN}	AN0 to AN7	-2.0	-	+2.0	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN7	AVRL	-	AVRH	V	
Reference voltage	AVRH	AVRH0	4.5	-	5.5	V	
	AVRL	AVRL0	-	0.0	-	V	
Power supply current	I_A	AVCC0	-	0.5	0.69	mA	
	I_{AH}		-	-	6.1	µA	[2]
	I_R	AVRH0	-	1	1.96	mA	
	I_{RH}		-	-	4.0	µA	[2]
Variation between channels	-	AN0 to AN7	-	-	4	LSB	

[1]: Time for each channel.

[2]: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

[3]: external impedance is 500Ω or less.

11.5.2 12-bit A/D Converter (4-channel simultaneous sampling) Electrical Characteristics

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total error	-	-	-	-	±6.0	LSB	
Linearity error	-	-	-	-	±4.0	LSB	
Differential linearity error	-	-	-	-	±1.9	LSB	
Zero transition voltage	V_{OT}	AN8 to AN11	AVRL+0.5LSB -8mV	-	AVRL+0.5LSB +8mV	V	1LSB= (V_{FST}-V_{OT})/ 4094
Full-scale transition voltage	V_{FST}	AN8 to AN11	AVRH-1.5LSB -8mV	-	AVRH-1.5LSB +8mV	V	
Sampling time	t_{SMP}	-	0.35	-	-	µs	[3]
Compare time	t_{CMP}	-	1.4	-	5.6	µs	[1]
A/D conversion time	t_{CNV}	-	1.75	-	-	µs	[1]
Analog port input current	I_{AIN}	AN8 to AN11	-1.0	-	+1.0	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN8 to AN11	AVRL	-	AVRH	V	
Reference voltage	AVRH	AVRH1	4.5	-	5.5	V	
	AVRL	AVRL1	-	0.0	-	V	
Power supply current	I_A	AVCC1	-	1.0	1.5	mA	
	I_{AH}		-	0.1	20	µA	[2]
	I_R	AVRH1	-	2	4	mA	
	I_{RH}		-	0.1	10	µA	[2]
Decoupling capacitance	C_{REF}	connected to VR1	1	-	-	µF	
Resumption Time	t_{RS}	-	10.9	-	-	ms	[4] [5]

[1]: Conversion time of 4-channel.

[2]: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

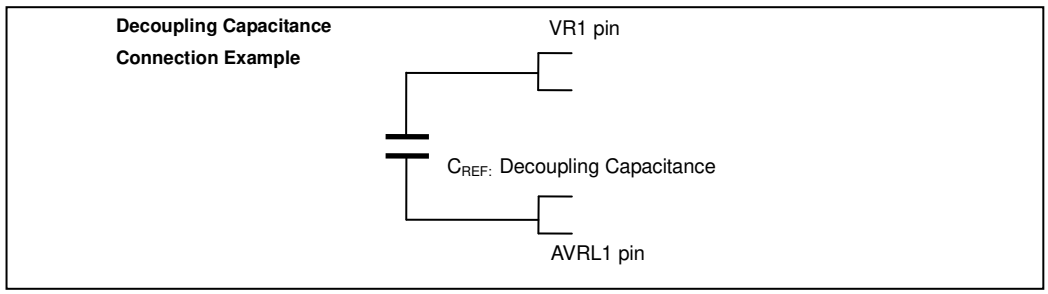
[3]: external impedance is 500Ω or less.

[4]: Calculate the minimum value by decoupling capacitance, the others parasitic capacitance value is defined as 0.

[5]: Resumption time is defined by the capacitance of the decoupling capacitance which connected to the pin VR1.

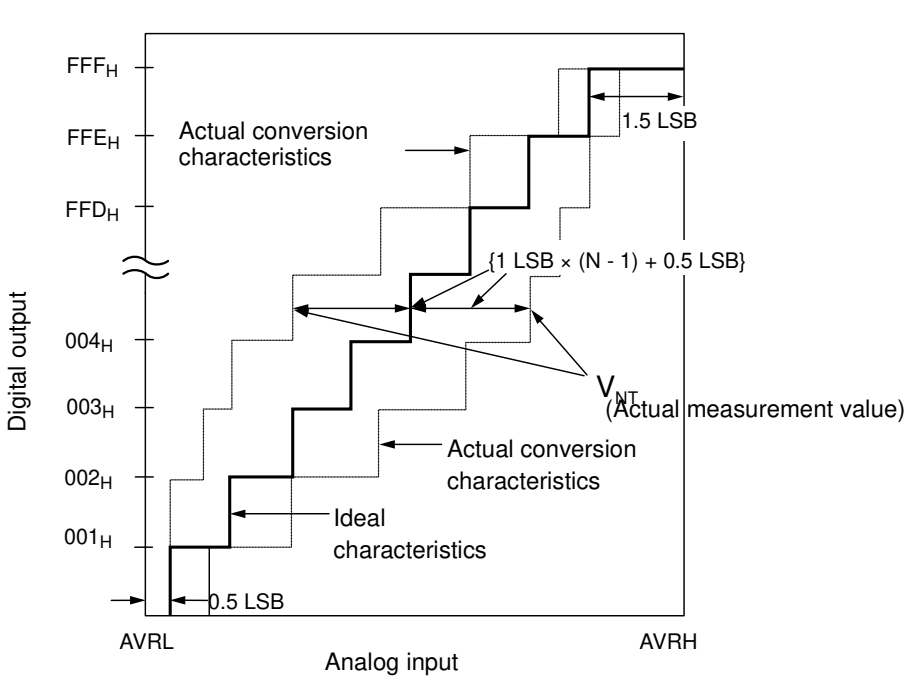
Resumption Time=9*C_{REF}*1.2k + 1µ[s]

C_{REF} :VR Decoupling capacitance [µF]



11.5.3 Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000"← →"0000 0000 0001") to the full-scale transition point ("1111 1111 1110"← →"1111 1111 1111").
- Differential linearity error : Deviation of the input voltage from the ideal value that is required to change the output code by LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linearity error.



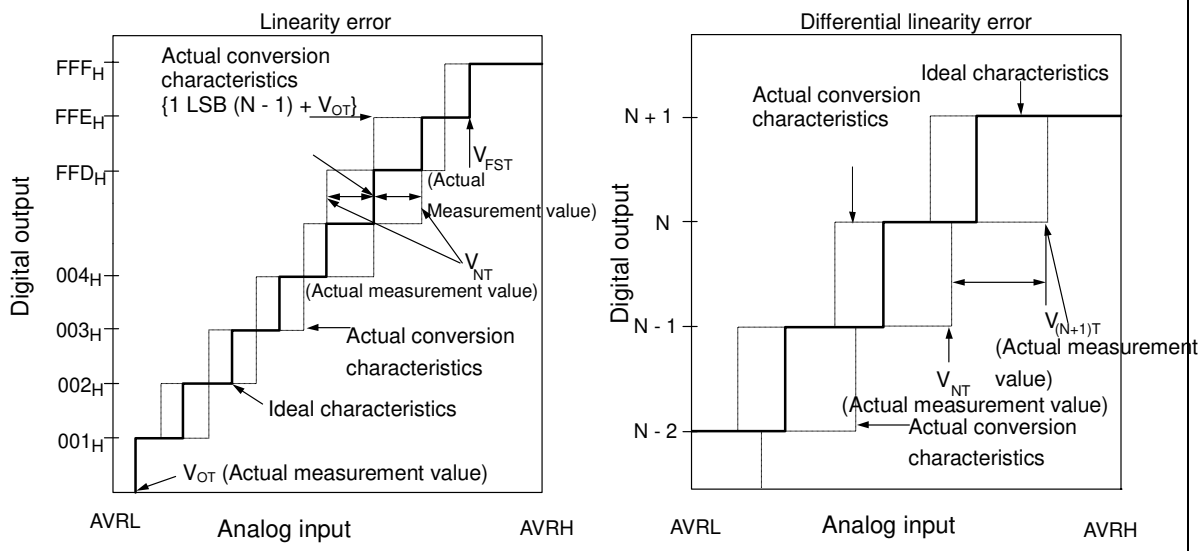
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1LSB \times (N-1) + V_{OT}\ \ LSB\}}{1LSB} \quad [LSB]$$

$$\text{1LSB (Ideal value)} = \frac{AVRH - AVRL}{4096} \quad [V]$$

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : Digital output is the voltage which transitions from (N - 1) to N.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \quad [LSB]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1\ LSB \quad [LSB]$$

$$1LSB = \frac{V_{FST} - V_{OT}}{4094} \quad [V]$$

V_{OT}: Voltage at which the digital output changes from "000_H" to "001_H".

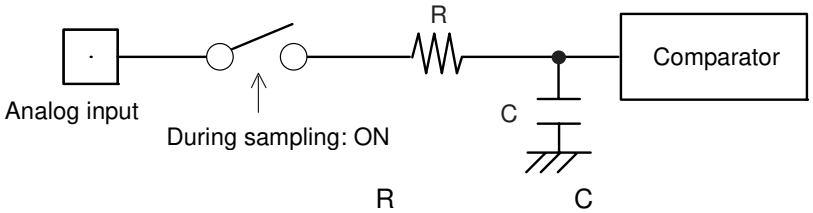
V_{FST} : Voltage at which the digital output changes from "FFE_H" to "FFF_H".

11.5.4 Notes on Using A/D Converter

About the output impedance of the analog input of external circuit

When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

Analog input circuit model



	R	C	
12bit A/D	2.0kΩ(Max)	11.65pF(Max)	(4.5V ≤ AV_{CC} ≤ 5.5V)
12bit A/D(4-channel simultaneous sampling)	5.0kΩ(Max)	11.0pF(Max)	(4.5V ≤ AV_{CC} ≤ 5.5V)

Note: Listed values must be considered as reference values.

11.6 Flash memory

11.6.1 Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	200	800	ms	8 Kbytes sector[1], excluding internal preprogramming time
	-	300	1100	ms	8 Kbytes sector[1], including internal preprogramming time
	-	400	2000	ms	64 Kbytes sector[1], excluding internal preprogramming time
	-	700	3700	ms	64 Kbytes sector[1], including internal preprogramming time
8-bit writing time	-	9	288	µs	Exclusive of overhead time at system level[1]
16-bit writing time	-	12	384	µs	Exclusive of overhead time at system level[1]
ECC writing time	-	9	288	µs	Exclusive of overhead time at system level[1]
Erase cycle[2]/Data retain time	1,000 cycles/20 years, 10,000 cycles/10 years, 100,000 cycles/5 years	-	-	-	Temperature at writing/erasing Tj<+105°C, Average T_A=+85°C[3]

[1]: The guaranteed value for erasure up to 100,000 cycles.

[2]: Number of erase cycles for each sector.

[3]: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

11.6.2 Notes

While the Flash memory is written or erased, shutdown of the external power (Vcc) is prohibited.

In the application system where Vcc might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}[1]), hold Vcc at 2.7V or more within the duration calculated by the following expression:

Td*[µs] + (period of PCLK [µs] × 257) + 50 [µs]

[1]: See “11.4 AC Characteristics 11.4.9 Low voltage detection (External low-voltage detection)”

11.7 D/A converter

(T_A:-40°C to +125°C, V_{CC}=5.0V±10%, AVcc2=5.0V±1.5%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	-	-	-	-	-	10	Bit	
Linearity error	-	-	-	-4		4	LSB	
Differential non-linearity error	-	-	-	-0.9	-	0.9	LSB	
conversion time	-	-	-	-	-	200	ns	C_{OUT}=5pF[1]
Power supply current [2]	IA	AVCC2	-	-	475	600	µA	Each channel
	IAH	AVCC2	-	-	-	21	µA	When powerdown Each channel

[1]: capacitance of internal node

[2]: The power supply current described only current value on D/A converter.

The power supply current of AVCC2 = 3 unit × (the power supply current of D/A converter) + 3 unit × (the power supply current of comparator) + (the power supply current of slope compensation).

11.8 Comparator

(T_A:-40°C to +125°C, V_{CC}=5.0V±10%, AVcc2=5.0V±1.5%V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input voltage	-	-	-	0	-	AVcc2-1	V	
Compare time	-	-	-	-	-	t_{CCMP}	ns	[1]
Power down delay time	-	-	-	-	-	50	ns	
Power supply current [2]	IA	AVCC2	-	-	565	785	µA	Each channel
	IAH	AVCC2	-	-	0.2	2.5	µA	When powerdown Each channel
Input offset voltage	-	CMP0 CMP1 CMP2	-	-12	-	12	mV	

[1]: t_{CCMP} is comparator clock cycle time.

[2]: The power supply current described only current value on D/A converter.

The power supply current of AVCC2 = 3 unit × (the power supply current of D/A converter) + 3 unit × (the power supply current of comparator) + the power supply current of slope compensation).

11.9 Slope compensation

(T_A:-40°C to +125°C, V_{CC}=5.0V±10%, $AV_{CC}2$=5.0V±1.5%, V_{SS}=$AV_{SS}2$=0.0V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Slope voltage	V_{slope}	(Vslope) [1]	-	0	-	AVcc2-1	V	[2]
				0.5	-	2.0	V	CTSI base
Operation cycle	T	(Vslope) [1]		2	-	10	µs	
Slope amount	dV_{slope}/dt	(Vslope) [1]	-	0.05	-	1.0	V/µs	
Slope output resolution	-	(Vslope) [1]	[3]	-10	-	+10	%	[5]
			[4]	-14	-	+14	%	
OFF time	t_{off}	(Vslope) [1]	-	200	-	-	ns	
Switching stability time of slope amount	-	-	-	-	-	10	µs	[6]
PD return time	-		-	-	-	20	µs	
Power supply current [8]	I_A	AVCC2	-	-	500	900	µA	
	I_{AH}	AVCC2	-	-	0.01	33	µA	When power down
Slope transmission error	-	CMP0	-	-3	-	+3	%	[7]
ESD resistance	-	CMP0	-	700	800	900	Ω	
SWS on resistance	-	-	-	-	-	7	kΩ	
SWE on resistance	-	-	-	-	-	20	Ω	
SWI on resistance	-	-	-	-	-	600	Ω	

[1]: (Vslope) is Voltage of internal node.

[2]: Please do not let the total of external voltage input from slope voltage and CMP0 exceeds AVcc2-1[V]. Besides, if reference voltage of the comparator is AVcc2-1 [V] or less, we do not erroneously judged even if the slope voltage is more than AVcc2-1 [V].

[3]: 1.0V/µs ≥ dV_{slope}/dt ≥ 0.1V/µs, 2.0V ≥ V_{slope} ≥ 0.5V, or voltage of internal node CTSI is defined as the reference.

[4]: 0.05V/µs ≤ dV_{slope}/dt<0.1V/µs, 2.0V ≥V_{slope} ≥ 0.5V, or voltage of internal node CTSI is defined as the reference.

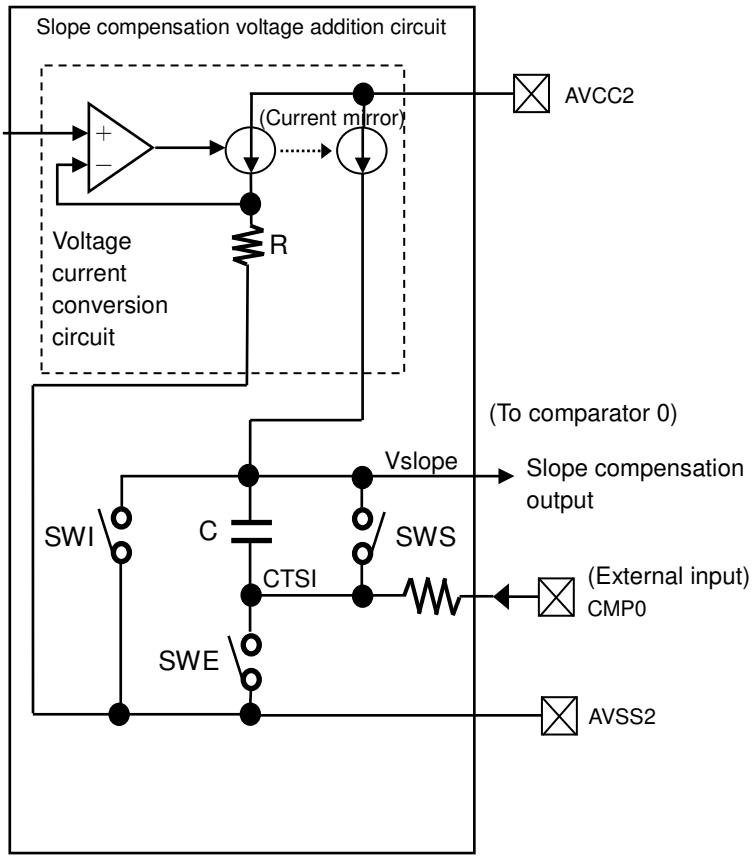
[5]: slope output resolution is the specification when calibration was performed. Calibration condition is dVslope/dt=0.4V/µs.

[6]: When SLPDADR register is switching

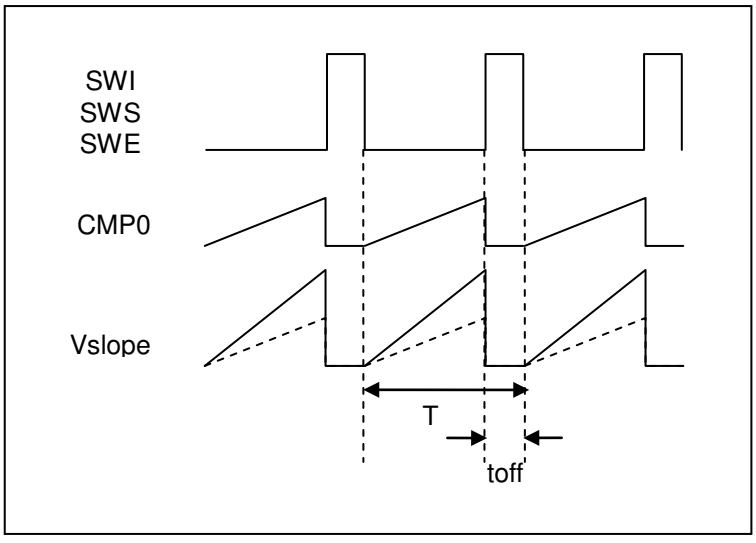
[7]: Slope transmission error is the specification when calibration was performed. Calibration condition is correction voltage is 3.0V, voltage lower limits is 1.0V.

[8]: The power supply current described only current value on D/A converter.

The power supply current of AVCC2 = 3 unit × (the power supply current of D/A converter) + 3 unit × (the power supply current of comparator) + (the power supply current of slope compensation).

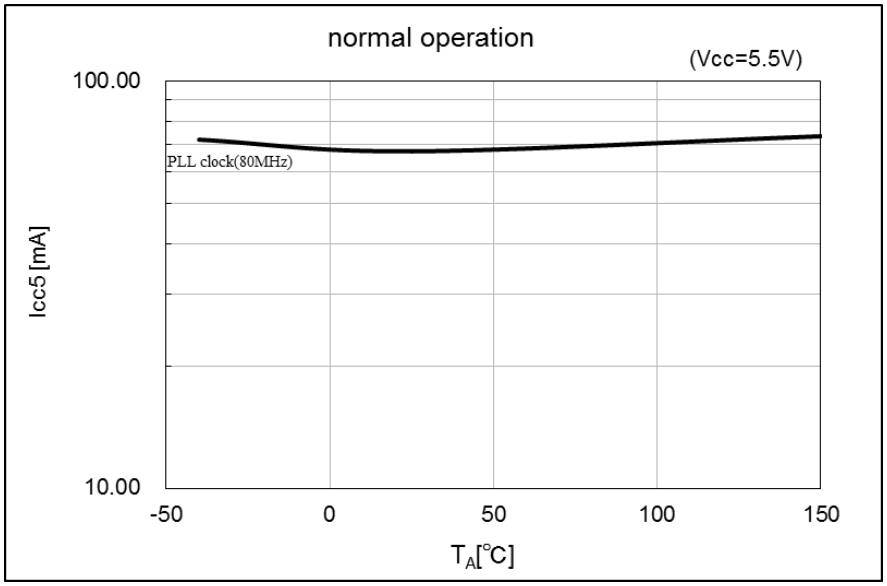


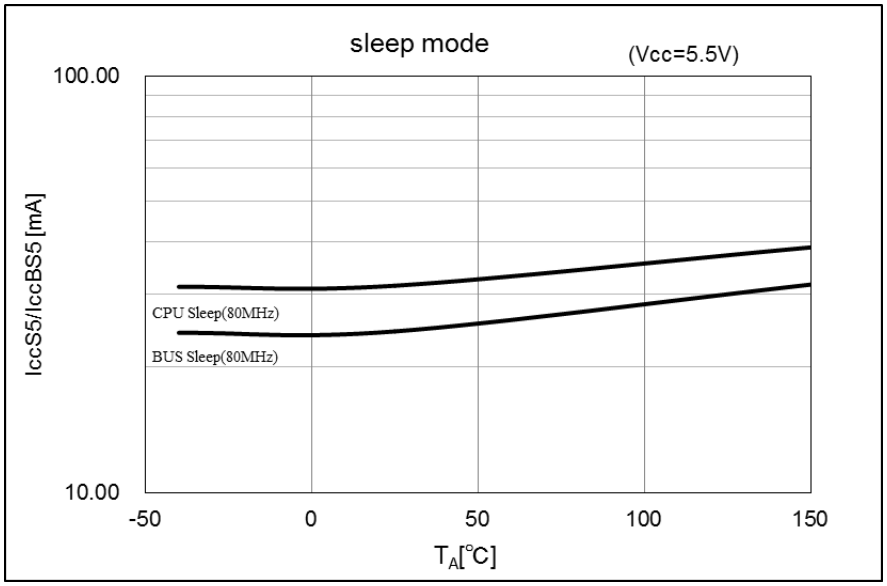
Operation cycle T/Off time toff

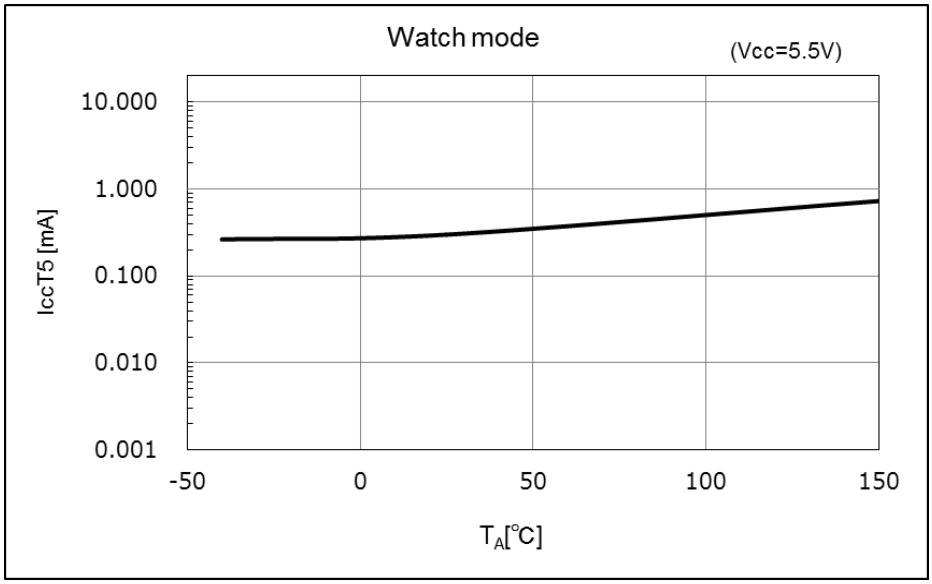


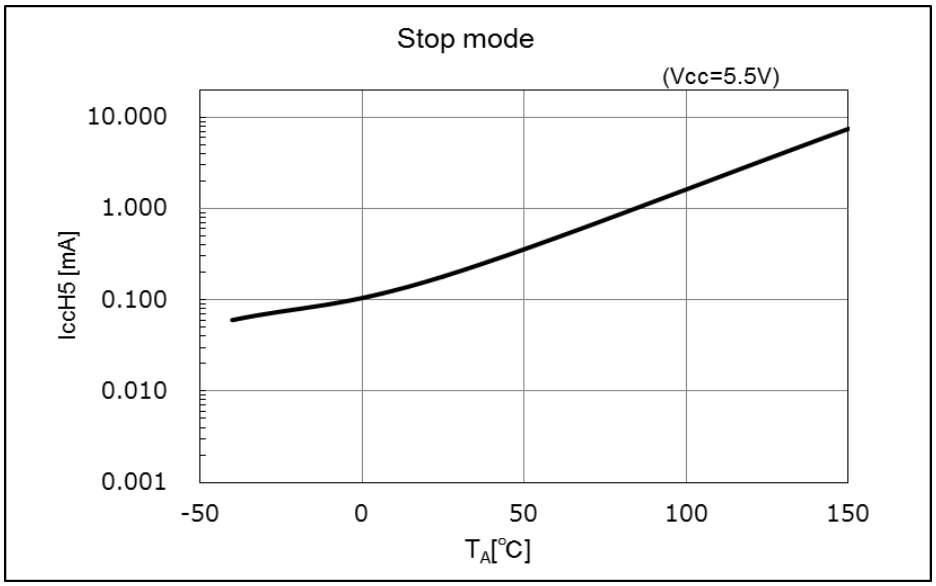
12. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.






Watch mode
(Vcc=5.5V)
10.000
1.000
0.100
0.010
0.001
IccT5 [mA]
-50
0
50
100
150
TA[°C]


Stop mode
(Vcc=5.5V)
10.000
1.000
0.100
0.010
0.001
IccH5 [mA]
-50
0
50
100
150
TA[°C]

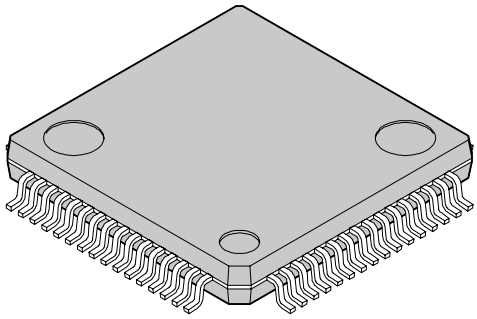
13. Ordering Information

Part number	Package*
MB91F552PMC1-GTE1	LQFP・64 pin, Plastic (FPT-64P-M24)

*: For details of the package, see "Package Dimensions".

14. Package Dimensions

64-pin plastic LQFP

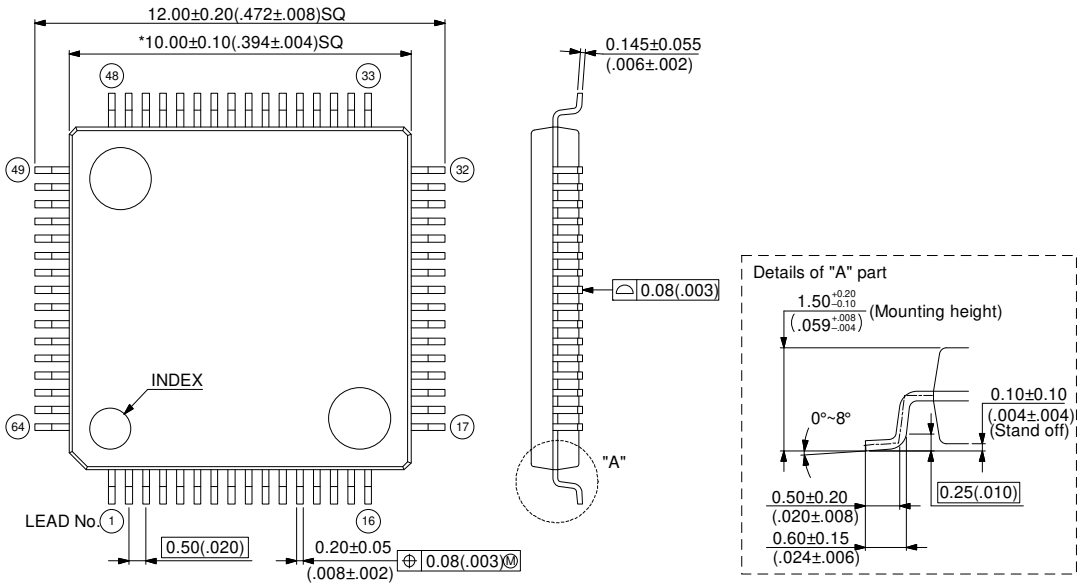


(FPT-64P-M24)

Lead pitch	0.50 mm
Package width × package length	10.0 × 10.0 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.32 g
Code (Reference)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values

15. Major Changes

Spansion Publication Number: MB91F552_DS705-00015

Page	Section	Change Results
Revision 1.0		
-	-	Initial release

NOTE: Please see "Document History" for later revised information.

Document History

Document Title: MB91550 Series, MB91F552, FR Family FR81S, 32-bit Microcontroller
Document Number: 002-04667

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	HIHA	04/25/2014	Migrated to Cypress and assigned document number 002-04667. No change to document contents or format.
*A	5179093	HIHA	03/17/2016	Updated to Cypress template

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