

N-Channel Enhancement Mode Power MOSFET

Description

The RM10N100S8 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

V_{DS} = 100V,I_D =10A

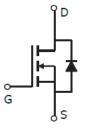
 $R_{DS(ON)}$ < 14m Ω @ V_{GS} =10V

 $R_{DS(ON)}$ < 21m Ω @ V_{GS} =4.5V

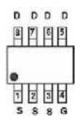
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current

Application

- DC/DC Primary Side Switch
- Telecom/Server
- Synchronous Rectification
- Halogen-free



Schematic diagram



Marking and pin assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
10N100	RM10N100S8	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings (T_A=25 ℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _G s	±20	V
Drain Current-Continuous	I _D	10	А
Drain Current-Continuous(T _C =100℃)	I _D (100℃)	7	А
Pulsed Drain Current	I _{DM}	70	А
Maximum Power Dissipation	P _D	3.1	W
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55 To 150	$^{\circ}$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	R _{θJA}	40	°C/W

Electrical Characteristics (T_A=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics				,		
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V,V _{GS} =0V	-	-	1	μΑ
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note2)			'			
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1.0	1.5	2.5	V
Drain-Source On-State Resistance	Б	V _{GS} =10V, I _D =10A	-	12	14	mΩ
	R _{DS(ON)}	V _{GS} =4.5V, I _D =10A	-	18	21	mΩ
Forward Transconductance	g FS	V _{DS} =10V,I _D =10A	-	10	-	S
Dynamic Characteristics (Note3)						
Input Capacitance	C _{lss}	., 50,(), 0,(-	1640	-	PF
Output Capacitance	Coss	V_{DS} =50V, V_{GS} =0V, F=1.0MHz	-	240	-	PF
Reverse Transfer Capacitance	C _{rss}	F=1.UMHZ	-	4	-	PF
Switching Characteristics (Note 3)			1			
Turn-on Delay Time	t _{d(on)}		-	14.2	-	nS
Turn-on Rise Time	t _r	V_{DD} =50V, I_D =1A, R_L =6 Ω ,	-	20.8	-	nS
Turn-Off Delay Time	t _{d(off)}	$R_G=1\Omega,V_{GS}=10V$	-	42	-	nS
Turn-Off Fall Time	t _f		-	30	-	nS
Total Gate Charge	Qg		-	27.8	-	nC
Gate-Source Charge	Q _{gs}	I _D =10A,V _{DD} =50V,V _{GS} =10V	-	3.5	-	nC
Gate-Drain Charge	Charge Q _{gd}		-	8.8	-	nC
Drain-Source Diode Characteristics	1	<u> </u>				1
Diode Forward Voltage (Note 2)	V _{SD}	V _{GS} =0V,I _S =10A	-	-	1.0	V

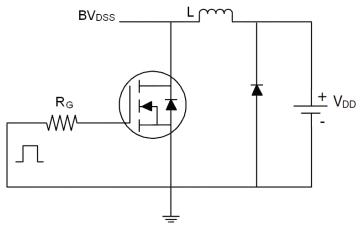
Notes:

- Repetitive Rating: Pulse width limited by maximum junction temperature.
 Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 3. Guaranteed by design, not subject to production

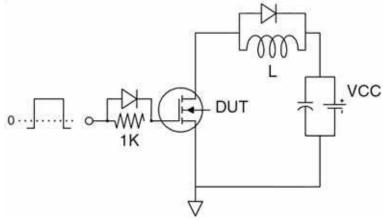


Test Circuit

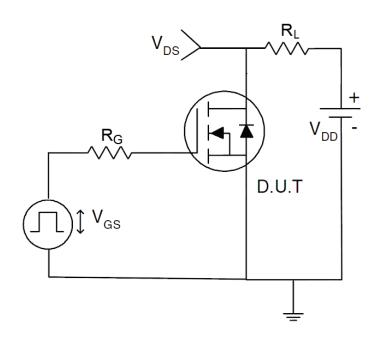
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit





RATING AND CHARACTERISTICS CURVES (RM10N100S8)

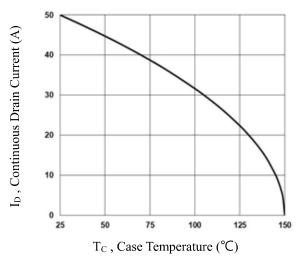


Fig.1 Continuous Drain Current vs. T_c

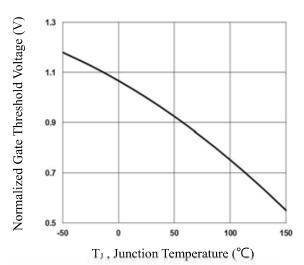


Fig.3 Normalized Vth vs. T_J

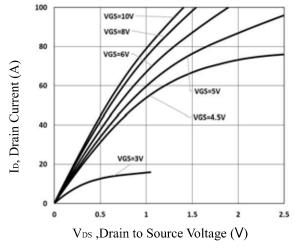


Fig.5 Typical Output Characteristics

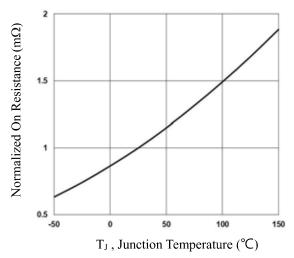


Fig.2 Normalized RDSON vs. TJ

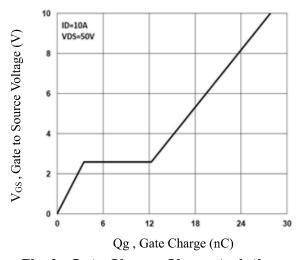


Fig.4 Gate Charge Characteristics

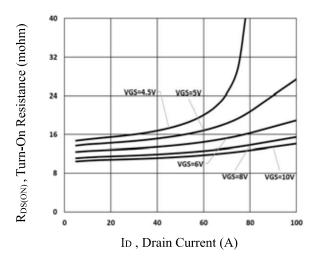


Fig.6 Turn-On Resistance vs. ID



RATING AND CHARACTERISTICS CURVES (RM10N100S8)

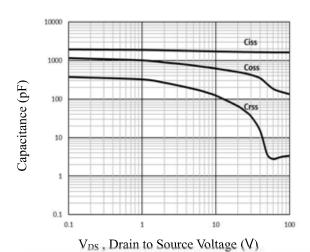


Fig.7 Capacitance Characteristics

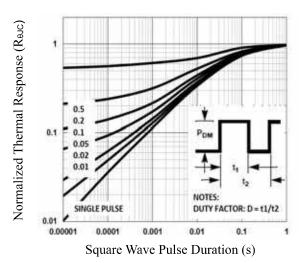


Fig.8 Normalized Transient Impedance

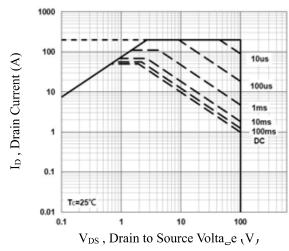


Fig.9 Maximum Safe Operation Area

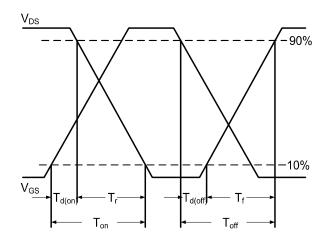


Fig.10 Switching Time Waveform

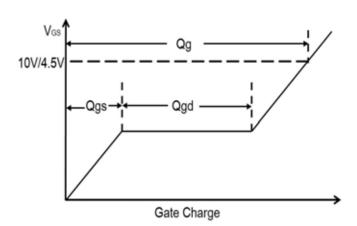
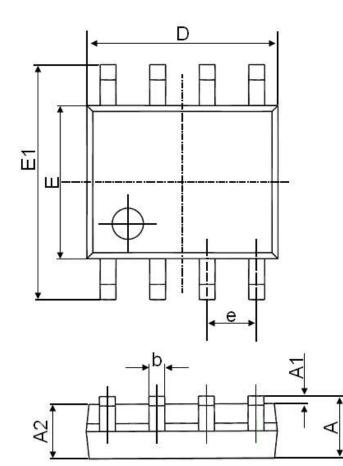
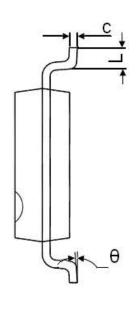


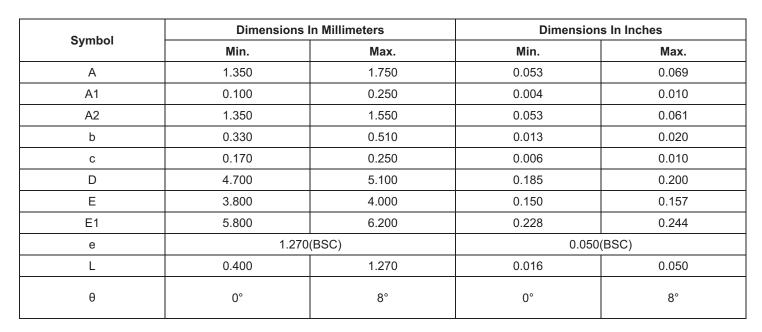
Fig.11 Gate Charge Waveform



SOP-8 Package Information









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