

**Industrial Grade low skew, 1-to-4 LVCMOS/LVTTL Fanout Buffer**

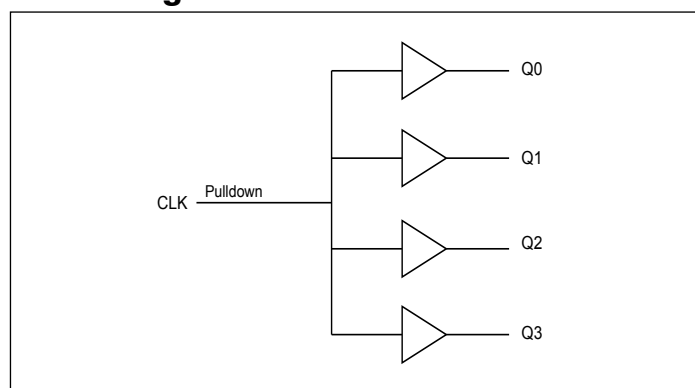
**Features**

- Four LVCMOS / LVTTL Outputs
- LVCMOS / LVTTL Clock Input
- CLK Accepts LVCMOS, LVTTL Input Levels
- Maximum Output Frequency: 200MHz
- Additive Phase Jitter, RMS: 0.173ps (Typical) @ 3.3V
- Output Skew: 45ps (Maximum) @ 3.3V
- Full 3.3V, 2.5V, 1.8V Operation Mode or 3.3V/2.5V/1.8V Core with 2.5V, 1.8V, 1.5V Supply Modes
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative.  
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green):
  - Small 8-pin SOIC(W) package saves board space

**Description**

The PI6C49CB04BJ is an industrial grade low-skew, 1-to-4 fanout buffer. Guaranteed output and part-to-part skew characteristics make the PI6C49CB04BJ ideal for clock distribution applications that demand well-defined performance and repeatability.

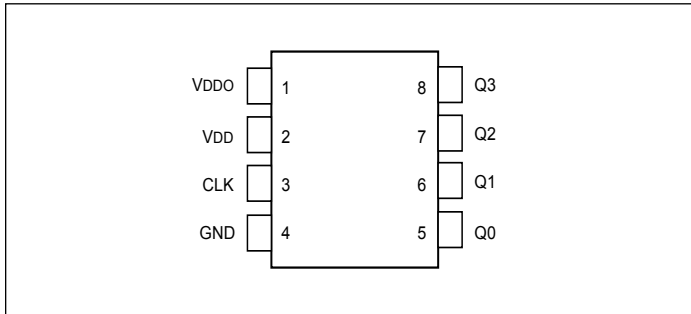
**Block Diagram**



**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Configuration



## Pin Descriptions

Pin#	Pin Name	Pin Type		Pin Description
1	V <sub>DDO</sub>	Power	—	Output supply pin
2	V <sub>DD</sub>	Power	—	Positive supply pin
3	CLK	Input	Pulldown	LVC MOS / LVTTL clock input
4	GND	Power	—	Power supply ground
5	Q0	Output	—	Single clock output. LVC MOS / LVTTL interface levels
6	Q1	Output	—	Single clock output. LVC MOS / LVTTL interface levels
7	Q2	Output	—	Single clock output. LVC MOS / LVTTL interface levels
8	Q3	Output	—	Single clock output. LVC MOS / LVTTL interface levels

Note: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

## Pin Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C <sub>IN</sub>	Input Capacitance	—	—	4	—	pF
C <sub>PD</sub>	Power Dissipation Capacitance (per Output)	V <sub>DD</sub> , V <sub>DDO</sub> = 3.465V	—	—	15	pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor	—	—	51	—	kΩ
R <sub>OUT</sub>	Output Impedance	V <sub>DD</sub> , V <sub>DDO</sub> > 2.5V	5	7	12	Ω

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage, $V_{DD}$ .....	4.6V
Inputs, $V_I$ .....	-0.5V to $V_{DD} + 0.5V$
Output, $V_O$ .....	-0.5V to $V_{DDO} + 0.5V$
Storage Temperature, $T_{STG}$ .....	-65°C to 150°C
ESD Protection (HBM).....	2000V
Junction Temperature .....	125 °C max

Note:  
Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40	—	+105	°C
Power Supply Voltage (Measured in Respect to GND)	+1.425	—	+3.6	V

## Power Supply DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Core Supply Voltage	3.3V Operation	3.0	3.3	3.6	V
		2.5V Operation	2.375	2.5	2.625	
		1.8V Operation	1.6	1.8	2.0	
VDDO	Output Power Supply Voltage	3.3V Supply	3.0	3.3	3.6	V
		2.5V Supply	2.375	2.5	2.625	
		1.8V Supply	1.6	1.8	2.0	
		1.5V Supply	1.425	1.5	1.575	
$I_{DD} + I_{DDO}$	Total Power Supply Current	5pF, 100MHz	—	—	38	mA

**DC Electrical Characteristics**
**VDD = 1.8V, VDDO = 1.5 V ±5%**, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage	—	1.7	1.8	1.89	V
VDDO	Output Operating Voltage	—	1.425	1.5	1.575	V
V <sub>IH</sub>	Input High Voltage	CLK <sup>(1)</sup>	0.9	—	3.6	V
V <sub>IL</sub>	Input Low Voltage	CLK <sup>(1)</sup>	—	—	0.575	V
I <sub>IH</sub>	Input High Current	CLK <sup>(1)</sup>	—	—	40	μA
I <sub>IL</sub>	Input Low Current	CLK <sup>(1)</sup>	—	—	1	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -6mA	0.95	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 6mA	—	—	0.45	V
IDD	Operating Supply Current	5pF, 160MHz	—	15	21	mA
		5pF, 100MHz	—	13	17	mA
		5pF, 50MHz	—	7	9	mA
		5pF, 25MHz	—	4	5.5	mA
Z <sub>O</sub>	Nominal Output Impedance	—	—	20	—	Ω
C <sub>IN</sub>	Input Capacitance	CLK	—	5	—	pF
I <sub>OS</sub>	Short-Circuit Current	—	—	±12	—	mA

Notes: 1. Nominal switching threshold is VDD/2.

**VDD, VDDO=1.8 V ±5%**, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD, VDDO	Operating Voltage	—	1.7	1.8	1.89	V
V <sub>IH</sub>	Input High Voltage	CLK <sup>(1)</sup>	1.1	—	3.6	V
V <sub>IL</sub>	Input Low Voltage	CLK <sup>(1)</sup>	—	—	0.6	V
I <sub>IH</sub>	Input High Current	CLK <sup>(1)</sup>	—	—	50	μA
I <sub>IL</sub>	Input Low Current	CLK <sup>(1)</sup>	—	—	1	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -8mA	1.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA	—	—	0.4	V
IDD	Operating Supply Current	5pF, 160MHz	—	22	28	mA
		5pF, 100MHz	—	17	21	mA
		5pF, 50MHz	—	9	12	mA
		5pF, 25MHz	—	5	7	mA
Z <sub>O</sub>	Nominal Output Impedance	—	—	20	—	Ω
C <sub>IN</sub>	Input Capacitance	CLK	—	5	—	pF
I <sub>OS</sub>	Short-Circuit Current	—	—	±20	—	mA

Notes: 1. Nominal switching threshold is VDD/2.

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**VDD, VDDO = 2.5 V ±5%**, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD, VDDO	Operating Voltage	—	2.375	2.5	2.625	V
V <sub>IH</sub>	Input High Voltage	CLK <sup>(1)</sup>	1.7	—	3.6	V
V <sub>IL</sub>	Input Low Voltage	CLK <sup>(1)</sup>	—	—	0.7	V
I <sub>IH</sub>	Input High Current	CLK <sup>(1)</sup>	—	—	60	μA
I <sub>IL</sub>	Input Low Current	CLK <sup>(1)</sup>	—	—	1	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -8mA	2	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA	—	—	0.4	V
IDD	Operating Supply Current	5pF, 100MHz	—	24	30	mA
		5pF, 50MHz	—	12	15	mA
		5pF, 25MHz	—	7	9	mA
Z <sub>O</sub>	Nominal Output Impedance	—	—	20	—	Ω
C <sub>IN</sub>	Input Capacitance	CLK	—	5	—	pF
I <sub>OS</sub>	Short-Circuit Current	—	—	±50	—	mA

Notes: 1. Nominal switching threshold is VDD/2.

**VDD, VDDO = 3.3 V ±10%**, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD, VDDO	Operating Voltage	—	3.0	3.3	3.6	V
V <sub>IH</sub>	Input High Voltage	CLK <sup>(1)</sup>	2.4	—	3.6	V
V <sub>IL</sub>	Input Low Voltage	CLK <sup>(1)</sup>	—	—	0.7	V
I <sub>IH</sub>	Input High Current	CLK <sup>(1)</sup>	—	—	85	μA
I <sub>IL</sub>	Input Low Current	CLK <sup>(1)</sup>	—	—	1	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -8 mA	2.8	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8 mA	—	—	0.2	V
IDD	Operating Supply Current	5pF, 100MHz	—	32	38	mA
		5pF, 50MHz	—	16	19	mA
		5pF, 25MHz	—	10	12	mA
Z <sub>O</sub>	Nominal Output Impedance	—	—	20	—	Ω
C <sub>IN</sub>	Input Capacitance	CLK	—	5	—	pF
I <sub>OS</sub>	Short-Circuit Current	—	—	±50	—	mA

Notes: 1. Nominal switching threshold is VDD/2.

### AC Electrical Characteristics

VDD = 1.8V, VDDO=1.5 V ±5%, Ambient temperature -40°C to +105° C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency	—	0	—	160	MHz
t <sub>OR</sub>	Output Rise Time	20% to 80%	—	1.0	1.5	ns
t <sub>OF</sub>	Output Fall Time	20% to 80%	—	1.0	1.5	ns
T <sub>PD</sub>	Propagation Delay (Note1)	—	2	3	5	ns
T <sub>SK</sub>	Output-to-Output Skew (Note2)	Rising edges at VDD/2	—	0	±250	ps

VDD, VDDO =1.8 V ±5%, Ambient temperature -40°C to +105° C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency	—	0	—	160	MHz
t <sub>OR</sub>	Output Rise Time	20% to 80%	—	1.0	1.5	ns
t <sub>OF</sub>	Output Fall Time	20% to 80%	—	1.0	1.5	ns
T <sub>PD</sub>	Propagation Delay (Note 1)	—	1.3	2	4	ns
T <sub>SK</sub>	Output-to-Output Skew (Note 2)	Rising edges at VDD/2	—	0	±250	ps
J <sub>ADD</sub>	Additive Jitter	@ 156.25MHz, 12k to 20MHz	—	0.1	—	ps

VDD, VDDO =2.5 V ±5%, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency	—	0	—	160	MHz
t <sub>OR</sub>	Output Rise Time	20% TO 80%	—	1.0	1.5	ns
t <sub>OF</sub>	Output Fall Time	20% TO 80%	—	1.0	1.5	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	—	0.8	1.5	3	ns
T <sub>SK</sub>	Output-to-Output Skew <sup>(2)</sup>	Rising edges at VDD/2	—	0	±250	ps
J <sub>ADD</sub>	Additive Jitter	@ 156.25MHz, 12k to 20MHz	—	0.05	—	ps

Notes:

1. With rail-to-rail input clock.
2. Between any two outputs with equal loading.

VDD, VDDO = 3.3 V ±10%, Ambient temperature -40°C to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency	—	0	—	100	MHz
t <sub>OR</sub>	Output Rise Time	20% TO 80%	—	1.0	1.5	ns
t <sub>OF</sub>	Output Fall Time	20% TO 80%	—	1.0	1.5	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	—	0.8	1.0	2.5	ns
T <sub>SK</sub>	Output-to-Output Skew <sup>(2)</sup>	Rising edges at VDD/2	—	0	±250	ps
J <sub>ADD</sub>	Additive Jitter	@ 156.25MHz, 12k to 20MHz	—	0.05	—	ps

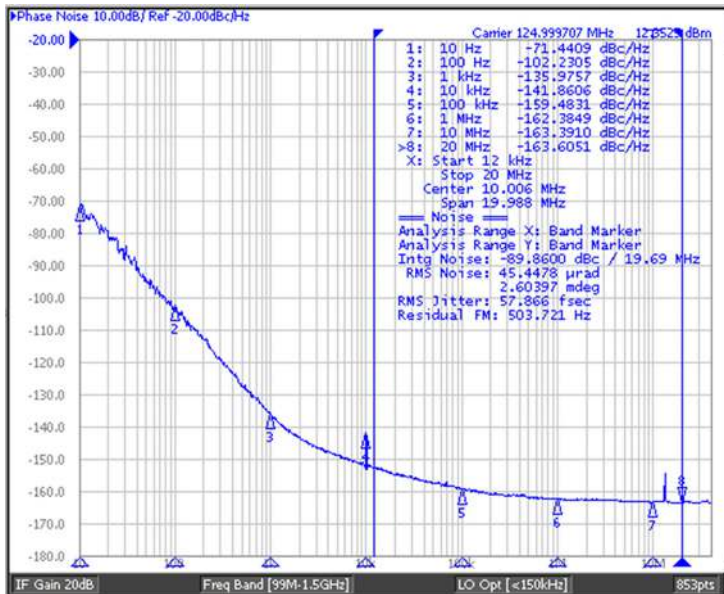
Notes:

1. With rail-to-rail input clock.
2. Between any two outputs with equal loading.

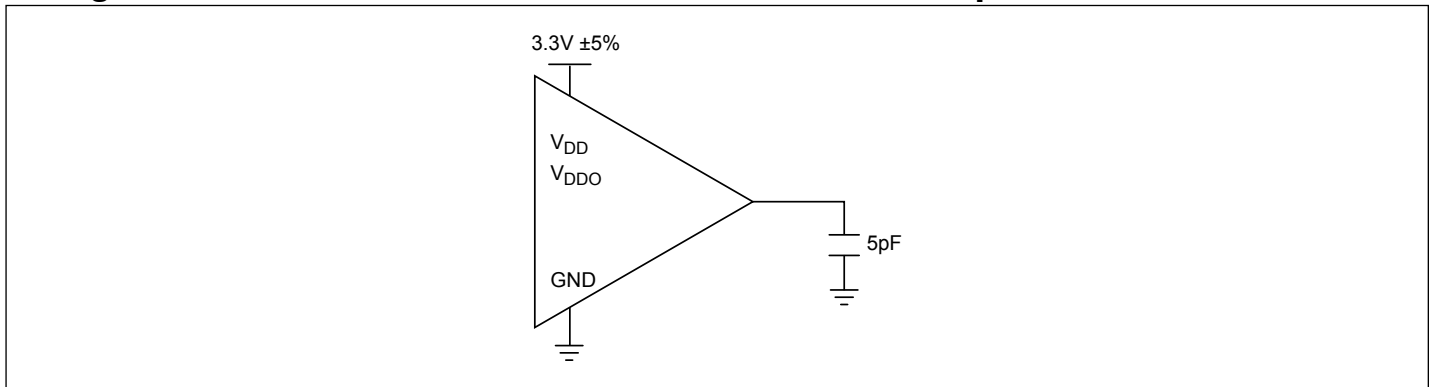
## Phase Noise and Additive Jitter

Output phase noise plot provided below.

$$\text{Additive jitter} = \sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$$



## Configuration Test Load Board Termination for LVCMOS Outputs



## Thermal Information

Symbol	Description	Condition	
$\Theta_{JA}$	Junction-to-Ambient Thermal Resistance	Still air	157°C/W
$\Theta_{JC}$	Junction-to-Case Thermal Resistance	—	42°C/W



**PI6C49CB04BJ**

**Part Marking**

PI6C49CB  
04BJWE  
YYWWXX  
○

YY: Year

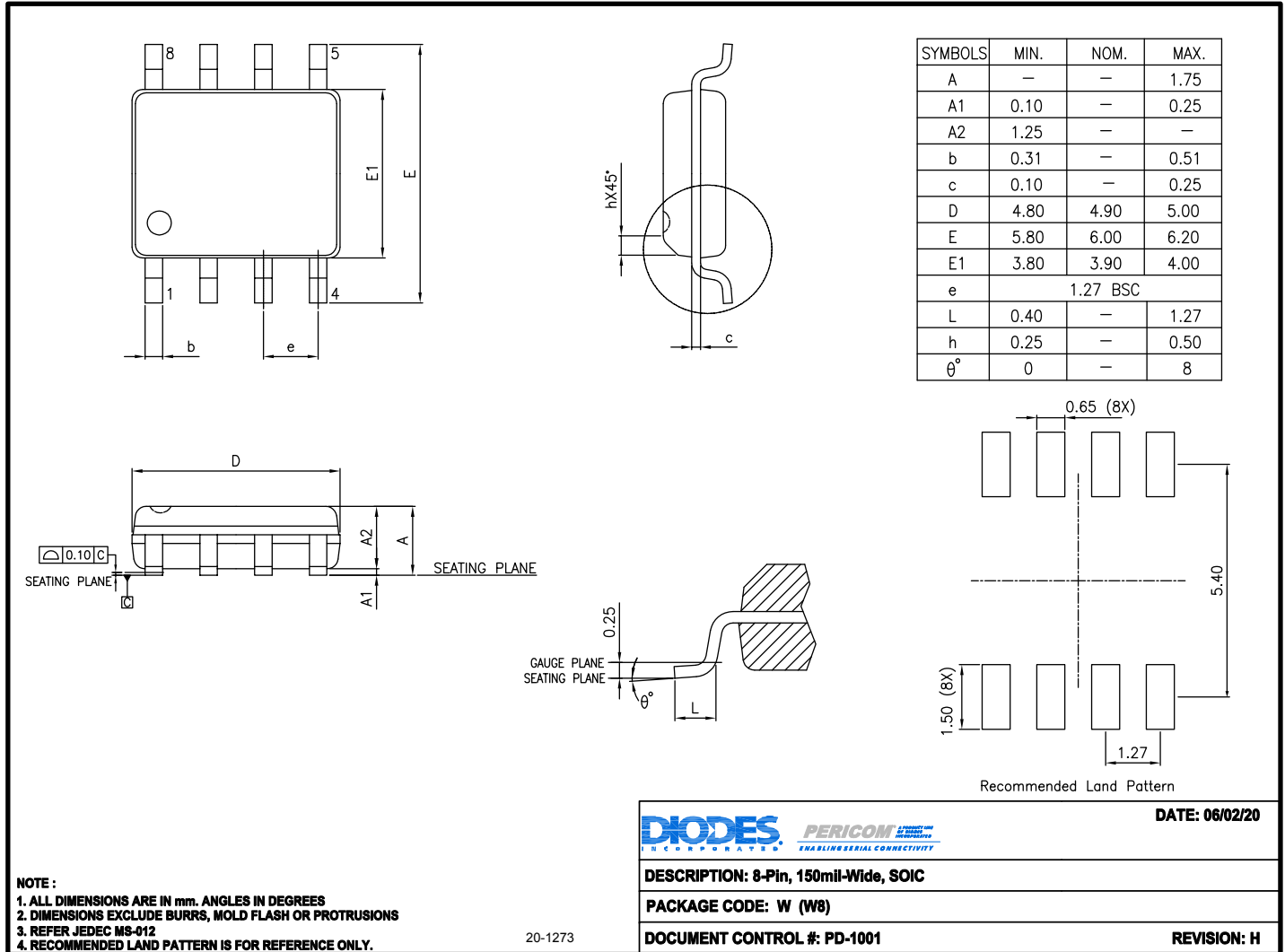
WW: Workweek

1st X: Assembly Code

2nd X: Fab Code

**Packaging Mechanical:**

8-SOIC (W)



For latest package information:

See <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>.

**Ordering Information**

Ordering Code	Package Code	Package Description
PI6C49CB04BJWEX	W	8-pin, 150mil-Wide (SOIC)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogens- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. J = Industrial Grade
5. E = Pb-free and Green
6. X suffix = Tape/Reel

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