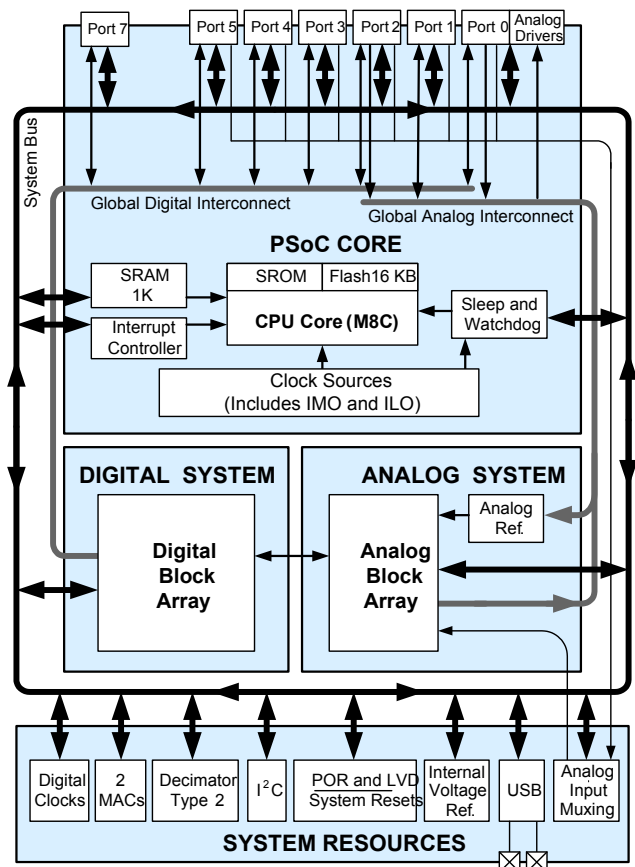


Features

- XRES pin to support in-system serial programming (ISSP) and external reset control in CY8C24894
- Powerful Harvard-architecture processor
 - M8C processor speeds up to 24 MHz
 - Two 8 × 8 multiply, 32-bit accumulate
 - Low power at high speed
 - Operating voltage: 3 V to 5.25 V
 - Industrial temperature range: -40 °C to +85 °C
 - USB temperature range: -10 °C to +85 °C
- Advanced peripherals (PSoC® Blocks)
 - Six rail-to-rail analog PSoC blocks provide:
 - Up to 14-bit analog-to-digital converters (ADCs)
 - Up to 9-bit digital-to-analog converters (DACs)
 - Programmable gain amplifiers (PGAs)
 - Programmable filters and comparators
 - Four digital PSoC blocks provide:
 - 8- to 32-bit timers, counters, and pulse width modulators (PWMs)
 - Cyclical redundancy check (CRC) and pseudo random sequence (PRS) modules
 - Full-duplex universal asynchronous receiver transmitter (UART)
 - Multiple serial peripheral interface (SPI) masters or slaves
 - Connectable to all general-purpose I/O (GPIO) pins
 - Complex peripherals by combining blocks
 - Capacitive sensing application (CSA) capability
- Full speed USB (12 Mbps)
 - Four unidirectional endpoints
 - One bidirectional control endpoint
 - USB 2.0 compliant
 - Dedicated 256 byte buffer
 - No external crystal required
- Flexible on-chip memory
 - 16 KB flash program storage 50,000 erase and write cycles
 - 1 KB static random access memory (SRAM) data storage
 - ISSP
 - Partial flash updates
 - Flexible protection modes
 - Electrically erasable programmable read-only memory (EEPROM) emulation in flash
- Programmable pin configurations
 - 25-mA sink, 10-mA source on all GPIOs
 - Pull-up, pull-down, high Z, strong, or open-drain drive modes on all GPIOs

- Up to 48 analog inputs on GPIOs
- Two 33 mA analog outputs on GPIOs
- Configurable interrupt on all GPIOs
- Precision, programmable clocking
 - Internal ±4% 24- / 48-MHz main oscillator
 - Internal oscillator for watchdog and sleep
 - 0.25% accuracy for USB with no external components
- Additional system resources
 - I²C slave, master, and multi-master to 400 kHz
 - Watchdog and sleep timers
 - User-configurable low-voltage detection (LVD)

Logic Block Diagram



Errata: For information on silicon errata, see "Errata" on page 64. Details include trigger conditions, devices affected, and proposed workaround.

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA92181, Resources Available for CapSense® Controllers](#). Following is an abbreviated list for CapSense devices:

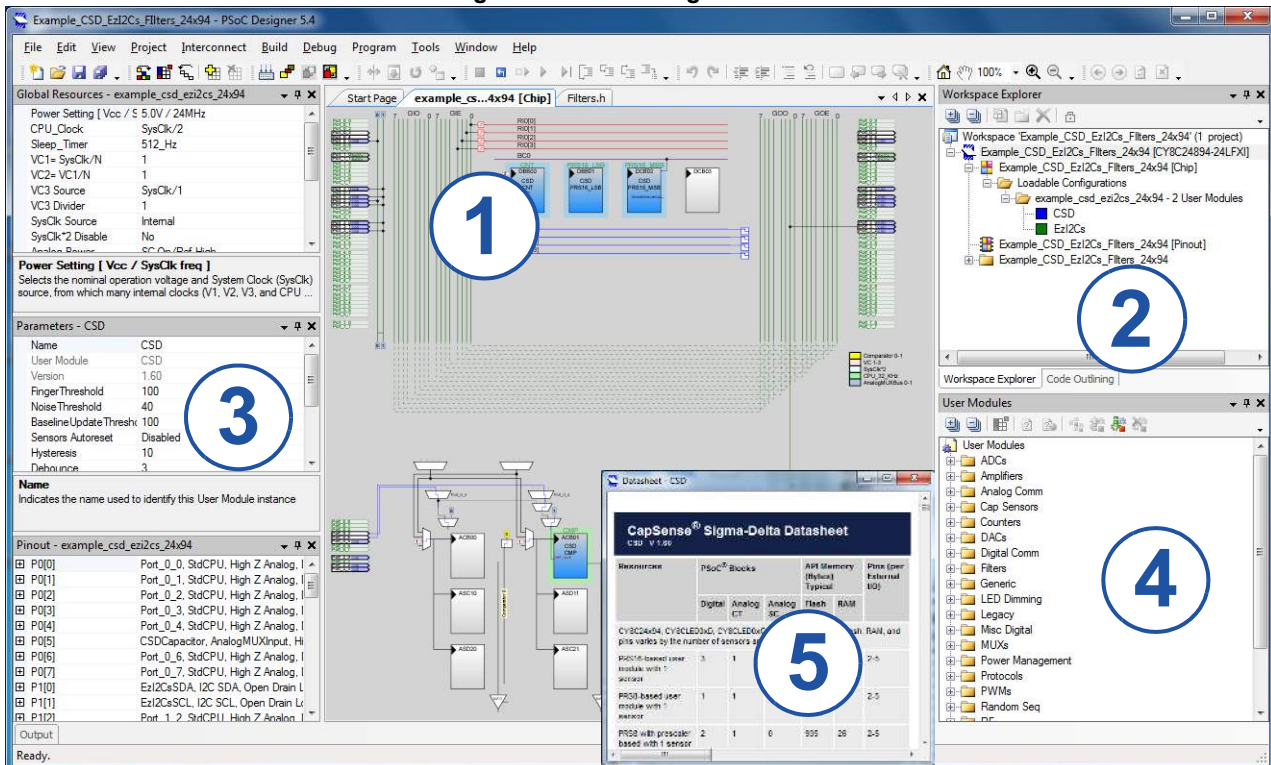
- Overview: [CapSense Portfolio](#), [CapSense Roadmap](#)
 - Product Selectors: [CapSense](#), [CapSense Plus](#), [CapSense Express](#), [PSoC3 with CapSense](#), [PSoC5 with CapSense](#), [PSoC4](#). In addition, [PSoC Designer](#) offers a device selection tool at the time of creating a new project.
 - Application notes: Cypress offers CapSense application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with CapSense are:
 - [AN64846: Getting Started With CapSense](#)
 - [AN2397: CapSense® Data Viewing Tools](#)
 - Technical Reference Manual (TRM):
 - [CY8CPLC20](#), [CY8CLED16P01](#), [CY8C29x66](#), [CY8C27x43](#), [CY8C24x94](#), [CY8C24x23](#), [CY8C24x23A](#), [CY8C22x13](#), [CY8C21x34](#), [CY8C21x34B](#), [CY8C21x23](#), [CY7C64215](#), [CY7C603xx](#), [CY8CNP1xx](#), and [CYWUSB6953 PSoC® Programmable System-on-Chip TRM](#)
 - Development Kits:
 - [CY3280-24x94 Universal CapSense Controller Board](#) features a predefined control circuitry and plug-in hardware to make prototyping and debugging easy. Programming and I2C-to-USB Bridge hardware are included for tuning and data acquisition.
 - [CY3280-BMM Matrix Button Module Kit](#) consists of eight CapSense sensors organized in a 4x4 matrix format to form 16 physical buttons and eight LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.
 - [CY3280-BSM Simple Button Module Kit](#) consists of ten CapSense buttons and ten LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.
- The [CY3217-MiniProg1](#) and [CY8CKIT-002 PSoC® MiniProg3](#) device provides an interface for flash programming.

PSoC Designer

[PSoC Designer](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on CapSense (see [Figure 1](#)). With PSoC Designer, you can:

1. Drag and drop User Modules to build your hardware system design in the main design workspace
2. Configure User Module
3. Configure User Module
4. Explore the library of user modules
5. Review user module datasheets

Figure 1. PSoC Designer Features



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PSoC Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional MCU-based system components with one low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, shown in the [Logic Block Diagram on page 1](#), consists of four main areas: the core, the system resources, the digital system, and the analog system. Configurable global bus resources allow combining all of the device resources into a complete custom system. Each CY8C24x94 PSoC device includes four digital blocks and six analog blocks. Depending on the PSoC package, up to 56 GPIOs are also included. The GPIOs provide access to the global digital and analog interconnects.

The PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO) and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor.

System resources provide these additional capabilities:

- Digital clocks for increased flexibility
- I²C functionality to implement an I²C master and slave
- An internal voltage reference, multi-master, that provides an absolute value of 1.3 V to a number of PSoC subsystems
- A switch-mode pump (SMP) that generates normal operating voltages from a single battery cell
- Various system resets supported by the M8C

The digital system consists of an array of digital PSoC blocks that may be configured into any number of digital peripherals. The digital blocks are connected to the GPIOs through a series of global buses. These buses can route any signal to any pin, freeing designs from the constraints of a fixed peripheral controller.

The analog system consists of six analog PSoC blocks, supporting comparators, and analog-to-digital conversion up to 10-bits of precision.

The Digital System

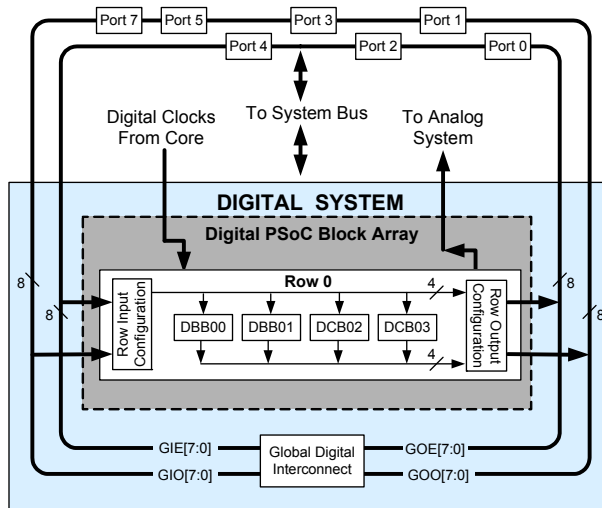
The digital system consists of four digital PSoC blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include:

- PWMs (8- to 32-bit)
- PWMs with dead band (8- to 32-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I²C slave and multi-master
- CRC/generator (8-bit)
- IrDA
- PRS generators (8- to 32-bit)

The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in [Table 1 on page 6](#).

Figure 2. Digital System Block Diagram



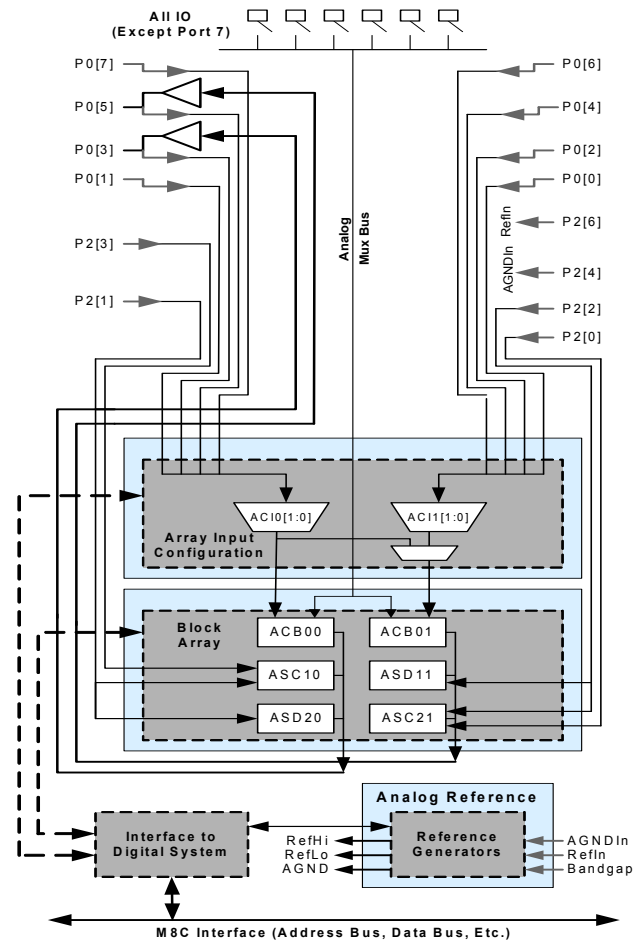
The Analog System

The analog system is composed of six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are as follows.

- ADCs (up to two, with 6- to 14-bit resolution, selectable as incremental, delta sigma, and successive approximation register (SAR))
- Filters (2 and 4 pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (one with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6- to 9-bit resolution)
- Multiplying DACs (up to two, with 6- to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC core resource)
- 1.3-V reference (as a system resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 3.

Figure 3. Analog System Block Diagram



The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin in ports 0–5. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It is split into two sections for simultaneous dual-channel processing. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Chip-wide mux that enables analog input from up to 48 I/O pins
- Crosspoint connection between any I/O pin combinations

Additional System Resources

System resources provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low-voltage detection, and power-on reset (POR). Brief statements describing the merits of each resource follow.

- Full speed USB (12 Mbps) with five configurable endpoints and 256 bytes of RAM. No external components required except for two series resistors. Wider than commercial temperature USB operation (–10 °C to +85 °C).
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks are generated using digital PSoC blocks as clock dividers.
- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- Decimator provides a custom hardware filter for digital signal processing applications including creation of Delta Sigma ADCs.
- The I²C module provides 100- and 400-kHz communication over two wires. Slave, master, multi-master are supported.
- Low-voltage detection interrupts signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3-V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific PSoC device groups. The device covered by this datasheet is shown in the highlighted row of the table.

Table 1. PSoC Device Characteristics

| PSoC Part Number | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size |
|------------------|-------------|--------------|----------------|---------------|----------------|----------------|-----------------------------|-----------|------------|
| CY8C29x66 | up to 64 | 4 | 16 | up to 12 | 4 | 4 | 12 | 2 K | 32 K |
| CY8C28xxx | up to 44 | up to 3 | up to 12 | up to 44 | up to 4 | up to 6 | up to 12 + 4 ^[1] | 1 K | 16 K |
| CY8C27x43 | up to 44 | 2 | 8 | up to 12 | 4 | 4 | 12 | 256 | 16 K |
| CY8C24x94 | up to 56 | 1 | 4 | up to 48 | 2 | 2 | 6 | 1 K | 16 K |
| CY8C24x23A | up to 24 | 1 | 4 | up to 12 | 2 | 2 | 6 | 256 | 4 K |
| CY8C23x33 | up to 26 | 1 | 4 | up to 12 | 2 | 2 | 4 | 256 | 8 K |
| CY8C22x45 | up to 38 | 2 | 8 | up to 38 | 0 | 4 | 6 ^[1] | 1 K | 16 K |
| CY8C21x45 | up to 24 | 1 | 4 | up to 24 | 0 | 4 | 6 ^[1] | 512 | 8 K |
| CY8C21x34 | up to 28 | 1 | 4 | up to 28 | 0 | 2 | 4 ^[1] | 512 | 8 K |
| CY8C21x23 | up to 16 | 1 | 4 | up to 8 | 0 | 2 | 4 ^[1] | 256 | 4 K |
| CY8C20x34 | up to 28 | 0 | 0 | up to 28 | 0 | 0 | 3 ^[1,2] | 512 | 8 K |
| CY8C20xx6 | up to 36 | 0 | 0 | up to 36 | 0 | 0 | 3 ^[1,2] | up to 2 K | up to 32 K |

Notes

1. Limited analog functionality.
2. Two analog blocks and one CapSense®.

Getting Started

For in-depth information, along with detailed programming information, see the [Technical Reference Manual](#) for this PSoC device.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at <http://www.cypress.com>.

Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

Solutions Library

Visit our growing [library of solution-focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog

- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
 - Hardware and software I²C slaves and masters
 - Full speed USB 2.0
 - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC[®] device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select [User Modules](#)
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM

User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations and external signals.

Pin Information

This section describes, lists, and illustrates the CY8C24x94 PSoC device family pins and pinout configuration.

The CY8C24x94 PSoC devices are available in the following packages, all of which are shown on the following pages. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

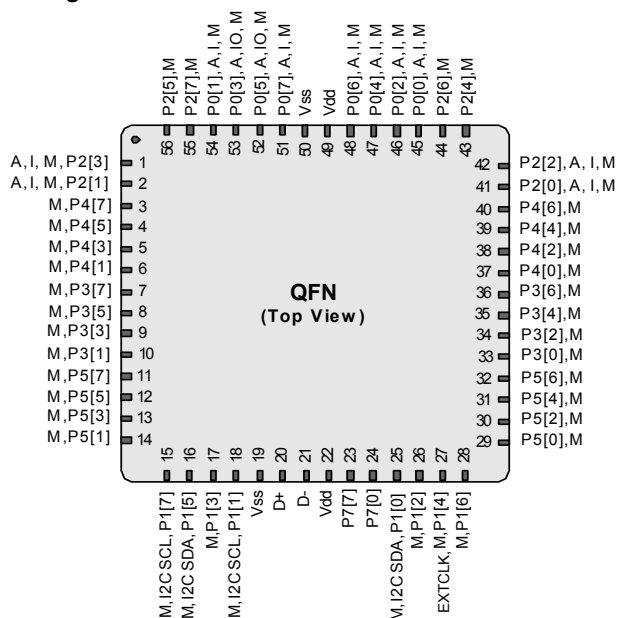
56-Pin Part Pinout

See LEGEND details and footnotes in Table 3 on page 10.

Table 2. 56-Pin Part Pinout (QFN^[6])

| Pin No. | Type | | Name | Description | Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|---|---------|---------|--------|-----------------|---|
| | Digital | Analog | | | | Digital | Analog | | |
| 1 | I/O | I, M | P2[3] | Direct switched capacitor block input | 44 | I/O | M | P2[6] | External voltage reference (VREF) input |
| 2 | I/O | I, M | P2[1] | Direct switched capacitor block input | 45 | I/O | I, M | P0[0] | Analog column mux input |
| 3 | I/O | M | P4[7] | | 46 | I/O | I, M | P0[2] | Analog column mux input |
| 4 | I/O | M | P4[5] | | 47 | I/O | I, M | P0[4] | Analog column mux input VREF |
| 5 | I/O | M | P4[3] | | 48 | I/O | I, M | P0[6] | Analog column mux input |
| 6 | I/O | M | P4[1] | | 49 | Power | | V _{DD} | Supply voltage |
| 7 | I/O | M | P3[7] | | 50 | Power | | V _{SS} | Ground connection ^[5] |
| 8 | I/O | M | P3[5] | | 51 | I/O | I, M | P0[7] | Analog column mux input |
| 9 | I/O | M | P3[3] | | 52 | I/O | I/O, M | P0[5] | Analog column mux input and column output |
| 10 | I/O | M | P3[1] | | 53 | I/O | I/O, M | P0[3] | Analog column mux input and column output |
| 11 | I/O | M | P5[7] | | 54 | I/O | I, M | P0[1] | Analog column mux input |
| 12 | I/O | M | P5[5] | | 55 | I/O | M | P2[7] | |
| 13 | I/O | M | P5[3] | | 56 | I/O | M | P2[5] | |
| 14 | I/O | M | P5[1] | | | | | | |
| 15 | I/O | M | P1[7] | I ² C serial clock (SCL) | | | | | |
| 16 | I/O | M | P1[5] | I ² C serial data (SDA) | | | | | |
| 17 | I/O | M | P1[3] | | | | | | |
| 18 | I/O | M | P1[1] | I ² C SCL, ISSP SCLK ^[4] | | | | | |
| 19 | Power | | V _{SS} | Ground connection ^[5] | | | | | |
| 20 | USB | | D+ | | | | | | |
| 21 | USB | | D- | | | | | | |
| 22 | Power | | V _{DD} | Supply voltage | | | | | |
| 23 | I/O | | P7[7] | | | | | | |
| 24 | I/O | | P7[0] | | | | | | |
| 25 | I/O | M | P1[0] | I ² C SDA, ISSP SDATA ^[4] | | | | | |
| 26 | I/O | M | P1[2] | | | | | | |
| 27 | I/O | M | P1[4] | Optional external clock input (EXTCLK) | | | | | |
| 28 | I/O | M | P1[6] | | | | | | |
| 29 | I/O | M | P5[0] | | | | | | |
| 30 | I/O | M | P5[2] | | | | | | |
| 31 | I/O | M | P5[4] | | | | | | |
| 32 | I/O | M | P5[6] | | | | | | |
| 33 | I/O | M | P3[0] | | | | | | |
| 34 | I/O | M | P3[2] | | | | | | |
| 35 | I/O | M | P3[4] | | | | | | |
| 36 | I/O | M | P3[6] | | | | | | |
| 37 | I/O | M | P4[0] | | | | | | |
| 38 | I/O | M | P4[2] | | | | | | |
| 39 | I/O | M | P4[4] | | | | | | |
| 40 | I/O | M | P4[6] | | | | | | |
| 41 | I/O | I, M | P2[0] | Direct switched capacitor block input | | | | | |
| 42 | I/O | I, M | P2[2] | Direct switched capacitor block input | | | | | |
| 43 | I/O | M | P2[4] | External analog ground (AGND) input | | | | | |

Figure 4. CY8C24794 56-Pin PSoC Device^[3]



Notes

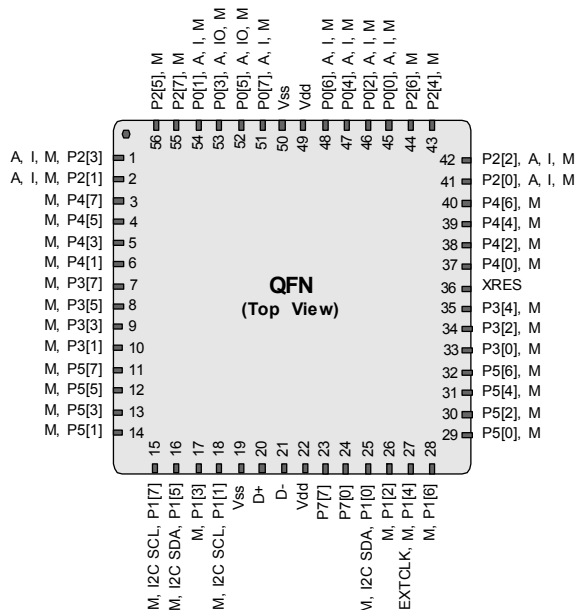
- This part cannot be programmed with Reset mode; use Power Cycle mode when programming.
- These are the ISSP pins, which are not High Z at POR. See the PSoC Technical Reference Manual for details.
- All V_{SS} pins should be brought out to one common GND plane.

56-Pin Part Pinout (with XRES)

Table 3. 56-Pin Part Pinout (QFN^[6])

| Pin No. | Type | | Name | Description | Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|--|---------|---------|--------|-----------------|---|
| | Digital | Analog | | | | Digital | Analog | | |
| 1 | I/O | I, M | P2[3] | Direct switched capacitor block input | 44 | I/O | M | P2[6] | External VREF input |
| 2 | I/O | I, M | P2[1] | Direct switched capacitor block input | 45 | I/O | I, M | P0[0] | Analog column mux input |
| 3 | I/O | M | P4[7] | | 46 | I/O | I, M | P0[2] | Analog column mux input |
| 4 | I/O | M | P4[5] | | 47 | I/O | I, M | P0[4] | Analog column mux input VREF |
| 5 | I/O | M | P4[3] | | 48 | I/O | I, M | P0[6] | Analog column mux input |
| 6 | I/O | M | P4[1] | | 49 | Power | | V _{DD} | Supply voltage |
| 7 | I/O | M | P3[7] | | 50 | Power | | V _{SS} | Ground connection ^[8] |
| 8 | I/O | M | P3[5] | | 51 | I/O | I, M | P0[7] | Analog column mux input |
| 9 | I/O | M | P3[3] | | 52 | I/O | I/O, M | P0[5] | Analog column mux input and column output |
| 10 | I/O | M | P3[1] | | 53 | I/O | I/O, M | P0[3] | Analog column mux input and column output |
| 11 | I/O | M | P5[7] | | 54 | I/O | I, M | P0[1] | Analog column mux input |
| 12 | I/O | M | P5[5] | | 55 | I/O | M | P2[7] | |
| 13 | I/O | M | P5[3] | | 56 | I/O | M | P2[5] | |
| 14 | I/O | M | P5[1] | | | | | | |
| 15 | I/O | M | P1[7] | I ² C SCL | | | | | |
| 16 | I/O | M | P1[5] | I ² C SDA | | | | | |
| 17 | I/O | M | P1[3] | | | | | | |
| 18 | I/O | M | P1[1] | I ² C SCL, ISSP SCLK ^[7] | | | | | |
| 19 | Power | | V _{SS} | Ground connection ^[8] | | | | | |
| 20 | USB | | D+ | | | | | | |
| 21 | USB | | D- | | | | | | |
| 22 | Power | | V _{DD} | Supply voltage | | | | | |
| 23 | I/O | | P7[7] | | | | | | |
| 24 | I/O | | P7[0] | | | | | | |
| 25 | I/O | M | P1[0] | I ² C SDA, ISSP SDATA ^[7] | | | | | |
| 26 | I/O | M | P1[2] | | | | | | |
| 27 | I/O | M | P1[4] | Optional EXTCLK | | | | | |
| 28 | I/O | M | P1[6] | | | | | | |
| 29 | I/O | M | P5[0] | | | | | | |
| 30 | I/O | M | P5[2] | | | | | | |
| 31 | I/O | M | P5[4] | | | | | | |
| 32 | I/O | M | P5[6] | | | | | | |
| 33 | I/O | M | P3[0] | | | | | | |
| 34 | I/O | M | P3[2] | | | | | | |
| 35 | I/O | M | P3[4] | | | | | | |
| 36 | Input | | XRES | Active high external reset with internal pull-down | | | | | |
| 37 | I/O | M | P4[0] | | | | | | |
| 38 | I/O | M | P4[2] | | | | | | |
| 39 | I/O | M | P4[4] | | | | | | |
| 40 | I/O | M | P4[6] | | | | | | |
| 41 | I/O | I, M | P2[0] | Direct switched capacitor block input | | | | | |
| 42 | I/O | I, M | P2[2] | Direct switched capacitor block input | | | | | |
| 43 | I/O | M | P2[4] | External AGND input | | | | | |

Figure 5. CY8C24894 56-Pin PSoC Device



LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Notes

- The center pad on the QFN package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.
- These are the ISSP pins, which are not High Z at POR. See the [PSoC Technical Reference Manual](#) for details.
- All V_{SS} pins should be brought out to one common GND plane.

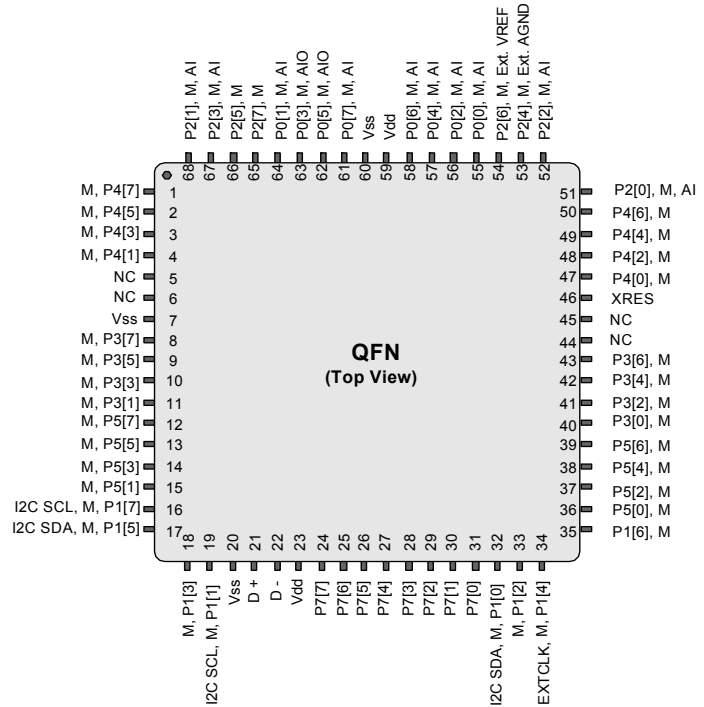
68-Pin Part Pinout

The following 68-pin QFN part table and drawing is for the CY8C24994 PSoC device.

Table 4. 68-Pin Part Pinout (QFN^[9])

| Pin No. | Type | | Name | Description | Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|--|---------|---------|--------|-----------------|---|
| | Digital | Analog | | | | Digital | Analog | | |
| 1 | I/O | M | P4[7] | | | | | | |
| 2 | I/O | M | P4[5] | | | | | | |
| 3 | I/O | M | P4[3] | | | | | | |
| 4 | I/O | M | P4[1] | | | | | | |
| 5 | | | NC | No connection. Pin must be left floating | | | | | |
| 6 | | | NC | No connection. Pin must be left floating | | | | | |
| 7 | Power | | V _{SS} | Ground connection ^[10] | | | | | |
| 8 | I/O | M | P3[7] | | | | | | |
| 9 | I/O | M | P3[5] | | | | | | |
| 10 | I/O | M | P3[3] | | | | | | |
| 11 | I/O | M | P3[1] | | | | | | |
| 12 | I/O | M | P5[7] | | | | | | |
| 13 | I/O | M | P5[5] | | | | | | |
| 14 | I/O | M | P5[3] | | | | | | |
| 15 | I/O | M | P5[1] | | | | | | |
| 16 | I/O | M | P1[7] | I ² C SCL | | | | | |
| 17 | I/O | M | P1[5] | I ² C SDA | | | | | |
| 18 | I/O | M | P1[3] | | | | | | |
| 19 | I/O | M | P1[1] | I ² C SCL ISSP SCLK ^[11] | | | | | |
| 20 | Power | | V _{SS} | Ground connection ^[10] | | | | | |
| 21 | USB | | D+ | | | | | | |
| 22 | USB | | D- | | | | | | |
| 23 | Power | | V _{DD} | Supply voltage | | | | | |
| 24 | I/O | | P7[7] | | | | | | |
| 25 | I/O | | P7[6] | | | | | | |
| 26 | I/O | | P7[5] | | | | | | |
| 27 | I/O | | P7[4] | | | | | | |
| 28 | I/O | | P7[3] | | | | | | |
| 29 | I/O | | P7[2] | | | | | | |
| 30 | I/O | | P7[1] | | | | | | |
| 31 | I/O | | P7[0] | | | | | | |
| 32 | I/O | M | P1[0] | I ² C SDA, ISSP SDATA ^[11] | 50 | I/O | M | P4[6] | |
| 33 | I/O | M | P1[2] | | 51 | I/O | I, M | P2[0] | Direct switched capacitor block input |
| 34 | I/O | M | P1[4] | Optional EXTCLK | 52 | I/O | I, M | P2[2] | Direct switched capacitor block input |
| 35 | I/O | M | P1[6] | | 53 | I/O | M | P2[4] | External AGND input |
| 36 | I/O | M | P5[0] | | 54 | I/O | M | P2[6] | External VREF input |
| 37 | I/O | M | P5[2] | | 55 | I/O | I, M | P0[0] | Analog column mux input |
| 38 | I/O | M | P5[4] | | 56 | I/O | I, M | P0[2] | Analog column mux input and column output |
| 39 | I/O | M | P5[6] | | 57 | I/O | I, M | P0[4] | Analog column mux input and column output |
| 40 | I/O | M | P3[0] | | 58 | I/O | I, M | P0[6] | Analog column mux input |
| 41 | I/O | M | P3[2] | | 59 | Power | | V _{DD} | Supply voltage |
| 42 | I/O | M | P3[4] | | 60 | Power | | V _{SS} | Ground connection ^[10] |
| 43 | I/O | M | P3[6] | | 61 | I/O | I, M | P0[7] | Analog column mux input, integration input #1 |
| 44 | | | NC | No connection. Pin must be left floating. | 62 | I/O | I/O, M | P0[5] | Analog column mux input and column output, integration input #2 |
| 45 | | | NC | No connection. Pin must be left floating. | 63 | I/O | I/O, M | P0[3] | Analog column mux input and column output |
| 46 | Input | | XRES | Active high pin reset with internal pull-down. | 64 | I/O | I, M | P0[1] | Analog column mux input |
| 47 | I/O | M | P4[0] | | 65 | I/O | M | P2[7] | |
| 48 | I/O | M | P4[2] | | 66 | I/O | M | P2[5] | |
| 49 | I/O | M | P4[4] | | 67 | I/O | I, M | P2[3] | Direct switched capacitor block input |
| | | | | | 68 | I/O | I, M | P2[1] | Direct switched capacitor block input |

Figure 6. CY8C24994 68-Pin PSoC Device



LEGEND A = Analog, I = Input, O = Output, NC = No connection. Pin must be left floating, M = Analog Mux Input.

Notes

- The center pad on the QFN package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.
- All V_{SS} pins should be brought out to one common GND plane.
- These are the ISSP pins, which are not High Z at POR. See the [PSoC Technical Reference Manual](#) for details.

68-Pin Part Pinout (On-Chip Debug)

The following 68-pin QFN part table and drawing is for the CY8C24094 OCD PSoc device.

Note: This part is only used for in-circuit debugging. It is NOT available for production.

Table 5. 68-Pin Part Pinout (QFN^[12])

| Pin No. | Type | | Name | Description | Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|--|---------|---------|--------|-----------------|---|
| | Digital | Analog | | | | Digital | Analog | | |
| 1 | I/O | M | P4[7] | | | | | | |
| 2 | I/O | M | P4[5] | | | | | | |
| 3 | I/O | M | P4[3] | | | | | | |
| 4 | I/O | M | P4[1] | | | | | | |
| 5 | | | OCDE | OCD even data I/O | | | | | |
| 6 | | | OCDO | OCD odd data output | | | | | |
| 7 | Power | | V _{SS} | Ground connection ^[13] | | | | | |
| 8 | I/O | M | P3[7] | | | | | | |
| 9 | I/O | M | P3[5] | | | | | | |
| 10 | I/O | M | P3[3] | | | | | | |
| 11 | I/O | M | P3[1] | | | | | | |
| 12 | I/O | M | P5[7] | | | | | | |
| 13 | I/O | M | P5[5] | | | | | | |
| 14 | I/O | M | P5[3] | | | | | | |
| 15 | I/O | M | P5[1] | | | | | | |
| 16 | I/O | M | P1[7] | I ² C SCL | | | | | |
| 17 | I/O | M | P1[5] | I ² C SDA | | | | | |
| 18 | I/O | M | P1[3] | | | | | | |
| 19 | I/O | M | P1[1] | I ² C SCL, ISSP SCLK ^[14] | | | | | |
| 20 | Power | | V _{SS} | Ground connection ^[13] | | | | | |
| 21 | USB | | D+ | | | | | | |
| 22 | USB | | D- | | | | | | |
| 23 | Power | | V _{DD} | Supply voltage | | | | | |
| 24 | I/O | | P7[7] | | | | | | |
| 25 | I/O | | P7[6] | | | | | | |
| 26 | I/O | | P7[5] | | | | | | |
| 27 | I/O | | P7[4] | | | | | | |
| 28 | I/O | | P7[3] | | | | | | |
| 29 | I/O | | P7[2] | | | | | | |
| 30 | I/O | | P7[1] | | | | | | |
| 31 | I/O | | P7[0] | | | | | | |
| 32 | I/O | M | P1[0] | I ² C SDA, ISSP SDATA ^[14] | 50 | I/O | M | P4[6] | |
| 33 | I/O | M | P1[2] | | 51 | I/O | I, M | P2[0] | Direct switched capacitor block input |
| 34 | I/O | M | P1[4] | Optional EXTCLK | 52 | I/O | I, M | P2[2] | Direct switched capacitor block input |
| 35 | I/O | M | P1[6] | | 53 | I/O | M | P2[4] | External AGND input |
| 36 | I/O | M | P5[0] | | 54 | I/O | M | P2[6] | External VREF input |
| 37 | I/O | M | P5[2] | | 55 | I/O | I, M | P0[0] | Analog column mux input |
| 38 | I/O | M | P5[4] | | 56 | I/O | I, M | P0[2] | Analog column mux input and column output |
| 39 | I/O | M | P5[6] | | 57 | I/O | I, M | P0[4] | Analog column mux input and column output |
| 40 | I/O | M | P3[0] | | 58 | I/O | I, M | P0[6] | Analog column mux input |
| 41 | I/O | M | P3[2] | | 59 | Power | | V _{DD} | Supply voltage |
| 42 | I/O | M | P3[4] | | 60 | Power | | V _{SS} | Ground connection ^[13] |
| 43 | I/O | M | P3[6] | | 61 | I/O | I, M | P0[7] | Analog column mux input, integration input #1 |
| 44 | | | HCLK | OCD high speed clock output | 62 | I/O | I/O, M | P0[5] | Analog column mux input and column output, integration input #2 |
| 45 | | | CCLK | OCD CPU clock output | 63 | I/O | I/O, M | P0[3] | Analog column mux input and column output |
| 46 | Input | | XRES | Active high pin reset with internal pull-down | 64 | I/O | I, M | P0[1] | Analog column mux input |
| 47 | I/O | M | P4[0] | | 65 | I/O | M | P2[7] | |
| 48 | I/O | M | P4[2] | | 66 | I/O | M | P2[5] | |
| 49 | I/O | M | P4[4] | | 67 | I/O | I, M | P2[3] | Direct switched capacitor block input |
| | | | | | 68 | I/O | I, M | P2[1] | Direct switched capacitor block input |

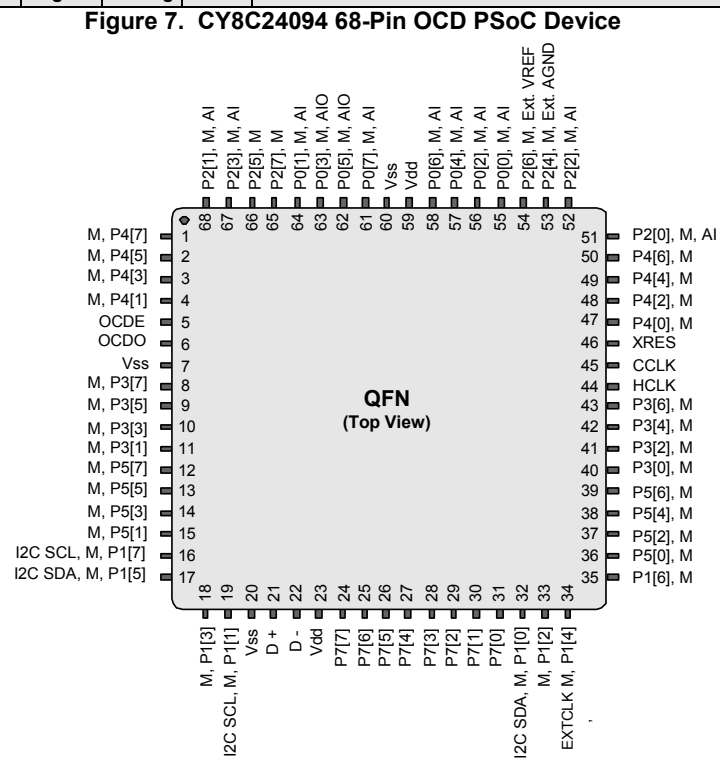
LEGEND A = Analog, I = Input, O = Output, M = Analog Mux Input, OCD = On-Chip Debugger.

Notes

12. The center pad on the QFN package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

13. All V_{SS} pins should be brought out to one common GND plane.

14. These are the ISSP pins, which are not High Z at POR. See the [PSoc Technical Reference Manual](#) for details.



100-Ball VFBGA Part Pinout

The 100-ball VFBGA part is for the CY8C24994 PSoC device.

Table 6. 100-Ball Part Pinout (VFBGA^[15])

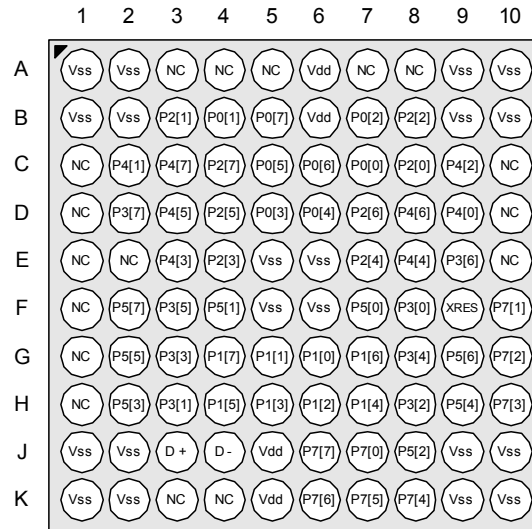
| Pin No. | Digital | Analog | Name | Description | Pin No. | Digital | Analog | Name | Description |
|---------|---------|--------|-----------------|---|---------|---------|--------|-----------------|--|
| A1 | Power | | V _{SS} | Ground connection | F1 | | | NC | No connection. Pin must be left floating |
| A2 | Power | | V _{SS} | Ground connection | F2 | I/O | M | P5[7] | |
| A3 | | | NC | No connection. Pin must be left floating | F3 | I/O | M | P3[5] | |
| A4 | | | NC | No connection. Pin must be left floating | F4 | I/O | M | P5[1] | |
| A5 | | | NC | No connection. Pin must be left floating | F5 | Power | | V _{SS} | Ground connection |
| A6 | Power | | V _{DD} | Supply voltage | F6 | Power | | V _{SS} | Ground connection |
| A7 | | | NC | No connection. Pin must be left floating | F7 | I/O | M | P5[0] | |
| A8 | | | NC | No connection. Pin must be left floating | F8 | I/O | M | P3[0] | |
| A9 | Power | | V _{SS} | Ground connection | F9 | | | XRES | Active high pin reset with internal pull-down |
| A10 | Power | | V _{SS} | Ground connection | F10 | I/O | | P7[1] | |
| B1 | Power | | V _{SS} | Ground connection | G1 | | | NC | No connection. Pin must be left floating |
| B2 | Power | | V _{SS} | Ground connection | G2 | I/O | M | P5[5] | |
| B3 | I/O | I, M | P2[1] | Direct switched capacitor block input | G3 | I/O | M | P3[3] | |
| B4 | I/O | I, M | P0[1] | Analog column mux input | G4 | I/O | M | P1[7] | I ² C SCL |
| B5 | I/O | I, M | P0[7] | Analog column mux input | G5 | I/O | M | P1[1] | I ² C SCL, ISSP SCLK ^[16] |
| B6 | Power | | V _{DD} | Supply voltage | G6 | I/O | M | P1[0] | I ² C SDA, ISSP SDATA ^[16] |
| B7 | I/O | I, M | P0[2] | Analog column mux input | G7 | I/O | M | P1[6] | |
| B8 | I/O | I, M | P2[2] | Direct switched capacitor block input | G8 | I/O | M | P3[4] | |
| B9 | Power | | V _{SS} | Ground connection | G9 | I/O | M | P5[6] | |
| B10 | Power | | V _{SS} | Ground connection | G10 | I/O | | P7[2] | |
| C1 | | | NC | No connection. Pin must be left floating | H1 | | | NC | No connection. Pin must be left floating |
| C2 | I/O | M | P4[1] | | H2 | I/O | M | P5[3] | |
| C3 | I/O | M | P4[7] | | H3 | I/O | M | P3[1] | |
| C4 | I/O | M | P2[7] | | H4 | I/O | M | P1[5] | I ² C SDA |
| C5 | I/O | I/O, M | P0[5] | Analog column mux input and column output | H5 | I/O | M | P1[3] | |
| C6 | I/O | I, M | P0[6] | Analog column mux input | H6 | I/O | M | P1[2] | |
| C7 | I/O | I, M | P0[0] | Analog column mux input | H7 | I/O | M | P1[4] | Optional EXTCLK |
| C8 | I/O | I, M | P2[0] | Direct switched capacitor block input | H8 | I/O | M | P3[2] | |
| C9 | I/O | M | P4[2] | | H9 | I/O | M | P5[4] | |
| C10 | | | NC | No connection. Pin must be left floating | H10 | I/O | | P7[3] | |
| D1 | | | NC | No connection. Pin must be left floating | J1 | Power | | V _{SS} | Ground connection |
| D2 | I/O | M | P3[7] | | J2 | Power | | V _{SS} | Ground connection |
| D3 | I/O | M | P4[5] | | J3 | USB | | D+ | |
| D4 | I/O | M | P2[5] | | J4 | USB | | D- | |
| D5 | I/O | I/O, M | P0[3] | Analog column mux input and column output | J5 | Power | | V _{DD} | Supply voltage |
| D6 | I/O | I, M | P0[4] | Analog column mux input | J6 | I/O | | P7[7] | |
| D7 | I/O | M | P2[6] | External VREF input | J7 | I/O | | P7[0] | |
| D8 | I/O | M | P4[6] | | J8 | I/O | M | P5[2] | |
| D9 | I/O | M | P4[0] | | J9 | Power | | V _{SS} | Ground connection |
| D10 | | | NC | No connection. Pin must be left floating | J10 | Power | | V _{SS} | Ground connection |
| E1 | | | NC | No connection. Pin must be left floating | K1 | Power | | V _{SS} | Ground connection |
| E2 | | | NC | No connection. Pin must be left floating | K2 | Power | | V _{SS} | Ground connection |
| E3 | I/O | M | P4[3] | | K3 | | | NC | No connection. Pin must be left floating |
| E4 | I/O | I, M | P2[3] | Direct switched capacitor block input | K4 | | | NC | No connection. Pin must be left floating |
| E5 | Power | | V _{SS} | Ground connection | K5 | Power | | V _{DD} | Supply voltage |
| E6 | Power | | V _{SS} | Ground connection | K6 | I/O | | P7[6] | |
| E7 | I/O | M | P2[4] | External AGND input | K7 | I/O | | P7[5] | |
| E8 | I/O | M | P4[4] | | K8 | I/O | | P7[4] | |
| E9 | I/O | M | P3[6] | | K9 | Power | | V _{SS} | Ground connection |
| E10 | | | NC | No connection. Pin must be left floating | K10 | Power | | V _{SS} | Ground connection |

LEGEND A = Analog, I = Input, O = Output, M = Analog Mux Input, NC = No connection. Pin must be left floating.

Notes

- 15. All V_{SS} pins should be brought out to one common GND plane.
- 16. These are the ISSP pins, which are not High Z at POR. See the [PSoC Technical Reference Manual](#) for details.

Figure 8. CY8C24094 OCD (Not for Production)



BGA (Top View)

100-Ball VFBGA Part Pinout (On-Chip Debug)

The following 100-pin VFBGA part table and drawing is for the CY8C24094 OCD PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 7. 100-Ball Part Pinout (VFBGA^[17])

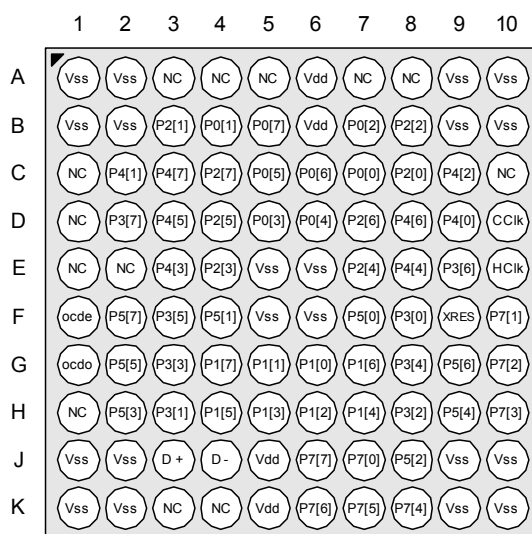
| Pin No. | Digital | Analog | Name | Description | Pin No. | Digital | Analog | Name | Description |
|---------|---------|--------|-----------------|---|---------|---------|--------|-----------------|--|
| A1 | Power | | V _{SS} | Ground connection | F1 | | | OCDE | OCD even data I/O |
| A2 | Power | | V _{SS} | Ground connection | F2 | I/O | M | P5[7] | |
| A3 | | | NC | No connection. Pin must be left floating | F3 | I/O | M | P3[5] | |
| A4 | | | NC | No connection. Pin must be left floating | F4 | I/O | M | P5[1] | |
| A5 | | | NC | No connection. Pin must be left floating. | F5 | Power | | V _{SS} | Ground connection |
| A6 | Power | | V _{DD} | Supply voltage. | F6 | Power | | V _{SS} | Ground connection |
| A7 | | | NC | No connection. Pin must be left floating. | F7 | I/O | M | P5[0] | |
| A8 | | | NC | No connection. Pin must be left floating. | F8 | I/O | M | P3[0] | |
| A9 | Power | | V _{SS} | Ground connection | F9 | | | XRES | Active high pin reset with internal pull-down |
| A10 | Power | | V _{SS} | Ground connection | F10 | I/O | | P7[1] | |
| B1 | Power | | V _{SS} | Ground connection | G1 | | | OCDO | OCD odd data output |
| B2 | Power | | V _{SS} | Ground connection | G2 | I/O | M | P5[5] | |
| B3 | I/O | I, M | P2[1] | Direct switched capacitor block input | G3 | I/O | M | P3[3] | |
| B4 | I/O | I, M | P0[1] | Analog column mux input | G4 | I/O | M | P1[7] | I ² C SCL |
| B5 | I/O | I, M | P0[7] | Analog column mux input | G5 | I/O | M | P1[1] | I ² C SCL, ISSP SCLK ^[18] |
| B6 | Power | | V _{DD} | Supply voltage | G6 | I/O | M | P1[0] | I ² C SDA, ISSP SDATA ^[18] |
| B7 | I/O | I, M | P0[2] | Analog column mux input | G7 | I/O | M | P1[6] | |
| B8 | I/O | I, M | P2[2] | Direct switched capacitor block input | G8 | I/O | M | P3[4] | |
| B9 | Power | | V _{SS} | Ground connection | G9 | I/O | M | P5[6] | |
| B10 | Power | | V _{SS} | Ground connection | G10 | I/O | | P7[2] | |
| C1 | | | NC | No connection. Pin must be left floating | H1 | | | NC | No connection. Pin must be left floating |
| C2 | I/O | M | P4[1] | | H2 | I/O | M | P5[3] | |
| C3 | I/O | M | P4[7] | | H3 | I/O | M | P3[1] | |
| C4 | I/O | M | P2[7] | | H4 | I/O | M | P1[5] | I ² C SDA |
| C5 | I/O | I/O, M | P0[5] | Analog column mux input and column output | H5 | I/O | M | P1[3] | |
| C6 | I/O | I, M | P0[6] | Analog column mux input | H6 | I/O | M | P1[2] | |
| C7 | I/O | I, M | P0[0] | Analog column mux input | H7 | I/O | M | P1[4] | Optional EXTCLK |
| C8 | I/O | I, M | P2[0] | Direct switched capacitor block input | H8 | I/O | M | P3[2] | |
| C9 | I/O | M | P4[2] | | H9 | I/O | M | P5[4] | |
| C10 | | | NC | No connection. Pin must be left floating | H10 | I/O | | P7[3] | |
| D1 | | | NC | No connection. Pin must be left floating | J1 | Power | | V _{SS} | Ground connection |
| D2 | I/O | M | P3[7] | | J2 | Power | | V _{SS} | Ground connection |
| D3 | I/O | M | P4[5] | | J3 | USB | | D+ | |
| D4 | I/O | M | P2[5] | | J4 | USB | | D- | |
| D5 | I/O | I/O, M | P0[3] | Analog column mux input and column output | J5 | Power | | V _{DD} | Supply voltage |
| D6 | I/O | I, M | P0[4] | Analog column mux input | J6 | I/O | | P7[7] | |
| D7 | I/O | M | P2[6] | External VREF input | J7 | I/O | | P7[0] | |
| D8 | I/O | M | P4[6] | | J8 | I/O | M | P5[2] | |
| D9 | I/O | M | P4[0] | | J9 | Power | | V _{SS} | Ground connection |
| D10 | | | CCLK | OCD CPU clock output | J10 | Power | | V _{SS} | Ground connection |
| E1 | | | NC | No connection. Pin must be left floating | K1 | Power | | V _{SS} | Ground connection |
| E2 | | | NC | No connection. Pin must be left floating | K2 | Power | | V _{SS} | Ground connection |
| E3 | I/O | M | P4[3] | | K3 | | | NC | No connection. Pin must be left floating |
| E4 | I/O | I, M | P2[3] | Direct switched capacitor block input | K4 | | | NC | No connection. Pin must be left floating |
| E5 | Power | | V _{SS} | Ground connection | K5 | Power | | V _{DD} | Supply voltage |
| E6 | Power | | V _{SS} | Ground connection | K6 | I/O | | P7[6] | |
| E7 | I/O | M | P2[4] | External AGND input | K7 | I/O | | P7[5] | |
| E8 | I/O | M | P4[4] | | K8 | I/O | | P7[4] | |
| E9 | I/O | M | P3[6] | | K9 | Power | | V _{SS} | Ground connection |
| E10 | | | HCLK | OCD high speed clock output | K10 | Power | | V _{SS} | Ground connection |

LEGEND A = Analog, I = Input, O = Output, M = Analog Mux Input, NC = No connection. Pin must be left floating, OCD = On-Chip Debugger.

Notes

- 17. All V_{SS} pins should be brought out to one common GND plane.
- 18. These are the ISSP pins, which are not High Z at POR. See the [PSoC Technical Reference Manual](#) for details.

Figure 9. CY8C24094 OCD (Not for Production)



BGA (Top View)

100-Pin Part Pinout (On-Chip Debug)

The 100-pin TQFP part is for the CY8C24094 OCD PSoC device.

Note: This part is only used for in-circuit debugging. It is NOT available for production.

Table 8. 100-Pin Part Pinout (TQFP^[19])

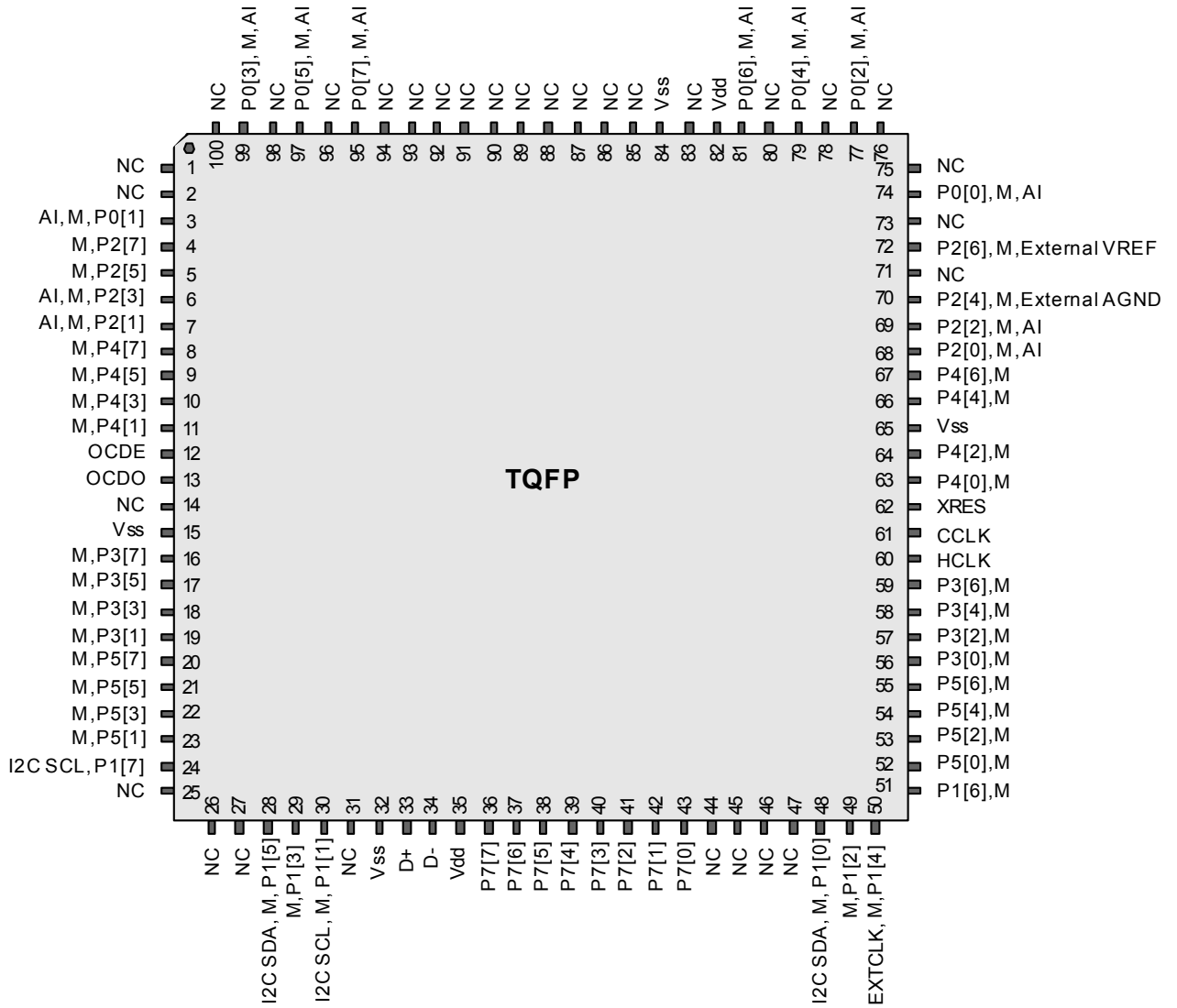
| Pin No. | Digital | Analog | Name | Description | Pin No. | Digital | Analog | Name | Description |
|---------|---------|--------|-----------------|---|---------|---------|--------|-----------------|---|
| 1 | | | NC | No connection. Pin must be left floating | 51 | I/O | M | P1[6] | |
| 2 | | | NC | No connection. Pin must be left floating | 52 | I/O | M | P5[0] | |
| 3 | I/O | I, M | P0[1] | Analog column mux input | 53 | I/O | M | P5[2] | |
| 4 | I/O | M | P2[7] | | 54 | I/O | M | P5[4] | |
| 5 | I/O | M | P2[5] | | 55 | I/O | M | P5[6] | |
| 6 | I/O | I, M | P2[3] | Direct switched capacitor block input | 56 | I/O | M | P3[0] | |
| 7 | I/O | I, M | P2[1] | Direct switched capacitor block input | 57 | I/O | M | P3[2] | |
| 8 | I/O | M | P4[7] | | 58 | I/O | M | P3[4] | |
| 9 | I/O | M | P4[5] | | 59 | I/O | M | P3[6] | |
| 10 | I/O | M | P4[3] | | 60 | | | HCLK | OCD high speed clock output |
| 11 | I/O | M | P4[1] | | 61 | | | CCLK | OCD CPU clock output |
| 12 | | | OCDE | OCD even data I/O | 62 | Input | | XRES | Active high pin reset with internal pull-down |
| 13 | | | OCDO | OCD odd data output | 63 | I/O | M | P4[0] | |
| 14 | | | NC | No connection. Pin must be left floating | 64 | I/O | M | P4[2] | |
| 15 | Power | | V _{SS} | Ground connection | 65 | Power | | V _{SS} | Ground connection |
| 16 | I/O | M | P3[7] | | 66 | I/O | M | P4[4] | |
| 17 | I/O | M | P3[5] | | 67 | I/O | M | P4[6] | |
| 18 | I/O | M | P3[3] | | 68 | I/O | I, M | P2[0] | Direct switched capacitor block input |
| 19 | I/O | M | P3[1] | | 69 | I/O | I, M | P2[2] | Direct switched capacitor block input |
| 20 | I/O | M | P5[7] | | 70 | I/O | | P2[4] | External AGND input |
| 21 | I/O | M | P5[5] | | 71 | | | NC | No connection. Pin must be left floating |
| 22 | I/O | M | P5[3] | | 72 | I/O | | P2[6] | External VREF input |
| 23 | I/O | M | P5[1] | | 73 | | | NC | No connection. Pin must be left floating |
| 24 | I/O | M | P1[7] | I ² C SCL | 74 | I/O | I | P0[0] | Analog column mux input |
| 25 | | | NC | No connection. Pin must be left floating | 75 | | | NC | No connection. Pin must be left floating |
| 26 | | | NC | No connection. Pin must be left floating | 76 | | | NC | No connection. Pin must be left floating |
| 27 | | | NC | No connection. Pin must be left floating | 77 | I/O | I, M | P0[2] | Analog column mux input and column output |
| 28 | I/O | | P1[5] | I ² C SDA | 78 | | | NC | No connection. Pin must be left floating |
| 29 | I/O | | P1[3] | | 79 | I/O | I, M | P0[4] | Analog column mux input and column output |
| 30 | I/O | | P1[1] | Crystal (XTALin), I ² C SCL, ISSP SCLK ^[20] | 80 | | | NC | No connection. Pin must be left floating |
| 31 | | | NC | No connection. Pin must be left floating | 81 | I/O | I, M | P0[6] | Analog column mux input |
| 32 | Power | | V _{SS} | Ground connection | 82 | Power | | V _{DD} | Supply voltage |
| 33 | USB | | D+ | | 83 | | | NC | No connection. Pin must be left floating |
| 34 | USB | | D- | | 84 | Power | | V _{SS} | Ground connection |
| 35 | Power | | V _{DD} | Supply voltage | 85 | | | NC | No connection. Pin must be left floating |
| 36 | I/O | | P7[7] | | 86 | | | NC | No connection. Pin must be left floating |
| 37 | I/O | | P7[6] | | 87 | | | NC | No connection. Pin must be left floating |
| 38 | I/O | | P7[5] | | 88 | | | NC | No connection. Pin must be left floating |
| 39 | I/O | | P7[4] | | 89 | | | NC | No connection. Pin must be left floating |
| 40 | I/O | | P7[3] | | 90 | | | NC | No connection. Pin must be left floating |
| 41 | I/O | | P7[2] | | 91 | | | NC | No connection. Pin must be left floating |
| 42 | I/O | | P7[1] | | 92 | | | NC | No connection. Pin must be left floating |
| 43 | I/O | | P7[0] | | 93 | | | NC | No connection. Pin must be left floating |
| 44 | | | NC | No connection. Pin must be left floating | 94 | | | NC | No connection. Pin must be left floating |
| 45 | | | NC | No connection. Pin must be left floating | 95 | I/O | I, M | P0[7] | Analog column mux input |
| 46 | | | NC | No connection. Pin must be left floating | 96 | | | NC | No connection. Pin must be left floating |
| 47 | | | NC | No connection. Pin must be left floating | 97 | I/O | I/O, M | P0[5] | Analog column mux input and column output |
| 48 | I/O | | P1[0] | Crystal (XTALout), I2C SDA, ISSP SDATA ^[20] | 98 | | | NC | No connection. Pin must be left floating |
| 49 | I/O | | P1[2] | | 99 | I/O | I/O, M | P0[3] | Analog column mux input and column output |
| 50 | I/O | | P1[4] | Optional EXTCLK | 100 | | | NC | No connection. Pin must be left floating |

LEGEND A = Analog, I = Input, O = Output, NC = No connection. Pin must be left floating, M = Analog Mux Input, OCD = On-Chip Debugger.

Notes

- 19. All V_{SS} pins should be brought out to one common GND plane.
- 20. These are the ISSP pins, which are not High Z at POR. See the [PSoC Technical Reference Manual](#) for details.

Figure 10. CY8C24094 OCD (Not for Production)



Register Reference

This section lists the registers of the CY8C24x94 PSoC device family. For detailed register information, see the [PSoC Technical Reference Manual](#).

Register Conventions

The register conventions specific to this section are listed in the following table.

| Convention | Description |
|------------|------------------------------|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XO1 bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XO1 bit is set to 1, the user is in Bank 1.

Note: In the following register mapping tables, blank fields are Reserved and should not be accessed.

Register Map Bank 0 Table: User Space

| Name | Addr (0, Hex) | Access | Name | Addr (0, Hex) | Access | Name | Addr (0, Hex) | Access | Name | Addr (0, Hex) | Access |
|----------|---------------|--------|-----------|---------------|--------|----------|---------------|--------|----------|---------------|--------|
| PRT0DR | 00 | RW | PMA0_DR | 40 | RW | ASC10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | PMA1_DR | 41 | RW | ASC10CR1 | 81 | RW | | C1 | |
| PRT0GS | 02 | RW | PMA2_DR | 42 | RW | ASC10CR2 | 82 | RW | | C2 | |
| PRT0DM2 | 03 | RW | PMA3_DR | 43 | RW | ASC10CR3 | 83 | RW | | C3 | |
| PRT1DR | 04 | RW | PMA4_DR | 44 | RW | ASD11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | PMA5_DR | 45 | RW | ASD11CR1 | 85 | RW | | C5 | |
| PRT1GS | 06 | RW | PMA6_DR | 46 | RW | ASD11CR2 | 86 | RW | | C6 | |
| PRT1DM2 | 07 | RW | PMA7_DR | 47 | RW | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DR | 08 | RW | USB_SOF0 | 48 | R | | 88 | | | C8 | |
| PRT2IE | 09 | RW | USB_SOF1 | 49 | R | | 89 | | | C9 | |
| PRT2GS | 0A | RW | USB_CR0 | 4A | RW | | 8A | | | CA | |
| PRT2DM2 | 0B | RW | USB/O_CR0 | 4B | # | | 8B | | | CB | |
| PRT3DR | 0C | RW | USB/O_CR1 | 4C | RW | | 8C | | | CC | |
| PRT3IE | 0D | RW | | 4D | | | 8D | | | CD | |
| PRT3GS | 0E | RW | EP1_CNT1 | 4E | # | | 8E | | | CE | |
| PRT3DM2 | 0F | RW | EP1_CNT | 4F | RW | | 8F | | | CF | |
| PRT4DR | 10 | RW | EP2_CNT1 | 50 | # | ASD20CR0 | 90 | RW | CUR_PP | D0 | RW |
| PRT4IE | 11 | RW | EP2_CNT | 51 | RW | ASD20CR1 | 91 | RW | STK_PP | D1 | RW |
| PRT4GS | 12 | RW | EP3_CNT1 | 52 | # | ASD20CR2 | 92 | RW | | D2 | |
| PRT4DM2 | 13 | RW | EP3_CNT | 53 | RW | ASD20CR3 | 93 | RW | IDX_PP | D3 | RW |
| PRT5DR | 14 | RW | EP4_CNT1 | 54 | # | ASC21CR0 | 94 | RW | MVR_PP | D4 | RW |
| PRT5IE | 15 | RW | EP4_CNT | 55 | RW | ASC21CR1 | 95 | RW | MVW_PP | D5 | RW |
| PRT5GS | 16 | RW | EP0_CR | 56 | # | ASC21CR2 | 96 | RW | I2C_CFG | D6 | RW |
| PRT5DM2 | 17 | RW | EP0_CNT | 57 | # | ASC21CR3 | 97 | RW | I2C_SCR | D7 | # |
| | 18 | | EP0_DR0 | 58 | RW | | 98 | | I2C_DR | D8 | RW |
| | 19 | | EP0_DR1 | 59 | RW | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | EP0_DR2 | 5A | RW | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | EP0_DR3 | 5B | RW | | 9B | | INT_CLR1 | DB | RW |
| PRT7DR | 1C | RW | EP0_DR4 | 5C | RW | | 9C | | INT_CLR2 | DC | RW |
| PRT7IE | 1D | RW | EP0_DR5 | 5D | RW | | 9D | | INT_CLR3 | DD | RW |
| PRT7GS | 1E | RW | EP0_DR6 | 5E | RW | | 9E | | INT_MSK3 | DE | RW |
| PRT7DM2 | 1F | RW | EP0_DR7 | 5F | RW | | 9F | | INT_MSK2 | DF | RW |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | AMUXCFG | 61 | RW | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | | 62 | | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | DEC_DH | E4 | RC |
| DBB01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | DEC_DL | E5 | RC |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | | 68 | | MUL1_X | A8 | W | MUL0_X | E8 | W |
| DCB02DR1 | 29 | W | | 69 | | MUL1_Y | A9 | W | MUL0_Y | E9 | W |
| DCB02DR2 | 2A | RW | | 6A | | MUL1_DH | AA | R | MUL0_DH | EA | R |
| DCB02CR0 | 2B | # | | 6B | | MUL1_DL | AB | R | MUL0_DL | EB | R |
| DCB03DR0 | 2C | # | TMP_DR0 | 6C | RW | ACC1_DR1 | AC | RW | ACC0_DR1 | EC | RW |
| DCB03DR1 | 2D | W | TMP_DR1 | 6D | RW | ACC1_DR0 | AD | RW | ACC0_DR0 | ED | RW |
| DCB03DR2 | 2E | RW | TMP_DR2 | 6E | RW | ACC1_DR3 | AE | RW | ACC0_DR3 | EE | RW |
| DCB03CR0 | 2F | # | TMP_DR3 | 6F | RW | ACC1_DR2 | AF | RW | ACC0_DR2 | EF | RW |
| | 30 | | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| | 31 | | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | DAC_D | FD | RW |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are reserved and should not be accessed.

Access is bit specific.

Register Map Bank 1 Table: Configuration Space

| Name | Addr (1, Hex) | Access | Name | Addr (1, Hex) | Access | Name | Addr (1, Hex) | Access | Name | Addr (1, Hex) | Access |
|---------|---------------|--------|-----------|---------------|--------|----------|---------------|--------|-----------|---------------|--------|
| PRT0DM0 | 00 | RW | PMA0_WA | 40 | RW | ASC10CR0 | 80 | RW | USB/O_CR2 | C0 | RW |
| PRT0DM1 | 01 | RW | PMA1_WA | 41 | RW | ASC10CR1 | 81 | RW | USB_CR1 | C1 | # |
| PRT0IC0 | 02 | RW | PMA2_WA | 42 | RW | ASC10CR2 | 82 | RW | | | |
| PRT0IC1 | 03 | RW | PMA3_WA | 43 | RW | ASC10CR3 | 83 | RW | | | |
| PRT1DM0 | 04 | RW | PMA4_WA | 44 | RW | ASD11CR0 | 84 | RW | EP1_CR0 | C4 | # |
| PRT1DM1 | 05 | RW | PMA5_WA | 45 | RW | ASD11CR1 | 85 | RW | EP2_CR0 | C5 | # |
| PRT1IC0 | 06 | RW | PMA6_WA | 46 | RW | ASD11CR2 | 86 | RW | EP3_CR0 | C6 | # |
| PRT1IC1 | 07 | RW | PMA7_WA | 47 | RW | ASD11CR3 | 87 | RW | EP4_CR0 | C7 | # |
| PRT2DM0 | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2DM1 | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2IC0 | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2IC1 | 0B | RW | | 4B | | | 8B | | | CB | |
| PRT3DM0 | 0C | RW | | 4C | | | 8C | | | CC | |
| PRT3DM1 | 0D | RW | | 4D | | | 8D | | | CD | |
| PRT3IC0 | 0E | RW | | 4E | | | 8E | | | CE | |
| PRT3IC1 | 0F | RW | | 4F | | | 8F | | | CF | |
| PRT4DM0 | 10 | RW | PMA0_RA | 50 | RW | | 90 | | GDI_O_IN | D0 | RW |
| PRT4DM1 | 11 | RW | PMA1_RA | 51 | RW | ASD20CR1 | 91 | RW | GDI_E_IN | D1 | RW |
| PRT4IC0 | 12 | RW | PMA2_RA | 52 | RW | ASD20CR2 | 92 | RW | GDI_O_OU | D2 | RW |
| PRT4IC1 | 13 | RW | PMA3_RA | 53 | RW | ASD20CR3 | 93 | RW | GDI_E_OU | D3 | RW |
| PRT5DM0 | 14 | RW | PMA4_RA | 54 | RW | ASC21CR0 | 94 | RW | | D4 | |
| PRT5DM1 | 15 | RW | PMA5_RA | 55 | RW | ASC21CR1 | 95 | RW | | D5 | |
| PRT5IC0 | 16 | RW | PMA6_RA | 56 | RW | ASC21CR2 | 96 | RW | | D6 | |
| PRT5IC1 | 17 | RW | PMA7_RA | 57 | RW | ASC21CR3 | 97 | RW | | D7 | |
| | 18 | | | 58 | | | 98 | | MUX_CR0 | D8 | RW |
| | 19 | | | 59 | | | 99 | | MUX_CR1 | D9 | RW |
| | 1A | | | 5A | | | 9A | | MUX_CR2 | DA | RW |
| | 1B | | | 5B | | | 9B | | MUX_CR3 | DB | RW |
| PRT7DM0 | 1C | RW | | 5C | | | 9C | | | DC | |
| PRT7DM1 | 1D | RW | | 5D | | | 9D | | OSC_GO_EN | DD | RW |
| PRT7IC0 | 1E | RW | | 5E | | | 9E | | OSC_CR4 | DE | RW |
| PRT7IC1 | 1F | RW | | 5F | | | 9F | | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | CMP_GO_EN | 64 | RW | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | | E5 | |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | | E6 | |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | | E7 | |
| DCB02FN | 28 | RW | | 68 | | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | | 69 | | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | | 6B | | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | TMP_DR0 | 6C | RW | | AC | | MUX_CR4 | EC | RW |
| DCB03IN | 2D | RW | TMP_DR1 | 6D | RW | | AD | | MUX_CR5 | ED | RW |
| DCB03OU | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| | 2F | | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| | 31 | | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | DAC_CR | FD | RW |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are reserved and should not be accessed.

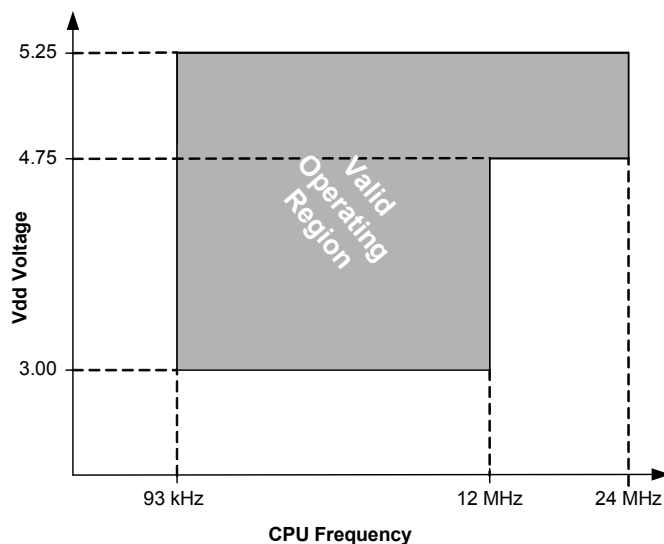
Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C24x94 PSoC device family. For the most up-to-date electrical specifications, confirm that you have the most recent datasheet by visiting <http://www.cypress.com>.

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications for devices running at greater than 12 MHz are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$ and $T_J \leq 82\text{ }^{\circ}\text{C}$.

Figure 11. Voltage Versus CPU Frequency



Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings

| Parameter | Description | Min | Typ | Max | Units | Notes |
|----------------|---|-------------------|-----|-------------------|--------------------|--|
| T_{STG} | Storage temperature | -55 | 25 | +100 | $^{\circ}\text{C}$ | Higher storage temperatures reduces data retention time. Recommended storage temperature is $+25\text{ }^{\circ}\text{C} \pm 25\text{ }^{\circ}\text{C}$. Extended duration storage temperatures higher than $65\text{ }^{\circ}\text{C}$ degrades reliability. |
| $T_{BAKETEMP}$ | Bake temperature | - | 125 | See package label | $^{\circ}\text{C}$ | |
| $t_{BAKETIME}$ | Bake time | See package label | - | 72 | Hours | |
| T_A | Ambient temperature with power applied | -40 | - | +85 | $^{\circ}\text{C}$ | |
| V_{DD} | Supply voltage on V_{DD} relative to V_{SS} | -0.5 | - | +6.0 | V | |
| $V_{I/O}$ | DC input voltage | $V_{SS} - 0.5$ | - | $V_{DD} + 0.5$ | V | |
| $V_{I/O2}$ | DC voltage applied to tristate | $V_{SS} - 0.5$ | - | $V_{DD} + 0.5$ | V | |
| $I_{MI/O}$ | Maximum current into any port pin | -25 | - | +50 | mA | |
| $I_{MAI/O}$ | Maximum current into any port pin configured as analog driver | -50 | - | +50 | mA | |
| ESD | Electrostatic discharge voltage | 2000 | - | - | V | Human body model ESD. |
| LU | Latch-up current | - | - | 200 | mA | |

Operating Temperature

Table 10. Operating Temperature

| Parameter | Description | Min | Typ | Max | Units | Notes |
|------------|-------------------------------|-----|-----|------|-------|--|
| T_A | Ambient temperature | -40 | - | +85 | °C | |
| T_{AUSB} | Ambient temperature using USB | -10 | - | +85 | °C | |
| T_J | Junction temperature | -40 | - | +100 | °C | The temperature rise from ambient to junction is package specific. See Thermal Impedance on page 49 . The user must limit the power consumption to comply with this requirement. |

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ °C} \leq T_A \leq 85\text{ °C}$, or 3.0 V to 3.6 V and $-40\text{ °C} \leq T_A \leq 85\text{ °C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 11. DC Chip-Level Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|-----------|---|-----|-----|------|-------|---|
| V_{DD} | Supply voltage | 3.0 | - | 5.25 | V | See DC POR and LVD specifications, Table 22 on page 38 . |
| I_{DD5} | Supply current, IMO = 24 MHz (5 V) | - | 14 | 27 | mA | Conditions are $V_{DD} = 5.0\text{ V}$, $T_A = 25\text{ °C}$, CPU = 3 MHz, SYSCCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. |
| I_{DD3} | Supply current, IMO = 24 MHz (3.3 V) | - | 8 | 14 | mA | Conditions are $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ °C}$, CPU = 3 MHz, SYSCCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.367 kHz, analog power = off. |
| I_{SB} | Sleep ^[21] (mode) current with POR, LVD, sleep timer, and WDT. ^[22] | - | 3 | 6.5 | μA | Conditions are with internal slow speed oscillator, $V_{DD} = 3.3\text{ V}$, $-40\text{ °C} \leq T_A \leq 55\text{ °C}$, analog power = off. |
| I_{SBH} | Sleep (mode) current with POR, LVD, Sleep Timer, and WDT at high temperature. ^[22] | - | 4 | 25 | μA | Conditions are with internal slow speed oscillator, $V_{DD} = 3.3\text{ V}$, $55\text{ °C} < T_A \leq 85\text{ °C}$, analog power = off. |

Notes

21. **Errata:** When the device is operating at 4.75 V to 5.25 V and the 3.3 V regulator is enabled, a short low pulse may be created on the DP signal line during device wake-up. The 15-20 μs low pulse of the DP line may be interpreted by the host computer as a deattach or the beginning of a wake-up. More details in "Errata" on page 64.
22. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 12. DC GPIO Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|------------------|-----------------------------------|-----------------------|-----|------|-------|---|
| R _{PU} | Pull-up resistor | 4 | 5.6 | 8 | kΩ | |
| R _{PD} | Pull-down resistor | 4 | 5.6 | 8 | kΩ | |
| V _{OH} | High output level | V _{DD} - 1.0 | – | – | V | I _{OH} = 10 mA, V _{DD} = 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or V _{DD} = 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I _{OH} budget. |
| V _{OL} | Low output level | – | – | 0.75 | V | I _{OL} = 25 mA, V _{DD} = 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or V _{DD} = 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 200 mA maximum combined I _{OL} budget. |
| I _{OH} | High level source current | 10 | – | – | mA | V _{OH} = V _{DD} - 1.0 V, see the limitations of the total current in the note for V _{OH} |
| I _{OL} | Low level sink current | 25 | – | – | mA | V _{OL} = 0.75 V, see the limitations of the total current in the note for V _{OL} |
| V _{IL} | Input low level | – | – | 0.8 | V | V _{DD} = 3.0 to 5.25. |
| V _{IH} | Input high level | 2.1 | – | – | V | V _{DD} = 3.0 to 5.25. |
| V _H | Input hysteresis | – | 60 | – | mV | |
| I _{IL} | Input leakage (absolute value) | – | 1 | – | nA | Gross tested to 1 μA. |
| C _{IN} | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C. |
| C _{OUT} | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C. |

DC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-10\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-10\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 13. DC Full Speed (12 Mbps) USB Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|----------------------|--------------------------------------|-----|-----|-----|-------|---|
| USB Interface | | | | | | |
| V _{DI} | Differential input sensitivity | 0.2 | – | – | V | (D+) – (D–) |
| V _{CM} | Differential input common mode range | 0.8 | – | 2.5 | V | |
| V _{SE} | Single ended receiver threshold | 0.8 | – | 2.0 | V | |
| C _{IN} | Transceiver capacitance | – | – | 20 | pF | |
| I _{I/O} | High Z state data line leakage | –10 | – | 10 | μA | 0 V < V _{IN} < 3.3 V. |
| R _{EXT} | External USB series resistor | 23 | – | 25 | Ω | In series with each USB pin. |
| V _{UOH} | Static output high, driven | 2.8 | – | 3.6 | V | 15 kΩ ± 5% to ground. Internal pull-up enabled. |
| V _{UOHI} | Static output high, idle | 2.7 | – | 3.6 | V | 15 kΩ ± 5% to ground. Internal pull-up enabled. |
| V _{UOL} | Static output low | – | – | 0.3 | V | 15 kΩ ± 5% to ground. Internal pull-up enabled. |
| Z _O | USB driver output impedance | 28 | – | 44 | Ω | Including R _{EXT} resistor. |
| V _{CRS} | D+/D– crossover voltage | 1.3 | – | 2.0 | V | |

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog continuous time PSoC blocks and the analog switched capacitor PSoC blocks. The guaranteed specifications are measured in the analog continuous time PSoC block.

Table 14. 5-V DC Operational Amplifier Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|----------------------|---|-----------------------|------|-----------------------|-------|---|
| V _{OSOA} | Input offset voltage (absolute value) | – | 1.6 | 10 | mV | |
| | Power = low, Opamp bias = high | – | 1.3 | 8 | mV | |
| | Power = high, Opamp bias = high | – | 1.2 | 7.5 | mV | |
| TCV _{OSOA} | Average input offset voltage drift | – | 7.0 | 35.0 | μV/°C | |
| I _{EBOA} | Input leakage current (Port 0 analog pins) | – | 20 | – | pA | Gross tested to 1 μA. |
| C _{INOA} | Input capacitance (Port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25 °C. |
| V _{CMOA} | Common mode voltage range | 0.0 | – | V _{DD} | V | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| | Common mode voltage range (high power or high Opamp bias) | 0.5 | – | V _{DD} – 0.5 | V | |
| G _{OLOA} | Open loop gain | | | | | |
| | Power = low, Opamp bias = high | 60 | – | – | dB | |
| | Power = high, Opamp bias = high | 80 | – | – | dB | |
| V _{OHIGHOA} | High output voltage swing (internal signals) | | | | | |
| | Power = low, Opamp bias = high | V _{DD} – 0.2 | – | – | V | |
| | Power = high, Opamp bias = high | V _{DD} – 0.5 | – | – | V | |
| V _{OLOWOA} | Low output voltage swing (internal signals) | | | | | |
| | Power = low, Opamp bias = high | – | – | 0.2 | V | |
| | Power = high, Opamp bias = high | – | – | 0.5 | V | |
| I _{SOA} | Supply current (including associated AGND buffer) | | | | | |
| | Power = low, Opamp bias = low | – | 400 | 800 | μA | |
| | Power = low, Opamp bias = high | – | 500 | 900 | μA | |
| | Power = medium, Opamp bias = low | – | 800 | 1000 | μA | |
| | Power = medium, Opamp bias = high | – | 1200 | 1600 | μA | |
| | Power = high, Opamp bias = high | – | 4600 | 6400 | μA | |
| PSRR _{OA} | Supply voltage rejection ratio | 65 | 80 | – | dB | V _{SS} ≤ V _{IN} ≤ (V _{DD} – 2.25) or (V _{DD} – 1.25 V) ≤ V _{IN} ≤ V _{DD} . |

Table 15. 3.3-V DC Operational Amplifier Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|----------------|---|--|--|---|--|---|
| $V_{OSO A}$ | Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high | – – – | 1.65 1.32 – | 10 8 – | mV mV mV | Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation |
| $TCV_{OSO A}$ | Average input offset voltage drift | – | 7.0 | 35.0 | $\mu\text{V}/^{\circ}\text{C}$ | |
| $I_{EBO A}$ | Input leakage current (port 0 analog pins) | – | 20 | – | pA | Gross tested to 1 μA . |
| $C_{INO A}$ | Input capacitance (port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25 $^{\circ}\text{C}$. |
| $V_{CMO A}$ | Common mode voltage range | 0.2 | – | $V_{DD} - 0.2$ | V | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| $G_{OLO A}$ | Open loop gain Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low | 60 60 80 | – – – | – – – | dB dB dB | Specification is applicable at Low opamp bias. For high opamp bias mode (except high power, High opamp bias), minimum is 60 dB. |
| $V_{OHIGHO A}$ | High output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low | $V_{DD} - 0.2$ $V_{DD} - 0.2$ $V_{DD} - 0.2$ | – – – | – – – | V V V | Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation |
| $V_{OLOWO A}$ | Low output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low | – – – | – – – | 0.2 0.2 0.2 | V V V | Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation |
| $I_{SO A}$ | Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high | – – – – – – | 400 500 800 1200 2400 – | 800 900 1000 1600 3200 – | μA μA μA μA μA μA | Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation |
| $PSRR_{O A}$ | Supply voltage rejection ratio | 65 | 80 | – | dB | $V_{SS} \leq V_{IN} \leq (V_{DD} - 2.25)$ or $(V_{DD} - 1.25 \text{ V}) \leq V_{IN} \leq V_{DD}$ |

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V at 25 $^{\circ}\text{C}$ and are for design guidance only.

Table 16. DC Low Power Comparator Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|--------------|--|-----|-----|--------------|---------------|-------|
| V_{REFLPC} | Low power comparator (LPC) reference voltage range | 0.2 | – | $V_{DD} - 1$ | V | |
| I_{SLPC} | LPC supply current | – | 10 | 40 | μA | |
| V_{OSLPC} | LPC voltage offset | – | 2.5 | 30 | mV | |

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 17. 5-V DC Analog Output Buffer Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|---------------|---|--|------------|--|--------------------------------|--|
| C_L | Load Capacitance | – | – | 200 | pF | This specification applies to the external circuit that is being driven by the analog output buffer. |
| V_{OSOB} | Input offset voltage (absolute value) | – | 3 | 12 | mV | |
| TCV_{OSOB} | Average input offset voltage drift | – | +6 | – | $\mu\text{V}/^{\circ}\text{C}$ | |
| V_{CMOB} | Common mode input voltage range | 0.5 | – | $V_{DD} - 1.0$ | V | |
| R_{OUTOB} | Output resistance Power = low Power = high | – – | 0.6 0.6 | – – | Ω Ω | |
| $V_{OHIGHOB}$ | High output voltage swing (Load = 32 ohms to $V_{DD}/2$) Power = low Power = high | $0.5 \times (V_{DD} + 1.1)$ $0.5 \times (V_{DD} + 1.1)$ | – – | – – | V V | |
| V_{OLOWOB} | Low output voltage swing (Load = 32 ohms to $V_{DD}/2$) Power = low Power = high | – – | – – | $0.5 \times (V_{DD} - 1.3)$ $0.5 \times (V_{DD} - 1.3)$ | V V | |
| I_{SOB} | Supply current including opamp bias cell (No Load) Power = low Power = high | – – | 1.1 2.6 | 5.1 8.8 | mA mA | |
| $PSRR_{OB}$ | Supply voltage rejection ratio | 53 | 64 | – | dB | $(0.5 \times (V_{DD} - 1.3)) \leq V_{OUT} \leq (V_{DD} - 2.3)$. |

Table 18. 3.3-V DC Analog Output Buffer Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|---------------|--|--|------------|--|------------------|--|
| C_L | Load Capacitance | – | – | 200 | pF | This specification applies to the external circuit that is being driven by the analog output buffer. |
| V_{OSOB} | Input offset voltage (absolute value) | – | 3 | 12 | mV | |
| TCV_{OSOB} | Average input offset voltage drift | – | +6 | – | $\mu V/^\circ C$ | |
| V_{CMOB} | Common mode input voltage range | 0.5 | – | $V_{DD} - 1.0$ | V | |
| R_{OUTOB} | Output resistance Power = low Power = high | – – | 1 1 | – – | W W | |
| $V_{OHIGHOB}$ | High output voltage swing (Load = 1 K ohms to $V_{DD}/2$) Power = low Power = high | $0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$ | – – | – – | V V | |
| V_{OLOWOB} | Low output voltage swing (Load = 1 K ohms to $V_{DD}/2$) Power = low Power = high | – – | – – | $0.5 \times V_{DD} - 1.0$ $0.5 \times V_{DD} - 1.0$ | V V | |
| I_{SOB} | Supply current including opamp bias cell (No load) Power = low Power = high | – – | 0.8 2.0 | 2.0 4.3 | mA mA | |
| $PSRR_{OB}$ | Supply voltage rejection ratio | 34 | 64 | – | dB | $(0.5 \times V_{DD} - 1.0) \leq V_{OUT} \leq (0.5 \times V_{DD} + 0.9)$. |

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 $^{\circ}\text{C}$ and are for design guidance only.

The guaranteed specifications for RefHi and RefLo are measured through the Analog Continuous Time PSoC blocks. The power levels for RefHi and RefLo refer to the Analog Reference Control register. AGND is measured at P2[4] in AGND bypass mode. Each Analog Continuous Time PSoC block adds a maximum of 10mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note: Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Note: Reference source has three power levels (high, medium and low). Accuracy of the reference source is less with low-power setting across temperature. It is recommended to use medium or high-power setting if the device is expected to operate across wide temperature limits.

Table 19. 5-V DC Analog Reference Specifications

| Reference ARF_CR [5:3] | Reference Power Settings | Parameter | Reference | Description | Min | Typ | Max | Units |
|------------------------|--|--------------------|-----------|------------------------------|----------------------------|----------------------------|----------------------------|-------|
| 0b000 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.229 | V _{DD} /2 + 1.290 | V _{DD} /2 + 1.346 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.038 | V _{DD} /2 | V _{DD} /2 + 0.040 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - Bandgap | V _{DD} /2 - 1.356 | V _{DD} /2 - 1.295 | V _{DD} /2 - 1.218 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.220 | V _{DD} /2 + 1.292 | V _{DD} /2 + 1.348 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.036 | V _{DD} /2 | V _{DD} /2 + 0.036 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - Bandgap | V _{DD} /2 - 1.357 | V _{DD} /2 - 1.297 | V _{DD} /2 - 1.225 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.221 | V _{DD} /2 + 1.293 | V _{DD} /2 + 1.351 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.036 | V _{DD} /2 | V _{DD} /2 + 0.036 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - Bandgap | V _{DD} /2 - 1.357 | V _{DD} /2 - 1.298 | V _{DD} /2 - 1.228 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.219 | V _{DD} /2 + 1.293 | V _{DD} /2 + 1.353 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.037 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.036 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - Bandgap | V _{DD} /2 - 1.359 | V _{DD} /2 - 1.299 | V _{DD} /2 - 1.229 | V |

Table 19. 5-V DC Analog Reference Specifications (continued)

| Reference ARF_CR [5:3] | Reference Power Settings | Parameter | Reference | Description | Min | Typ | Max | Units |
|------------------------|--|--------------------|-----------|---|----------------------------|----------------------------|----------------------------|-------|
| 0b001 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] + P2[6] - 0.092 | P2[4] + P2[6] - 0.011 | P2[4] + P2[6] + 0.064 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] - P2[6] - 0.031 | P2[4] - P2[6] + 0.007 | P2[4] - P2[6] + 0.056 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] + P2[6] - 0.078 | P2[4] + P2[6] - 0.008 | P2[4] + P2[6] + 0.063 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] - P2[6] - 0.031 | P2[4] - P2[6] + 0.004 | P2[4] - P2[6] + 0.043 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] + P2[6] - 0.073 | P2[4] + P2[6] - 0.006 | P2[4] + P2[6] + 0.062 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] - P2[6] - 0.032 | P2[4] - P2[6] + 0.003 | P2[4] - P2[6] + 0.038 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] + P2[6] - 0.073 | P2[4] + P2[6] - 0.006 | P2[4] + P2[6] + 0.062 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] - P2[6] - 0.034 | P2[4] - P2[6] + 0.002 | P2[4] - P2[6] + 0.037 | V |
| 0b010 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.037 | V _{DD} - 0.007 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.036 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.036 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.005 | V _{SS} + 0.029 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.034 | V _{DD} - 0.006 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.036 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.035 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.024 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.032 | V _{DD} - 0.005 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.036 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.035 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.003 | V _{SS} + 0.022 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.031 | V _{DD} - 0.005 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.037 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.035 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.003 | V _{SS} + 0.020 | V |

Table 19. 5-V DC Analog Reference Specifications (continued)

| Reference ARF_CR [5:3] | Reference Power Settings | Parameter | Reference | Description | Min | Typ | Max | Units |
|------------------------|--|--------------------|-----------|--|---------------|---------------|---------------|-------|
| 0b011 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | 3 × Bandgap | 3.760 | 3.884 | 4.006 | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.522 | 2.593 | 2.669 | V |
| | | V _{REFLO} | Ref Low | Bandgap | 1.252 | 1.299 | 1.342 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | 3 × Bandgap | 3.766 | 3.887 | 4.010 | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.523 | 2.594 | 2.670 | V |
| | | V _{REFLO} | Ref Low | Bandgap | 1.252 | 1.297 | 1.342 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | 3 × Bandgap | 3.769 | 3.888 | 4.013 | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.523 | 2.594 | 2.671 | V |
| | | V _{REFLO} | Ref Low | Bandgap | 1.251 | 1.296 | 1.343 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | 3 × Bandgap | 3.769 | 3.889 | 4.015 | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.523 | 2.595 | 2.671 | V |
| | | V _{REFLO} | Ref Low | Bandgap | 1.251 | 1.296 | 1.344 | V |
| 0b100 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.483 + P2[6] | 2.582 + P2[6] | 2.674 + P2[6] | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.522 | 2.593 | 2.669 | V |
| | | V _{REFLO} | Ref Low | 2 × Bandgap – P2[6] (P2[6] = 1.3 V) | 2.524 – P2[6] | 2.600 – P2[6] | 2.676 – P2[6] | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.490 + P2[6] | 2.586 + P2[6] | 2.679 + P2[6] | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.523 | 2.594 | 2.669 | V |
| | | V _{REFLO} | Ref Low | 2 × Bandgap – P2[6] (P2[6] = 1.3 V) | 2.523 – P2[6] | 2.598 – P2[6] | 2.675 – P2[6] | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.493 + P2[6] | 2.588 + P2[6] | 2.682 + P2[6] | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.523 | 2.594 | 2.670 | V |
| | | V _{REFLO} | Ref Low | 2 × Bandgap – P2[6] (P2[6] = 1.3 V) | 2.523 – P2[6] | 2.597 – P2[6] | 2.675 – P2[6] | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.494 + P2[6] | 2.589 + P2[6] | 2.685 + P2[6] | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.523 | 2.595 | 2.671 | V |
| | | V _{REFLO} | Ref Low | 2 × Bandgap – P2[6] (P2[6] = 1.3 V) | 2.522 – P2[6] | 2.596 – P2[6] | 2.676 – P2[6] | V |

Table 19. 5-V DC Analog Reference Specifications (continued)

| Reference ARF_CR [5:3] | Reference Power Settings | Parameter | Reference | Description | Min | Typ | Max | Units |
|------------------------|--|--------------------|-----------|---|-----------------|-------------------------|-------------------------|-------|
| 0b101 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.218 | P2[4] + 1.291 | P2[4] + 1.354 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.335 | P2[4] – 1.294 | P2[4] – 1.237 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.221 | P2[4] + 1.293 | P2[4] + 1.358 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.337 | P2[4] – 1.297 | P2[4] – 1.243 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.222 | P2[4] + 1.294 | P2[4] + 1.360 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.338 | P2[4] – 1.298 | P2[4] – 1.245 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.221 | P2[4] + 1.294 | P2[4] + 1.362 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.340 | P2[4] – 1.298 | P2[4] – 1.245 | V |
| 0b110 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | 2 × Bandgap | 2.513 | 2.593 | 2.672 | V |
| | | V _{AGND} | AGND | Bandgap | 1.264 | 1.302 | 1.340 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.008 | V _{SS} + 0.038 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | 2 × Bandgap | 2.514 | 2.593 | 2.674 | V |
| | | V _{AGND} | AGND | Bandgap | 1.264 | 1.301 | 1.340 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.005 | V _{SS} + 0.028 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | 2 × Bandgap | 2.514 | 2.593 | 2.676 | V |
| | | V _{AGND} | AGND | Bandgap | 1.264 | 1.301 | 1.340 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.024 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | 2 × Bandgap | 2.514 | 2.593 | 2.677 | V |
| | | V _{AGND} | AGND | Bandgap | 1.264 | 1.300 | 1.340 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.003 | V _{SS} + 0.021 | V |

Table 19. 5-V DC Analog Reference Specifications (continued)

| Reference ARF_CR [5:3] | Reference Power Settings | Parameter | Reference | Description | Min | Typ | Max | Units |
|------------------------|--|--------------------|-----------|-----------------|-----------------|-------------------------|-------------------------|-------|
| 0b111 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | 3.2 × Bandgap | 4.028 | 4.144 | 4.242 | V |
| | | V _{AGND} | AGND | 1.6 × Bandgap | 2.028 | 2.076 | 2.125 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.008 | V _{SS} + 0.034 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | 3.2 × Bandgap | 4.032 | 4.142 | 4.245 | V |
| | | V _{AGND} | AGND | 1.6 × Bandgap | 2.029 | 2.076 | 2.126 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.005 | V _{SS} + 0.025 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | 3.2 × Bandgap | 4.034 | 4.143 | 4.247 | V |
| | | V _{AGND} | AGND | 1.6 × Bandgap | 2.029 | 2.076 | 2.126 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.021 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | 3.2 × Bandgap | 4.036 | 4.144 | 4.249 | V |
| | | V _{AGND} | AGND | 1.6 × Bandgap | 2.029 | 2.076 | 2.126 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.003 | V _{SS} + 0.019 | V |

Table 20. 3.3-V DC Analog Reference Specifications

| Reference ARF_CR [5:3] | Reference Power Settings | Parameter | Reference | Description | Min | Typ | Max | Units |
|------------------------|--|--------------------|-----------|---|----------------------------|----------------------------|----------------------------|-------|
| 0b000 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.200 | V _{DD} /2 + 1.290 | V _{DD} /2 + 1.365 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.030 | V _{DD} /2 | V _{DD} /2 + 0.034 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 – Bandgap | V _{DD} /2 – 1.346 | V _{DD} /2 – 1.292 | V _{DD} /2 – 1.208 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.196 | V _{DD} /2 + 1.292 | V _{DD} /2 + 1.374 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.029 | V _{DD} /2 | V _{DD} /2 + 0.031 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 – Bandgap | V _{DD} /2 – 1.349 | V _{DD} /2 – 1.295 | V _{DD} /2 – 1.227 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.204 | V _{DD} /2 + 1.293 | V _{DD} /2 + 1.369 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.030 | V _{DD} /2 | V _{DD} /2 + 0.030 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 – Bandgap | V _{DD} /2 – 1.351 | V _{DD} /2 – 1.297 | V _{DD} /2 – 1.229 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.189 | V _{DD} /2 + 1.294 | V _{DD} /2 + 1.384 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.032 | V _{DD} /2 | V _{DD} /2 + 0.029 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 – Bandgap | V _{DD} /2 – 1.353 | V _{DD} /2 – 1.297 | V _{DD} /2 – 1.230 | V |
| 0b001 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] + P2[6] – 0.105 | P2[4] + P2[6] – 0.008 | P2[4] + P2[6] + 0.095 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] – P2[6] – 0.035 | P2[4] – P2[6] + 0.006 | P2[4] – P2[6] + 0.053 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] + P2[6] – 0.094 | P2[4] + P2[6] – 0.005 | P2[4] + P2[6] + 0.073 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] – P2[6] – 0.033 | P2[4] – P2[6] + 0.002 | P2[4] – P2[6] + 0.042 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] + P2[6] – 0.094 | P2[4] + P2[6] – 0.003 | P2[4] + P2[6] + 0.075 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] – P2[6] – 0.035 | P2[4] – P2[6] | P2[4] – P2[6] + 0.038 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] + P2[6] – 0.095 | P2[4] + P2[6] – 0.003 | P2[4] + P2[6] + 0.080 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] – P2[6] – 0.038 | P2[4] – P2[6] | P2[4] – P2[6] + 0.038 | V |

Table 20. 3.3-V DC Analog Reference Specifications (continued)

| Reference ARF_CR [5:3] | Reference Power Settings | Parameter | Reference | Description | Min | Typ | Max | Units |
|------------------------|---|--------------------|-----------|---|----------------------------|-------------------------|----------------------------|-------|
| 0b010 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.119 | V _{DD} - 0.005 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.028 | V _{DD} /2 | V _{DD} /2 + 0.029 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.022 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.131 | V _{DD} - 0.004 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.028 | V _{DD} /2 | V _{DD} /2 + 0.028 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.003 | V _{SS} + 0.021 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.111 | V _{DD} - 0.003 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.029 | V _{DD} /2 | V _{DD} /2 + 0.028 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.002 | V _{SS} + 0.017 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.128 | V _{DD} - 0.003 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.029 | V _{DD} /2 | V _{DD} /2 + 0.029 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.002 | V _{SS} + 0.019 | V |
| 0b011 | All power settings. Not allowed for 3.3 V. | - | - | - | - | - | - | - |
| 0b100 | All power settings. Not allowed for 3.3 V. | - | - | - | - | - | - | - |
| 0b101 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.214 | P2[4] + 1.291 | P2[4] + 1.359 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4] - Bandgap (P2[4] = V _{DD} /2) | P2[4] - 1.335 | P2[4] - 1.292 | P2[4] - 1.200 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.219 | P2[4] + 1.293 | P2[4] + 1.357 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4] - Bandgap (P2[4] = V _{DD} /2) | P2[4] - 1.335 | P2[4] - 1.295 | P2[4] - 1.243 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.222 | P2[4] + 1.294 | P2[4] + 1.356 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4] - Bandgap (P2[4] = V _{DD} /2) | P2[4] - 1.337 | P2[4] - 1.296 | P2[4] - 1.244 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.224 | P2[4] + 1.295 | P2[4] + 1.355 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4] - Bandgap (P2[4] = V _{DD} /2) | P2[4] - 1.339 | P2[4] - 1.297 | P2[4] - 1.244 | V |

Table 20. 3.3-V DC Analog Reference Specifications (continued)

| Reference ARF_CR [5:3] | Reference Power Settings | Parameter | Reference | Description | Min | Typ | Max | Units |
|------------------------|--|--------------------|-----------|-----------------|-----------------|-------------------------|-------------------------|-------|
| 0b110 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | 2 × Bandgap | 2.510 | 2.595 | 2.655 | V |
| | | V _{AGND} | AGND | Bandgap | 1.276 | 1.301 | 1.332 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.006 | V _{SS} + 0.031 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | 2 × Bandgap | 2.513 | 2.594 | 2.656 | V |
| | | V _{AGND} | AGND | Bandgap | 1.275 | 1.301 | 1.331 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.021 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | 2 × Bandgap | 2.516 | 2.595 | 2.657 | V |
| | | V _{AGND} | AGND | Bandgap | 1.275 | 1.301 | 1.331 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.003 | V _{SS} + 0.017 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | 2 × Bandgap | 2.520 | 2.595 | 2.658 | V |
| | | V _{AGND} | AGND | Bandgap | 1.275 | 1.300 | 1.331 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.002 | V _{SS} + 0.015 | V |
| 0b111 | All power settings. Not allowed for 3.3 V. | – | – | – | – | – | – | – |

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. DC Analog PSoC Block Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|-----------------|---|-----|------|-----|-------|-------|
| R _{CT} | Resistor unit value (continuous time) | – | 12.2 | – | kΩ | |
| C _{SC} | Capacitor unit value (switched capacitor) | – | 80 | – | fF | |

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V or 3.3 V at 25 °C and are for design guidance only.

Note: The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the [PSoC Technical Reference Manual](#) for more information on the VLT_CR register.

Table 22. DC POR and LVD Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|------------------------------------|--|------|------|----------------------|-------|-------|
| V _{PPOR0R} | V _{DD} value for PPOR trip (positive ramp) PORLEV[1:0] = 00b | | 2.91 | | V | |
| V _{PPOR1R} | PORLEV[1:0] = 01b | – | 4.39 | – | V | |
| V _{PPOR2R} | PORLEV[1:0] = 10b | | 4.55 | | V | |
| V _{PPOR0} ^[23] | V _{DD} value for PPOR trip (negative ramp) PORLEV[1:0] = 00b | | 2.82 | | V | |
| V _{PPOR1} ^[23] | PORLEV[1:0] = 01b | – | 4.39 | – | V | |
| V _{PPOR2} ^[23] | PORLEV[1:0] = 10b | | 4.55 | | V | |
| V _{PH0} | PPOR hysteresis PORLEV[1:0] = 00b | – | 92 | – | mV | |
| V _{PH1} | PORLEV[1:0] = 01b | – | 0 | – | mV | |
| V _{PH2} | PORLEV[1:0] = 10b | – | 0 | – | mV | |
| V _{LVD0} | V _{DD} value for LVD trip VM[2:0] = 000b | 2.86 | 2.92 | 2.98 ^[24] | V | |
| V _{LVD1} | VM[2:0] = 001b | 2.96 | 3.02 | 3.08 | V | |
| V _{LVD2} | VM[2:0] = 010b | 3.07 | 3.13 | 3.20 | V | |
| V _{LVD3} | VM[2:0] = 011b | 3.92 | 4.00 | 4.08 | V | |
| V _{LVD4} | VM[2:0] = 100b | 4.39 | 4.48 | 4.57 | V | |
| V _{LVD5} | VM[2:0] = 101b | 4.55 | 4.64 | 4.74 ^[25] | V | |
| V _{LVD6} | VM[2:0] = 110b | 4.63 | 4.73 | 4.82 | V | |
| V _{LVD7} | VM[2:0] = 111b | 4.72 | 4.81 | 4.91 | V | |

Notes

23. **Errata:** When V_{DD} of the device is pulled below ground just before power on, the first read from each 8K Flash page may be corrupted. This issue does not affect Flash page 0 because it is the selected page upon reset. More details in “Errata” on page 64.

24. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.

25. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 23. DC Programming Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|-----------------------|---|-----------------------|-----|------------------------|-------|--|
| V _{DDP} | V _{DD} for programming and erase | 4.5 | 5 | 5.5 | V | This specification applies to the functional requirements of external programmer tools |
| V _{DDL} | Low V _{DD} for verify | 3 | 3.1 | 3.2 | V | This specification applies to the functional requirements of external programmer tools |
| V _{DDHV} | High V _{DD} for verify | 5.1 | 5.2 | 5.3 | V | This specification applies to the functional requirements of external programmer tools |
| V _{DDWRITE} | Supply voltage for flash write operation | 3 | | 5.25 | V | This specification applies to this device when it is executing internal flash writes |
| I _{DDP} | Supply current during programming or verify | – | 15 | 30 | mA | |
| V _{ILP} | Input low voltage during programming or verify | – | – | 0.8 | V | |
| V _{IHP} | Input high voltage during programming or verify | 2.1 | – | – | V | |
| I _{ILP} | Input current when applying V _{ILP} to P1[0] or P1[1] during programming or verify | – | – | 0.2 | mA | Driving internal pull-down resistor. |
| I _{IHP} | Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify | – | – | 1.5 | mA | Driving internal pull-down resistor. |
| V _{OLV} | Output low voltage during programming or verify | – | – | V _{SS} + 0.75 | V | |
| V _{OHV} | Output high voltage during programming or verify | V _{DD} – 1.0 | – | V _{DD} | V | |
| Flash _{ENPB} | Flash endurance (per block) ^[26] | 50,000 | – | – | – | Erase/write cycles per block. |
| Flash _{ENT} | Flash endurance (total) ^[27] | 1,800,000 | – | – | – | Erase/write cycles. |
| Flash _{DR} | Flash data retention | 10 | – | – | Years | |

DC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 24. DC I²C Specifications ^[28]

| Parameter | Description | Min | Typ | Max | Units | Notes |
|--------------------|------------------|-----------------------|-----|------------------------|-------|-----------------------------------|
| V _{ILI2C} | Input low level | – | – | 0.3 × V _{DD} | V | 3.0 V ≤ V _{DD} ≤ 3.6 V |
| | | – | – | 0.25 × V _{DD} | V | 4.75 V ≤ V _{DD} ≤ 5.25 V |
| V _{IHI2C} | Input high level | 0.7 × V _{DD} | – | – | V | 3.0 V ≤ V _{DD} ≤ 5.25 V |

Notes

26. The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.

27. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and ensure that no single block ever sees more than 50,000 cycles).

For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing.

See the Flash APIs application note [Design Aids – Reading and Writing PSOC® Flash – AN2015](#) for more information.

28. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I²C GPIO pins also meet the mentioned specifications.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. AC Chip Level Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|--------------------------------------|---|-------|------|--------------------------|-------|---|
| F _{IMO245V} | Internal main oscillator frequency for 24 MHz (5 V) | 23.04 | 24 | 24.96 ^[29] | MHz | Trimmed for 5 V operation using factory trim values. |
| F _{IMO243V} | Internal main oscillator frequency for 24 MHz (3.3 V) | 22.08 | 24 | 25.92 ^[30] | MHz | Trimmed for 3.3 V operation using factory trim values. |
| F _{IMOUSB5V} | Internal main oscillator frequency with USB (5 V) Frequency locking enabled and USB traffic present. | 23.94 | 24 | 24.06 | MHz | $-10\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ $4.35 \leq V_{DD} \leq 5.15$ |
| F _{IMOUSB3V} | Internal main oscillator frequency with USB (3.3 V) Frequency locking enabled and USB traffic present. | 23.94 | 24 | 24.06 | MHz | $-0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$ $3.15 \leq V_{DD} \leq 3.45$ |
| F _{CPU1} | CPU frequency (5 V nominal) | 0.093 | 24 | 24.96 ^[29] | MHz | SLIMO Mode = 0. |
| F _{CPU2} | CPU frequency (3.3 V nominal) | 0.086 | 12 | 12.96 ^[30] | MHz | SLIMO Mode = 0. |
| F _{BLK5} | Digital PSoC block frequency (5 V nominal) | 0 | 48 | 49.92 ^[29,31] | MHz | Refer to the AC digital block Specifications. |
| F _{BLK3} | Digital PSoC block frequency (3.3 V nominal) | 0 | 24 | 25.92 ^[31] | MHz | |
| F _{32K1} | Internal low speed oscillator frequency | 15 | 32 | 64 | kHz | |
| F _{32K_U} | Internal low speed oscillator untrimmed frequency | 5 | – | 100 | kHz | After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing |
| t _{XRST} | External reset pulse width | 10 | – | – | μs | |
| DC _{24M} | 24 MHz duty cycle | 40 | 50 | 60 | % | |
| DC _{ILO} | Internal low speed oscillator duty cycle | 20 | 50 | 80 | % | |
| Step _{24M} | 24 MHz trim step size | – | 50 | – | kHz | |
| F _{out48M} | 48 MHz output frequency | 46.08 | 48.0 | 49.92 ^[29,30] | MHz | Trimmed. Utilizing factory trim values. |
| F _{MAX} | Maximum frequency of signal on row input or row output. | – | – | 12.96 | MHz | |
| SR _{POWER_UP} | Power supply slew rate | – | – | 250 | V/ms | V _{DD} slew rate during power-up. |
| t _{POWERUP} | Time from end of POR to CPU executing code | – | 16 | 100 | ms | Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual . |
| t _{jit_IMO} ^[32] | 24 MHz IMO cycle-to-cycle jitter (RMS) | – | 200 | 1200 | ps | |
| | 24 MHz IMO long term N cycle-to-cycle jitter (RMS) | – | 900 | 6000 | ps | N = 32 |
| | 24 MHz IMO period jitter (RMS) | – | 200 | 900 | ps | |

Notes

29. 4.75 V < V_{DD} < 5.25 V.

30. 3.0 V < V_{DD} < 3.6 V. See application note [Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012](#) for information on trimming for operation at 3.3 V.

31. See the individual user module datasheets for information on maximum frequencies for user modules.

32. Refer to Cypress Jitter Specifications application note, [Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054](#) for more information.

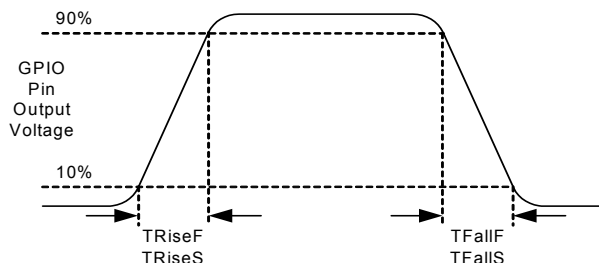
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. AC GPIO Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|--------------------|---|-----|-----|-----|-------|--|
| F_{GPIO} | GPIO operating frequency | 0 | – | 12 | MHz | Normal strong mode |
| t_{RiseF} | Rise time, normal strong mode, $C_{\text{load}} = 50\text{ pF}$ | 3 | – | 18 | ns | $V_{\text{DD}} = 4.5\text{ to }5.25\text{ V}$, 10% to 90% |
| t_{FallF} | Fall time, normal strong mode, $C_{\text{load}} = 50\text{ pF}$ | 2 | – | 18 | ns | $V_{\text{DD}} = 4.5\text{ to }5.25\text{ V}$, 10% to 90% |
| t_{RiseS} | Rise time, slow strong mode, $C_{\text{load}} = 50\text{ pF}$ | 10 | 27 | – | ns | $V_{\text{DD}} = 3\text{ to }5.25\text{ V}$, 10% to 90% |
| t_{FallS} | Fall time, slow strong mode, $C_{\text{load}} = 50\text{ pF}$ | 10 | 22 | – | ns | $V_{\text{DD}} = 3\text{ to }5.25\text{ V}$, 10% to 90% |

Figure 12. GPIO Timing Diagram



AC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-10\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-10\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 27. AC Full Speed (12 Mbps) USB Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|----------------------|--|------------|-----|------------|-------|----------------|
| t_{RFS} | Transition rise time | 4 | – | 20 | ns | For 50 pF load |
| t_{FSS} | Transition fall time | 4 | – | 20 | ns | For 50 pF load |
| t_{RFMS} | Rise/fall time matching: (t_R/t_F) | 90 | – | 111 | % | For 50 pF load |
| t_{DRATEFS} | Full speed data rate | 12 – 0.25% | 12 | 12 + 0.25% | Mbps | |

AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog continuous time PSoC block.

Power = high and Opamp bias = high is not supported at 3.3 V.

Table 28. 5-V AC Operational Amplifier Specifications

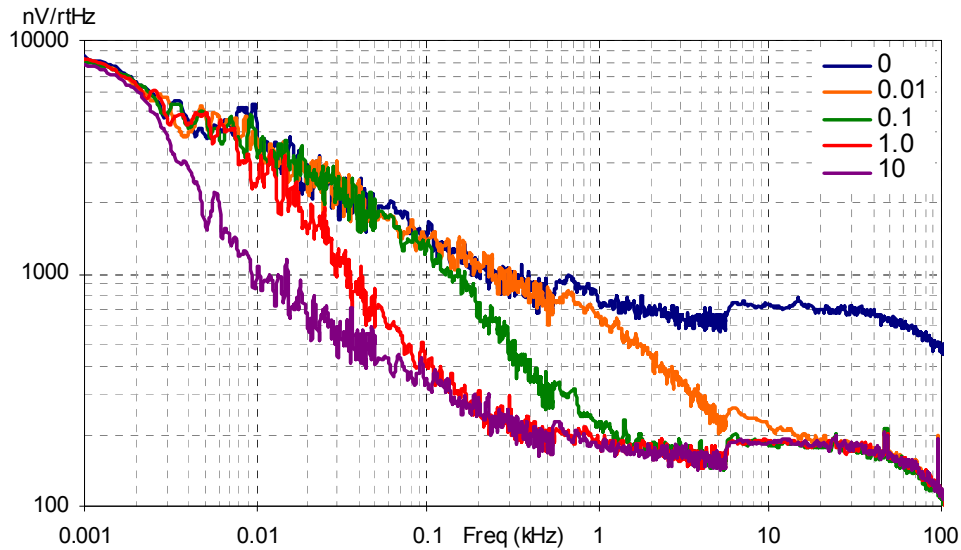
| Parameter | Description | Min | Typ | Max | Units |
|------------|---|------|-----|------|------------------|
| t_{ROA} | Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) | | | | |
| | Power = low, Opamp bias = low | – | – | 3.9 | μs |
| | Power = medium, Opamp bias = high | – | – | 0.72 | μs |
| t_{SOA} | Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) | | | | |
| | Power = low, Opamp bias = low | – | – | 5.9 | μs |
| | Power = medium, Opamp bias = high | – | – | 0.92 | μs |
| SR_{ROA} | Rising slew rate (20% to 80%)(10 pF load, unity gain) | | | | |
| | Power = low, Opamp bias = low | 0.15 | – | – | V/ μs |
| | Power = medium, Opamp bias = high | 1.7 | – | – | V/ μs |
| SR_{FOA} | Falling slew rate (20% to 80%)(10 pF load, unity gain) | | | | |
| | Power = low, Opamp bias = low | 0.01 | – | – | V/ μs |
| | Power = medium, Opamp bias = high | 0.5 | – | – | V/ μs |
| BW_{OA} | Gain bandwidth product | | | | |
| | Power = low, Opamp bias = low | 0.75 | – | – | MHz |
| | Power = medium, Opamp bias = high | 3.1 | – | – | MHz |
| E_{NOA} | Noise at 1 kHz (Power = medium, Opamp bias = high) | | 100 | – | nV/rt-Hz |

Table 29. 3.3-V AC Operational Amplifier Specifications

| Parameter | Description | Min | Typ | Max | Units |
|------------|---|------|-----|------|------------------|
| t_{ROA} | Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) | | | | |
| | Power = low, Opamp bias = low | – | – | 3.92 | μs |
| t_{SOA} | Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) | | | | |
| | Power = low, Opamp bias = low | – | – | 5.41 | μs |
| SR_{ROA} | Rising slew rate (20% to 80%)(10 pF load, unity gain) | | | | |
| | Power = low, Opamp bias = low | 0.31 | – | – | V/ μs |
| SR_{FOA} | Falling slew rate (20% to 80%)(10 pF load, Unity Gain) | | | | |
| | Power = low, Opamp bias = low | 0.24 | – | – | V/ μs |
| BW_{OA} | Gain bandwidth product | | | | |
| | Power = low, Opamp bias = low | 0.67 | – | – | MHz |
| E_{NOA} | Noise at 1 kHz (Power = medium, Opamp bias = high) | | 100 | – | nV/rt-Hz |

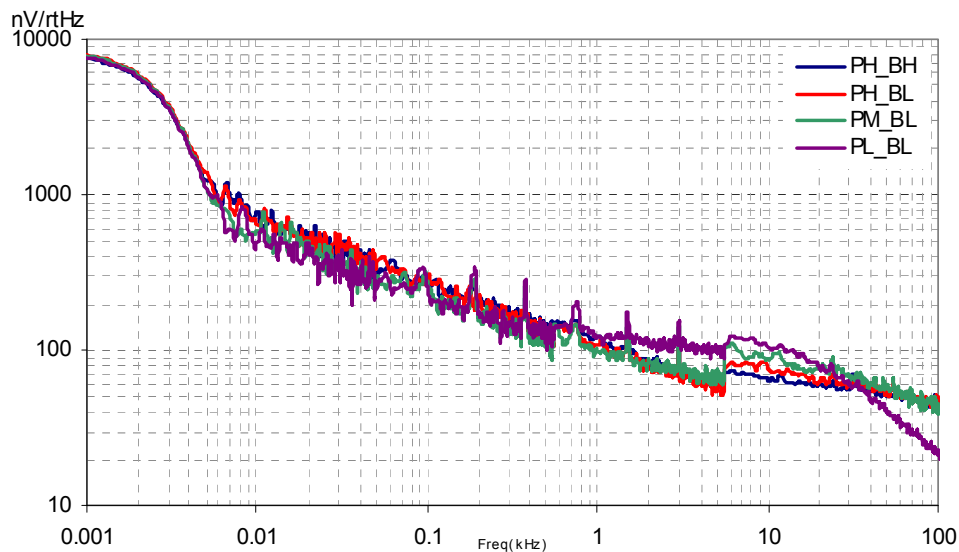
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1 K resistance and the external capacitor.

Figure 13. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to $1/f$, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 14. Typical Opamp Noise



AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 30. AC Low Power Comparator Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|------------|-------------------|-----|-----|-----|---------------|--|
| t_{RLPC} | LPC response time | – | – | 50 | μs | $\geq 50\text{ mV}$ overdrive comparator reference set within V_{REFLPC} . |

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 31. AC Digital Block Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|-------------------|--|--------------------|-----|-------|------|---|
| All functions | Block input clock frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.92 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 25.92 | MHz | |
| Timer | Input clock frequency | | | | | |
| | No capture, $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.92 | MHz | |
| | No capture, $V_{DD} < 4.75\text{ V}$ | – | – | 25.92 | MHz | |
| | With capture | – | – | 25.92 | MHz | |
| | Capture pulse width | 50 ^[33] | – | – | ns | |
| Counter | Input clock frequency | | | | | |
| | No enable input, $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.92 | MHz | |
| | No enable input, $V_{DD} < 4.75\text{ V}$ | – | – | 25.92 | MHz | |
| | With enable input | – | – | 25.92 | MHz | |
| | Enable input pulse width | 50 ^[33] | – | – | ns | |
| | Kill pulse width | | | | | |
| | Asynchronous restart mode | 20 | – | – | ns | |
| | Synchronous restart mode | 50 ^[33] | – | – | ns | |
| | Disable mode | 50 ^[33] | – | – | ns | |
| | Input clock frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.92 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 25.92 | MHz | |
| CRCPRS (PRS Mode) | Input clock frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.92 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 25.92 | MHz | |
| CRCPRS (CRC Mode) | Input clock frequency | – | – | 24.6 | MHz | |
| SPIM | Input clock frequency | – | – | 8.2 | MHz | The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2. |
| SPIS | Input clock (SCLK) frequency | – | – | 4.1 | MHz | The input clock is the SPI SCLK in SPIS mode. |
| | Width of SS_negated between transmissions | 50 ^[33] | – | – | ns | |

Note

³³. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 31. AC Digital Block Specifications (continued)

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|-------------|-----------------------------------|-----|-----|-------|------|---|
| Transmitter | Input clock frequency | | | | | The baud rate is equal to the input clock frequency divided by 8. |
| | $V_{DD} \geq 4.75$ V, 2 stop bits | – | – | 49.92 | MHz | |
| | $V_{DD} \geq 4.75$ V, 1 stop bit | – | – | 24.6 | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 24.6 | MHz | |
| Receiver | Input clock frequency | | | | | The baud rate is equal to the input clock frequency divided by 8. |
| | $V_{DD} \geq 4.75$ V, 2 stop bits | – | – | 49.92 | MHz | |
| | $V_{DD} \geq 4.75$ V, 1 stop bit | – | – | 24.6 | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 24.6 | MHz | |

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 32. AC External Clock Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|--------------|--------------------------------|-------|-----|-------|---------------|-------|
| F_{OSCEXT} | Frequency for USB applications | 23.94 | 24 | 24.06 | MHz | |
| – | Duty cycle | 47 | 50 | 53 | % | |
| – | Power-up to IMO switch | 150 | – | – | μs | |

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 33. 5-V AC Analog Output Buffer Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|--------------------|--|--------------|--------|------------|--------------|-------|
| t _{ROB} | Rising settling time to 0.1%, 1 V Step, 100 pF load | – | – | 2.5 | μs | |
| | Power = low Power = high | – – | – – | 2.5 2.5 | μs μs | |
| t _{SOB} | Falling settling time to 0.1%, 1 V Step, 100 pF load | – | – | 2.2 | μs | |
| | Power = low Power = high | – – | – – | 2.2 2.2 | μs μs | |
| SR _{ROB} | Rising slew rate (20% to 80%), 1 V Step, 100 pF load | 0.65 | – | – | V/μs | |
| | Power = low Power = high | 0.65 0.65 | – – | – – | V/μs V/μs | |
| SR _{FOB} | Falling slew rate (80% to 20%), 1 V Step, 100 pF load | 0.65 | – | – | V/μs | |
| | Power = low Power = high | 0.65 0.65 | – – | – – | V/μs V/μs | |
| BW _{OBSS} | Small signal bandwidth, 20 mV _{pp} , 3 dB BW, 100 pF load | 0.8 | – | – | MHz | |
| | Power = low Power = high | 0.8 0.8 | – – | – – | MHz MHz | |
| BW _{OBLs} | Large signal bandwidth, 1 V _{pp} , 3 dB BW, 100 pF load | 300 | – | – | kHz | |
| | Power = low Power = high | 300 300 | – – | – – | kHz kHz | |

Table 34. 3.3-V AC Analog Output Buffer Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|--------------------|---|------------|--------|------------|--------------|-------|
| t _{ROB} | Rising settling time to 0.1%, 1 V Step, 100 pF load | – | – | 3.8 | μs | |
| | Power = low Power = high | – – | – – | 3.8 3.8 | μs μs | |
| t _{SOB} | Falling settling time to 0.1%, 1 V Step, 100 pF load | – | – | 2.6 | μs | |
| | Power = low Power = high | – – | – – | 2.6 2.6 | μs μs | |
| SR _{ROB} | Rising slew rate (20% to 80%), 1 V Step, 100 pF load | 0.5 | – | – | V/μs | |
| | Power = low Power = high | 0.5 0.5 | – – | – – | V/μs V/μs | |
| SR _{FOB} | Falling slew rate (80% to 20%), 1 V Step, 100 pF load | 0.5 | – | – | V/μs | |
| | Power = low Power = high | 0.5 0.5 | – – | – – | V/μs V/μs | |
| BW _{OBSS} | Small signal bandwidth, 20 mV _{pp} , 3dB BW, 100 pF load | 0.7 | – | – | MHz | |
| | Power = low Power = high | 0.7 0.7 | – – | – – | MHz MHz | |
| BW _{OBLs} | Large signal bandwidth, 1 V _{pp} , 3dB BW, 100 pF load | 200 | – | – | kHz | |
| | Power = low Power = high | 200 200 | – – | – – | kHz kHz | |

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 35. AC Programming Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|---------------------|--|-----|-----|---------------------|-------|---|
| t_{RSCLK} | Rise time of SCLK | 1 | – | 20 | ns | |
| t_{FSCLK} | Fall time of SCLK | 1 | – | 20 | ns | |
| t_{SSCLK} | Data setup time to falling edge of SCLK | 40 | – | – | ns | |
| t_{HSCLK} | Data hold time from falling edge of SCLK | 40 | – | – | ns | |
| F_{SCLK} | Frequency of SCLK | 0 | – | 8 | MHz | |
| t_{ERASEB} | Flash erase time (block) | – | 10 | – | ms | |
| t_{WRITE} | Flash block write time | – | 40 | – | ms | |
| t_{DSCLK} | Data out delay from falling edge of SCLK | – | – | 45 | ns | $V_{DD} > 3.6$ |
| t_{DSCLK3} | Data out delay from falling edge of SCLK | – | – | 50 | ns | $3.0 \leq V_{DD} \leq 3.6$ |
| $t_{ERASEALL}$ | Flash erase time (bulk) | – | 40 | – | ms | Erase all blocks and protection fields at once |
| $t_{PROGRAM_HOT}$ | Flash block erase + flash block write time | – | – | 100 ^[34] | ms | $0\text{ }^{\circ}\text{C} \leq T_j \leq 100\text{ }^{\circ}\text{C}$ |
| $t_{PROGRAM_COLD}$ | Flash block erase + flash block write time | – | – | 200 ^[34] | ms | $-40\text{ }^{\circ}\text{C} \leq T_j \leq 0\text{ }^{\circ}\text{C}$ |

Note

34. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. See the Flash APIs application note [Design Aids – Reading and Writing PSoC® Flash – AN2015](#) for more information.

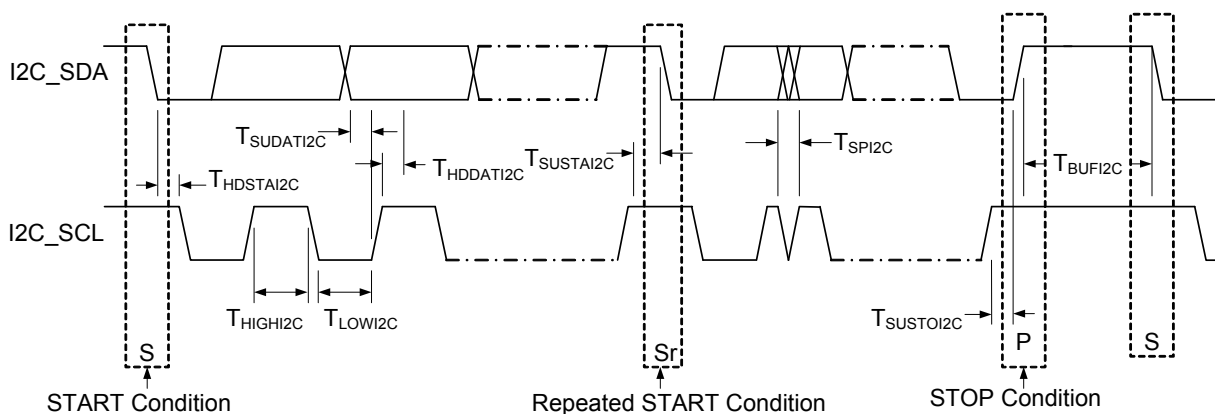
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 36. AC Characteristics of the I²C SDA and SCL Pins for V_{DD}

| Parameter | Description | Standard Mode | | Fast Mode | | Units | Notes |
|-----------------------|---|---------------|-----|---------------------|-----|-------|-------|
| | | Min | Max | Min | Max | | |
| F _{SCL I2C} | SCL clock frequency | 0 | 100 | 0 | 400 | kHz | |
| t _{HDSTAI2C} | Hold time (repeated) start condition. After this period, the first clock pulse is generated | 4.0 | – | 0.6 | – | μs | |
| t _{LOWI2C} | Low period of the SCL clock | 4.7 | – | 1.3 | – | μs | |
| t _{HIGHI2C} | High period of the SCL clock | 4.0 | – | 0.6 | – | μs | |
| t _{SUSTAI2C} | Setup time for a repeated start condition | 4.7 | – | 0.6 | – | μs | |
| t _{HDDATI2C} | Data hold time | 0 | – | 0 | – | μs | |
| t _{SUDATI2C} | Data setup time | 250 | – | 100 ^[35] | – | ns | |
| t _{SUSTOI2C} | Setup time for stop condition | 4.0 | – | 0.6 | – | μs | |
| t _{BUFI2C} | Bus free time between a stop and start condition | 4.7 | – | 1.3 | – | μs | |
| t _{SPI2C} | Pulse width of spikes suppressed by the input filter | – | – | 0 | 50 | ns | |

Figure 15. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

35. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU, DAT} \geq 250\text{ ns}$ it must meet. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If the device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU, DAT} = 1000 + 250 = 1250\text{ ns}$ (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Thermal Impedance

Table 37. Thermal Impedances per Package

| Package | Typical θ_{JA} ^[36] |
|----------------------------|---------------------------------------|
| 56-Pin QFN ^[37] | 12.93 °C/W |
| 68-Pin QFN ^[37] | 13.05 °C/W |
| 100-Ball VFBGA | 65 °C/W |
| 100-Pin TQFP | 51 °C/W |

Solder Reflow Peak Specifications

Table 38 shows the solder reflow temperature limits that must not be exceeded.

Table 38. Solder Reflow Specifications

| Package | Maximum Peak Temperature (T_C) | Maximum Time above $T_C - 5$ °C |
|----------------|------------------------------------|---------------------------------|
| 56-Pin QFN | 260 °C | 30 seconds |
| 68-Pin QFN | 260 °C | 30 seconds |
| 100-Ball VFBGA | 260 °C | 30 seconds |
| 100-Pin TQFP | 260 °C | 30 seconds |

Notes

36. $T_J = T_A + \text{POWER} \times \theta_{JA}$.

37. To achieve the thermal impedance specified for the QFN package, see the *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at <http://www.amkor.com>.

Development Tool Selection

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at <http://www.cypress.com> and includes a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube in-circuit emulator and PSoC MiniProg. PSoC programmer is available free of charge at <http://www.cypress.com>.

Development Kits

All development kits can be purchased from the [Cypress Online Store](#).

CY3215-DK Basic Development Kit

The **CY3215-DK** is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation, and the software interface enables you to run, halt, and single step the processor, and view the content of specific memory locations. Advance emulation features are also supported through PSoC Designer. The kit includes:

- PSoC Designer software CD
- ICE-Cube in-circuit Emulator
- ICE Flex-Pod for CY8C29x66 family
- Cat-5 adapter
- MiniEval programming board
- 110 ~ 240 V power supply, Euro-Plug adapter
- iMAGEcraft C compiler (registration required)
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466-24PXI 28-PDIP chip samples

Evaluation Tools

All evaluation tools can be purchased from the [Cypress Online Store](#).

CY3210-MiniProg1

The **CY3210-MiniProg1** kit enables you to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-Pin CY8C29466-24PXI PDIP PSoC device sample
- 28-Pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-PSoCEval1

The **CY3210-PSoCEval1** kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- 28-Pin CY8C29466-24PXI PDIP PSoC device sample (2)
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3214-PSoCEvalUSB

The **CY3214-PSoCEvalUSB** evaluation kit features a development board for the CY8C24794-24LTXI PSoC device. The board supports both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB board
- LCD module
- MiniProg programming unit
- Mini USB cable
- PSoC Designer and Example Projects CD
- Getting Started guide
- Wire pack

Device Programmers

All device programmers can be purchased from the [Cypress Online Store](#).

CY3216 Modular Programmer

The [CY3216 Modular Programmer kit](#) features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular programmer base
- Three programming module cards
- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 39. Emulation and Programming Accessories

| Part # | Pin Package | Flex-Pod Kit ^[38] | Foot Kit ^[39] | Adapter ^[40] |
|------------------|-------------|------------------------------|--------------------------|--|
| CY8C24794-24LQXI | 56-pin QFN | CY3250-24X94QFN | None | Adapters can be found at http://www.emulation.com . |

CY3207ISSP In-System Serial Programmer (ISSP)

The [CY3207ISSP](#) is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

Notes

38. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.

39. Foot kit includes surface mount feet that are soldered to the target PCB.

40. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters are found at <http://www.emulation.com>.

Ordering Information

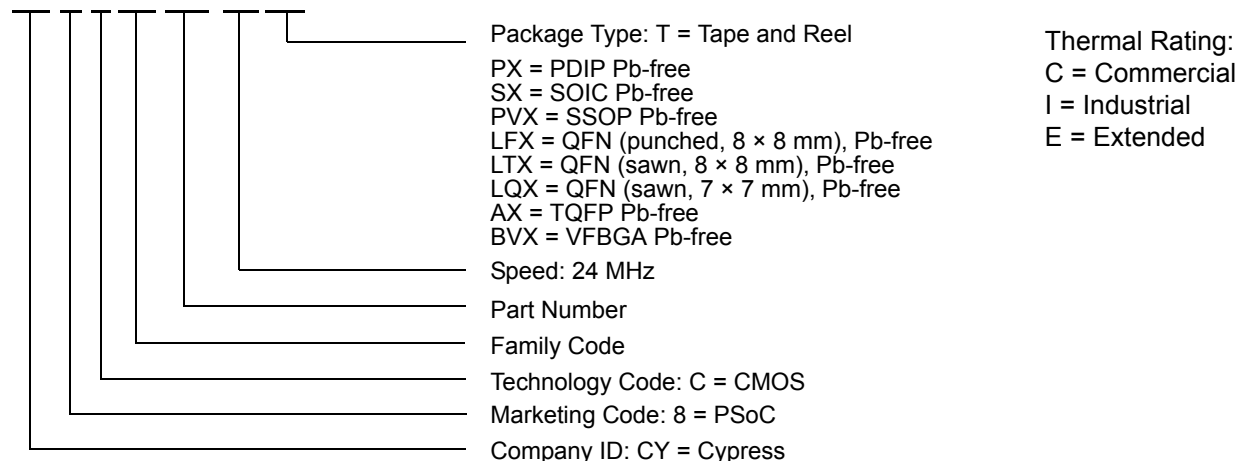
Table 40. CY8C24x94 PSoC Device's Key Features and Ordering Information

| Package | Package diagram | Ordering Code | Flash (Bytes) | SRAM (Bytes) | Temperature Range | Digital Blocks | Analog Blocks | Digital I/O Pins | Analog Inputs | Analog Outputs | XRES Pin |
|--|-----------------|-------------------|---------------|--------------|-------------------|----------------|---------------|------------------|---------------|----------------|----------|
| 100-pin OCD TQFP ^[41] | 51-85048 | CY8C24094-24AXI | 16 K | 1 K | -40 °C to +85 °C | 4 | 6 | 56 | 48 | 2 | Yes |
| 56-pin (7 × 7 mm) QFN | 001-58740 | CY8C24794-24LQXI | 16 K | 1 K | -40 °C to +85 °C | 4 | 6 | 50 | 48 | 2 | No |
| 56-pin (7 × 7 mm) QFN (Tape and Reel) | | CY8C24794-24LQXIT | 16 K | 1 K | -40 °C to +85 °C | 4 | 6 | 50 | 48 | 2 | No |
| 56-pin (8 × 8 mm) QFN (Sawn) | 001-53450 | CY8C24794-24LTXI | 16 K | 1 K | -40 °C to +85 °C | 4 | 6 | 50 | 48 | 2 | No |
| 56-pin (8 × 8 mm) QFN (Sawn) (Tape and Reel) | | CY8C24794-24LTXIT | 16 K | 1 K | -40 °C to +85 °C | 4 | 6 | 50 | 48 | 2 | No |
| 56-pin (8 × 8 mm) QFN (Sawn) | 001-53450 | CY8C24894-24LTXI | 16 K | 1 K | -40 °C to +85 °C | 4 | 6 | 49 | 47 | 2 | Yes |
| 56-pin (8 × 8 mm) QFN (Sawn) (Tape and Reel) | | CY8C24894-24LTXIT | 16 K | 1 K | -40 °C to +85 °C | 4 | 6 | 49 | 47 | 2 | Yes |
| 68-pin (8 × 8 mm) QFN (Sawn) | 001-09618 | CY8C24994-24LTXI | 16 K | 1 K | -40 °C to +85 °C | 4 | 6 | 56 | 48 | 2 | Yes |
| 68-pin QFN (8 × 8 mm) (Sawn) (Tape and Reel) | | CY8C24994-24LTXIT | 16 K | 1 K | -40 °C to +85 °C | 4 | 6 | 56 | 48 | 2 | Yes |

Note: For die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions

CY 8 C 24 XXX SP XXT



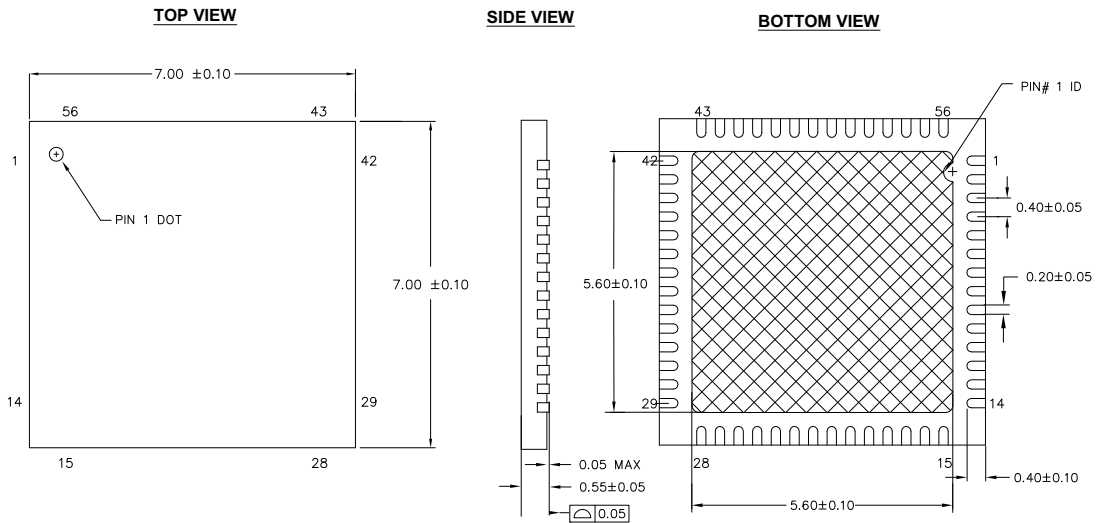
Note
 41. This part may be used for in-circuit debugging. It is NOT available for production.

Packaging Dimensions


This section illustrates the package specification for the CY8C24x94 PSoC devices, along with the thermal impedance for the package and solder reflow peak temperatures.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod dimension drawings at <http://www.cypress.com/design/MR10161>.

Figure 16. 56-pin QFN (7 × 7 × 0.6 mm) LR56A/LQ56A 5.6 × 5.6 E-Pad (Sawn) Package Outline, 001-58740

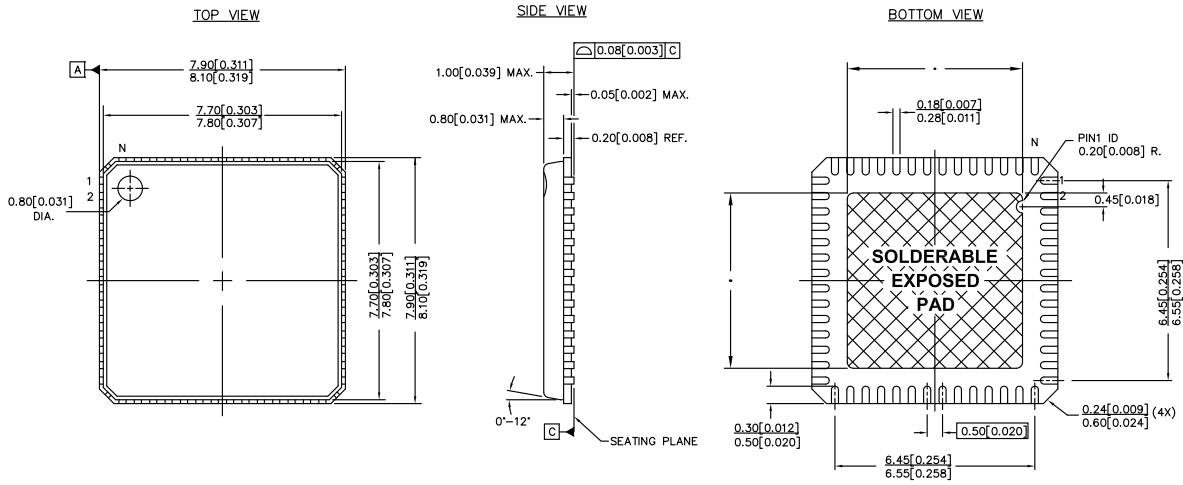


NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-58740 °C

Figure 17. 56-pin QFN (8 × 8 × 1.0 mm) LF56A/LY56A 4.5 × 5.2 E-Pad (Subcon Punch Type Pkg.) Package Outline, 001-12921



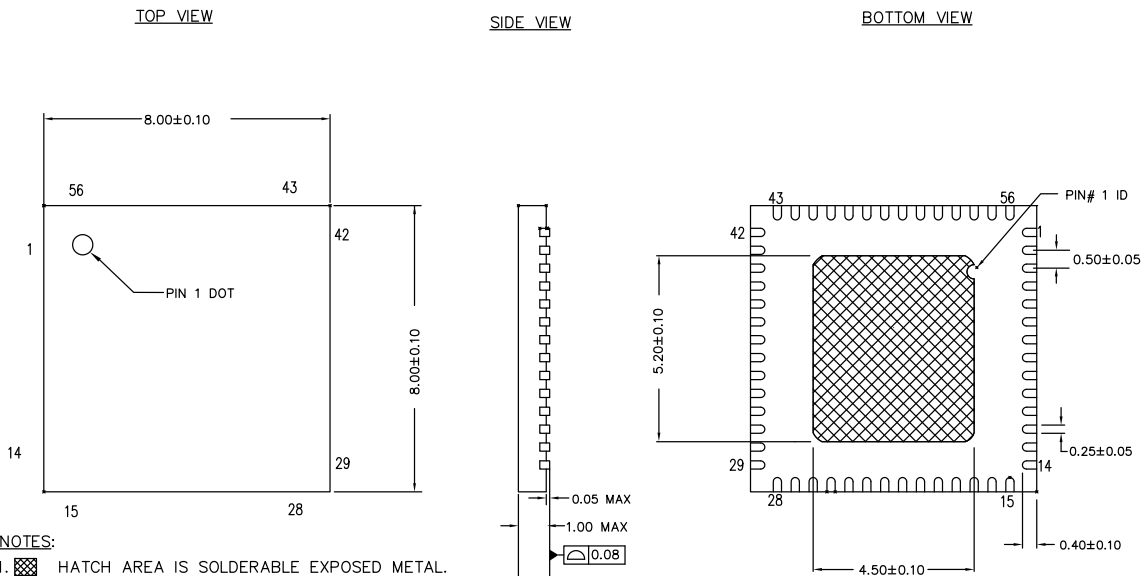
NOTES:

1. [HATCH] HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.162g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

| PART # | DESCRIPTION |
|--------|-------------|
| LF56A | STANDARD |
| LY56A | PB-FREE |

001-12921 *C

Figure 18. 56-pin QFN (8 × 8 × 1.0 mm) LT56B 4.5 × 5.2 E-Pad (Sawn) Package Outline, 001-53450

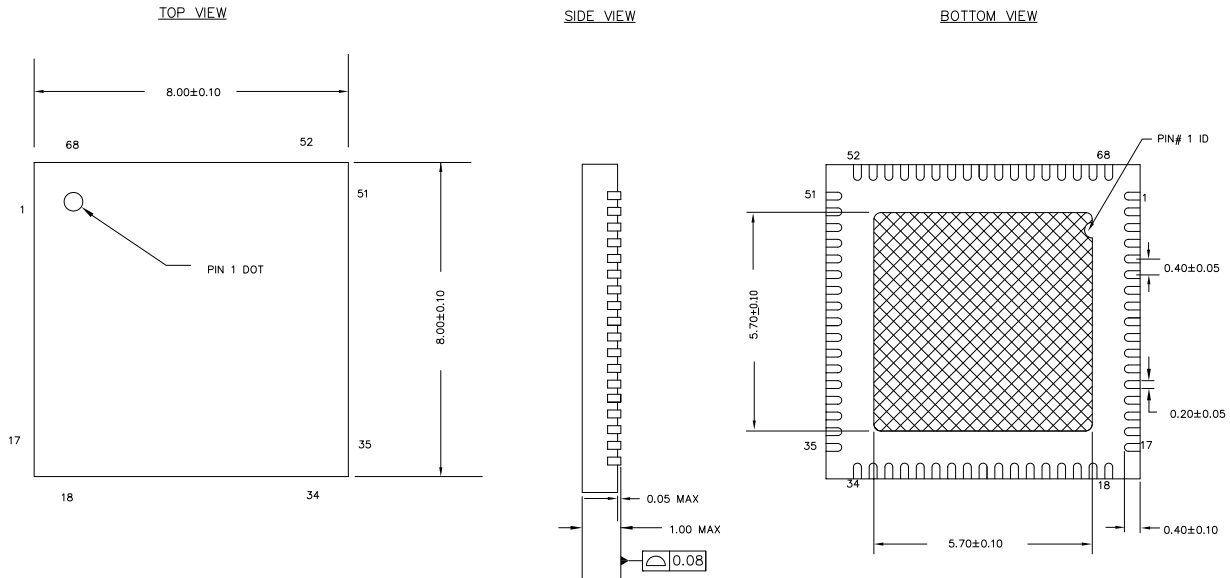


NOTES:


1. [HATCH] HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 162 ± 16 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-53450 *D

Figure 19. 68-pin QFN (8 × 8 × 1.0 mm) LT68 5.7 × 5.7 E-Pad (Sawn Type) Package Outline, 001-09618

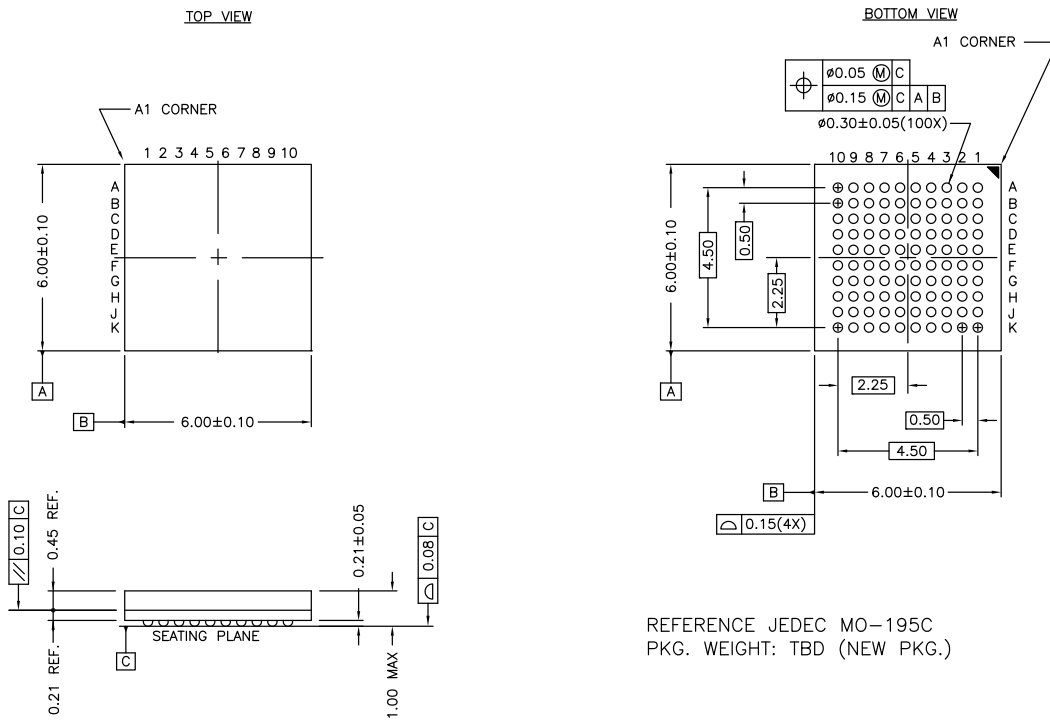


NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

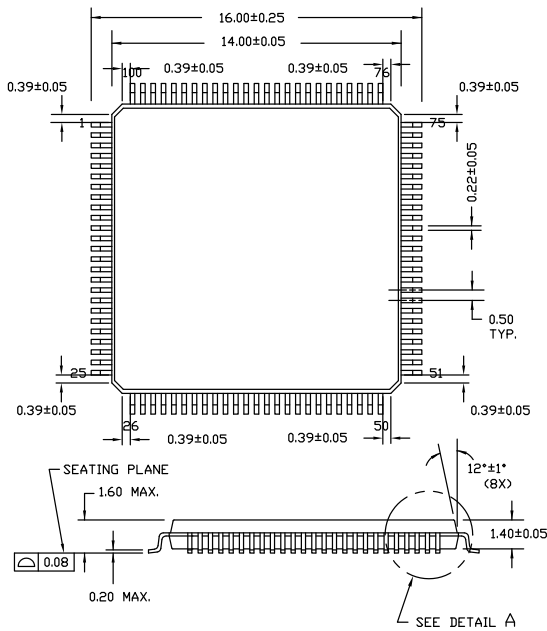
001-09618 *E

Figure 20. 100-ball VFBGA (6 × 6 × 1.0 mm) BZ100 Package Outline, 51-85209



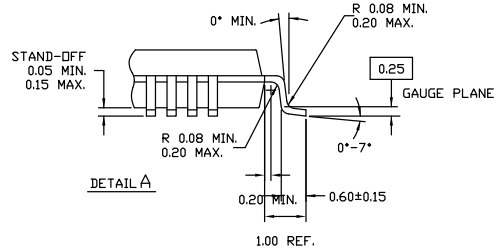
51-85209 *F

Figure 21. 100-pin TQFP (14 × 14 × 1.4 mm) A100SA Package Outline, 51-85048

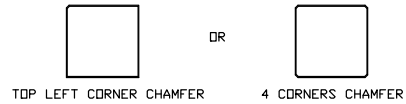


NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS



NOTE: PKG. CAN HAVE



51-85048 *J

Important Note

- For information on the preferred dimensions for mounting QFN packages, see the Application Note, *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at <http://www.amkor.com>.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Acronyms

Acronyms Used

The following table lists the acronyms that are used in this document.

| Acronym | Description | Acronym | Description |
|---------|---|---------|---|
| AC | alternating current | MIPS | million instructions per second |
| ADC | analog-to-digital converter | OCD | on-chip debug |
| API | application programming interface | PCB | printed circuit board |
| CMOS | complementary metal oxide semiconductor | PDIP | plastic dual-in-line package |
| CPU | central processing unit | PGA | programmable gain amplifier |
| CRC | cyclic redundancy check | POR | power-on reset |
| CT | continuous time | PPOR | precision power-on reset |
| DAC | digital-to-analog converter | PRS | pseudo-random sequence |
| DC | direct current | PSoC® | Programmable System-on-Chip™ |
| DTMF | dual-tone multi-frequency | PWM | pulse-width modulator |
| EEPROM | electrically erasable programmable read-only memory | QFN | quad flat no leads |
| GPIO | general purpose I/O | SAR | successive approximation register |
| ICE | in-circuit emulator | SC | switched capacitor |
| IDE | integrated development environment | SLIMO | slow IMO |
| ILO | internal low-speed oscillator | SOIC | small-outline integrated circuit |
| IMO | internal main oscillator | SPI™ | serial peripheral interface |
| I/O | input/output | SRAM | static random-access memory |
| IrDA | infrared data association | SROM | supervisory read-only memory |
| ISSP | In-System Serial Programming | TQFP | thin quad flat pack |
| LCD | liquid crystal display | UART | universal asynchronous receiver / transmitter |
| LED | light-emitting diode | USB | universal serial bus |
| LPC | low power comparator | VFBGA | very fine-pitch ball grid array |
| LVD | low-voltage detect | WDT | watchdog timer |
| MAC | multiply-accumulate | XRES | external reset |
| MCU | microcontroller unit | | |

Document Conventions

Units of Measure

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|--------|-----------------|--------|-----------------|
| °C | degree Celsius | mV | millivolt |
| dB | decibels | nA | nanoampere |
| fF | femtofarad | ns | nanosecond |
| kHz | kilohertz | nV | nanovolt |
| kΩ | kilohms | Ω | ohms |
| MHz | megahertz | pA | picoampere |
| μA | microampere | pF | picofarad |
| μs | microsecond | ps | picosecond |
| μV | microvolt | % | percent |
| mA | milliampere | rt-Hz | root hertz |
| mm | millimeter | V | volt |
| ms | millisecond | W | watt |

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.

Glossary

| | |
|---|---|
| active high | <ol style="list-style-type: none"> A logic signal having its asserted state as the logic 1 state. A logic signal having the logic 1 state as the higher voltage of the two states. |
| analog blocks | The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more. |
| analog-to-digital (ADC) | A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation. |
| API (Application Programming Interface) | A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications. |
| asynchronous | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal. |
| Bandgap reference | A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference. |
| bandwidth | <ol style="list-style-type: none"> The frequency range of a message or information processing system measured in hertz. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum. |
| bias | <ol style="list-style-type: none"> A systematic deviation of a value from a reference value. The amount by which the average of a set of values departs from a reference value. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device. |

Glossary *(continued)*

| | |
|-------------------------------|--|
| block | <ol style="list-style-type: none">1. A functional unit that performs a single function, such as an oscillator.2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block. |
| buffer | <ol style="list-style-type: none">1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written.2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.3. An amplifier used to lower the output impedance of a system. |
| bus | <ol style="list-style-type: none">1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns.2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0].3. One or more conductors that serve as a common connection for a group of related devices. |
| clock | The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks. |
| comparator | An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements. |
| compiler | A program that translates a high level language, such as C, into machine language. |
| configuration space | In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'. |
| crystal oscillator | An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components. |
| cyclic redundancy check (CRC) | A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression. |
| data bus | A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions. |
| debugger | A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory. |
| dead band | A period of time when neither of two or more signals are in their active state or in transition. |
| digital blocks | The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI. |
| digital-to-analog (DAC) | A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation. |
| duty cycle | The relationship of a clock period high time to its low time, expressed as a percent. |
| emulator | Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system. |

Glossary (continued)

| | |
|---------------------------------|--|
| external reset (XRES) | An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state. |
| flash | An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off. |
| Flash block | The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes. |
| frequency | The number of cycles or events per unit of time, for a periodic function. |
| gain | The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB. |
| I ² C | A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I ² C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I ² C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode. |
| ICE | The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer). |
| input/output (I/O) | A device that introduces data into or extracts data from a system. |
| interrupt | A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed. |
| interrupt service routine (ISR) | A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution. |
| jitter | <ol style="list-style-type: none"> 1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles. |
| low-voltage detect (LVD) | A circuit that senses V _{DD} and provides an interrupt to the system when V _{DD} falls lower than a selected threshold. |
| M8C | An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space. |
| master device | A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the slave device . |
| microcontroller | An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor. |
| mixed-signal | The reference to a circuit containing both analog and digital techniques and components. |

Glossary (continued)

| | |
|-----------------------------|---|
| modulator | A device that imposes a signal on a carrier. |
| noise | <ol style="list-style-type: none">1. A disturbance that affects a signal and that may distort the information carried by the signal.2. The random variations of one or more characteristics of any entity such as voltage, current, or data. |
| oscillator | A circuit that may be crystal controlled and is used to generate a clock frequency. |
| parity | A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity). |
| phase-locked loop (PLL) | An electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. |
| pinouts | The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names. |
| port | A group of pins, usually eight. |
| power on reset (POR) | A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset. |
| PSoC [®] | Cypress Semiconductor's PSoC [®] is a registered trademark and Programmable System-on-Chip [™] is a trademark of Cypress. |
| PSoC Designer [™] | The software for Cypress' Programmable System-on-Chip technology. |
| pulse width modulator (PWM) | An output in the form of duty cycle which varies as a function of the applied measurand |
| RAM | An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in. |
| register | A storage device with a specific capacity, such as a bit or byte. |
| reset | A means of bringing a system back to a know state. See hardware reset and software reset. |
| ROM | An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in. |
| serial | <ol style="list-style-type: none">1. Pertaining to a process in which all events occur one after the other.2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel. |
| settling time | The time it takes for an output signal or value to stabilize after the input has changed from one value to another. |
| shift register | A memory storage device that sequentially shifts a word either left or right to output a stream of serial data. |
| slave device | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |

Glossary *(continued)*

| | |
|----------------|---|
| SRAM | An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device. |
| SROM | An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash. |
| stop bit | A signal following a character or block that prepares the receiving device to receive the next character or block. |
| synchronous | <ol style="list-style-type: none">1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal.2. A system whose operation is synchronized by a clock signal. |
| tristate | A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net. |
| UART | A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits. |
| user modules | Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level API (Application Programming Interface) for the peripheral function. |
| user space | The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program. |
| V_{DD} | A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V. |
| V_{SS} | A name for a power net meaning "voltage source." The most negative power supply signal. |
| watchdog timer | A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time. |

Errata

This section describes the errata for the CY8C24x94 device. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

| Part Number |
|-------------|
| CY8C24x94 |

CY8C24x94 Errata Summary

The following table defines the errata applicability to available devices.

| Items | Part Number |
|---|-------------|
| 1. The DP line of the USB interface may pulse low when the PSoC device wakes from sleep causing an unexpected wake-up of the host computer. | CY8C24x94 |
| 2. Invalid Flash reads may occur if Vdd is pulled to -0.5 V just before power on. | CY8C24x94 |
| 3. PMA Index Register fails to auto-increment with CPU_Clock set to SysClk/1 (24 MHz). | CY8C24x94 |
| 4. The Internal Main Oscillator (IMO) frequency parameter (FIMO245V) may increase over a period of time during usage in the field and exceed the maximum spec limit of 24.96 MHz. | CY8C24x94 |

1. The DP line of the USB interface may pulse low when the PSoC device wakes from sleep causing an unexpected wake-up of the host computer.

■ PROBLEM DEFINITION

When the device is operating at 4.75 V to 5.25 V and the 3.3 V regulator is enabled, a short low pulse may be created on the DP signal line during device wake-up. The 15-20 μ s low pulse of the DP line may be interpreted by the host computer as a deattach or the beginning of a wake-up.

■ TRIGGER CONDITION(S)

The bandgap reference voltage used by the 3.3 V regulator decreases during sleep due to leakage. Upon device wake up, the bandgap is reenabled and after a delay for settling, the 3.3 V regulator is enabled. On some devices the 3.3 V regulator that is used to generate the USB DP signal may be enabled before the bandgap is fully stabilized. This can cause a low pulse on the regulator output and DP signal line until the bandgap stabilizes. In applications where Vdd is 3.3 V, the regulator is not used and therefore the DP low pulse is not generated.

■ WORKAROUND

To prevent the DP signal from pulsing low, keep the bandgap enabled during sleep. The most efficient method is to set the No Buzz bit in the OSC_CR0 register. The No Buzz bit keeps the bandgap powered and output stable during sleep. Setting the No Buzz bit results in nominal 100 μ A increase to sleep current. Leaving the analog reference block enabled during sleep also resolves this issue because it forces the bandgap to remain enabled. An example for disabling the No Buzz bit is listed below.

Assembly

```
M8C_SetBank1
or reg[OSC_CR0], 0x20
M8C_SetBank0
```

C

```
OSC_CR0 |= 0x20;
```

2. Invalid Flash reads may occur if Vdd is pulled to -0.5 V just before power on.

■ PROBLEM DEFINITION

When Vdd of the device is pulled below ground just before power on, the first read from each 8K Flash page may be corrupted. This issue does not affect Flash page 0 because it is the selected page upon reset.

■ TRIGGER CONDITION(S)

When Vdd is pulled below ground before power on, an internal Flash reference may deviate from its nominal voltage. The reference deviation tends to result in the first Flash read from that page returning 0xFF. During the first read from each page, the reference is reset resulting in all future reads returning the correct value. A short delay of 5 μ s before the first real read provides time for the reference voltage to stabilize.

■ WORKAROUND

To prevent an invalid Flash read, a dummy read from each Flash page must occur before use of the pages. A delay of 5 μ s must occur after the dummy read and before a real read. The dummy reads occurs as soon as possible and must be located in Flash page 0 before a read from any other Flash page. An example for reading a byte of memory from each Flash page is listed below. Placed it in boot.tpl and boot.asm immediately after the 'start:' label.

```
// dummy read from each 8K Flash page
// page 1
mov A, 0x20      // MSB
mov X, 0x00      // LSB
romx
// wait at least 5  $\mu$ s
mov X, 14
loop1:
dec X
jnz loop1
```

3. PMA Index Register fails to auto-increment with CPU_Clock set to SysClk/1 (24 MHz).

■ PROBLEM DEFINITION

When the device is operating at 4.75 to 5.25 V and the CPU_Clock is set to SysClk/1 (24 MHz), the USB PMA Index Register may fail to increment automatically when used in an OUT endpoint configuration at Full-Speed. When the application program attempts to use the bReadOutEP() function the first byte in the PMA buffer is always returned.

■ TRIGGER CONDITION(S)

An internal flip-flop hold problem associated with Index Register increment function. All reads of the associated RAM originate from the first byte. The hold problem has no impact on other circuits or functions within the device.

■ WORKAROUND

To make certain that the index register properly increments, set the CPU_Clock to SysClk/2 (12 MHz) during the read of the PMA buffer. An example for the clock adjustment method is listed below.

PSoC Designer™ 4.3 User Module workaround: PSoC Designer Release 4.3 and subsequent releases includes a revised full-speed USB User Module with the revised firmware work-around included (see example below).

```
;;  
;; 24 MHz read PMA workaround  
;;  
M8C_SetBank1  
mov A, reg[OSC_CR0]  
push A  
and A, 0xf8 ;clear the clock bits (briefly chg the cpu_clk to 3 MHz)  
or A, 0x02 ;will set clk to 12Mhz  
  
mov reg[OSC_CR0],A ;clk is now set at 12 MHz  
M8C_SetBank0  
.loop:  
  mov A, reg[PMA0_DR] ; Get the data from the PMA space  
  mov [X], A ; save it in data array  
  inc X ; increment the pointer  
  dec [USB_APITemp+1] ; decrement the counter  
  jnz .loop ; wait for count to zero out  
;;  
;; 24MHz read PMA workaround (back to previous clock speed)  
;;  
pop A ;recover previous reg[OSC_CR0] value  
M8C_SetBank1  
mov reg[OSC_CR0],A ;clk is now set at previous value  
M8C_SetBank0  
;;  
;; end 24Mhz read PMA workaround
```

4. The Internal Main Oscillator (IMO) frequency parameter (FIMO245V) may increase over a period of time during usage in the field and exceed the maximum spec limit of 24.96 MHz.

■ **PROBLEM DEFINITION**

When the device has been operating at 4.75 V to 5.25 V for a cumulatively long duration in the field, the IMO Frequency may slowly increase over the duration of usage in the field and eventually exceed the maximum spec limit of 24.96 MHz. This may affect applications that are sensitive to the max value of IMO frequency, such as those using UART communication and result in a functional failure.

■ **TRIGGER CONDITION(S)**

Very long (cumulative) usage of the device in the operating voltage range of 4.75V to 5.25V, with the IMO clock running continuously, could lead to the degradation. Higher power supply voltage and lower ambient temperature are worst-case conditions for the degradation.

■ **WORKAROUND**

Operating the device with the power supply voltage range of 3.0 V to 3.6 V, would avoid the degradation of IMO Frequency beyond the max spec limit of 24.96 MHz.

■ **FIX STATUS**

A new revision of the silicon, with a fix for this issue, is expected to be available from August 1st 2015.

Document History Page

| Document Title: CY8C24094/CY8C24794/CY8C24894/CY8C24994, PSoC [®] Programmable System-on-Chip [™] Document Number: 38-12018 | | | | |
|--|---------|-----------------|-----------------|--|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 133189 | NWJ | 01/27/2004 | New silicon and new document – Advance datasheet. |
| *A | 251672 | SFV | See ECN | First Preliminary datasheet. Changed title to encompass only the CY8C24794 because the CY8C24494 and CY8C24694 are not being offered by Cypress. |
| *B | 289742 | HMT | See ECN | Add standard DS items from SFV memo. Add Analog Input Mux on pinouts. 2 MACs. Change 512 bytes of SRAM to 1 K. Add dimension key to package. Remove HAPI. Update diagrams, registers and specs. |
| *C | 335236 | HMT | See ECN | Add CY logo. Update CY copyright. Update new CY.com URLs. Re-add ISSP programming pinout notation. Add Reflow Temp. table. Update features (MAC, Oscillator, and voltage range), registers (INT_CLR2/MSK2, second MAC), and specs. (Rext, IMO, analog output buffer...). |
| *D | 344318 | HMT | See ECN | Add new color and logo. Expand analog arch. diagram. Fix I/O #. Update Electrical Specifications. |
| *E | 346774 | HMT | See ECN | Add USB temperature specifications. Make datasheet Final. |
| *F | 349566 | HMT | See ECN | Remove USB logo. Add URL to preferred dimensions for mounting MLF packages. |
| *G | 393164 | HMT | See ECN | Add new device, CY8C24894 56-pin MLF with XRES pin. Add Fimousb3v char. to specs. Upgrade to CY Perform logo and update corporate address and copyright. |
| *H | 469243 | HMT | See ECN | Add ISSP note to pinout tables. Update typical and recommended Storage Temperature per industrial specs. Update Low Output Level maximum I/OL budget. Add FLS_PR1 to Register Map Bank 1 for users to specify which Flash bank should be used for SROM operations. Add two new devices for a 68-pin QFN and 100-ball VFBGA under RPNs: CY8C24094 and CY8C24994. Add two packages for 68-pin QFN. Add OCD non-production pinouts and package diagrams. Update CY branding and QFN convention. Add new Dev. Tool section. Update copyright and trademarks. |
| *I | 561158 | HMT | See ECN | Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add CY8C20x34 to PSoC Device Characteristics table. Add detailed dimensions to 56-pin QFN package diagram and update revision. Secure one package diagram/manufacturing per QFN. Update emulation pod/feet kit part numbers. Fix pinout type-o per TestTrack. |
| *J | 728238 | HMT | See ECN | Add CapSense SNR requirement reference. Update figure standards. Update Technical Training paragraphs. Add QFN package clarifications and dimensions. Update ECN-ed Amkor dimensioned QFN package diagram revisions. Reword SNR reference. Add new 56-pin QFN spec. |
| *K | 2552459 | AZIE / PYRS | 08/14/08 | Add footnote on AGND descriptions to avoid using P2[4] for digital signaling as it may add noise to AGND. Remove reference to CMP_GO_EN1 in Map Bank 1 Table on Address 65; this register has no functionality on 24xxx. Add footnote on die sales. Add description 'Optional External Clock Input' on P1[4] to match description of P1[4]. |
| *L | 2616550 | OGNE / PYRS | 12/05/08 | Updated Programmable Pin Configuration detail. Changed title from PSoC [®] Mixed-Signal Array to PSoC [®] Programmable System-on-Chip [™] |
| *M | 2657956 | DPT / PYRS | 02/11/09 | Added package diagram 001-09618 and updated Ordering Information table |

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|---|---------|------------------|-----------------|---|
| Document Number: 38-12018 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *N | 2708135 | BRW | 05/18/2009 | Added Note in the Pin Information section on page 8. Removed reference to Hi-Tech Lite Compiler in the section Development Tools Selection on page 42. |
| *O | 2718162 | DPT | 06/11/2009 | Added 56-Pin QFN (Sawn) package diagram and updated ordering information |
| *P | 2762161 | RLRM | 09/10/2009 | Updated the following parameters: DC _{ILO} , F _{32K_U} , F _{IMO6} , T _{POWERUP} , T _{ERASE_ALL} , T _{PROGRAM_HOT} , and T _{PROGRAM_COLD} . Added SR _{POWER_UP} parameter in AC specs table. |
| *Q | 2768530 | RLRM | 09/24/09 | Ordering Information table: Changed XRES Pin value for CY8C24894-24LTXI and CY8C24894-24LTXIT to 'Yes'. |
| *R | 2817938 | KRIS | 11/30/09 | Ordering Information : Updated CY8C24894-24LTXI and CY8C24894-24LTXIT parts as Sawn and updated the Digital I/O and Analog Pin values Added Contents page. Updated 68 QFN package diagram (51-85124) |
| *S | 2846641 | RLRM | 1/12/10 | Added package diagram 001-58740 and updated Development Tools section. |
| *T | 2867363 | ANUP | 01/27/10 | Modified Note 9 to remove voltage range 2.4 V to 3.0 V |
| *U | 2901653 | NJF | 03/30/2010 | Updated Cypress website links Added T _{XRST} , DC24M, T _{BAKETEMP} and T _{BAKETIME} parameters Removed reference to 2.4 V Removed sections 'Third Party Tools' 'Build a PSoC Emulator into your Board' Updated package diagrams Removed inactive parts from ordering information table. |
| *V | 2938528 | VMAD | 05/28/2010 | Updated content to match current style guide and datasheet template. No technical updates |
| *W | 3028596 | NJF | 09/20/10 | Added PSoC Device Characteristics table. Added DC I ² C Specifications table. Added F _{32K_U} max limit. Added T _{jitter_IMO} specification, removed existing jitter specifications. Updated Analog reference tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I ² C Timing Diagram. They were updated for clearer understanding. Updated Figure 12 since the labelling for y-axis was incorrect. Template and styles update. |
| *X | 3082244 | NXZ | 11/09/2010 | Sunset review; no updates. |
| *Y | 3111357 | BTK / NJF / ARVM | 12/15/10 | Updated solder reflow specifications. Removed F _{IMO6} spec from AC chip-level specifications table. Removed the following pruned parts from the ordering information table and their references in the datasheet. 1) CY8C24794-24LFXI 2) CY8C24794-24LFXIT 3) CY8C24894-24LFXI 4) CY8C24894-24LFXIT |
| *Z | 3126167 | BTK / ANBA / PKS | 01/03/11 | Updated ordering information. Removed the package diagram spec 51-85214 since there are no MPNs in the ordering information table that corresponds with this package. Updated ordering code definitions for clearer understanding. |
| AA | 3367463 | BTK / GIR | 09/22/11 | Updated V _{REFHI} values for parameter '0b100' under Table 19 on page 30 . Updated text under Table 19 on page 30 . The text "Pin must be left floating" is included under Description of NC pin in Table 4 on page 11 , Table 6 on page 13 , Table 7 on page 15 , and Table 8 on page 17 . Updated Table 38 on page 49 to give more clarity. |

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| Document Title: CY8C24094/CY8C24794/CY8C24894/CY8C24994, PSoC [®] Programmable System-on-Chip™ | | | | |
|---|---------|-----------------|-----------------|--|
| Document Number: 38-12018 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| AB | 3404970 | MATT | 10/13/11 | Removed prune device CY8C24994-24BVXI from Ordering Information . |
| AC | 3461872 | CSAI | 12/13/2011 | Sunset review; no content update |
| AD | 3503402 | PMAD | 01/20/2012 | Updated V _{OH} and V _{OL} section in Table 12 . |
| AE | 3545509 | PSAI | 03/08/2012 | Updated link to 'Technical reference Manual'. |
| AF | 3862667 | CSAI | 01/09/2013 | Updated Ordering Information (Updated part numbers). Updated Packaging Dimensions : spec 001-53450 – Changed revision from *B to *C. spec 001-09618 – Changed revision from *D to *E. spec 51-85048 – Changed revision from *E to *G. |
| AG | 3979302 | CSAI | 04/23/2013 | Updated Packaging Dimensions : spec 001-58740 – Changed revision from ** to *A. Added Errata . |
| AH | 4074544 | CSAI | 07/23/2013 | Added Errata Footnotes (Note 21, 23) Updated Electrical Specifications : Updated DC Electrical Characteristics : Updated DC Chip-Level Specifications : Added Note 21 and referred the same note in “Sleep Mode” in description of I _{SB} parameter in Table 11 . Updated DC POR and LVD Specifications : Added Note 23 and referred the same note in V _{PPOR0} , V _{PPOR1} , V _{PPOR2} parameters in Table 22 . Updated to new template. |
| AI | 4596835 | DIMA | 12/15/2014 | Updated Pin Information : Updated 56-Pin Part Pinout : Updated Table 2 : Added Note 5 and referred the same note in description of pin 19 and pin 50. Updated 56-Pin Part Pinout (with XRES) : Updated Table 3 : Added Note 8 and referred the same note in description of pin 19 and pin 50. Updated 68-Pin Part Pinout : Updated Table 4 : Added Note 10 and referred the same note in description of pin 7, pin 20 and pin 60. Updated 68-Pin Part Pinout (On-Chip Debug) : Updated Table 5 : Added Note 13 and referred the same note in description of pin 7, pin 20 and pin 60. Updated 100-Ball VFBGA Part Pinout : Updated Table 6 : Added Note 15 and referred the same note in caption of Table 6 . Updated 100-Ball VFBGA Part Pinout (On-Chip Debug) : Updated Table 7 : Added Note 17 and referred the same note in caption of Table 7 . Updated 100-Pin Part Pinout (On-Chip Debug) : Updated Table 8 : Added Note 19 and referred the same note in caption of Table 8 . Updated Packaging Dimensions : spec 001-12921 – Changed revision from *B to *C. spec 001-53450 – Changed revision from *C to *D. spec 51-85209 – Changed revision from *D to *E. spec 51-85048 – Changed revision from *G to *I. Completing Sunset Review. |
| AJ | 4622083 | SLAN | 01/13/2015 | Added More Information section. |

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|---|---------|-----------------|-----------------|--|
| Document Number: 38-12018 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| AK | 4684565 | PSI | 03/12/2015 | Updated Packaging Dimensions : spec 001-58740 – Changed revision from *A to *B. Updated Errata . |
| AL | 5699855 | AESATP12 | 04/20/2017 | Updated logo and copyright. |
| AM | 5638269 | RJVB | 07/04/2017 | Updated Electrical Specifications : Updated DC Electrical Characteristics : Updated DC Analog Reference Specifications : Updated description. Updated Packaging Dimensions : spec 001-58740 – Changed revision from *B to *C. |

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