PSMN013-100ES

N-channel 100V 13.9mΩ standard level MOSFET in I2PAK.

Rev. 3 — 29 September 2011 Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement MOSFET in I2PAK package qualified to 175C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	100	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1	[1]	-	-	68	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2		-	-	170	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 15$ A; $T_j = 100$ °C; see Figure 11		-	-	25	mΩ
		$V_{GS} = 10$ V; $I_D = 15$ A; $T_j = 25$ °C; see Figure 12; see Figure 11	[2]	-	11	13.9	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10$ V; $I_D = 25$ A; $V_{DS} = 50$ V; see Figure 14; see Figure 13		-	17	-	nC

Table 1. Quick reference data *...continued*

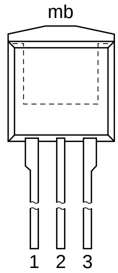
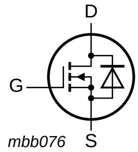
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(tot)}$	total gate charge	V_{GS} = 10 V; I_D = 25 A; V_{DS} = 50 V; see Figure 13; see Figure 14	-	59	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 68 A; V_{sup} ≤ 100 V; unclamped; R_{GS} = 50 Ω	-	-	127	mJ

[1] Continuous current is limited by package.

[2] Measured 3 mm from package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT226 (I2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN013-100ES	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	100	V
V_{DGR}	drain-gate voltage	$T_j \leq 175$ °C; $T_j \geq 25$ °C; $R_{GS} = 20$ kΩ		-	100	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 100$ °C; see Figure 1	[1]	-	47	A
		$V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1	[1]	-	68	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C		-	272	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2		-	170	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25$ °C	[1]	-	68	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C		-	272	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 68$ A; $V_{sup} \leq 100$ V; unclamped; $R_{GS} = 50$ Ω		-	127	mJ

[1] Continuous current is limited by package.

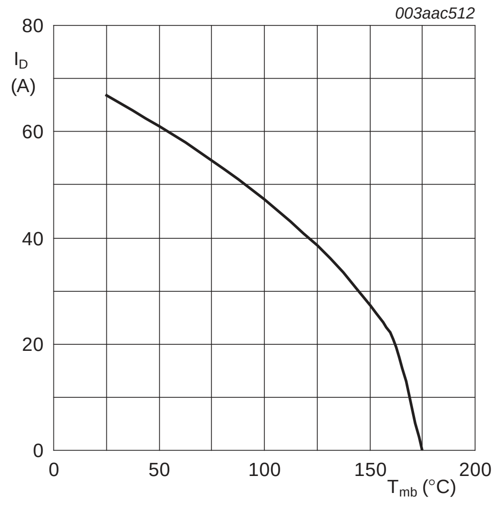
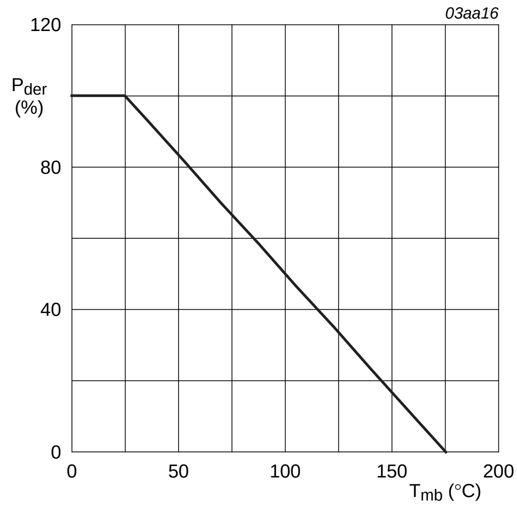


Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 3	-	0.5	0.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	60	-	K/W

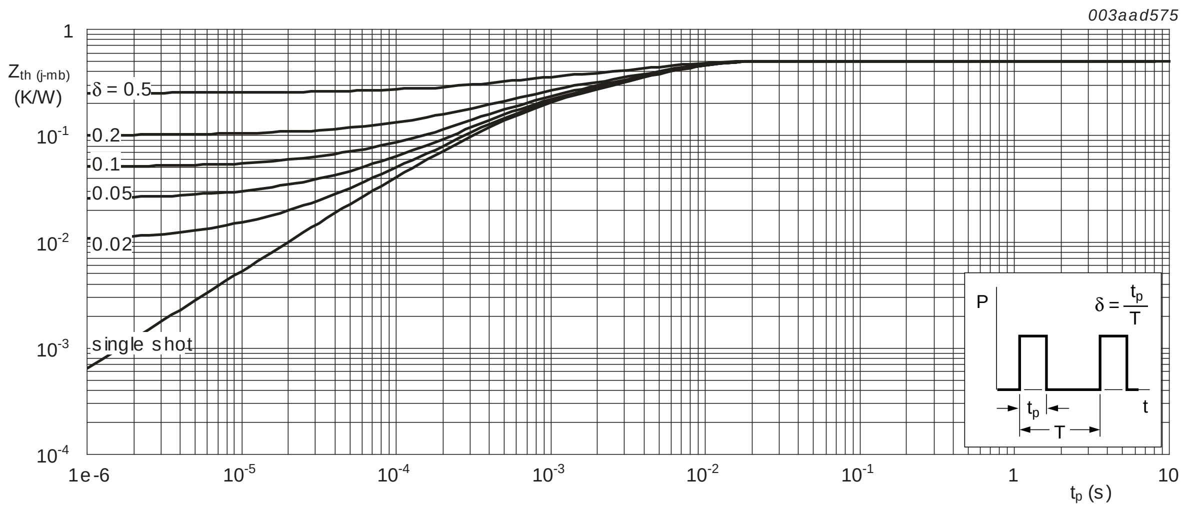


Fig 3. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

6. Characteristics

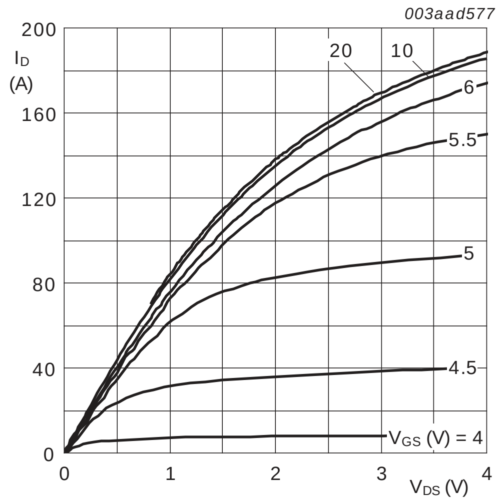
Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 9		1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10; see Figure 9		2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 10		-	-	4.8	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C		-	-	100	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.06	2	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; T_j = 175 °C; see Figure 11		-	30	38.9	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 100 °C; see Figure 11		-	-	25	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C; see Figure 12; see Figure 11	[1]	-	11	13.9	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz		-	1	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; see Figure 13; see Figure 14		-	59	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	47.6	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; see Figure 13; see Figure 14		-	13.8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; see Figure 14		-	9.2	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	4.6	-	nC
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; see Figure 14; see Figure 13		-	17	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	V_{DS} = 50 V; see Figure 14; see Figure 13		-	4.4	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 15		-	3195	-	pF
C_{oss}	output capacitance			-	221	-	pF
C_{rss}	reverse transfer capacitance			-	136	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 4.7 Ω; T_j = 25 °C		-	20.7	-	ns
t_r	rise time			-	25	-	ns
$t_{d(off)}$	turn-off delay time			-	52.5	-	ns
t_f	fall time			-	24	-	ns

Table 6. Characteristics *…continued*

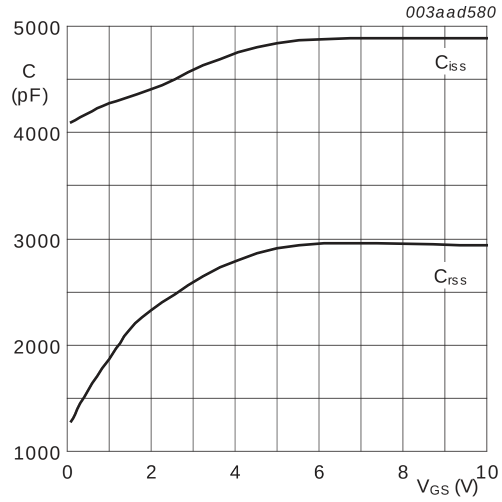
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 16	-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = 100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V	-	52	-	ns
Q_r	recovered charge		-	109	-	nC

[1] Measured 3 mm from package.



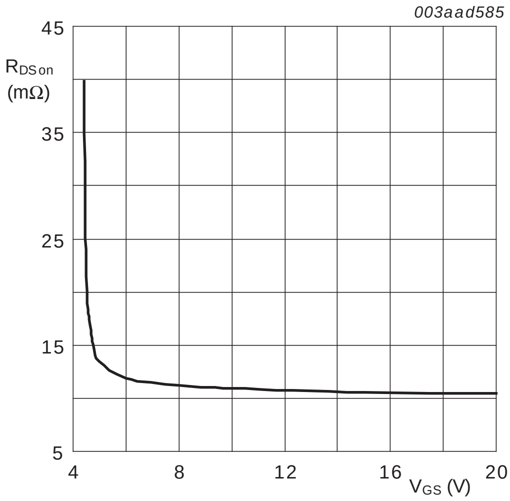
$T_j = 25°C$

Fig 4. Output characteristics: drain current as a function of drain-source voltage; typical values



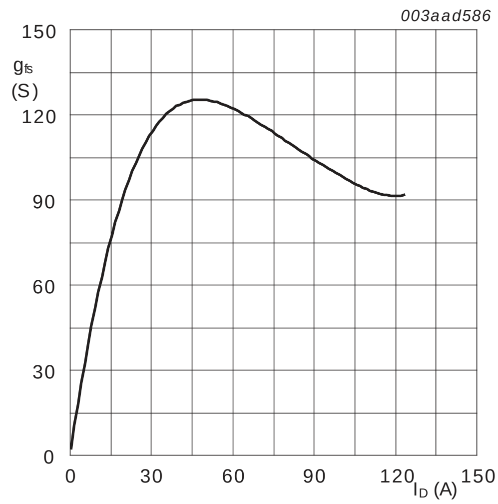
$V_{DS} = 0V; f = 1MHz$

Fig 5. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



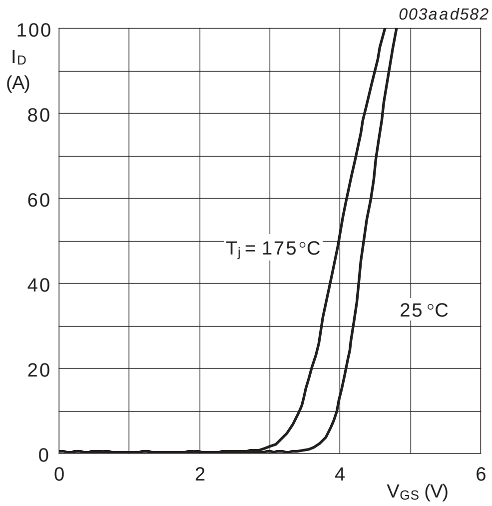
$T_j = 25°C$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



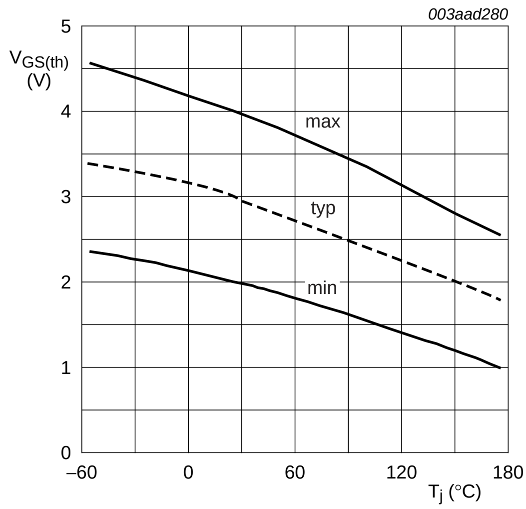
$T_j = 25°C; V_{DS} = 15V$

Fig 7. Forward transconductance as a function of drain current; typical values



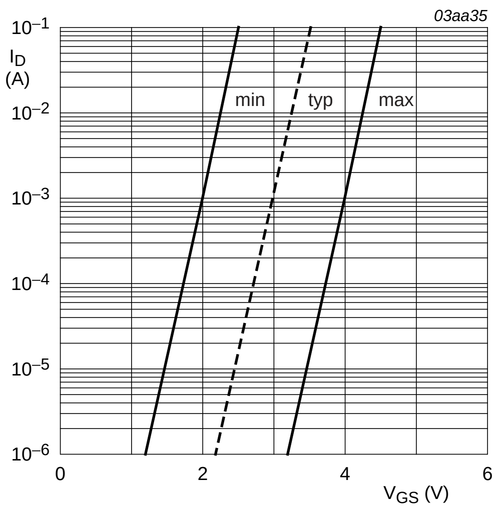
$V_{DS} > I_D \times R_{DSon}$

Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values



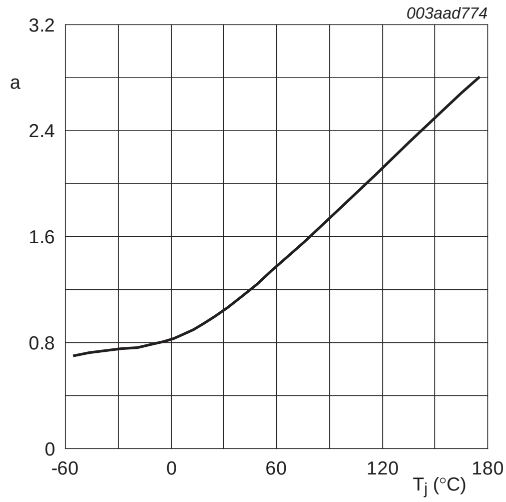
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



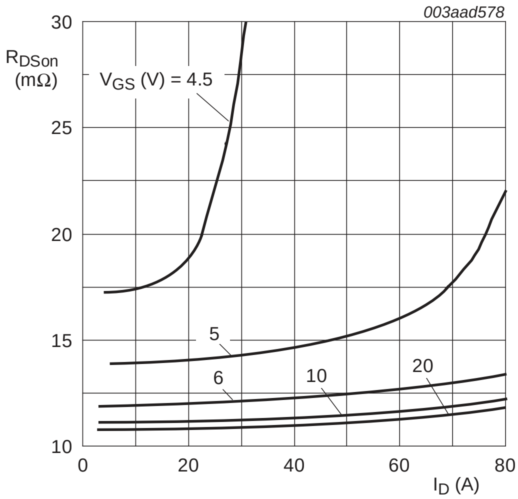
$T_j = 25\,°C; V_{DS} = 5V$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



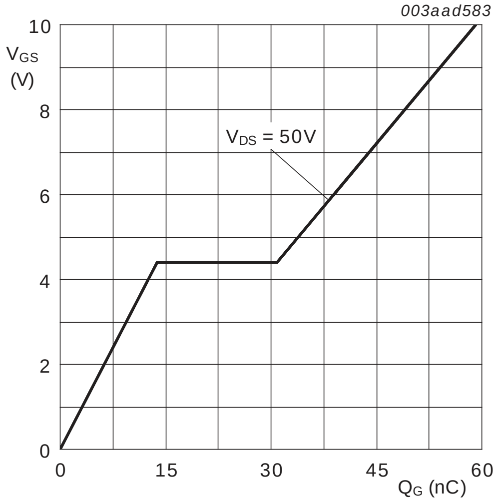
$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25°C$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



$T_j = 25°C; I_D = 25A$

Fig 13. Gate-source voltage as a function of gate charge; typical values

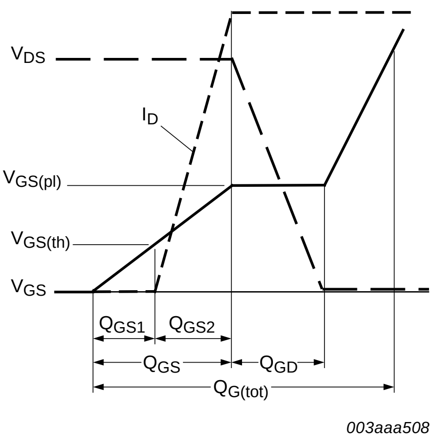
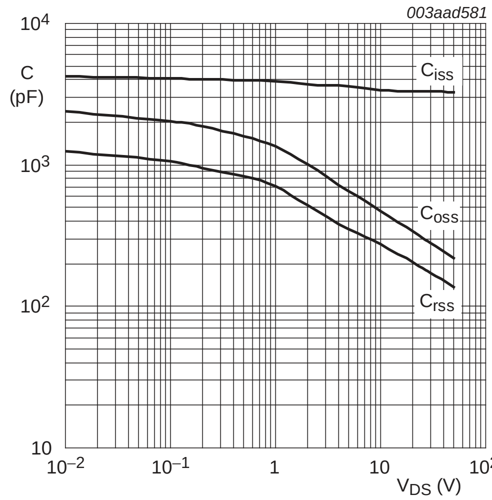
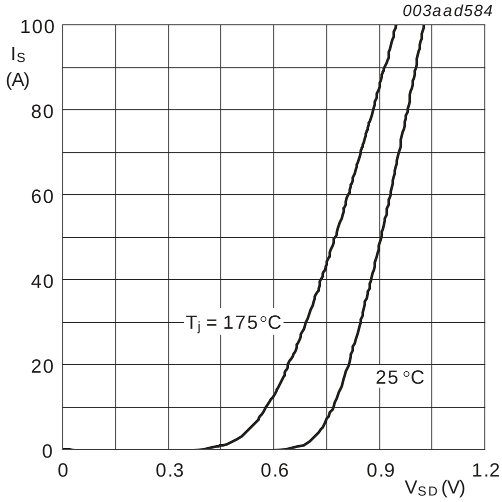


Fig 14. Gate charge waveform definitions



$V_{GS} = 0V; f = 1MHz$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

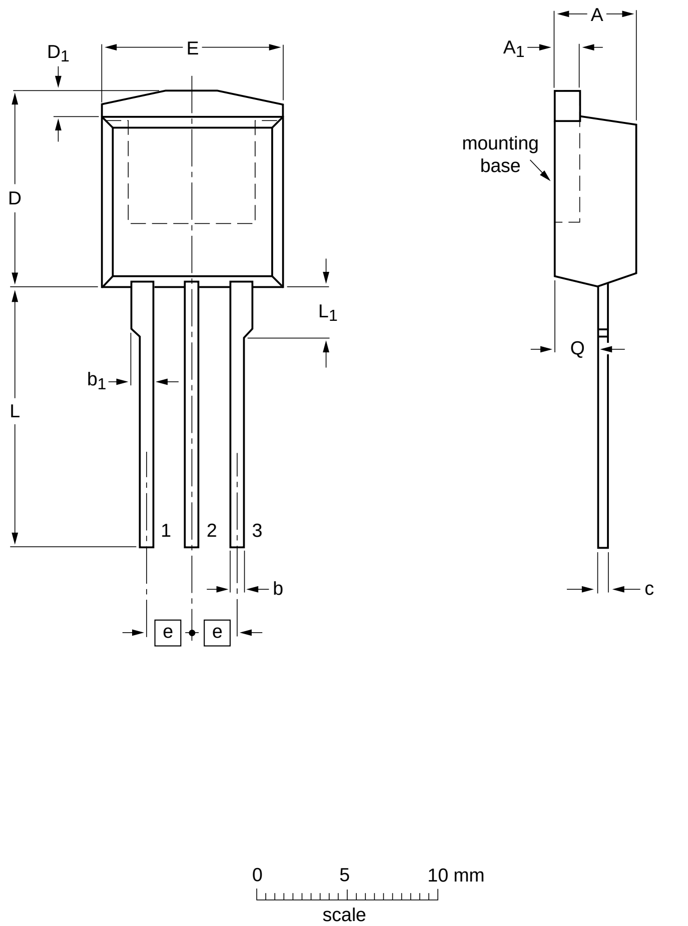


$V_{GS} = 0V$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-262 **SOT226**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D max	D_1	E	e	L	L_1	Q
mm	4.5 4.1	1.40 1.27	0.85 0.60	1.3 1.0	0.7 0.4	11	1.6 1.2	10.3 9.7	2.54	15.0 13.5	3.30 2.79	2.6 2.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT226		TO-262				~~06-02-14~~ 09-08-25

Fig 17. Package outline SOT226 (I2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN013-100ES v.3	20110929	Product data sheet	-	PSMN013-100ES v.2
Modifications:	• Status changed from objective to product. • Various changes to content.			
PSMN013-100ES v.2	20100219	Objective data sheet	-	PSMN013-100ES v.1

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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11. Contents

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Date of release: 29 September 2011