

# FDD6670AS

## 30V N-Channel PowerTrench® SyncFET™

### General Description

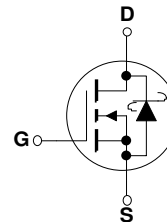
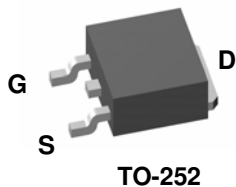
The FDD6670AS is designed to replace a single MOSFET and Schottky diode in synchronous DC:DC power supplies. This 30V MOSFET is designed to maximize power conversion efficiency, providing a low  $R_{DS(ON)}$  and low gate charge. The FDD6670AS includes a patented combination of a MOSFET monolithically integrated with a schottky diode. The performance of the FDD6670AS as the low-side switch in a synchronous rectifier is indistinguishable from the performance of the FDD6670A in parallel with a Schottky diode.

### Applications

- DC/DC converter
- Low side notebook

### Features

- 76 A, 30 V  $R_{DS(ON)}$  max= 8.0 mΩ @  $V_{GS} = 10$  V  
 $R_{DS(ON)}$  max= 10.4 mΩ @  $V_{GS} = 4.5$  V
- Includes SyncFET Schottky body diode
- Low gate charge (29nC typical)
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	±20	V
$I_D$	Drain Current – Continuous (Note 3)	76	A
	– Pulsed (Note 1a)	100	
$P_D$	Power Dissipation (Note 1)	70	W
		3.2	
		1.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD6670AS	FDD6670AS	13"	16mm	2500 units

Electrical Characteristics <span style="float: right;">T<sub>A</sub> = 25°C unless otherwise noted</span>						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Drain-Source Avalanche Ratings</b> (Note 2)						
W <sub>DSS</sub>	Drain-Source Avalanche Energy	Single Pulse, V <sub>DD</sub> = 15 V, I <sub>D</sub> =14A			245	mJ
I <sub>AR</sub>	Drain-Source Avalanche Current				14	A
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, Referenced to 25°C		29		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			500	μA
		V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C		6.5		mA
I <sub>GSS</sub>	Gate-Body Leakage	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA
<b>On Characteristics</b> (Note 2)						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1 mA	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, Referenced to 25°C		-3.3		mV/°C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13.8 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 11.7 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13.8A, T <sub>J</sub> = 125°C		6.8 8.3 9.3	8.0 10.4 11.6	mΩ
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 5 V	50			A
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 13.8 A		52		S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		1580		pF
C <sub>oss</sub>	Output Capacitance			440		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			170		pF
R <sub>G</sub>	Gate Resistance	V <sub>GS</sub> = 15 mV, f = 1.0 MHz		1.8		Ω
<b>Switching Characteristics</b> (Note 2)						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		10	20	ns
t <sub>r</sub>	Turn-On Rise Time			12	22	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			28	45	ns
t <sub>f</sub>	Turn-Off Fall Time			20	36	ns
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 4.5 V, R <sub>GEN</sub> = 6 Ω		15	27	ns
t <sub>r</sub>	Turn-On Rise Time			16	29	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			26	42	ns
t <sub>f</sub>	Turn-Off Fall Time			13	23	ns
Q <sub>g(TOT)</sub>	Total Gate Charge at V <sub>GS</sub> =10V	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 13.8 A,		29	40	nC
Q <sub>g(TOT)</sub>	Total Gate Charge at V <sub>GS</sub> =5V			16	22	nC
Q <sub>gs</sub>	Gate-Source Charge			4.6		nC
Q <sub>gd</sub>	Gate-Drain Charge			5.5		nC
<b>Drain-Source Diode Characteristics</b>						
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3.5 A (Note 2) V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7 A (Note 2)		0.46 0.59	0.7	V
t <sub>rr</sub>	Diode Reverse Recovery Time	I <sub>F</sub> = 3.5 A,		20		ns
Q <sub>rr</sub>	Diode Reverse Recovery Charge	d <sub>I</sub> /d <sub>t</sub> = 300 A/μs (Note 3)		15		nC

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

### Notes:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $R_{\theta JA} = 40^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper



b)  $R_{\theta JA} = 96^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

3. Maximum current is calculated as:
- $$\sqrt{\frac{P_D}{R_{DS(ON)}}$$

where  $P_D$  is maximum power dissipation at  $T_C = 25^\circ\text{C}$  and  $R_{DS(on)}$  is at  $T_{J(max)}$  and  $V_{GS} = 10\text{V}$ . Package current limitation is 21A

## Typical Characteristics

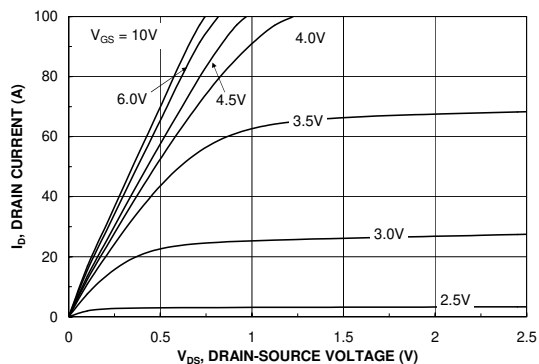


Figure 1. On-Region Characteristics.

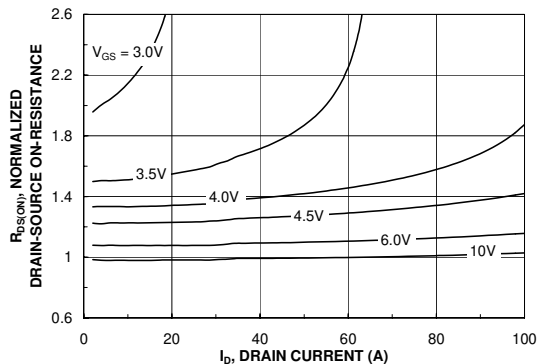


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

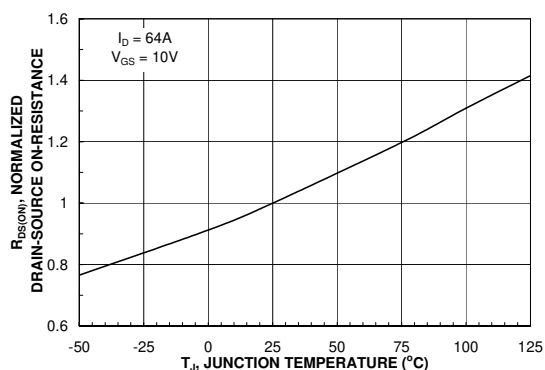


Figure 3. On-Resistance Variation with Temperature.

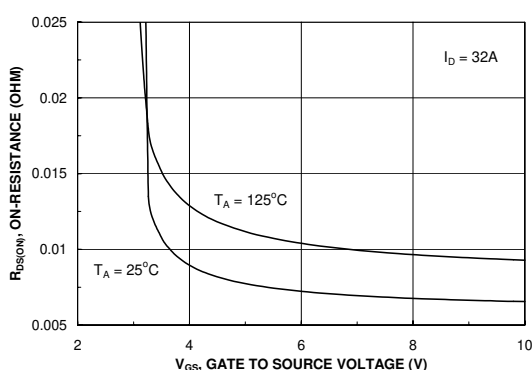


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

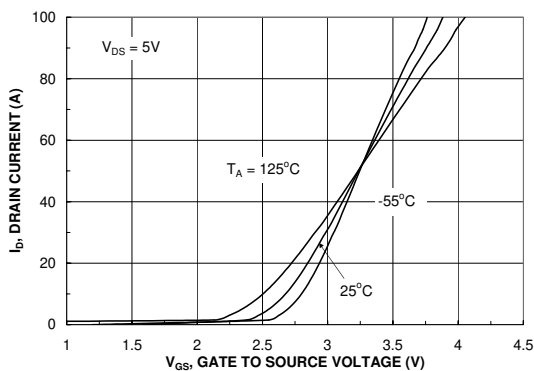


Figure 5. Transfer Characteristics.

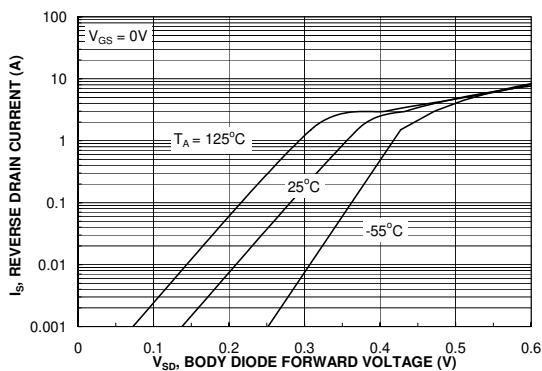


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

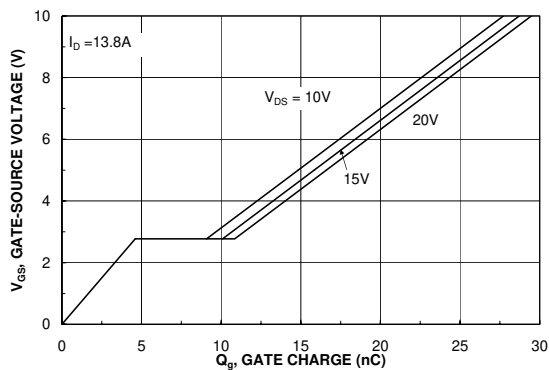


Figure 7. Gate Charge Characteristics.

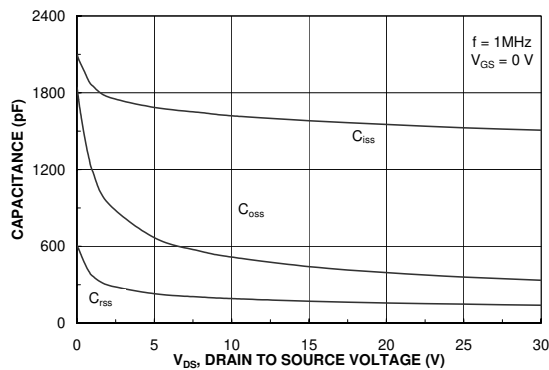


Figure 8. Capacitance Characteristics.

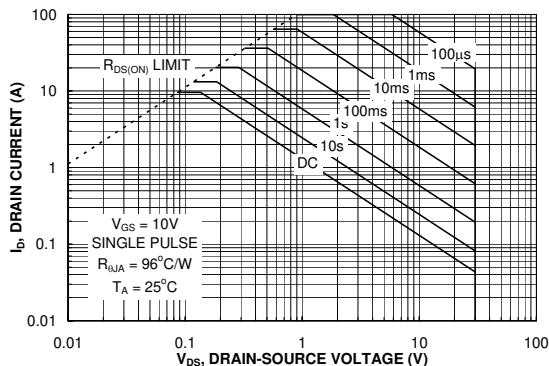


Figure 9. Maximum Safe Operating Area.

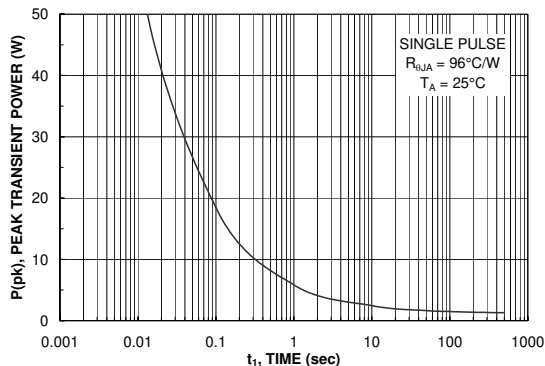


Figure 10. Single Pulse Maximum Power Dissipation.

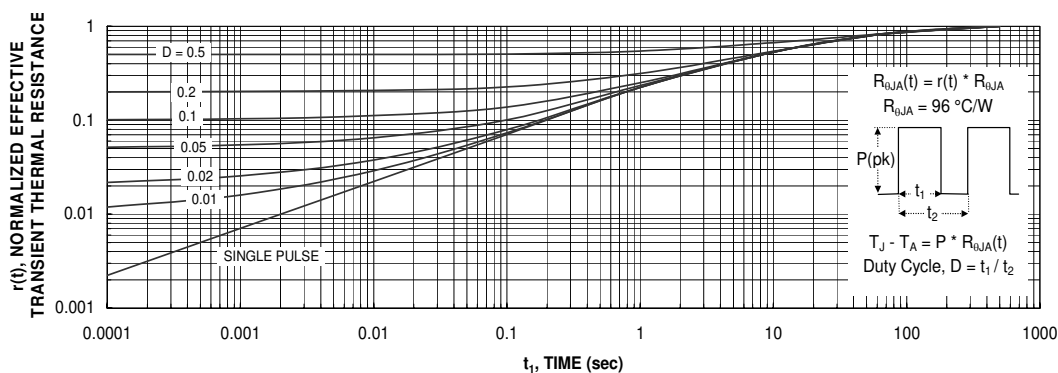


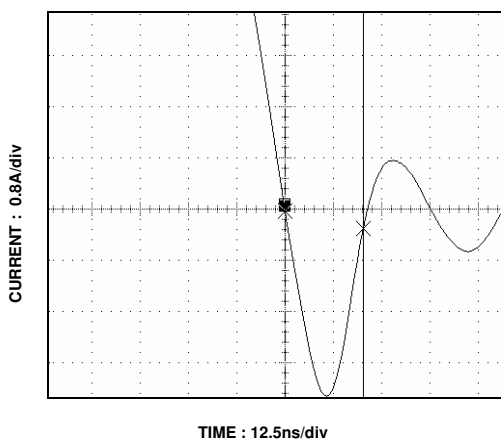
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

## Typical Characteristics (continued)

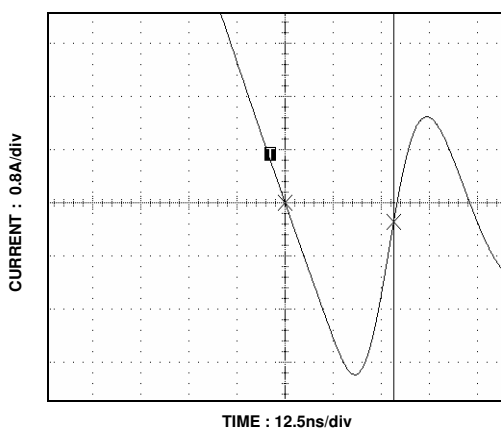
### SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 12 shows the reverse recovery characteristic of the FDD6670AS.



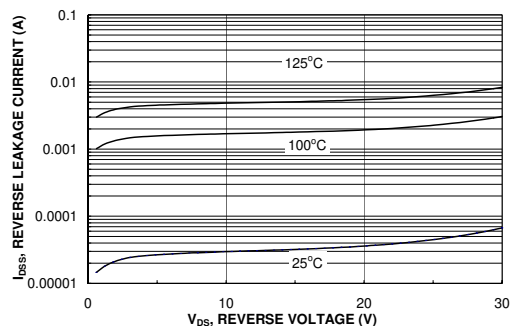
**Figure 12. FDD6670AS SyncFET body diode reverse recovery characteristic.**

For comparison purposes, Figure 13 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDD6670A).



**Figure 13. Non-SyncFET (FDD6670A) body diode reverse recovery characteristic.**

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.



**Figure 14. SyncFET body diode reverse leakage versus drain-source voltage and temperature.**

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