AD9467 FMC Card

Part # 6026-410-001P-BOARD

Hide Details

IC: Analog Devices AD9467 16-Bit, 250 MSPS A/D Converter

Connector(s): FMC (FPGA Mezzanine Card) 160-pin connector

- Features the powerful Analog Devices AD9467 A/D Converter on an FMC board (FPGA Mezzanine Card)
- **AD9467 specs:**
  - 16 bit resolution
  - Single channel
  - IF optimization capability used to improve SFDR
  - 250MSPS sample rate
  - LVDS interface
  - Diff-Uni & SE-Uni analog input types
- **Applications:**
  - Multicarrier, multimode cellular receivers
  - Antenna array positioning
  - Power amplifier linearization
  - Broadband wireless
  - Radar
  - Infrared imaging
  - Communications instrumentation

The new AD9467 FMC board allows users to rapidly prototype and verify system developments using Xilinx FPGA development boards equipped with an FMC header. This card can help engineers de-risk the development cycle and accelerate time-to-market by providing production ready reference HDL code and software for use in end products.

The AD9467 ADC:
The ADI AD9467 FMC board is based on the AD9467, which is a 16-Bit, 250 MSPS analog-to-digital converter that operates on 35% less power at 25% higher sampling rate than any other 16-bit data converter. The AD9467 provides a new level of signal processing performance for test and measurement instrumentation, defense electronics, and communications applications where high resolution over a wide bandwidth is needed. The AD9467 delivers resolution and a fast sample rate while simultaneously achieving a high SFDR (spurious-free dynamic range) of up to 100 dBFs and SNR (signal-to-noise ratio) performance of 76.4 dBFS. The device's SFDR of 90 dBFS up to 300 MHz analog input and 60-femtosecond rms (root mean square) jitter helps lower the signal chain bill of materials component count by allowing engineers to increase system performance at higher intermediate frequencies, thereby reducing the number of signal down-conversion stages.

Product Highlights:

1. IF optimization capability used to improve SFDR.
2. Outstanding SFDR performance for IF sampling applications such as multicarrier, multimode 3G, and 4G cellular base station receivers.
3. Ease of use: on-chip reference, high input impedance buffer, adjustable analog input range, and an output clock to simplify data capture.
4. Packaged in a Pb-free, 72-lead LFCSP package.
5. Clock duty cycle stabilizer (DCS) maintains overall ADC performance over a wide range of input clock pulse widths.
6. Standard serial port interface (SPI) supports various product features and functions, such as data formatting (offset binary, twos complement, or Gray coding).