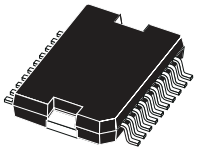
L9825

Octal Low-side Driver For Resistive and Inductive Loads With Serial / Parallel Input Control, Output Protection and Diagnostic

- OUTPUTS CURRENT CAPABILITY UP TO 1A, $R_{ON} \leq 0,75\Omega$ AT $T_J = 25°C$
- PARALLEL CONTROL INPUTS FOR OUTPUTS 1 AND 2
- SPI CONTROL FOR OUTPUTS 1 TO 8
- RESET FUNCTION WITH RESET SIGNAL AT NRES PIN OR UNDERVOLTAGE AT V_{CC}
- INTRINSIC OUTPUT VOLTAGE CLAMPING AT TYP. 50V
- OVERCURRENT SHUTDOWN AT OUTPUTS 1 TO 6
- SHORT CIRCUIT CURRENT LIMITATION AND SELECTIVE THERMAL SHUTDOWN AT OUTPUTS 7 AND 8
- OUTPUT STATUS DATA AVAILABLE ON THE SPI

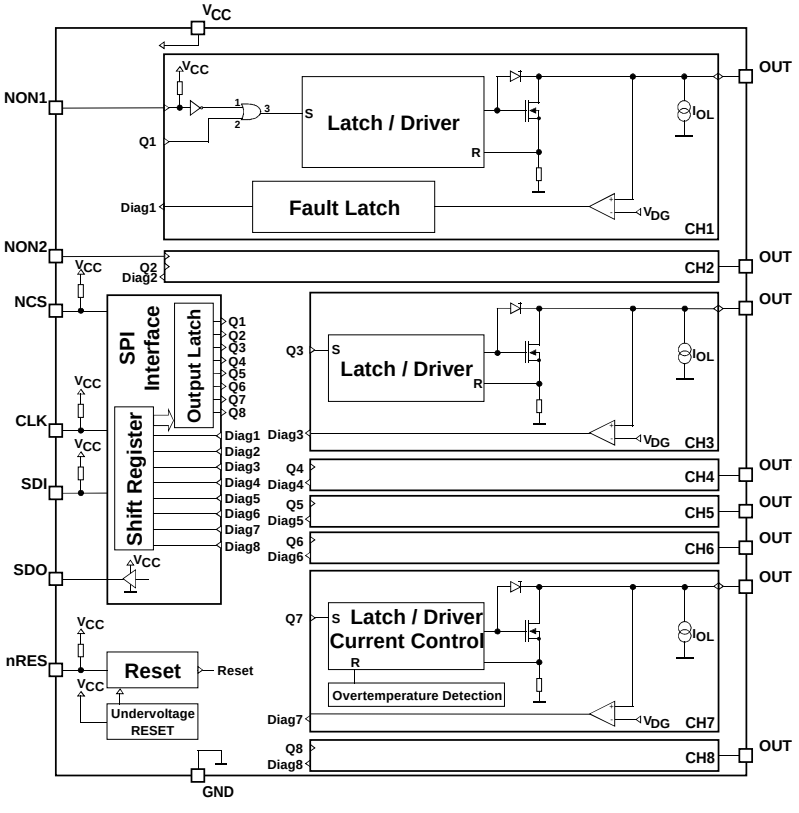


PowerSO20
ORDERING NUMBER: L9825

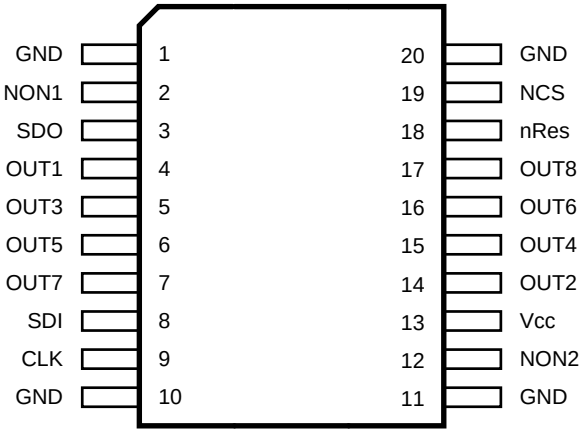
DESCRIPTION

L9825 is a Octal Low-Side Driver Circuit, dedicated for automotive applications. Output voltage clamping is provided for flyback current recirculation, when inductive loads are driven. Chip Select and Serial Peripheral Interface for outputs control and diagnostic data transfer. Parallel Control inputs for two outputs.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



POWSO20

PIN DESCRIPTION

N°	Pin	Function
1	GND	device ground
2	NON1	control input 1
3	SDO	serial data output
4	Out 1	output 1
5	Out 3	output 3
6	Out 5	output 5
7	Out 7	output 7
8	SDI	serial data input
9	CLK	serial clock
10	GND	device ground
11	GND	device ground
12	NON2	control input 2
13	V_{CC}	supply voltage
14	Out 2	output 2
15	Out 4	output 4
16	Out 6	output 6
17	Out 8	output 8
18	nRes	asynchronous nRes
19	NCS	chip select (active low)
20	GND	device ground

ABSOLUTE MAXIMUM RATINGS

For voltages and currents applied externally to the device:

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 to 7	V
Inputs and data lines (NONx, NCS, CLK, SDI, nRes)			
V_{IN}	Voltage (NONx, NCS, CLK, SDI)	-0.3 to 7	V
V_{IN}	Voltage (nRes)	-0.3 to 7	V
I_{IN}	Protection diodes current [1)] ($T \leq 1ms$)	-20 to 20	mA
Outputs (Out1 ... Out8)			
V_{OUTc}	Continuous output voltage	-1.0 to 45	V
I_{OUT}	Output current [2)]	-3 to 2.05	A
E_{OUTcl}	Output clamp energy ($I_{OUT} \leq 0.5A$)	20	mJ

Notes: 1. All inputs are protected against ESD according to MIL 883C; tested with HBM at 2KV. It corresponds to a dissipated energy $E \leq 0,2mJ$.
2. Transient pulses in accordance to DIN40839 part 1, 3 and ISO 7637 Part 1, 3.

For currents determined within the device:

Outputs (Out1 ... Out8)			
I_{OUT}	Output current (Out1 ... Out6)	2.05	A
I_{OUT}	Output current (Out7, Out8)	1.75	A
	Total average-current all outputs [3)]	4.5 (Min.)	A

3. When operating the device with short circuit at more than 2 outputs at the same time, damage due to electrical overstress may occur.

THERMAL DATA

Symbol	Parameter	Value	Unit
Thermal shutdown			
T_{JSC}	Thermal shutdown threshold Min. Typ.	150 165	°C °C
Thermal resistance			
$R_{thjc\text{-}one}$	Single output (junction case) Max.	13	°C/W
$R_{thjc\text{-}all}$	All outputs (junction case) Max.	1.6	°C/W

ELECTRICAL CHARACTERISTCS

(4.5V ≤ V_{CC} ≤ 5.5V; -40°C ≤ T_J ≤ 150°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply voltage						
I_{ccSTB}	Standby current	without load			5	mA
I_{ccOPM}	Operating mode	$I_{OUT1 \ldots 8}$ = 500mA SPI - CLK = 3MHz NCS = LOW SDO no load			5	mA
ΔI_{CC}	ΔI_{CC} during reverse output current	I_{out} = -3A			100	mA
Inputs (NONx. NCS, CLK, SDI, nRes)						
V_{INL}	Low level		-0.3		$0.2 \cdot V_{CC}$	V
V_{INH}	High level		$0.7 \cdot V_{CC}$		V_{CC}+0.3	V
V_{hyst}	Hysteresis voltage		0.85			V
I_{IN}	Input current	$V_{IN} = V_{CC}$			10	µA
R_{IN}	Pullup resistance		50		250	kΩ
C_{IN}	Input capacitance				10	pF
Serial data outputs						
V_{SDOH}	High output level	I_{SDO} = -4mA	V_{CC} -0.4			V
V_{SDOL}	Low output level	I_{SDO} = 3,2mA			0.4	V
I_{SDOL}	Tristate leakage current	NCS = high; 0V ≤ V_{SDO} ≤ V_{CC}	-10		10	µA
C_{SDO}	Output capacitance	f_{SDO} = 300kHz			10	pF
Outputs OUT 1 ... 8						
$I_{OUTL1 - 8}$	Leakage current	OUTx = OFF; V_{OUTx} = 25V; V_{CC} = 5V			100	µA
$I_{OUTL1 - 8}$	Leakage current	OUTx = OFF; V_{OUTx} = 16V; V_{CC} = 5V			100	µA
$I_{OUTL1 - 8}$	Leakage current	OUTx = OFF; V_{OUTx} = 16V; V_{CC} = 1V			10	µA
V_{clp}	Output clamp voltage	1mA ≤ I_{clp} ≤ I_{outp}; I_{test} = 10mA with correlation	45		60	V
R_{DSon}	On resistance OUT 1 ... 8	I_{OUT} = 500mA; T_j = +150°C			1.5	W
C_{OUT}	Output capacitance	V_{OUT} = 16V; f = 1MHz			300	pF
Outputs short circuit protection						
I_{SBC}	Overcurrent shutoff threshold	OUT1 ... OUT6	1.05	1.4	2.05	A
I_{LIM}	Short circuit current limitation	OUT7; OUT8	1.05	1.4	1.75	A
t_{SCB}	Delay shutdown	for output 1 ... 6; I_{OUT} ≤ 1/2 I_{SBC}	0.2	3	12	µs

ELECTRICAL CHARACTERISTCS (continued)

($4.5V \le V_{CC} \le 5.5V$; $-40°C \le T_J \le 150°C$; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Diagnostics						
V_{DG}	Diagnostic threshold voltage		$0.32 \cdot V_{CC}$		$0.4 \cdot V_{CC}$	V
I_{OL}	Open load detection sink current	$V_{out} = V_{DG}$	20		100	µA
t_{df}	Diagnostic detection filter time for output 1 & 2 on each diagnostic condition		15		50	µs
Outputs timing						
t_{don1}	Turn ON delay of OUT 1 and 2	$NON_{1,2}$ = 50% to $V_{OUT} = 0.9 \cdot V_{bat}$ NCS = 50% to $V_{OUT} = 0.9 \cdot V_{bat}$			5	µs
t_{don2}	Turn ON delay of OUT 3 to 8	NCS = 50% to $V_{OUT} = 0.9 \cdot V_{bat}$			10	µs
t_{doff}	Turn OFF delay of OUT 1 to 8	NCS = 50% to $V_{OUT} = 0.1 \cdot V_{bat}$ $NON_{1,2}$ = 50% to $V_{OUT} = 0.1 \cdot V_{bat}$			10	µs
dUon1/dt	Turn ON voltage slew-rate	For output 3 to 8; 90% to 30% of V_{bat}; $R_L = 500\Omega$; $V_{bat} = 16V$	0.7		3.5	V/µs
dUon2/dt	Turn ON voltage slew-rate	For output 1 and 2; 90% to 30% of V_{bat}; $R_L = 500\Omega$; $V_{bat} = 16V$	2		10	V/µs
dUoff1/dt	Turn OFF voltage slew-rate	For output 1 to 8; 30% to 90% of V_{bat}; $R_L = 500\Omega$; $V_{bat} = 16V$	2		10	V/µs
dUoff2/dt	Turn OFF voltage slew-rate	For output 1 to 8; 30% to 80% of V_{bat}; $R_L = 500\Omega$; $V_{bat} = 0.9 \cdot V_{clp}$	2		15	V/µs
Serial diagnostic link (Load capacitor at SDO = 100pF)						
f_{clk}	Clock frequency	50% duty cycle	3			MHz
t_{clh}	Minimum time CLK = HIGH		160			ns
t_{cll}	Minimum time CLK = LOW		160			ns
t_{pcld}	Propagation delay CLK to data at SDO valid	$4.9V \le V_{CC} \le 5.1V$			100	ns
t_{csdv}	NCS = LOW to data at SDO active				100	ns
t_{sclch}	CLK low before NCS low	Setup time CLK to NCS change H/L	100			ns
t_{hclcl}	CLK change L/H after NCS = low		100			ns
t_{scld}	SDI input setup time	CLK change H/L after SDI data valid	20			ns
t_{hcld}	SDI input hold time	SDI data hold after CLK change H/L			20	ns
t_{sclcl}	CLK low before NCS high		150			ns
t_{hclch}	CLK high after NCS high		150			ns
t_{pchdz}	NCS L/H to output data float				100	ns
	NCS pulse filter time	Multiple of 8 CLK cycles				

FUNCTIONAL DESCRIPTION

General

The L9825 integrated circuit features 8 power low-side-driver outputs. Data is transmitted to the device using the Serial Peripheral Interface, SPI protocol. Outputs 1 and 2 can be controlled parallel or serial. The power outputs features voltage clamping function for flyback current recirculation and are protected against short circuit to Vbat.

The diagnostics recognizes two outputs fault conditions: 1) overcurrent for outputs 1 to 6 , overcurrent and thermal overload for outputs 7 and 8 in switch-on condition and 2) open load or short to GND in switch-off condition for all outputs. The outputs status can be read out via the serial interface.

The chip internal reset is a OR function of the external nRes signal and internally generated undervoltage nRes signal.

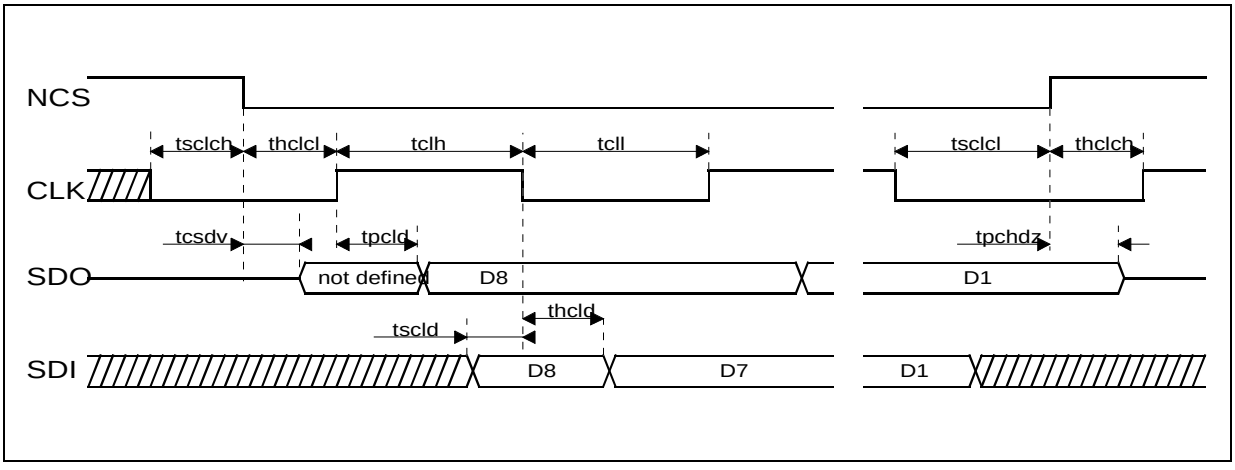
Output Stages Control

Each output is controlled with its latch and with common reset line, which enables all eight outputs. Outputs 1 and 2 can be controlled also by its NON1, NON2 inputs. It allows PWM control independently on the SPI. These inputs features internal pull-up resistors to assure that the outputs are switched off, when the inputs are open.

The control data are transmitted via the SDI input, the timing of the serial interface is shown in Fig. 1.

The device is selected with low NCS signal and the input data are transferred into the 8 bit shift register at every falling CLK edge. The rising edge of the NCS latches the new data from the shift register to the drivers.

Figure 1. Timing of the Serial Interface

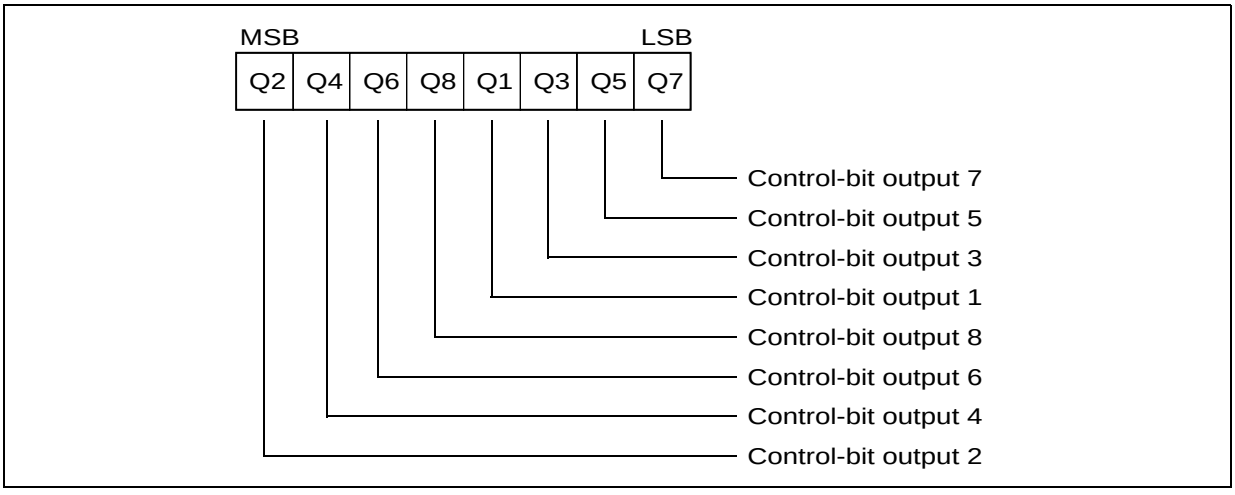


The SPI register data are transferred to the output latch at rising NCS edge. The digital filter between NCS and the output latch ensures that the data are transferred only after 8 CLK cycles or multiple of 8 CLK cycles since the last NCS falling edge. The NCS changes only at low CLK.

Table 1. Outputs Control

Outputs 1, 2:					**Outputs 3 to 8:**		
NON1,2	1	0	0	1			
SPI-bit 1,2	0	0	1	1	SPI-bit 3...8	0	1
Output 1, 2	off	on	on	on	Output 3...8	off	on

Figure 2. Output Control register structure



Power outputs characteristics for flyback current, outputs short circuit protection and diagnostics

For output currents flowing into the circuit the output voltages are limited. The typical value of this voltage is 50V. This function allows that the flyback current of a inductive load recirculates into the circuit; the flyback energy is absorbed in the chip.

Output short circuit protection for outputs 1 to 6 (dedicated for loads without inrush current): when the output current exceeds the short circuit threshold, the corresponding output overload latch is set and the output is switched off immediately.

Output short circuit protection for outputs 7 and 8 (dedicated for loads with inrush current, as lamps): when the load current would exceed the short circuit limit value, the corresponding output goes in a current regulation mode. The output current is determined by the output characteristics and the output voltage depends on the load resistance. In this mode high power is dissipated in the output transistor and its temperature increases rapidly. When the power transistor temperature exceeds the thermal shutdown threshold, the overload latch is set and the corresponding output switched off.

For the load diagnostic in output off condition each output features a diagnostic current sink, typ 60µA.

Diagnostics

The output voltage at all outputs is compared with the diagnostic threshold, typ $0.38 \cdot V_{CC}$.

Outputs 1 and 2 features dedicated fault latches. The output status signal is filtered and latched. The fault latches are cleared during NCS low. The latch stores the status bit, so the first reading after the error occurred might be wrong. The second reading is right.

Table 2. Diagnostic for outputs 1 and 2 in parallel controlled mode.

Output 1, 2	Output-voltage	Status-bit	Output-mode
off	> DG-threshold	high	correct operation
off	< DG-threshold	low	fault condition 2)
on	< DG-threshold	high	correct operation
on	> DG-threshold	low	fault condition 1)

Fault condition 1) "output short circuit to Vbat" : the output was switched on and the voltage at the output exceeded the diagnostics threshold due to overcurrent, the output overload latch was set and the output has been switched off. The diagnostic bit is low.

Fault condition 2) "open load" or "output short circuit to GND" : the output is switched off and the voltage at the output drops below the diagnostics threshold, because the load current is lower than the output diagnostic current source, the load is interrupted. The diagnostic bit is low.

For outputs 3 to 8 the output status signals, are fed directly to the SPI register.

Table 3. Diagnostic for outputs 1 to 8 in SPI controlled mode.

Output 1 ... 8	Output-voltage	Status-bit	Output-mode
off	> DG-threshold	high	correct operation
off	< DG-threshold	low	fault condition 2)
on	< DG-threshold	low	correct operation
on	> DG-threshold	high	fault condition 1)

The fault condition 1) "output short circuit to Vbat" :

For outputs 3 to 6 is the same as of outputs 1 and 2.

For outputs 7 and 8 : the output was switched on and the voltage at the output exceeds the diagnostics threshold. The output operates in current regulation mode or has been switched off due to thermal shutdown. The status bit is low.

Fault condition 2) "open load" or "output short circuit to GND" is the same as of outputs 1 and 2.

At the falling edge of NCS the output status data are transferred to the shift register. When NSC is low, data bits contained in the shift register are transferred to SDO output et every rising CLK edge.

Figure 3. The Pulse Diagram to Read the Outputs Status Register

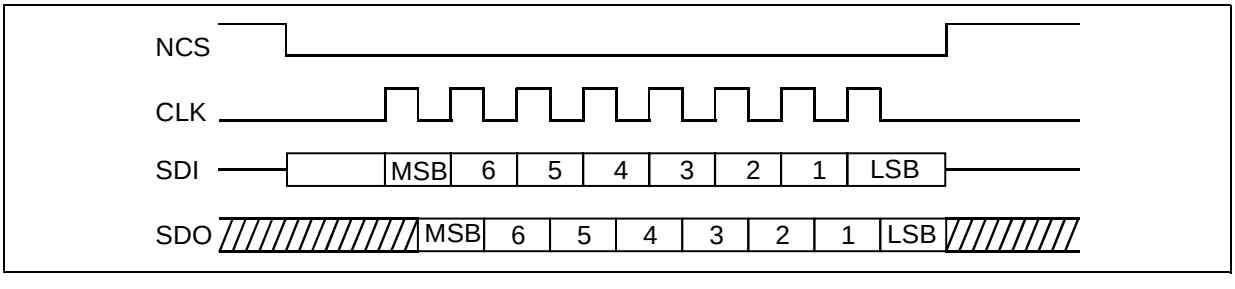
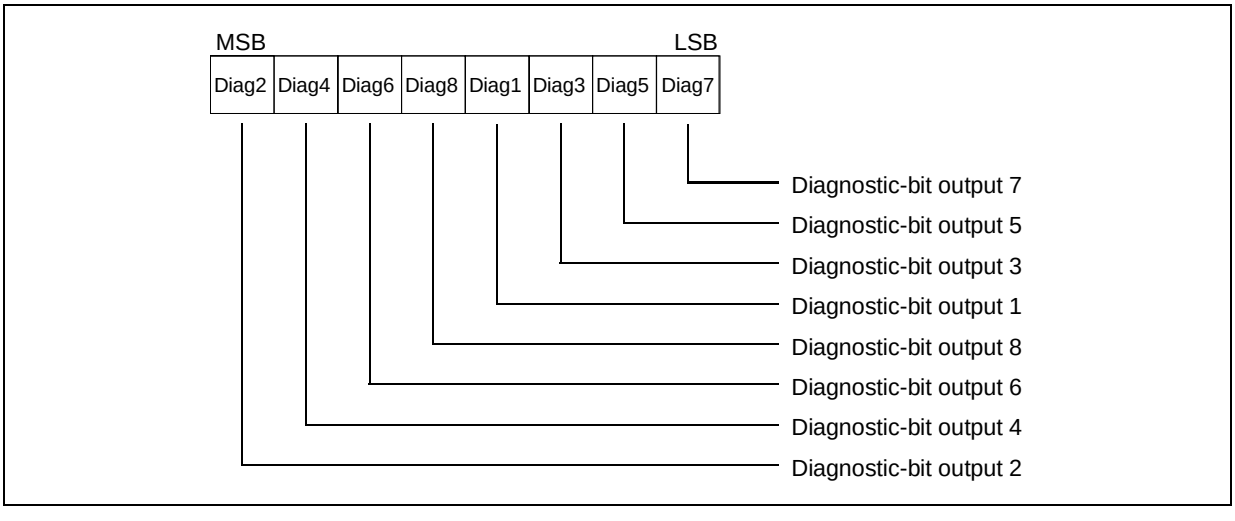
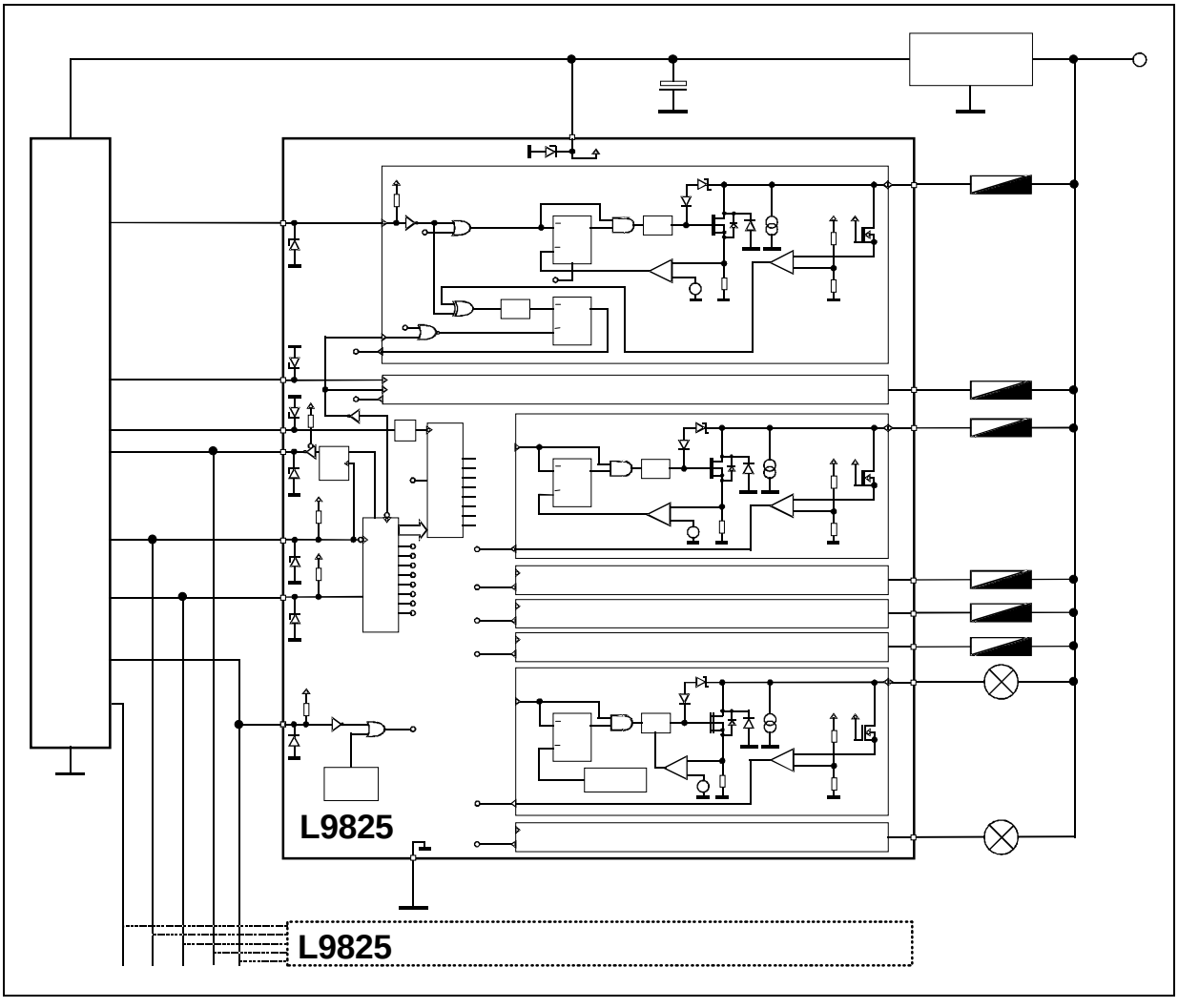


Figure 4. The Structure of the Outputs Status Register



APPLICATION NOTES

Figure 5. Typical Application Circuit Diagram



For higher current driving capability two outputs of the same kind can be paralleled. In this case the maximum flyback energy should not exceed the limit value for single output.

The immunity of the circuit with respect to the transients at the output is verified during the characterization for Test Pulses 1, 2 and 3a, 3b, DIN40839 or ISO7637 part 3. The Test Pulses are coupled to the outputs with 200pF series capacitor. All outputs withstand testpulses without damage.

The correct function of the circuit with the Test Pulses coupled to the outputs is verified during the characterization for the typical application with R = 16W to 200W, L= 0 to 600mH loads. The Test Pulses are coupled to the outputs with 200pF series capacitor.

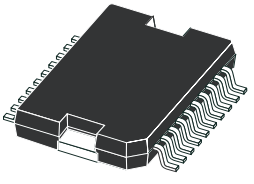
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1 (2)	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8˚(typ.)					
S	8˚(max.)					
T		10			0.394	

(1) “D and E1” do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006”)
- Critical dimensions: “E”, “G” and “a3”.

(2) For subcontractors, the limit is the one quoted in jedec MO-166

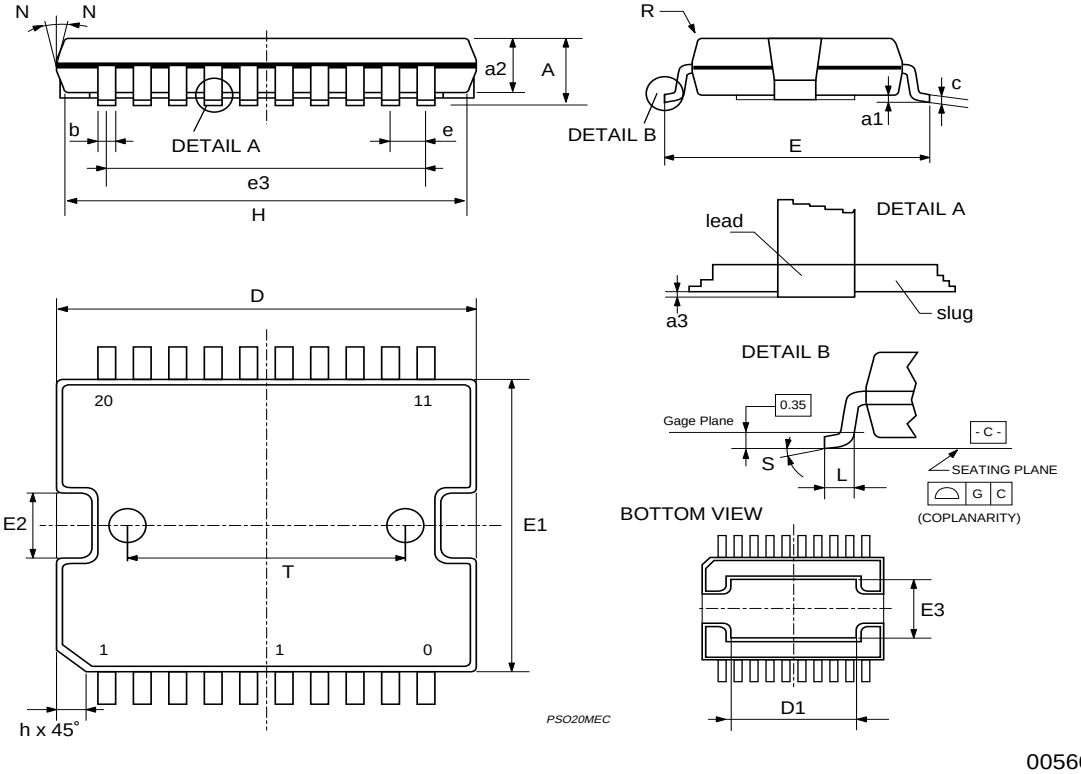
OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



JEDEC MO-166

PowerSO-20



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