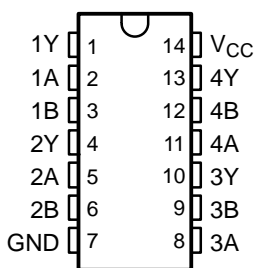


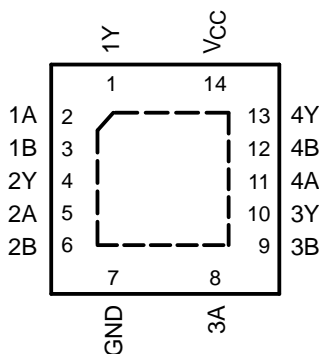
**FEATURES**

- Operate From 1.65 V to 3.6 V
- Specified From –40°C to 85°C, –40°C to 125°C, and –55°C to 125°C
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.4 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

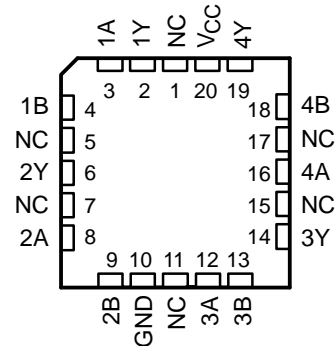
SN54LVC02A . . . J OR W PACKAGE  
SN74LVC02A . . . D, DB, NS, OR PW PACKAGE  
(TOP VIEW)



SN74LVC02A . . . RGY PACKAGE  
(TOP VIEW)



SN54LVC02A . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

**DESCRIPTION/ORDERING INFORMATION**

The SN54LVC02A quadruple 2-input positive-NOR gate is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC02A quadruple 2-input positive-NOR gate is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The 'LVC02A devices perform the Boolean function  $Y = \overline{A + B}$  or  $Y = \overline{A} \cdot \overline{B}$  in positive logic.

**ORDERING INFORMATION**

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC02ARGYR	LC02A
–40°C to 125°C	SOIC – D	Tube of 50	SN74LVC02AD	LVC02A
		Reel of 2500	SN74LVC02ADR	
		Reel of 250	SN74LVC02ADT	
	SOP – NS	Reel of 2000	SN74LVC02ANSR	LVC02A
	SSOP – DB	Reel of 2000	SN74LVC02ADBR	LC02A
	TSSOP – PW	Tube of 90	SN74LVC02APW	LC02A
Reel of 2000		SN74LVC02APWR		
Reel of 250		SN74LVC02APWT		
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC02AJ	SNJ54LVC02AJ
	CFP – W	Tube of 150	SNJ54LVC02AW	SNJ54LVC02AW
	LCCC – FK	Tube of 55	SNJ54LVC02AFK	SNJ54LVC02AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN54LVC02A, SN74LVC02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCAS280Q—JANUARY 1993—REVISED JULY 2005

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

**FUNCTION TABLE  
(EACH GATE)**

INPUTS		OUTPUT Y
A	B	
H	X	L
X	H	L
L	L	H

**LOGIC DIAGRAM, EACH GATE (POSITIVE LOGIC)**



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage range	-0.5	6.5	V	
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V	
$V_O$	Output voltage range <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V	
$I_{IK}$	Input clamp current	$V_I < 0$		-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50	mA
$I_O$	Continuous output current			±50	mA
	Continuous current through $V_{CC}$ or GND			±100	mA
$\theta_{JA}$	Package thermal impedance	D package <sup>(4)</sup>		86	°C/W
		DB package <sup>(4)</sup>		96	
		NS package <sup>(4)</sup>		76	
		PW package <sup>(4)</sup>		113	
		RGY package <sup>(5)</sup>		47	
$T_{stg}$	Storage temperature range	-65	150	°C	
$P_{tot}$	Power dissipation	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ <sup>(6)(7)</sup>		500	mW

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.
- (6) For the D package: above  $70^\circ\text{C}$ , the value of  $P_{tot}$  derates linearly with 8 mW/K.
- (7) For the DB, NS, and PW packages: above  $60^\circ\text{C}$ , the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

**Recommended Operating Conditions<sup>(1)</sup>**

			SN54LVC02A		UNIT
			–55°C to 125°C		
			MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	V
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7 V		–12	mA
		V <sub>CC</sub> = 3 V		–24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Recommended Operating Conditions<sup>(1)</sup>**

			SN74LVC02A						UNIT
			T <sub>A</sub> = 25°C		–40°C to 85°C		–40°C to 125°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		0.65 × V <sub>CC</sub>		0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		1.7		1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		2		2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>		0.35 × V <sub>CC</sub>		0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		0.7		0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8		0.8		0.8		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	0	5.5	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	–4		–4		–4		mA
		V <sub>CC</sub> = 2.3 V	–8		–8		–8		
		V <sub>CC</sub> = 2.7 V	–12		–12		–12		
		V <sub>CC</sub> = 3 V	–24		–24		–24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4		4		4		mA
		V <sub>CC</sub> = 2.3 V	8		8		8		
		V <sub>CC</sub> = 2.7 V	12		12		12		
		V <sub>CC</sub> = 3 V	24		24		24		

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LVC02A, SN74LVC02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCAS280Q–JANUARY 1993–REVISED JULY 2005

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	SN54LVC02A			UNIT
			–55°C to 125°C			
			MIN	TYP	MAX	
$V_{OH}$	$I_{OH} = -100 \mu A$	2.7 V to 3.6 V	$V_{CC} - 0.2$			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
	$I_{OH} = -24 \text{ mA}$	3 V	2.4			
$V_{OL}$	$I_{OL} = 100 \mu A$	2.7 V to 3.6 V	0.2			V
	$I_{OL} = 12 \text{ mA}$	2.7 V	0.4			
	$I_{OL} = 24 \text{ mA}$	3 V	0.55			
$I_I$	$V_I = 5.5 \text{ V}$ or GND	3.6 V	$\pm 5$			$\mu A$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	10			$\mu A$
$\Delta I_{CC}$	One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GND	2.7 V to 3.6 V	500			$\mu A$
$C_i$	$V_I = V_{CC}$ or GND	3.3 V	5 <sup>(1)</sup>			pF

(1)  $T_A = 25^\circ C$

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PAR-AMETER	TEST CONDITIONS	$V_{CC}$	SN74LVC02A						UNIT	
			$T_A = 25^\circ C$			–40°C to 85°C		–40°C to 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
$V_{OH}$	$I_{OH} = -100 \mu A$	1.65 V to 3.6 V	$V_{CC} - 0.2$			$V_{CC} - 0.2$		$V_{CC} - 0.3$		V
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.29			1.2		1.05		
	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			1.7		1.55		
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			2.2		2.05		
	$I_{OH} = -24 \text{ mA}$	3 V	2.4			2.4		2.25		
$V_{OL}$	$I_{OL} = 100 \mu A$	1.65 V to 3.6 V	0.1			0.2		0.3		V
	$I_{OL} = 4 \text{ mA}$	1.65 V	0.24			0.45		0.6		
	$I_{OL} = 8 \text{ mA}$	2.3 V	0.3			0.7		0.75		
	$I_{OL} = 12 \text{ mA}$	2.7 V	0.4			0.4		0.6		
	$I_{OL} = 24 \text{ mA}$	3 V	0.55			0.55		0.8		
$I_I$	$V_I = 5.5 \text{ V}$ or GND	3.6 V	$\pm 1$			$\pm 5$		$\pm 20$		$\mu A$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	1			10		40		$\mu A$
$\Delta I_{CC}$	One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GND	2.7 V to 3.6 V	500			500		5000		$\mu A$
$C_i$	$V_I = V_{CC}$ or GND	3.3 V	5							pF

### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN54LVC02A		UNIT
				–55°C to 125°C		
				MIN	MAX	
t <sub>pd</sub>	A or B	Y	2.7 V	5.4		ns
			3.3 V ± 0.3 V	1	4.4	

### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

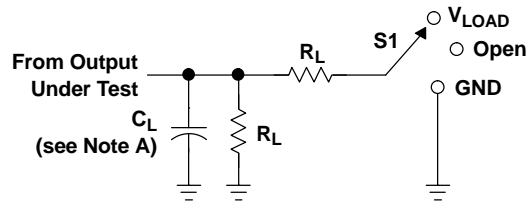
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN74LVC02A						UNIT	
				T <sub>A</sub> = 25°C			–40°C to 85°C		–40°C to 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN		MAX
t <sub>pd</sub>	A or B	Y	1.8 V ± 0.15 V	1	3.8	8.4	1	8.9	1	10.4	ns
			2.5 V ± 0.2 V	1	2.9	6.9	1	7.4	1	9.5	
			2.7 V	1	3	5.2	1	5.4	1	7	
			3.3 V ± 0.3 V	1	3.6	4.2	1	4.4	1	5.5	
t <sub>sk(o)</sub>			3.3 V ± 0.3 V				1		1.5	ns	

### Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per gate	f = 10 MHz	1.8 V	7.5	pF
			2.5 V	8.5	
			3.3 V	9.5	

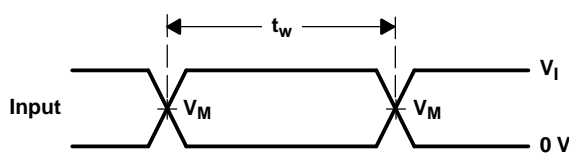
PARAMETER MEASUREMENT INFORMATION



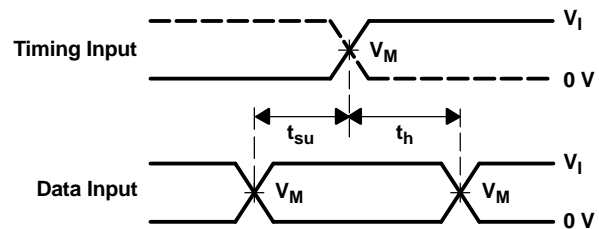
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

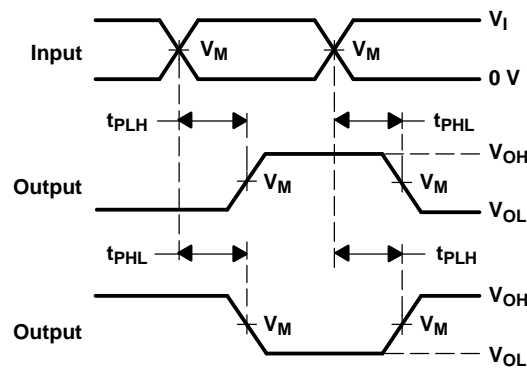
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



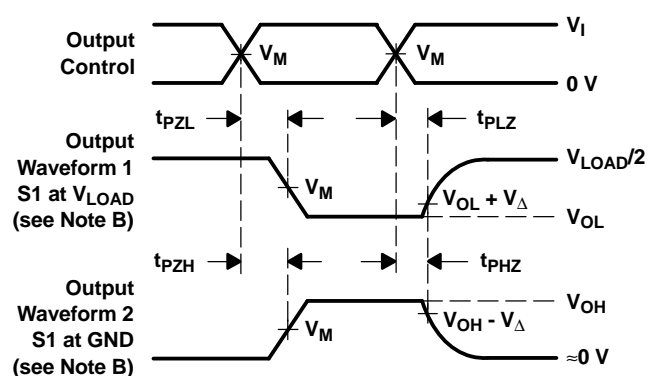
VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9760401Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9760401Q2A SNJ54LVC 02AFK	<a href="#">Samples</a>
5962-9760401QCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760401QC A SNJ54LVC02AJ	<a href="#">Samples</a>
5962-9760401QDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760401QD A SNJ54LVC02AW	<a href="#">Samples</a>
SN74LVC02AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02A	<a href="#">Samples</a>
SN74LVC02ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02A	<a href="#">Samples</a>
SN74LVC02ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02A	<a href="#">Samples</a>
SN74LVC02ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02A	<a href="#">Samples</a>
SN74LVC02ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02A	<a href="#">Samples</a>
SN74LVC02APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02A	<a href="#">Samples</a>
SN74LVC02APWE4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02A	<a href="#">Samples</a>
SN74LVC02APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02A	<a href="#">Samples</a>
SN74LVC02APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02A	<a href="#">Samples</a>
SN74LVC02ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC02A	<a href="#">Samples</a>
SNJ54LVC02AFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9760401Q2A SNJ54LVC 02AFK	<a href="#">Samples</a>
SNJ54LVC02AJ	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760401QC A SNJ54LVC02AJ	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LVC02AW	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760401QD A SNJ54LVC02AW	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54LVC02A, SN74LVC02A :**



- Catalog : [SN74LVC02A](#)
- Automotive : [SN74LVC02A-Q1](#), [SN74LVC02A-Q1](#)
- Enhanced Product : [SN74LVC02A-EP](#), [SN74LVC02A-EP](#)
- Military : [SN54LVC02A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC02ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC02ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC02ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC02APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC02APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC02ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC02ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVC02ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LVC02ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LVC02APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC02APWT	TSSOP	PW	14	250	356.0	356.0	35.0
SN74LVC02ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

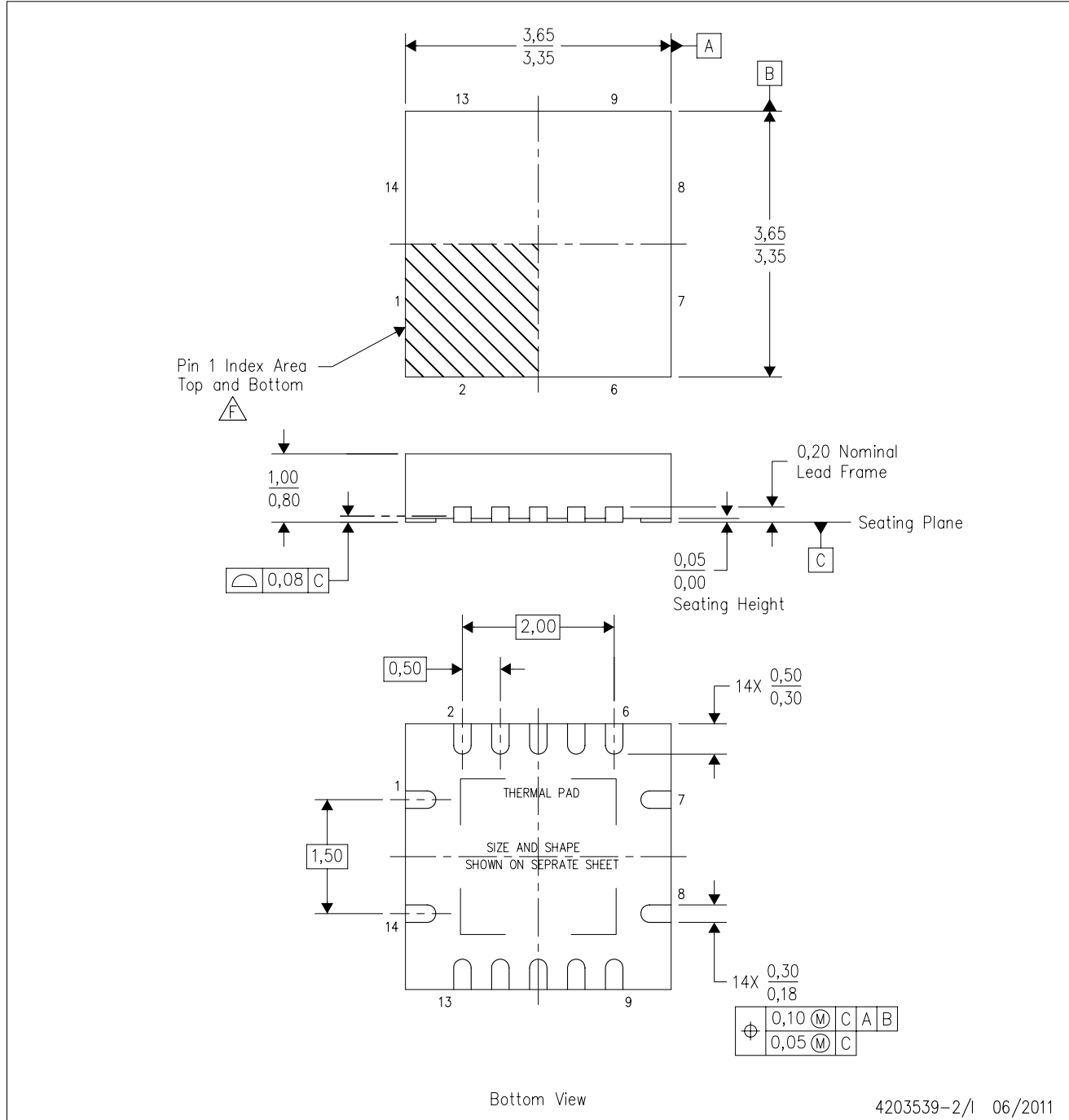
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9760401Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9760401QDA	W	CFP	14	1	506.98	26.16	6220	NA
SN74LVC02AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC02APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC02APWE4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC02AFK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54LVC02AW	W	CFP	14	1	506.98	26.16	6220	NA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

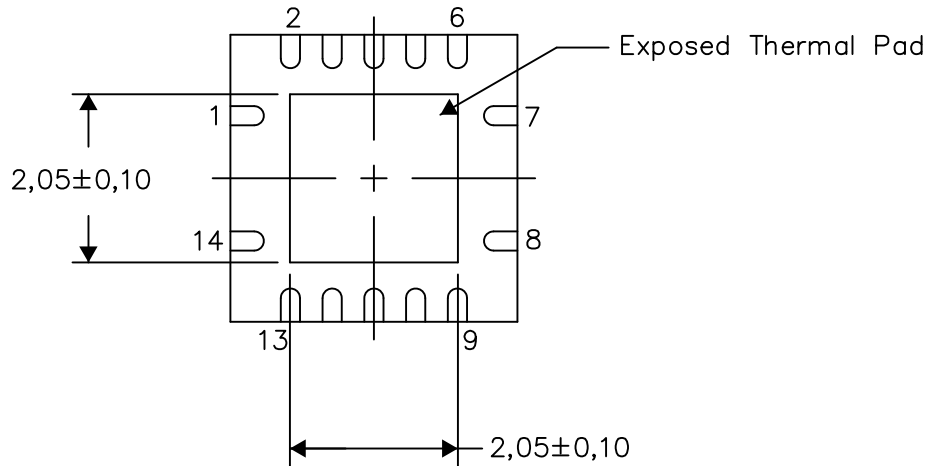
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

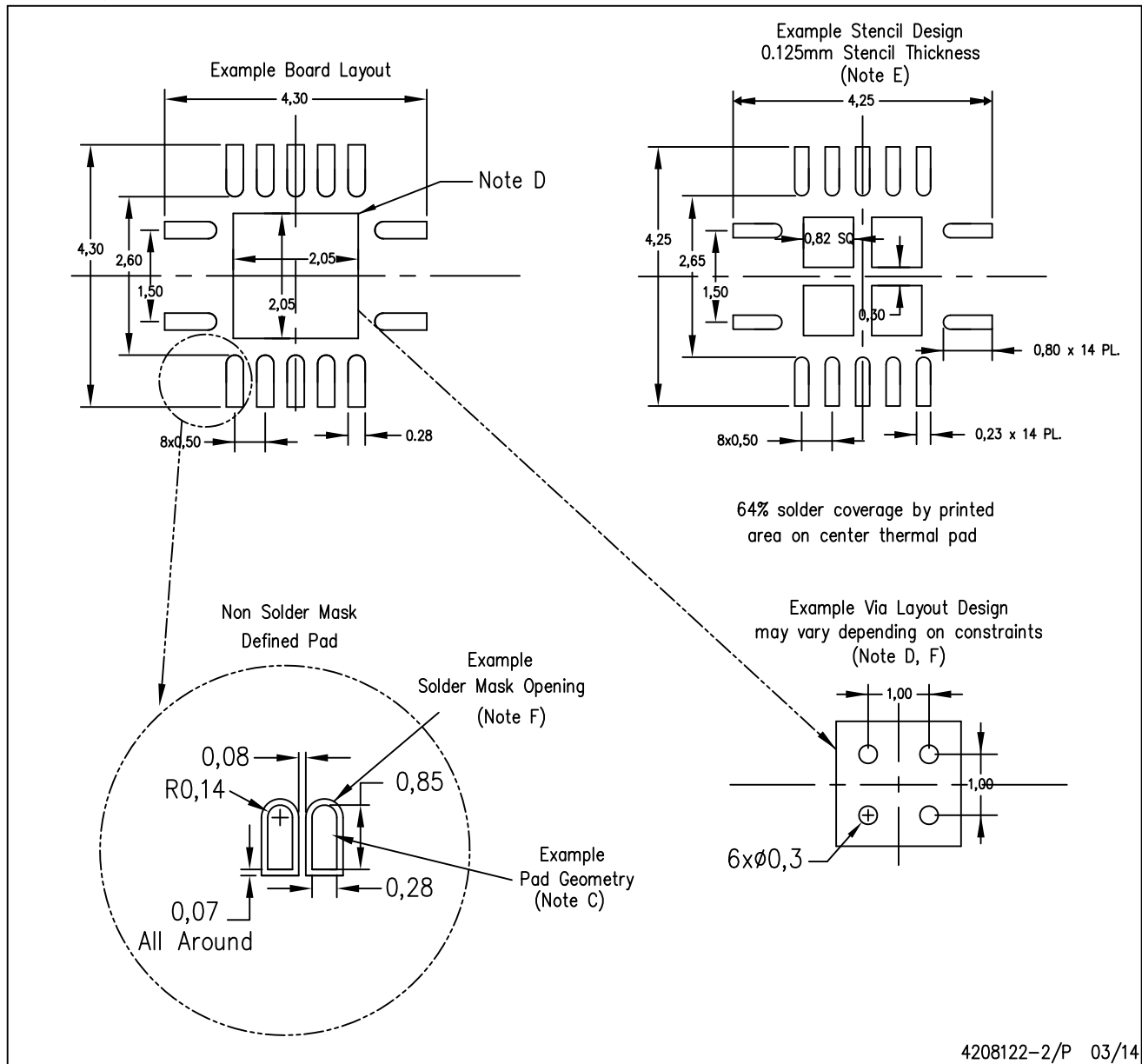
Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F14

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G



J0014A

# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



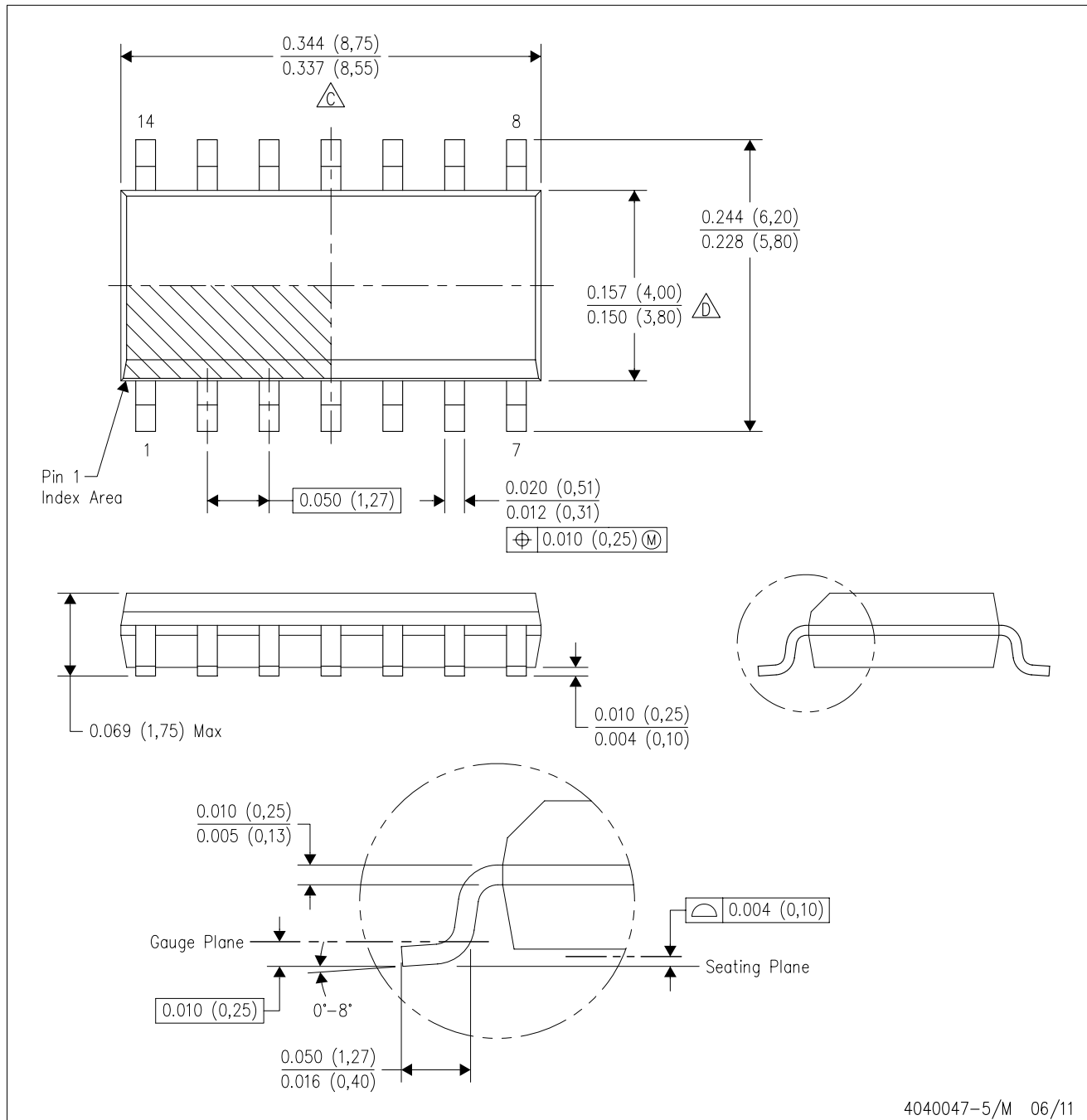
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X





4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

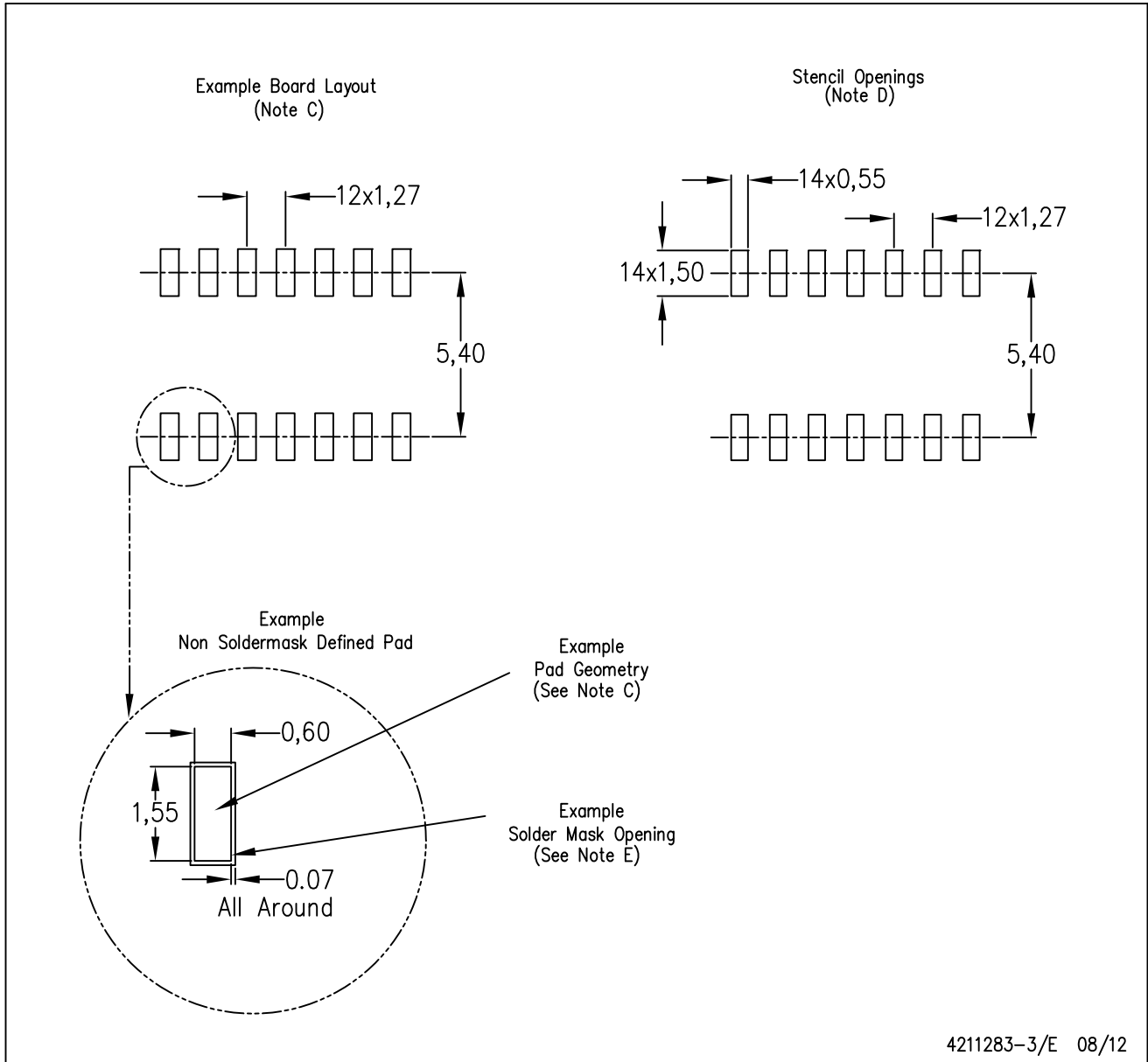


4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

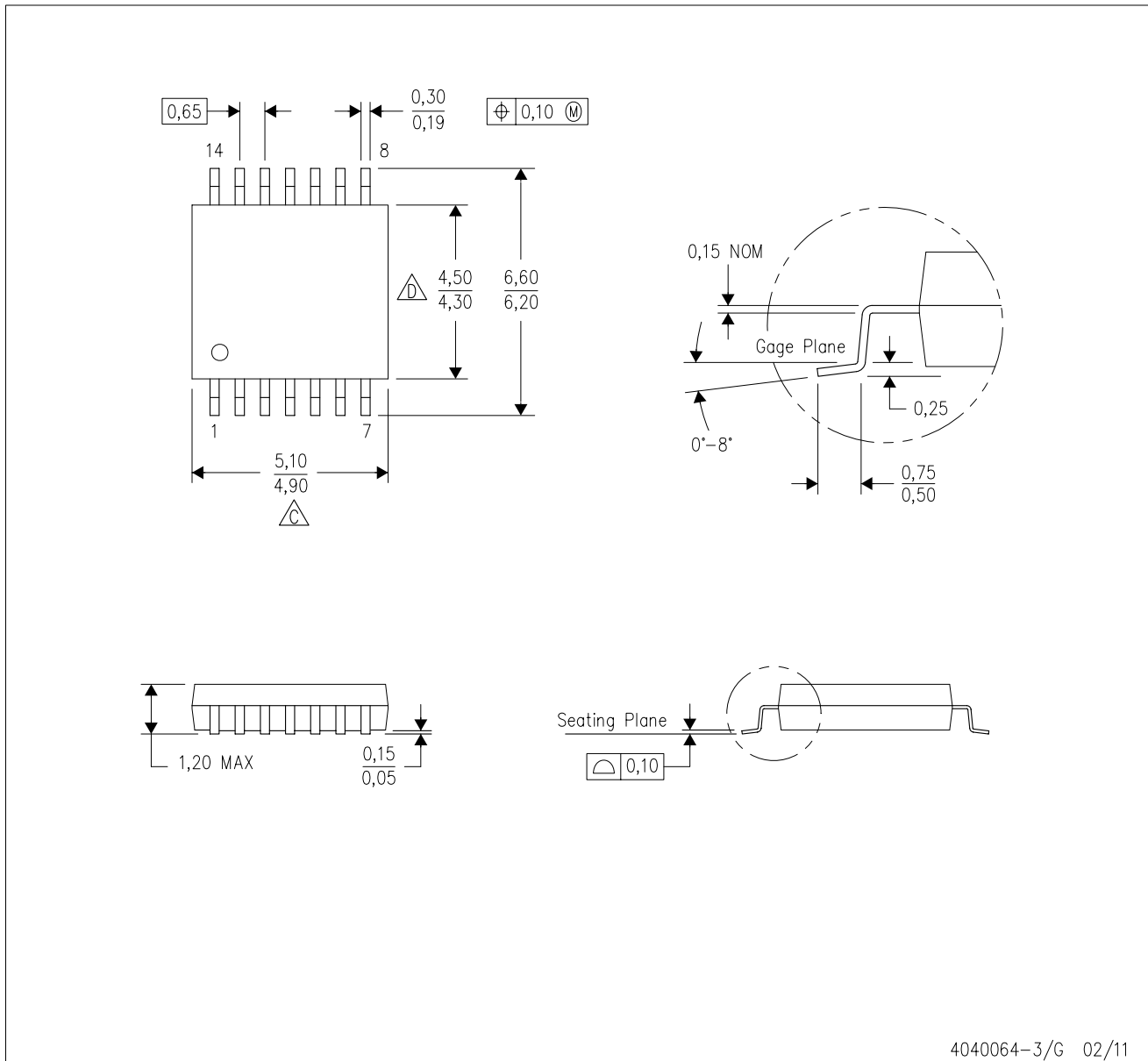


4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

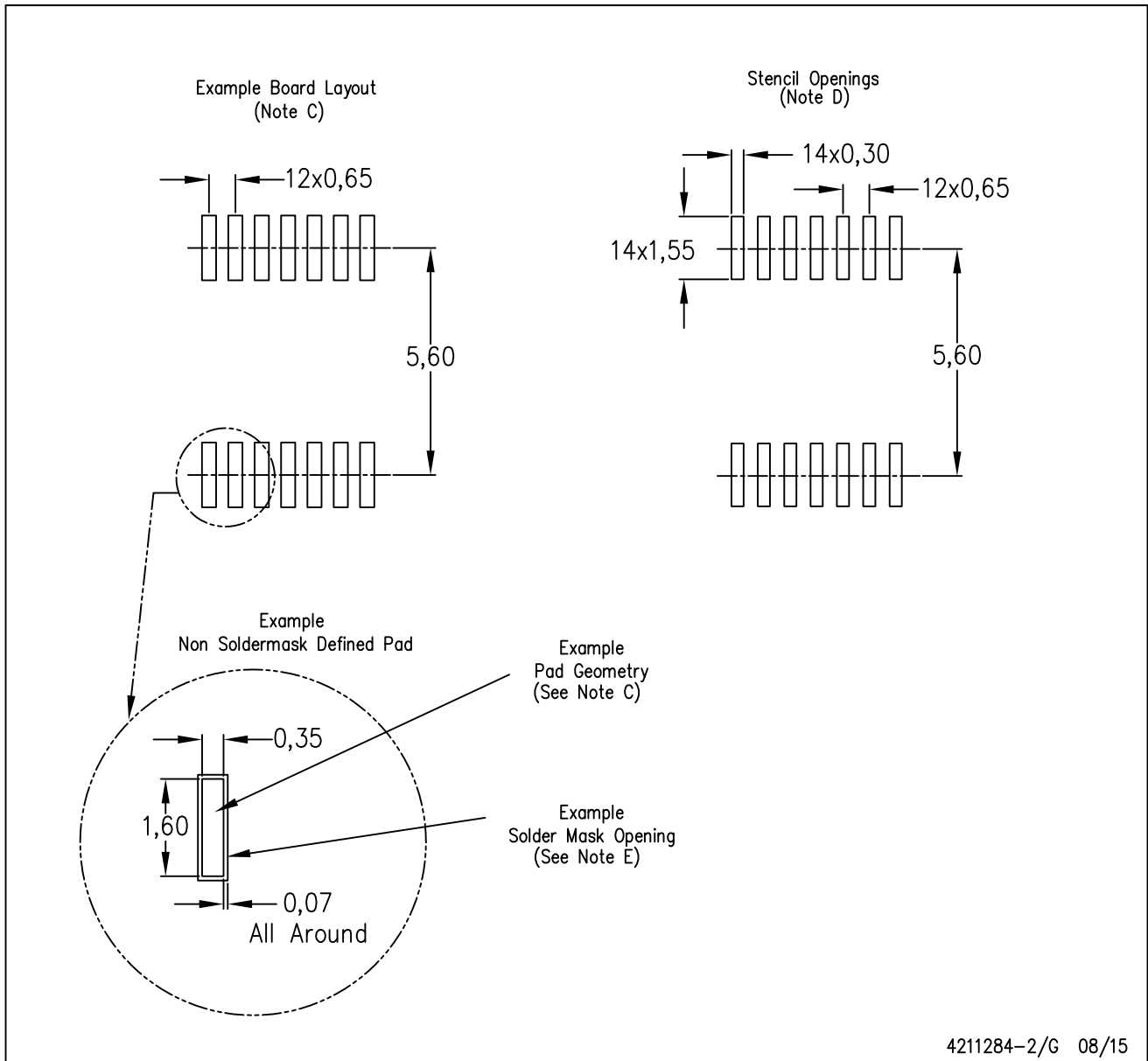


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

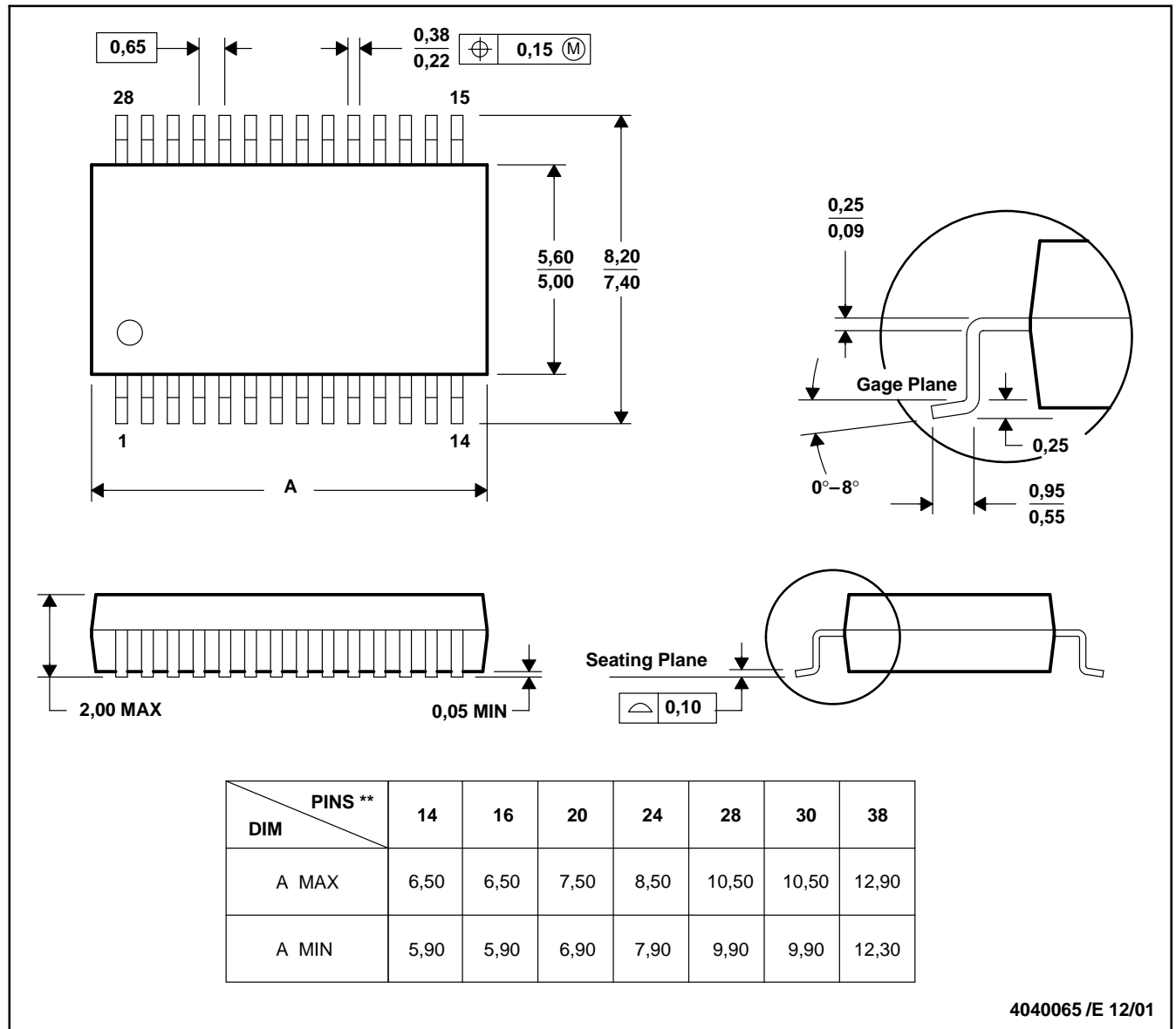


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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