Apacer

RoHS Recast Compliant

Industrial microSD 5.0

CH210-MSD Product Specifications

(WD TLC BiCS4 96 Layers)

October 14, 2022

Version 1.2

Apacer Technology Inc.
1F, No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City, Taiwan, R.O.C
Tel: +886-2-2267-8000 Fax: +886-2-2267-2261
www.apacer.com

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Specifications Overview:

- **Fully Compatible with SD Card Association Specifications**
  - Physical Layer Specification Ver6.1
  - Security Specification Ver5.0
- **Capacity**
  - 16, 32, 64 GB
- **Performance**[1]
  - Sequential read: Up to 90 MB/sec
  - Sequential write: Up to 70 MB/sec
  - Random read (4K): Up to 1,300 IOPS
  - Random write (4K): Up to 300 IOPS
- **Flash Management**
  - Built-in advanced ECC algorithm
  - Global Wear Leveling
  - Flash bad-block management
  - Power Failure Management
  - Flash Translation Layer: Page Mapping
  - S.M.A.R.T.
  - SMART Read Refresh™
  - SLC-liteX
- **NAND Flash Type:** WD TLC BiCS4 96 Layers
- **SD-Protocol Compatible**
- **Supports SD SPI Mode**
- **Backward Compatible with 3.0 and 2.0**
- **Endurance (in Terabytes Written: TBW)**
  - 16 GB: 195 TBW
  - 32 GB: 382 TBW
  - 64 GB: 713 TBW
- **Temperature Range**
  - Operating: -25°C to 85°C
  - Storage: -40°C to 85°C
- **Operating Voltage: 2.7V ~ 3.6V**
- **Power Consumption**[1]
  - Operating: 70 mA
  - Standby: 260 µA
- **Bus Speed Mode:** Supports Class 10 with U3 and UHS-I[2]
  - SDR12: SDR up to 25MHz 1.8V signaling
  - SDR25: SDR up to 50MHz 1.8V signaling
  - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
  - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
  - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec
- **Physical Dimensions**
  - 15mm (L) x 11mm (W) x 1mm (H)
- **Supports Video Speed Class: V30**
- **RoHS Recast Compliant**

Notes:
1. Varies from capacities. Performance values presented here are typical and measured based on USB 3.0 card reader. The results may vary depending on settings and platforms.
2. Timing in 1.8V signaling is different from that of 3.3V signaling. Operation mode selection command is complaint with SD 3.0, referring to SDA's Part 1, Physical Layer Specification, Ver 3.01 (Section 3.9).

Table of Contents

1. General Description

Apacer microSD CH210-MSD is compatible with the microSD card version 5.0. The command list supports [Physical Layer Specification Ver6.10 Final] definitions. Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver5.0 Final] Specifications.

The microSD 5.0 card comes with 8-pin interface. It can alternate communication protocols between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption. It supports capacity up to 64GB with exFAT SDXC.

Apacer microSD CH210-MSD Secure Digital 5.0 with high performance, good reliability and wide compatibility is nowadays one of the most popular cards with customized firmware techniques in semi-industrial/medical markets already.

1.1 Functional Block

The microSD contains a card controller and a memory core for the SD standard interface.

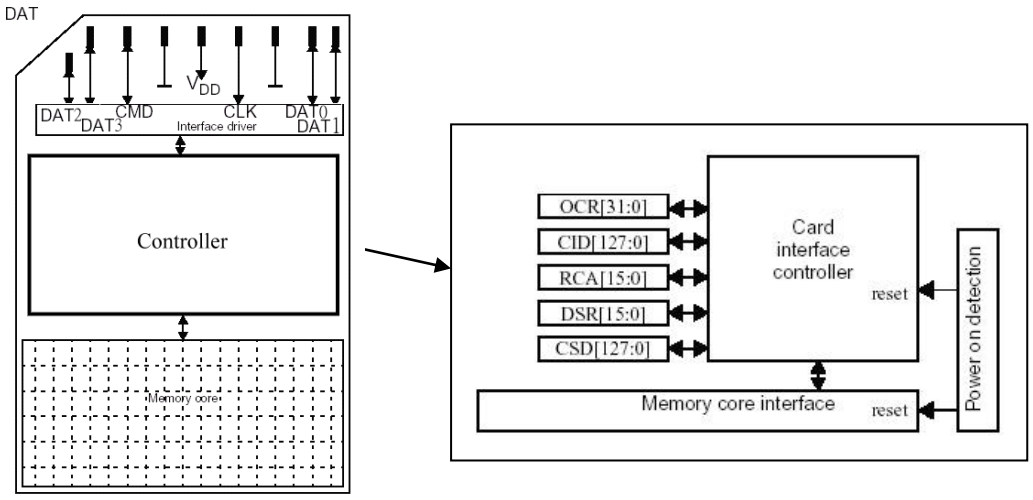


Figure 1-1 Functional Block Diagram

1.2 Flash Management

1.2.1 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Apacer implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.2.2 Powerful ECC Algorithms

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. To protect data from corruption, the microSD card whose controller supports up to 120bits ECC circuits applies the advanced ECC Algorithm that can detect and correct errors occur during read process.

1.2.3 Global Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Global Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing writes and erase cycles across the media.

Apacer provides Global Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing Global Wear Leveling algorithm, the life expectancy of the NAND Flash is greatly improved.

1.2.4. Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the microSD card, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

1.2.5 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. Apacer provides a program named SmartInfo Tool to observe Apacer’s SD and microSD cards. Note that this tool can only support Apacer’s industrial SD and microSD cards. This tool will display firmware version, endurance life ratio, good block ratio, and so forth.

1.2.6 SMART Read Refresh™

Apacer’s SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

1.2.7 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve microSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

1.2.8 SLC-liteX

SLC-liteX is based on 3D NAND technology. The firmware is carefully tweaked by our engineering team so as to offer the greatest number of P/E cycles in this format – 30,000, which is 10 times more than MLC or industrial 3D TLC. The longest lifespans are therefore available at reasonable cost.

2. Product Specifications

2.1 Card Architecture

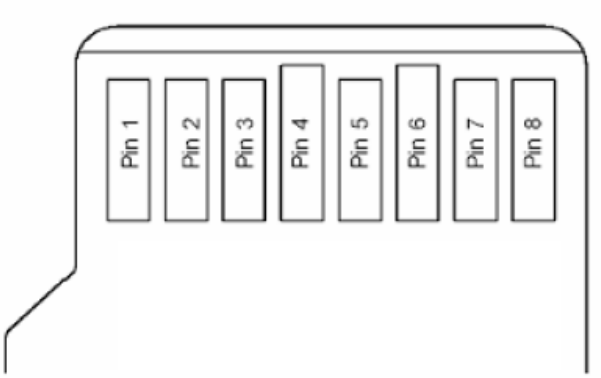


Figure 2-1 Card Architecture

2.2 Pin Assignment

Table 2-1 Pin Descriptions

Pin	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	DAT2	Data line[bit 2]	Reserved	
2	CD/DAT3	Card Detect/Data line [bit 3]	CS	Chip select
3	CMD	Command/Response	DI	Data in
4	VDD	Supply voltage	VDD	Supply voltage
5	CLK	Clock	SCLK	Clock
6	VSS	Supply voltage ground	VSS	Supply voltage ground
7	DAT0	Data line[bit 0]	DO	Data out
8	DAT1	Data line[bit 1]	Reserved	

2.3 Capacity

The following table shows the specific capacity for the SD 5.0 card.

Table 2-2 Capacity Specifications

Capacity	Total bytes
16 GB	16,009,658,368
32 GB	32,099,975,744
64 GB	64,183,336,960

Note: Total bytes are viewed under Windows operating system and were measured by SD format too.

2.4 Performance

Performances of the SD 5.0 card are shown in the table below.

Table 2-3 Performance Specifications

Capacity / Performance	16 GB	32 GB	64 GB
Sequential Read (MB/s)	85	90	90
Sequential Write (MB/s)	48	70	70
Random Read IOPS (4K)	1,300	1,300	1,200
Random Write IOPS (4K)	200	300	200

Notes:
- Results may differ from various flash configurations or host system setting.
- Sequential read/write is based on CrystalDiskMark 5.2.1 with file size 1,000MB.
- Random read/write is measured using IOMeter with Queue Depth 32.
- Performance results are measured based on USB 3.0 card reader.

2.5 Electrical

Table 2-4 Operating Voltages

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Power Supply Voltage	2.7	3.6	V

Table 2-5 Power Consumption

Capacity / Mode	16 GB	32 GB	64 GB
Operating (mA)	70	70	70
Standby (µA)	245	230	260

Notes:
- All values are typical and may vary depending on flash configurations or host system settings.
- Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.
- Power is measured based on USB 3.0 card reader.

2.6 Endurance

The endurance of a storage device is predicted by TeraBytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 2-6 Endurance Specifications

Capacity	TeraBytes Written
16 GB	195
32 GB	382
64 GB	713

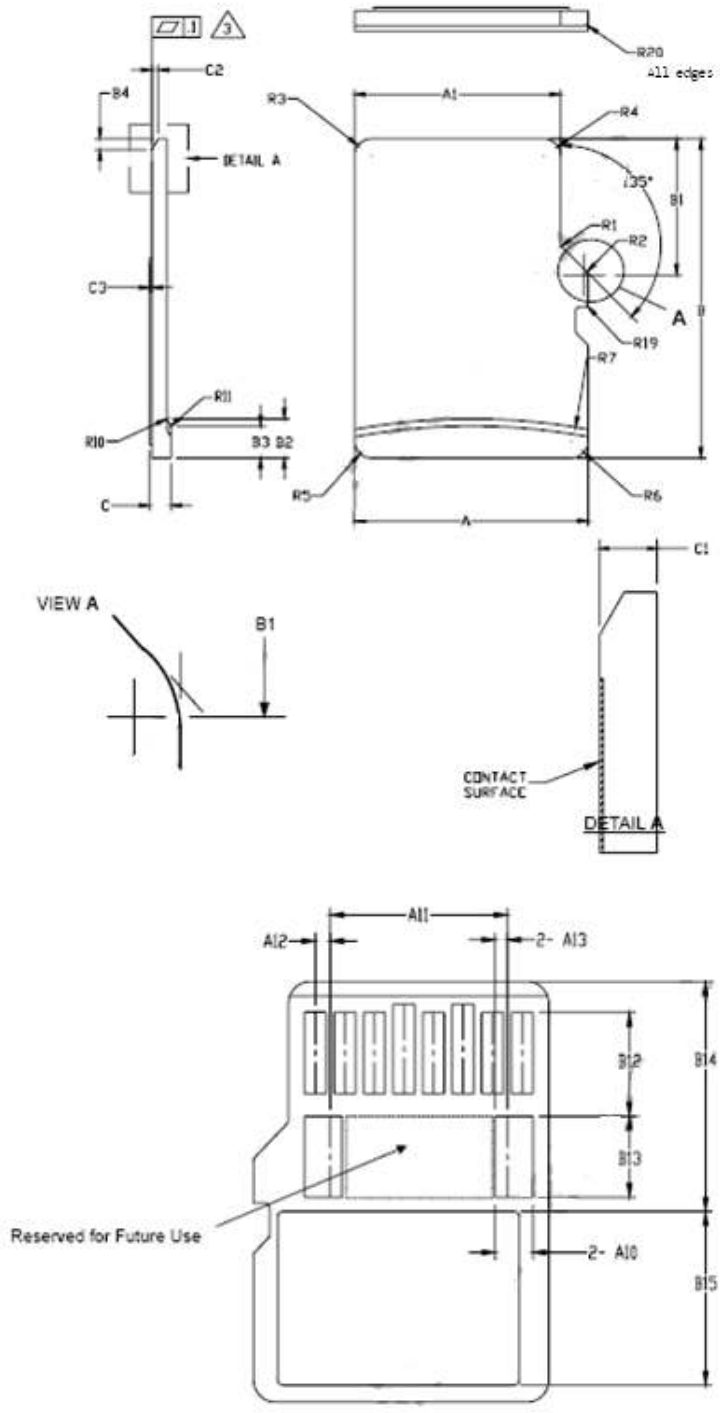
Notes:

- Flash vendor guaranteed 3D SLC-liteX P/E cycle: 30K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1024 GB

3. Physical Characteristics

3.1 Physical Dimensions

Dimensions: 15mm (L) x 11mm (W) x 1mm (H)



	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

Figure 3-1 Physical Dimensions

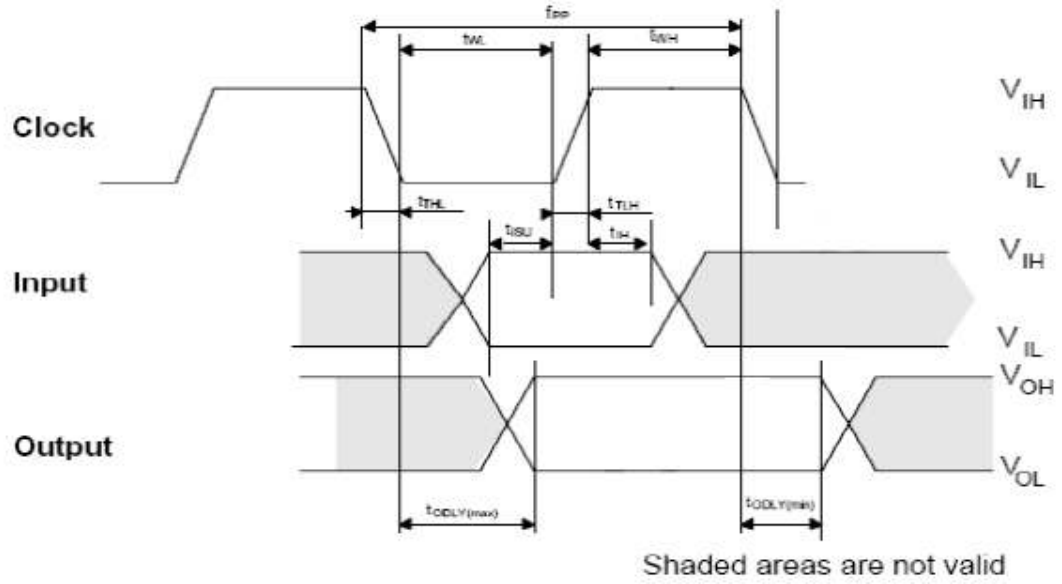
3.2 Durability Specifications

Table 3-1 Durability Specifications

Item	Specifications
Temperature	Operating: -25°C to 85°C Storage:-40°C to 85°C
Shock	1,500G, 0.5ms
Vibration	20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop	150cm free fall, 6 face of each
Bending	≧10N, hold 1min/5times
Torque	0.1N-m or 2.5deg, hold 5min/5times
Salt Spray	Concentration: 3% NaCl at 35°C (storage for 24 hours)
Waterproof	JIS IPX7 compliance Water temperature 25°C Water depth: the lowest point of unit is locating 1000mm below surface (storage for 30 mins)
X-Ray Exposure	0.1 Gy of medium-energy radiation (70 KeV to 140 KeV, cumulative dose per year) to both sides of the card (storage for 30 mins)
Durability	10,000 times mating cycle
ESD	Pass

4. AC Characteristics

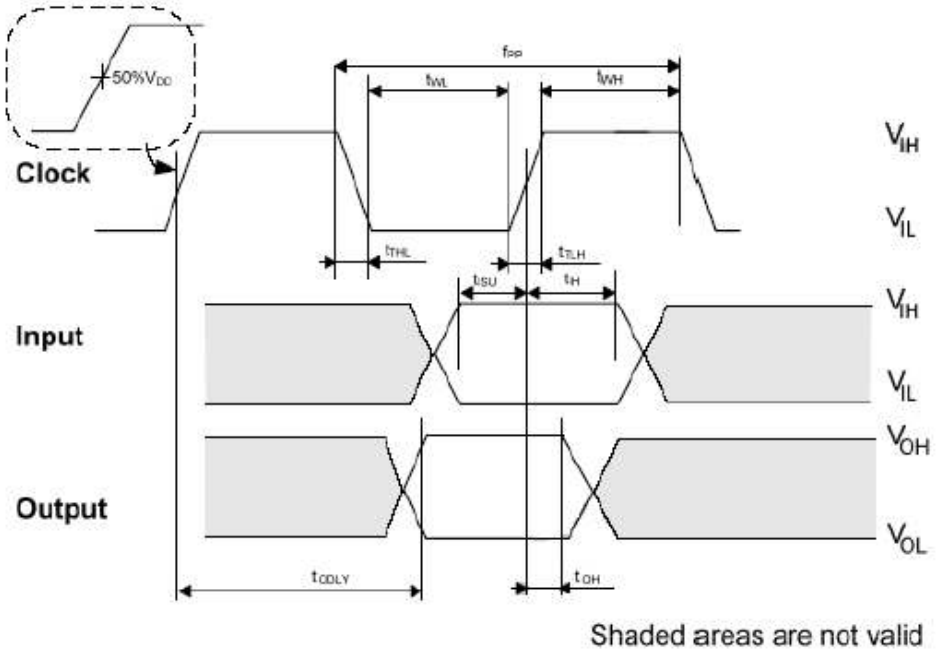
4.1 microSD Interface Timing (Default)



Symbol	Parameter	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency Data Transfer Mode	0	25	MHz	C_{card} ≤ 10 pF (1 card)
f_{OD}	Clock frequency Identification Mode	0*/100	400	kHz	C_{card} ≤ 10 pF (1 card)
t_{WL}	Clock low time	10		ns	C_{card} ≤ 10 pF (1 card)
t_{WH}	Clock high time	10		ns	C_{card} ≤ 10 pF (1 card)
t_{TLH}	Clock rise time		10	ns	C_{card} ≤ 10 pF (1 card)
t_{THL}	Clock fall time		10	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
t_{ISU}	Input setup time	5		ns	C_{card} ≤ 10 pF (1 card)
t_{IH}	Input hold time	5		ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
t_{ODLY}	Output Delay time during Data Transfer Mode	0	14	ns	C_L ≤ 40 pF (1 card)
t_{ODLY}	Output Delay time during Identification Mode	0	50	ns	C_L ≤ 40 pF (1 card)

*0Hz means to stop the clock. The given minimum frequency range is for cases that require the clock to be continued.

4.2 microSD Interface Timing (High-Speed Mode)

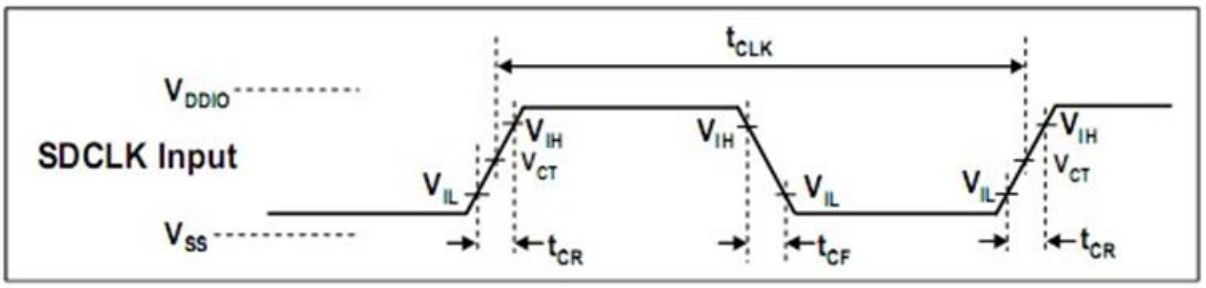


Symbol	Parameter	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency Data Transfer Mode	0	50	MHz	C_{card} ≤ 10 pF (1 card)
t_{WL}	Clock low time	7		ns	C_{card} ≤ 10 pF (1 card)
t_{WH}	Clock high time	7		ns	C_{card} ≤ 10 pF (1 card)
t_{TLH}	Clock rise time		3	ns	C_{card} ≤ 10 pF (1 card)
t_{THL}	Clock fall time		3	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
t_{ISU}	Input setup time	6		ns	C_{card} ≤ 10 pF (1 card)
t_{IH}	Input hold time	2		ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
t_{ODLY}	Output Delay time during Data Transfer Mode		14	ns	C_L ≤ 40 pF (1 card)
T_{OH}	Output Hold Time	2.5		ns	C_L ≤ 15 pF (1 card)
C_L	Total System capacitance of each line*		40	pF	C_L ≤ 15 pF (1 card)

*In order to satisfy severe timing, host shall run on only one card

4.3 microSD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes)

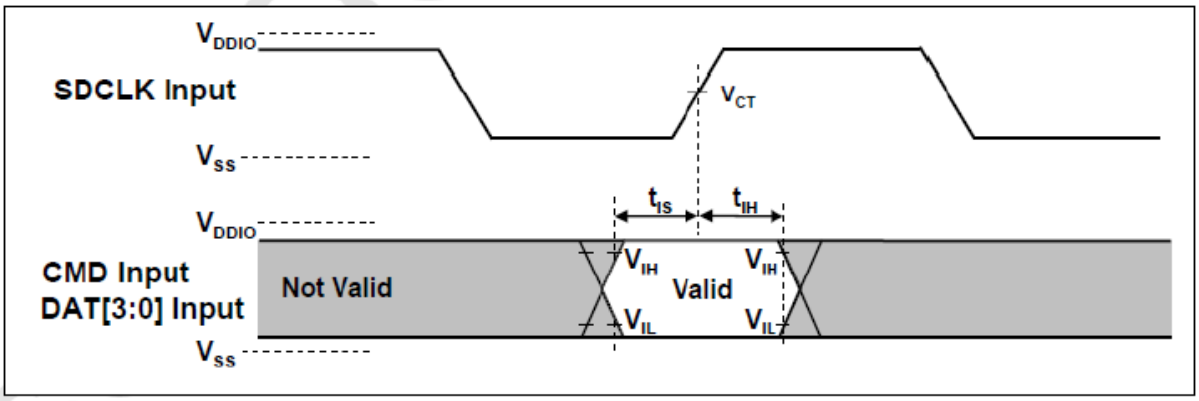
4.3.1 Input



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT} = 0.975V
t_{CR}, t_{CF}	-	0.2 t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

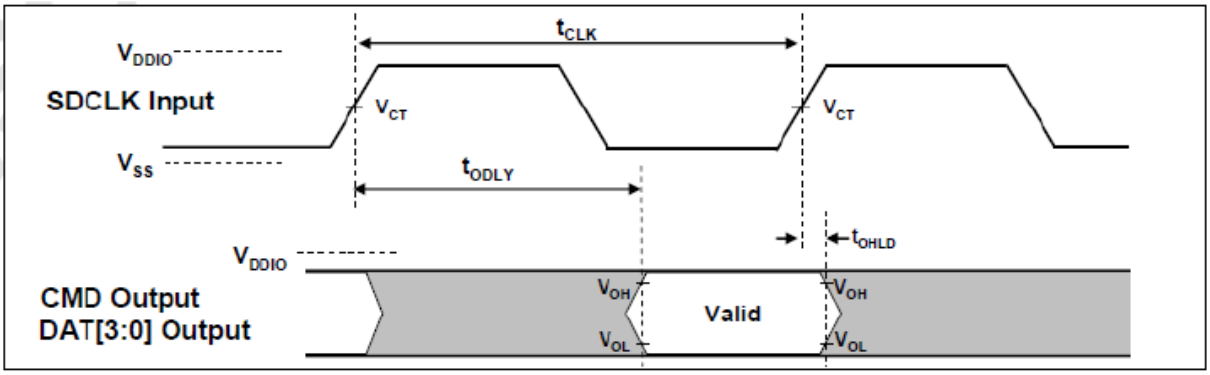
SDR50 and SDR104 Input Timing



Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.8	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.8	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

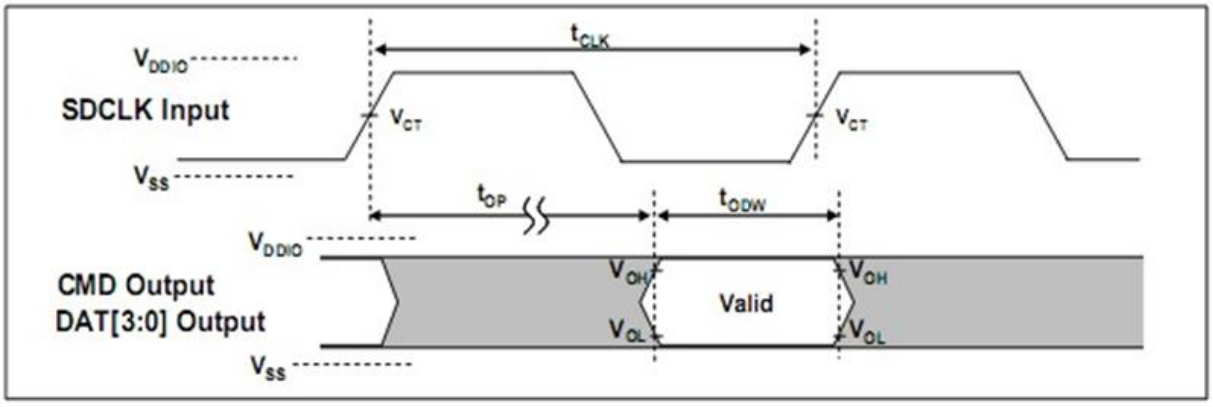
4.3.2 Output



Output Timing of Fixed Data Window

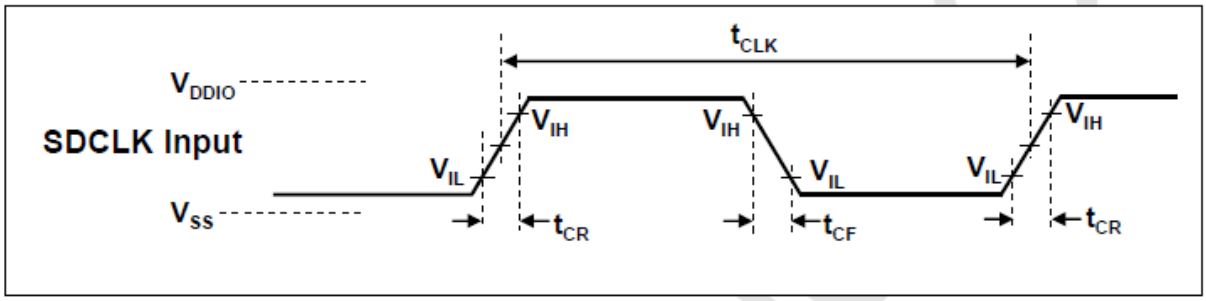
Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK} ≥10.0ns, C_L=30pF, using driver Type B, for SDR50.
t_{ODLY}	-	14	ns	t_{CLK} ≥20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). C_L=15pF

Output (SDR104 mode)



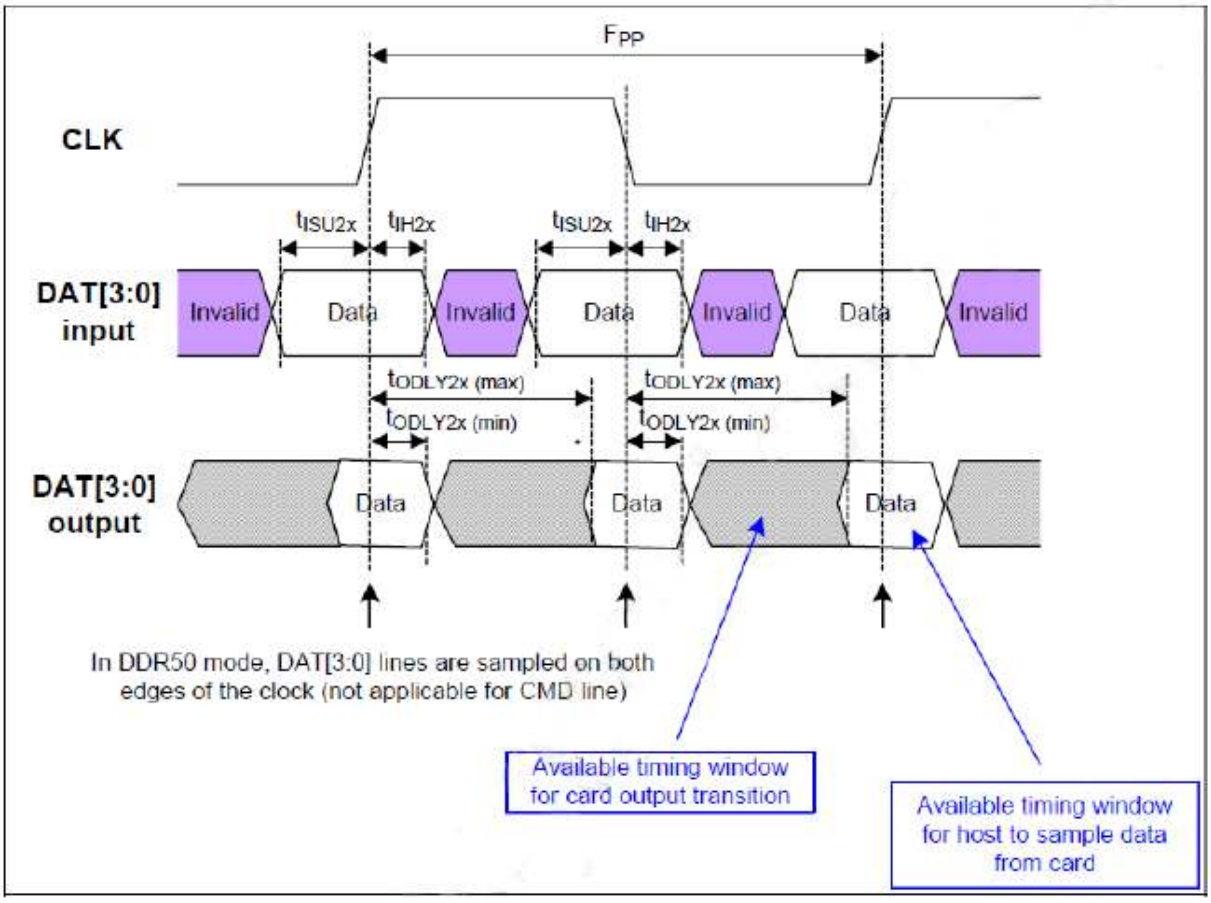
Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

4.4 microSD Interface Timing (DDR50 Mode)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2 t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameter	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
t_{ISU}	Input setup time	3	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{IH}	Input hold time	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Output CMD (referenced to CLK rising edge)					
t_{ODLY}	Output Delay time during Data Transfer Mode	-	13.7	ns	$C_L \leq 30$ pF (1 card)
T_{OH}	Output Hold time	1.5	-	ns	$C_L \geq 15$ pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
t_{ISU2x}	Input setup time	3	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{IH2x}	Input hold time	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
t_{ODLY2x}	Output Delay time during Data Transfer Mode	-	7.0	ns	$C_L \leq 25$ pF (1 card)
T_{OH2x}	Output Hold time	1.5	-	ns	$C_L \geq 15$ pF (1 card)

5. Product Ordering Information

5.1 Product Code Designations

Apacer's CH210-MSD is available in different configurations and densities. See the chart below for a comprehensive list of options for the CH210-MSD series devices.

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	A	K	6	.	8	4	8	X	S	A	.	0	0	1	0	1

Code 1-3 (Product Line & Form Factor)	CH210-MSD
Code 5-6 (Model/Solution)	CH210
Code 7-8 (Product Capacity)	8G: 16GB 8H: 32GB 8J: 64GB
Code 9 (Flash Type & Product Temp)	3D SLC-liteX Standard Temperature
Code 10 (Product Spec)	microSD Card
Code 12-14 (Version Number)	Random numbers generated by system
Code 15-16 (Firmware Version)	Firmware page mode

5.2 Valid Combinations

The following table lists the available models of the CH210-MSD series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Capacity	Valid Combination
16GB	AK6.848GSA.00101
32GB	AK6.848HSA.00101
64GB	AK6.848JSA.00101

Revision History

Revision	Description	Date
1.0	Initial release	6/9/2021
1.1	Modified model name error at 5.1 Product Code Designations	7/9/2021
1.2	Modified t_{ISU} min for Input CMD at the Bus Timings – Parameters Values (DDR50 Mode) table	10/14/2022

Global Presence

Taiwan (Headquarters)
Apacer Technology Inc.
1F., No.32, Zhongcheng Rd., Tucheng Dist.,
New Taipei City 236, Taiwan R.O.C.
Tel: 886-2-2267-8000
Fax: 886-2-2267-2261
amtsales@apacer.com

U.S.A.
Apacer Memory America, Inc.
46732 Lakeview Blvd., Fremont, CA 94538
Tel: 1-408-518-8699
Fax: 1-510-249-9551
sa@apacerus.com

Japan
Apacer Technology Corp.
6F, Daiyontamachi Bldg., 2-17-12, Shibaura, Minato-Ku,
Tokyo, 108-0023, Japan
Tel: 81-3-5419-2668
Fax: 81-3-5419-0018
jpservices@apacer.com

Europe
Apacer Technology B.V.
Science Park Eindhoven 5051 5692 EB Son,
The Netherlands
Tel: 31-40-267-0000
Fax: 31-40-290-0686
sales@apacer.nl

China
Apacer Electronic (Shanghai) Co., Ltd
Room D, 22/FL, No.2, Lane 600, JieyunPlaza,
Tianshan RD, Shanghai, 200051, China
Tel: 86-21-6228-9939
Fax: 86-21-6228-9936
sales@apacer.com.cn

India
Apacer Technologies Pvt Ltd,
1874, South End C Cross, 9th Block Jayanagar,
Bangalore-560069, India
Tel: 91-80-4152-9061/62
Fax: 91-80-4170-0215
sales_india@apacer.com