



# PSMN045-100HL

N-channel 100 V, 45 mOhm, logic level MOSFET in LPAK56D using TrenchMOS technology

26 September 2022

Product data sheet

## 1. General description

Dual logic level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology.

## 2. Features and benefits

- High peak drain current  $I_{DM}$
- Copper clip and flexible Leads
- High operating junction temperature  $T_j = 175\text{ °C}$
- Superior reliability
- Low body diode reverse recovery charge  $Q_r$

## 3. Applications

- Synchronous rectifier
- Forward and flyback converter
- Industrial drive
- Power management system
- Uninterruptible Power Supply (UPS)

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$V_{GS} = 5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	21	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	53	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics FET1 and FET2</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a>	-	38.3	45	mΩ
		$V_{GS} = 5\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 175\text{ °C}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	103	124	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 5\text{ A}$ ; $V_{DS} = 80\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	7.3	-	nC
$Q_{G(tot)}$	total gate charge		-	18.5	-	nC
<b>Avalanche ruggedness FET1 and FET2</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 21\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; <a href="#">Fig. 4</a>	[1] [2]	-	48	mJ

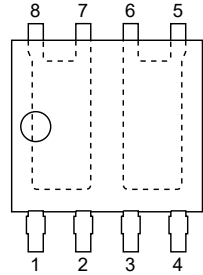
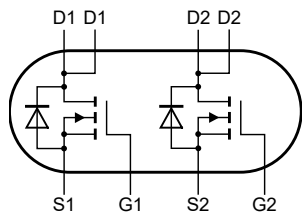
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode FET1 and FET2</b>						
Q <sub>r</sub>	recovered charge	I <sub>S</sub> = 5 A; di <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; T <sub>J</sub> = 25 °C	-	42.9	-	nC

- [1] Refer to application note AN10273 for further information
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

### 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFAK56D; Dual LFAK (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

### 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN045-100HL	LFAK56D; Dual LFAK	plastic, single ended surface mounted package (LFAK56D); 8 leads	SOT1205

### 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN045-100HL	45RL10H

### 8. Limiting values

Table 5. Limiting values

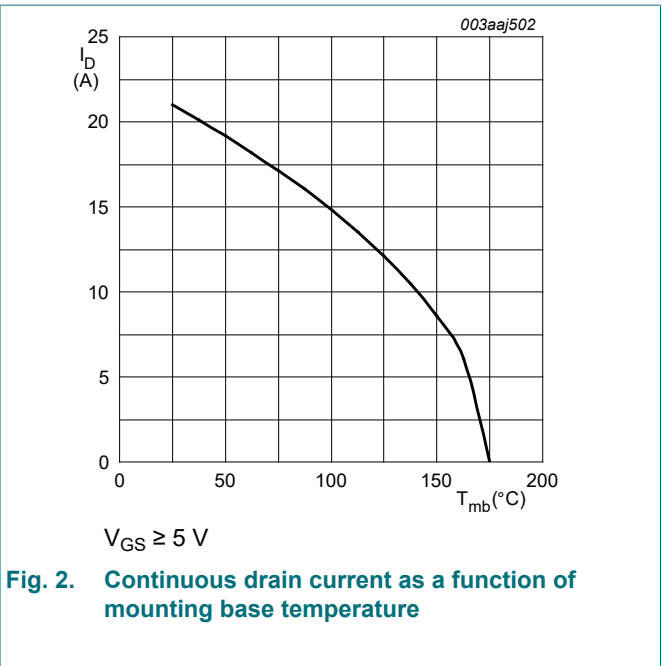
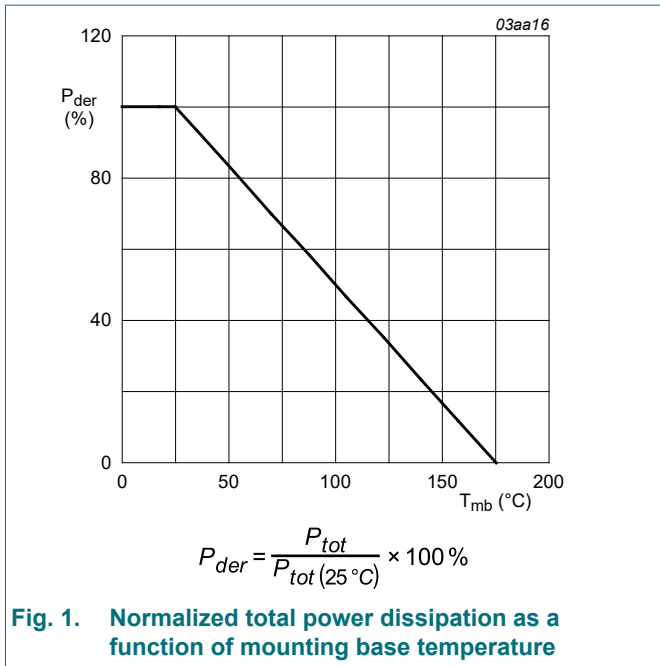
In accordance with the Absolute Maximum Rating System (IEC 60134).

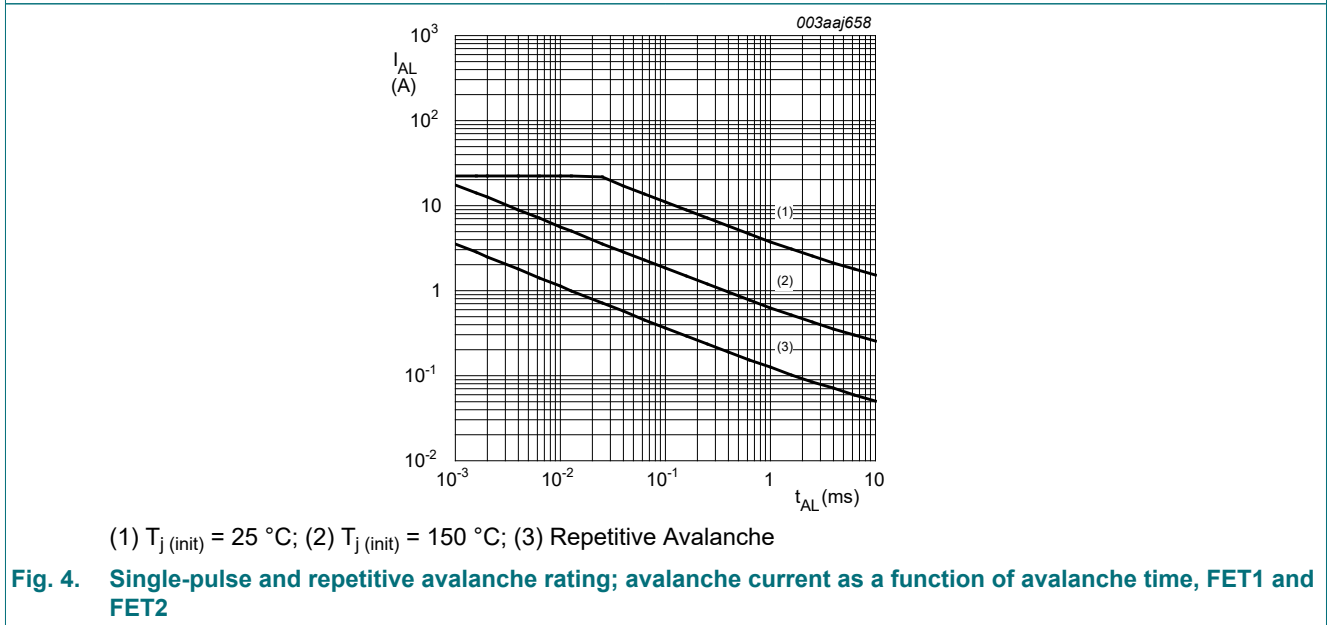
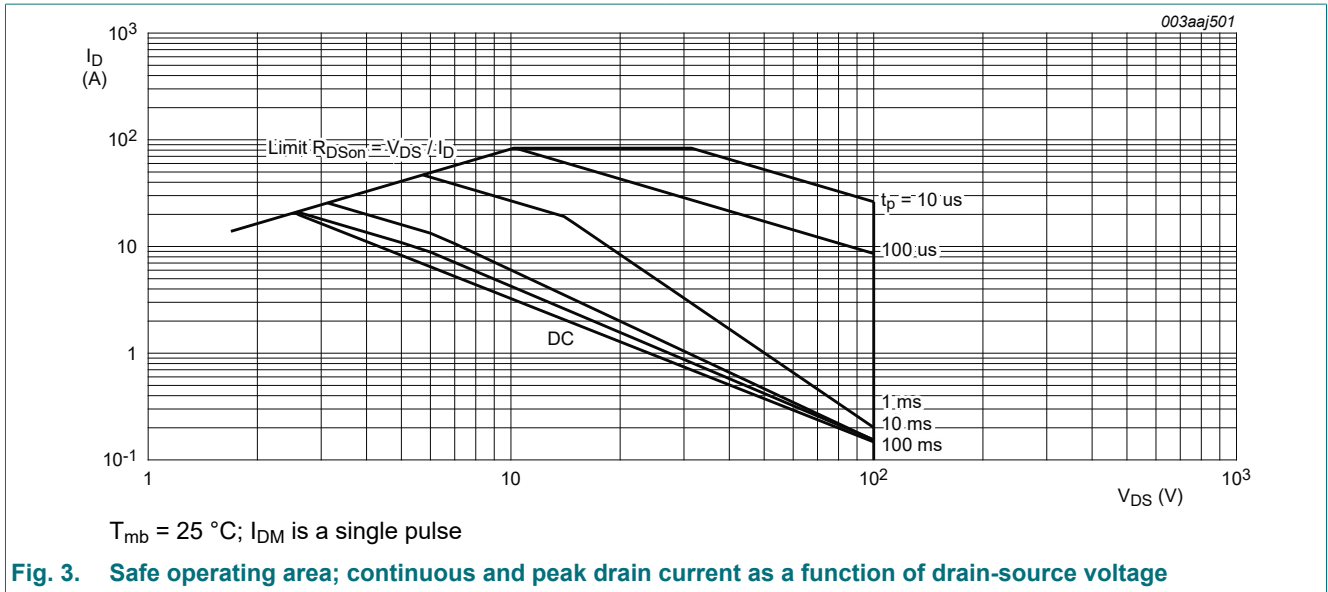
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>J</sub> ≤ 175 °C	-	100	V
V <sub>DGR</sub>	drain-gate voltage	25 °C ≤ T <sub>J</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ	-	100	V
V <sub>GS</sub>	gate-source voltage	DC; T <sub>J</sub> ≤ 175 °C	-10	10	V
		Pulsed; T <sub>J</sub> ≤ 175 °C	[1] [2]	-15	15
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; Fig. 1	-	53	W

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Symbol	Parameter	Conditions	Min	Max	Unit
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; Fig. 2	-	21	A
		V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 100 °C; Fig. 2	-	15	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; Fig. 3	-	83	A
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
<b>Source-drain diode FET1 and FET2</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	21	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	83	A
<b>Avalanche ruggedness FET1 and FET2</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 21 A; V <sub>sup</sub> ≤ 100 V; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; Fig. 4	[3] [4]	-	48 mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T<sub>j</sub> and/or V<sub>GS</sub>.
- [3] Refer to application note AN10273 for further information
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C





## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	-	2.84	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

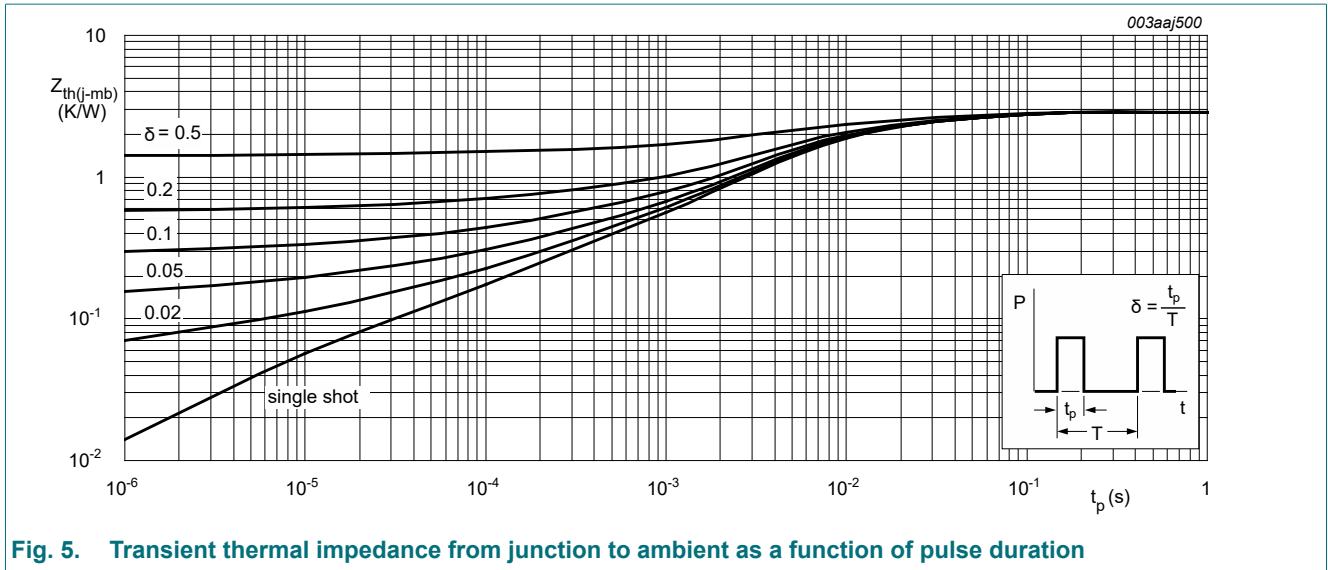


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration

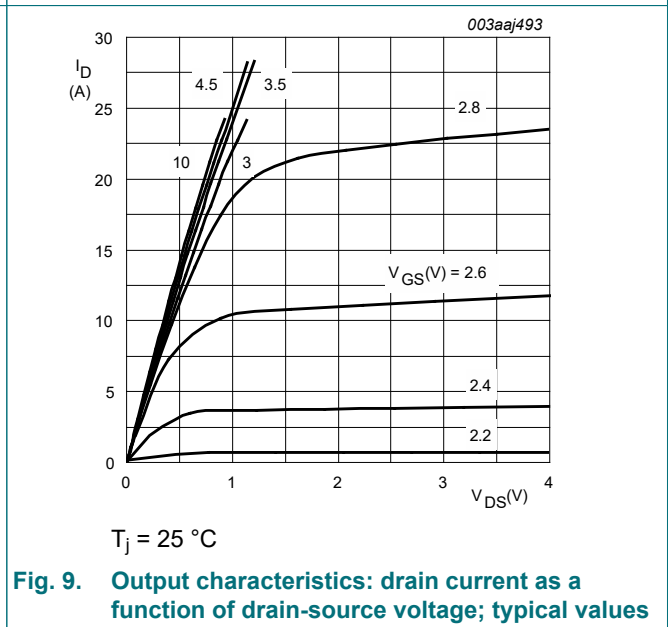
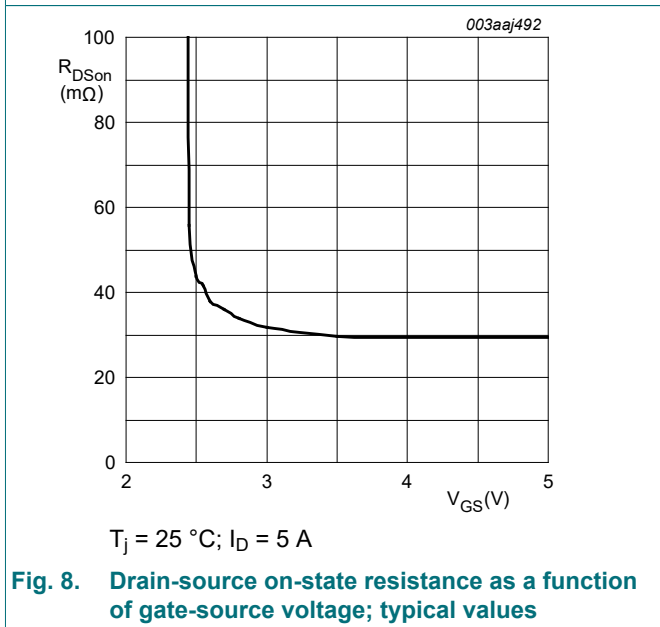
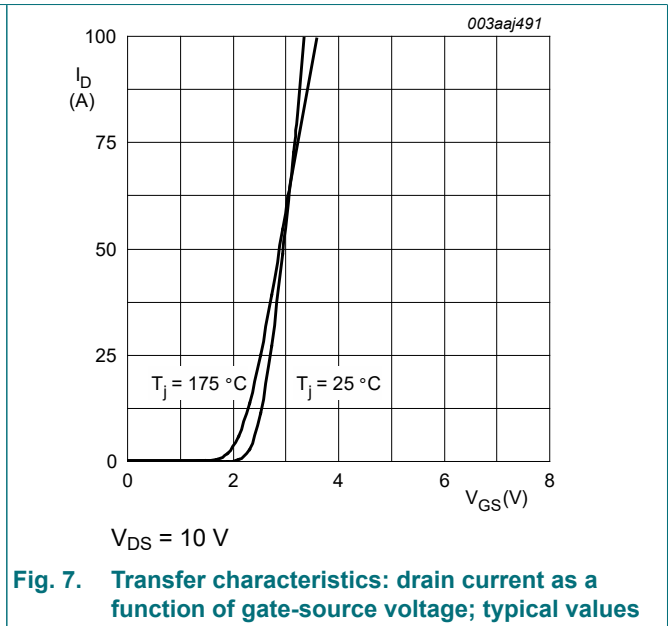
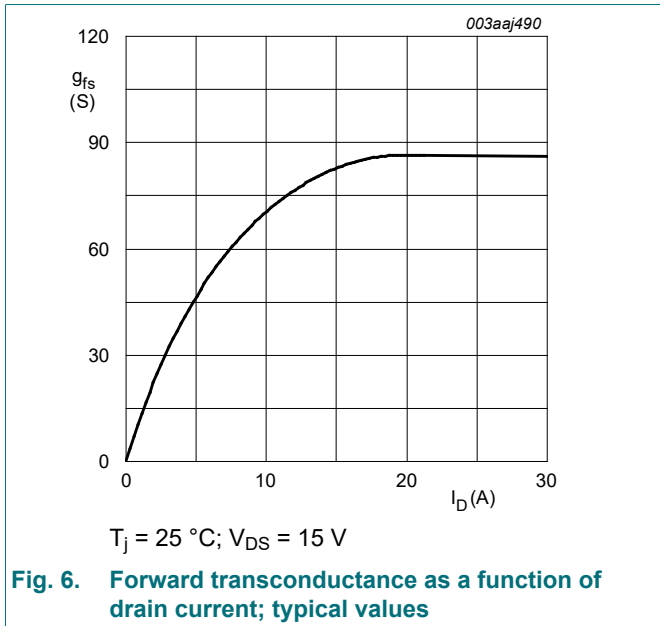
## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	$\mu A$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 12</a>	-	38.3	45	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 13</a>	-	103	124	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 12</a>	-	35.3	42	m $\Omega$
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 5 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	18.5	-	nC
$Q_{GS}$	gate-source charge		-	3.5	-	nC
$Q_{GD}$	gate-drain charge		-	7.3	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 16</a>	-	1614	2152	pF
$C_{oss}$	output capacitance		-	113	136	pF
$C_{rss}$	reverse transfer capacitance		-	72	99	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 80 \text{ V}; R_L = 16 \text{ } \Omega; V_{GS} = 5 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	10.2	-	ns
$t_r$	rise time		-	18.1	-	ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(off)}$	turn-off delay time		-	26.6	-	ns
$t_f$	fall time		-	17.5	-	ns
<b>Source-drain diode FET1 and FET2</b>						
$V_{SD}$	source-drain voltage	$I_S = 10\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 17	-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 5\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;	-	29.6	-	ns
$Q_r$	recovered charge	$V_{DS} = 50\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$	-	42.9	-	nC



N-channel 100 V, 45 mOhm, logic level MOSFET in LPAK56D using TrenchMOS technology

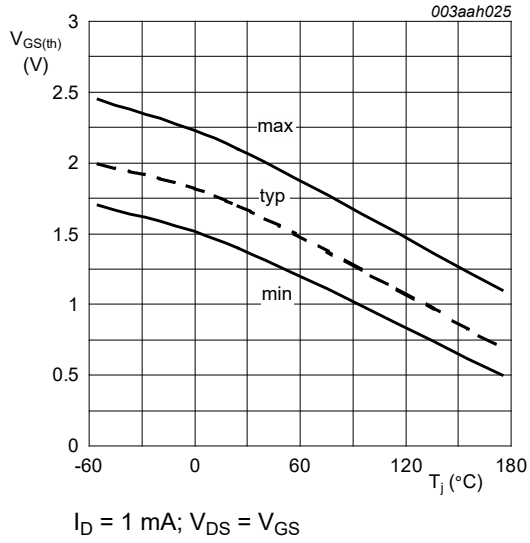


Fig. 10. Gate-source threshold voltage as a function of junction temperature

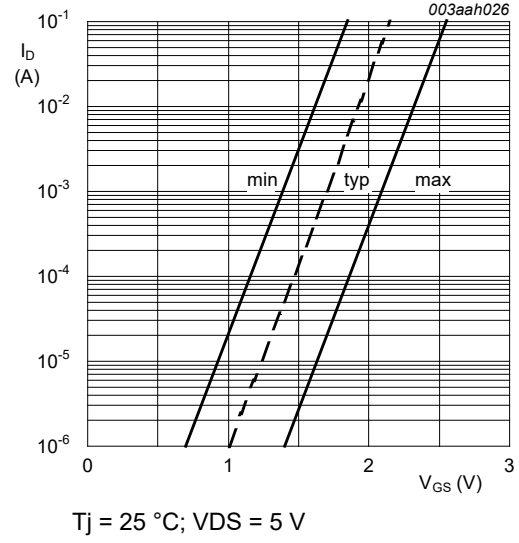


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

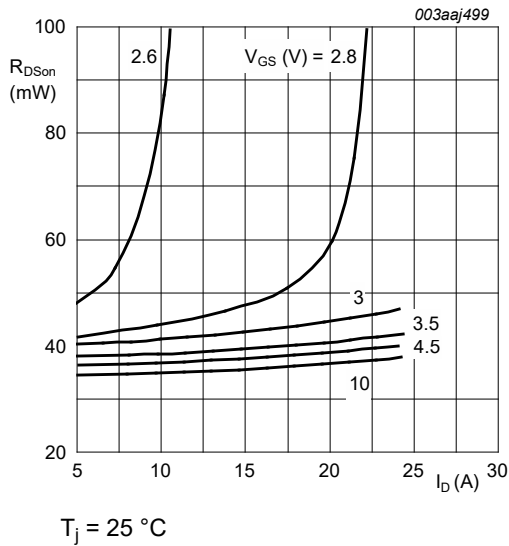


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

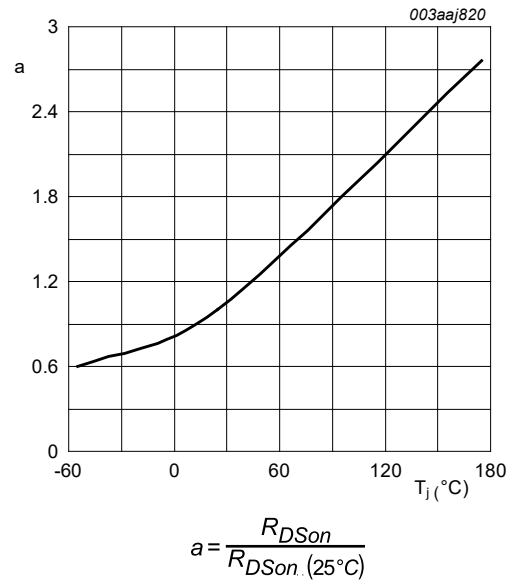


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

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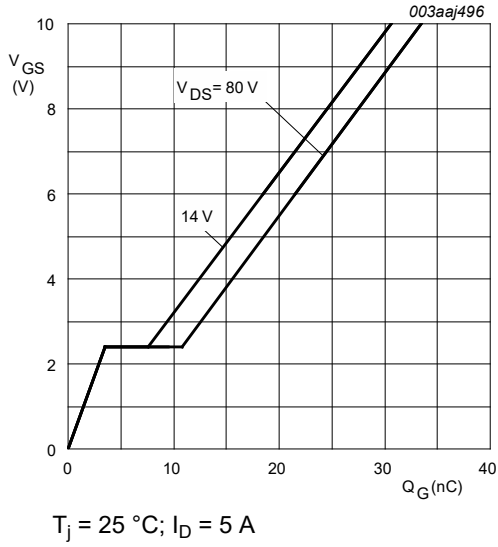


Fig. 14. Gate-source voltage as a function of gate charge; typical values

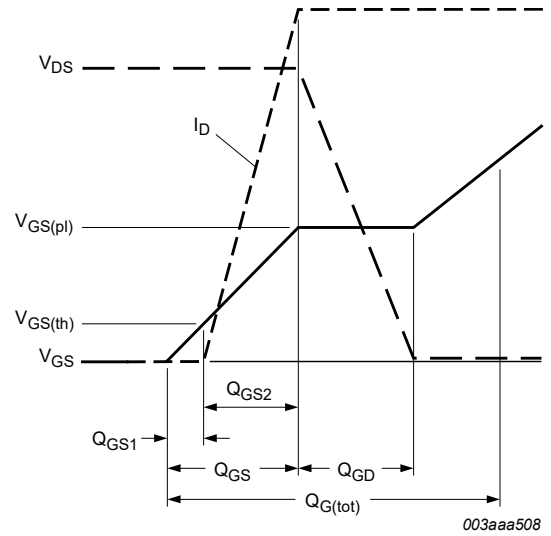


Fig. 15. Gate charge waveform definitions

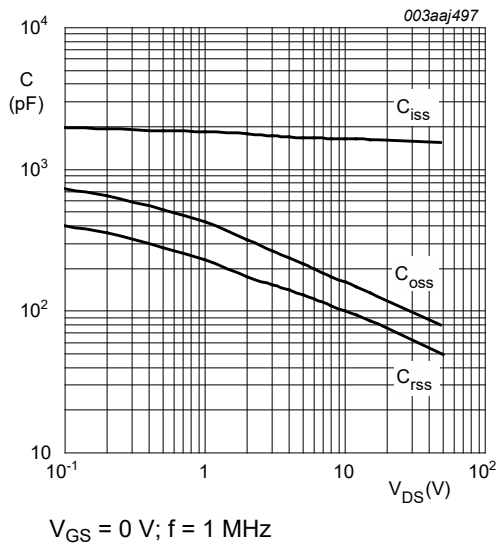


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

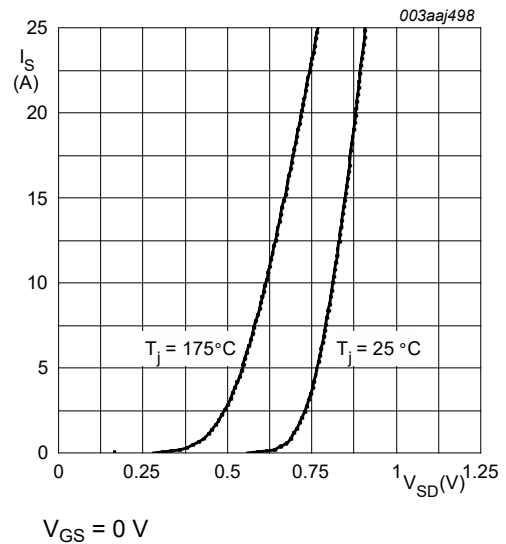


Fig. 17. Source current as a function of source-drain voltage; typical values



### 11. Package outline

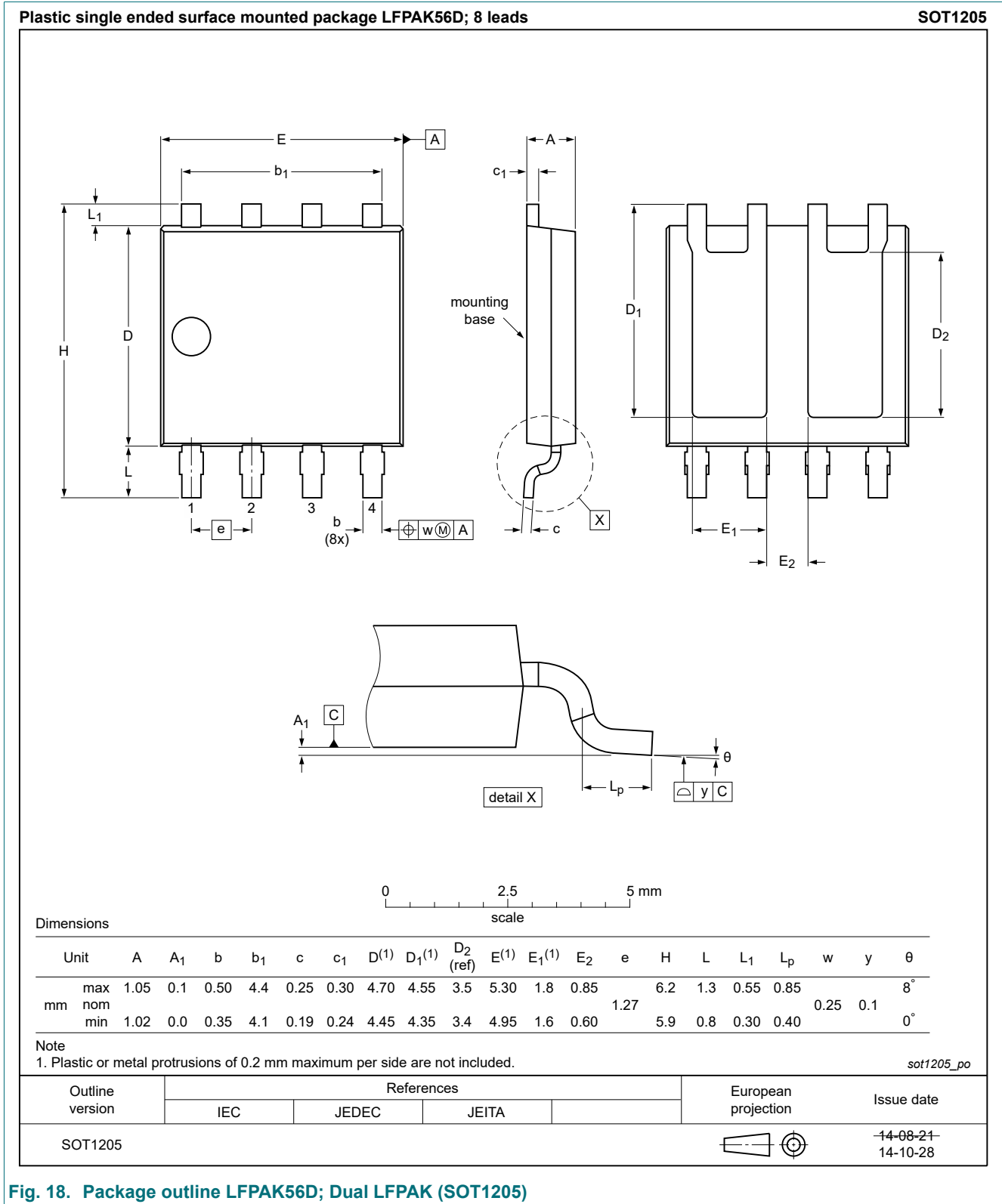


Fig. 18. Package outline LPAK56D; Dual LPAK (SOT1205)

## 12. Soldering

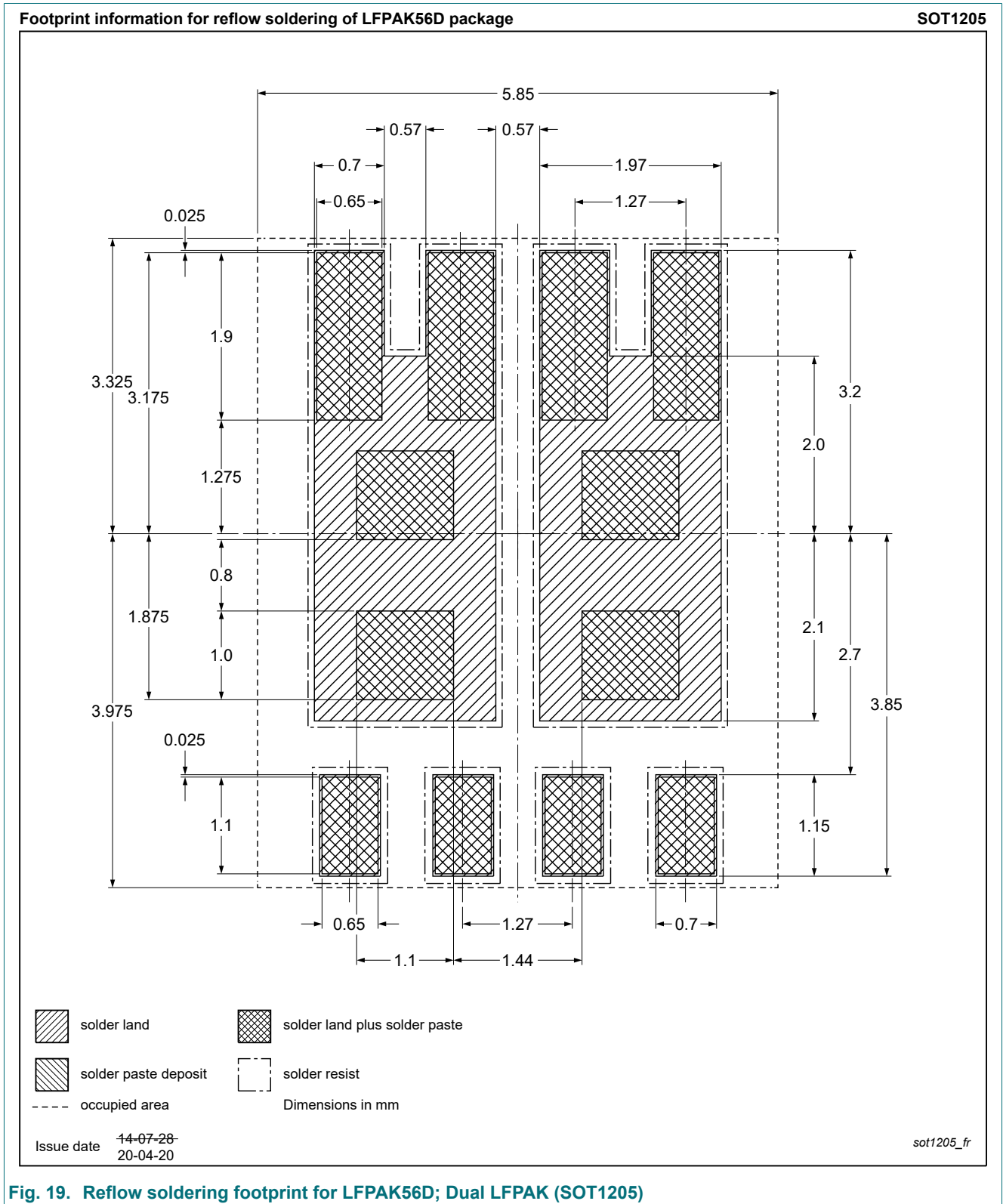


Fig. 19. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

## 13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Date of release: 26 September 2022

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