IS31AP2110

20W STEREO CLASS-D AUDIO AMPLIFIER WITH POWER LIMIT AND DYNAMIC TEMPERATURE CONTROL

November 2015

GENERAL DESCRIPTION

The IS31AP2110 is a high efficiency stereo Class-D audio amplifier with adjustable power limit function and dynamic temperature control. The loudspeaker driver operates from 8~26V supply voltage and analog circuit operates at 3.3V supply voltage. It can deliver 20W/CH output power into 8Ω loudspeaker within 0.2% THD+N and without external heat sink when playing music.

IS31AP2110 provides parallel BTL (Mono) application, and it can deliver 40W into 4Ω loudspeaker within 0.11% THD+N. The adjustable power limit function allows user to set a voltage rail lower than half of 3.3V to limit the amount of current through the speaker.

Output DC detection prevents speaker damage from long-time current stress. The dynamic temperature control is a gain control system. As chip junction temperature higher than a warning level, the gain level will decrease until junction temperature lower than the warning level.

The output short circuit and over temperature protection include auto-recovery feature.

The IS31AP2110 is available in a thermally enhanced eTSSOP-28 package.

FEATURES

- Single supply voltage
  - 8V ~ 26V for loudspeaker driver
  - Built-in LDO output 3.3V for others
- Loudspeaker power from 24V supply
  - BTL Mode: 20W/CH into 8Ω @0.2% THD+N
  - PBTL Mode: 40W/CH into 4Ω @0.11% THD+N
- Loudspeaker power from 13V supply
  - BTL Mode: 10W/CH into 8Ω @10% THD+N
- 87% efficient Class-D operation eliminates need for heat sink
- Differential inputs
- Four selectable, fixed gain settings
- Internal oscillator
- Short-Circuit protection with auto recovery option
- Under-voltage detection
- Over-voltage protection
- Pop noise and click noise reduction
- Adjustable power limit function for speaker protection
- Output DC detection for speaker protection
- Filter-Free operation
- Over temperature protection with auto recovery
- Dynamic temperature control prevents chip from over heating

APPLICATIONS

- TV audio
- Bluetooth speaker system
- Docking speaker system
- Consumer audio equipment

TYPICAL APPLICATION CIRCUIT

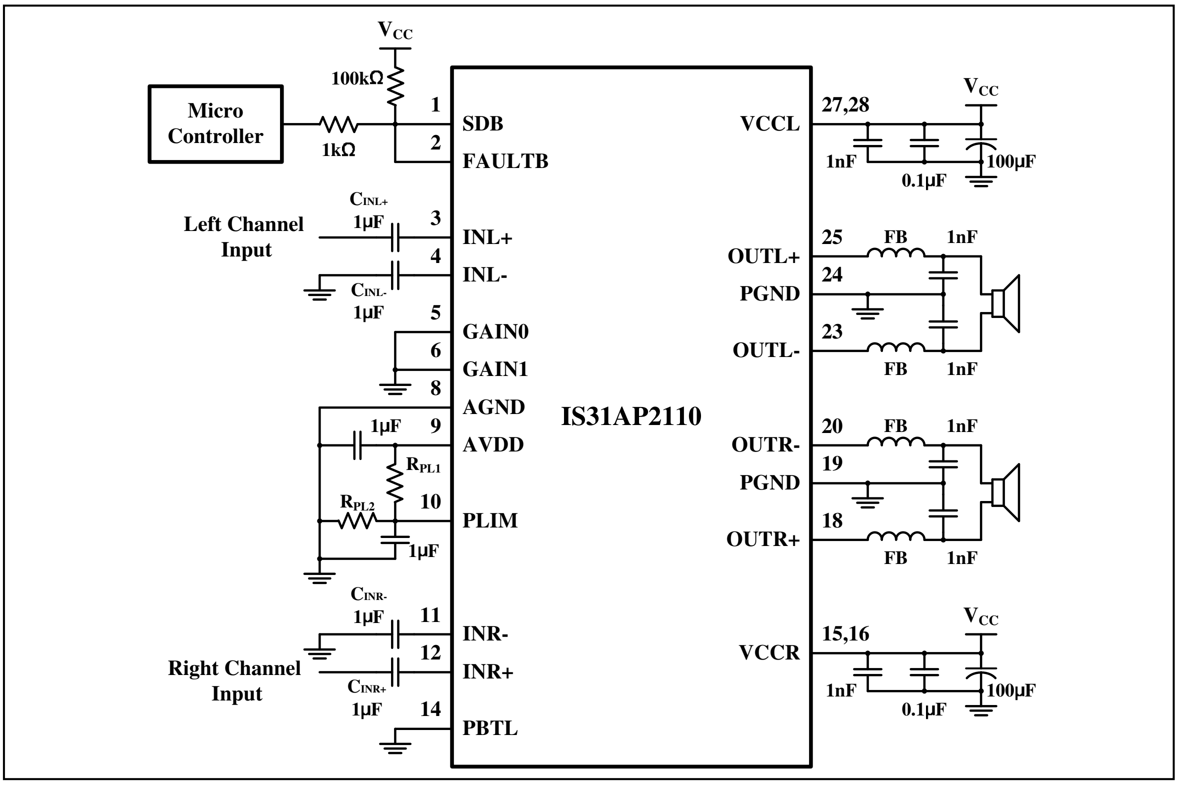


Figure 1 Typical Application Circuit (for BTL Stereo, Single-ended Input)

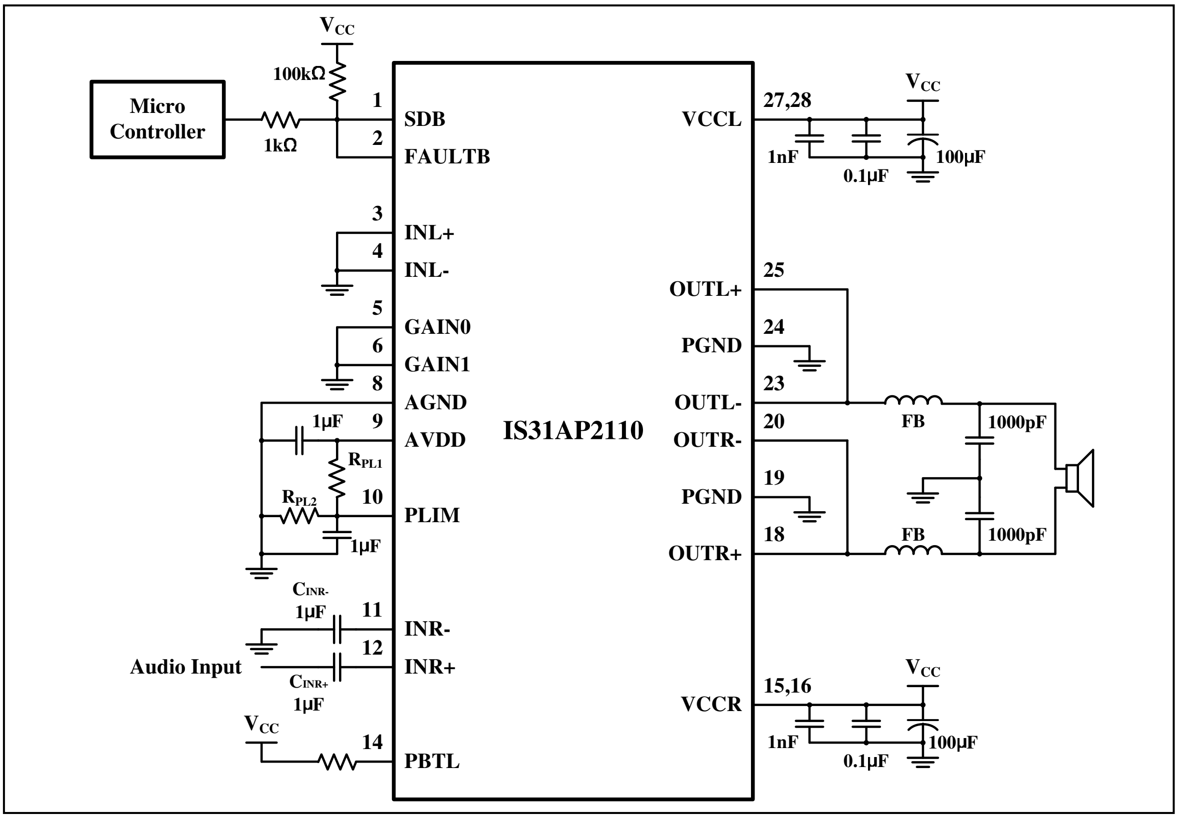
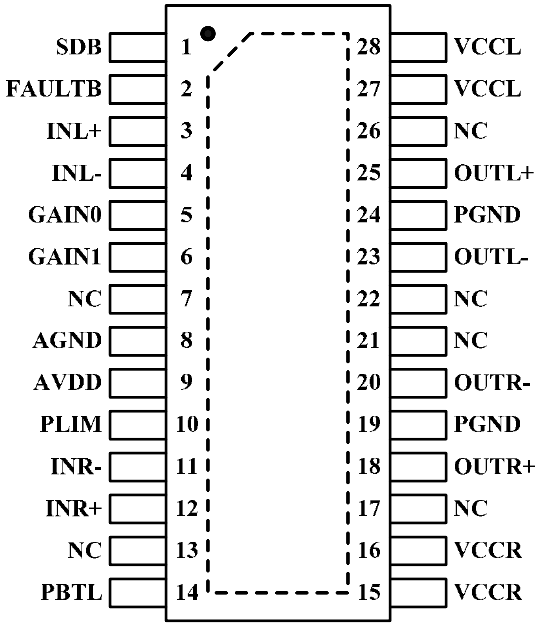


Figure 2 Typical Application Circuit (for Parallel BTL Mono, Single-ended Input)

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-28	

PIN DESCRIPTION

No.	Pin	Description
1	SDB	Shutdown signal for IC (Low = disabled, output Hi-Z; High = operational). Voltage compliance to 26V.
2	FAULTB	Open drain output used to display short circuit or dc detect fault. Voltage compliant to 26V. Short circuit faults can be set to auto-recovery by connecting FAULTB pin to SDB pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling V_{CC}.
3	INL+	Positive audio input for left channel. Biased at 1.65V.
4	INL-	Negative audio input for left channel. Biased at 1.65V.
5	GAIN0	Gain select least significant bit. Voltage compliance to 26V.
6	GAIN1	Gain select most significant bit. Voltage compliance to 26V.
7,13,17, 21,22,26	NC	Not connected.
8	AGND	Analog signal ground. Connect to the thermal pad.
9	AVDD	3.3V regulated output.
10	PLIM	Power limit level adjustment. Connect a resistor divider from AVDD to GND to set power limit. Give V_{PLIMIT} <1.55V to set power limit level. Connect to both of AVDD (>1.55V) and GND are all without power limit feature.
11	INR-	Negative audio input for right channel. Biased at 1.65V.
12	INR+	Positive audio input for right channel. Biased at 1.65V.
14	PBTL	Parallel BTL mode switch, high for parallel BTL output. Voltage compliance to 26V.
15, 16	VCCR	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
18	OUTR+	Class-D H-bridge positive output for right channel.
19	PGND	Power ground for the H-bridges.
20	OUTR-	Class-D H-bridge negative output for right channel.
23	OUTL-	Class-D H-bridge negative output for left channel.
24	PGND	Power ground for the H-bridges.
25	OUTL+	Class-D H-bridge positive output for left channel.
27, 28	VCCL	High-voltage power supply for left-channel. Right channel and left channel power supply inputs are connect internal.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION
Industrial Range: -40°C To +85°C

Order Part No.	Package	QTY
IS31AP2110-ZLS2-TR	eTSSOP-28, Lead-free	2500/Reel
IS31AP2110-ZLS2	eTSSOP-28, Lead-free	50/Tube

ABSOLUTE MAXIMUM RATINGS

Supply voltage (VCCR, VCCL), V_{CC}	−0.3V ~ +30V
Interface pin voltage, (SDB, GAIN0, GAIN1, PBTL, FAULTB) (PLIM, INL+, INL-, INR+, INR-)	−0.3V ~ +26V −0.3V ~ +3.6V
Minimum load resistance, R_L, (BTL: V_{CC} > 15V) (BTL: V_{CC} ≤ 15V) PBTL	4.8Ω 3.2Ω 3.2Ω
Thermal resistance, θ_{JA}	28°C/W
Maximum junction temperature, T_{JMAX}	150°C
Storage temperature range, T_{STG}	−65°C ~ +150°C
Operating temperature range, T_A	−40°C ~ +85°C
ESD (HBM) ESD (CDM)	±2kV ±500V

Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=24V, T_A=25°C, R_L=8Ω (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage to VCCL, VCCR		8		26	V
I_{CC}	Quiescent current	V_{SDB} = 2V, no load		32	50	mA
		V_{SDB} = 2V, no load, V_{CC} = 12V		20	35	
I_{SD}	Shutdown current	V_{SDB} = 0.8V, no load		<10	25	μA
		V_{SDB} = 0.8V, no load, V_{CC} = 12V		<10	25	
I_{SC}	L/R channel over current protection	V_{SDB} = 2V, V_{CC} = 24V		8		A
$R_{DS(ON)}$	Drain-source on-state resistance-High side PMOS	V_{CC}=12V, Id=500mA, T_J=25°C		300		mΩ
	Drain-source on-state resistance-Low side NMOS			200		
V_{OS}	Class-D output offset voltage (measured differential)	V_I = 0, Gain= 36dB		15		mV
G	Gain	Gain1= 0.8V, Gain0=0.8V	18	20	22	dB
		Gain1= 0.8V, Gain0= 2V	24	26	28	
		Gain1= 2V, Gain0= 0.8V	30	32	34	
		Gain1= 2V, Gain0= 2V	34	36	38	
t_{ON}	Turn-on time	V_{SDB} = 2V		51		ms
t_{OFF}	Turn-off time	V_{SDB} = 0.8V		4		μs
AV_{DD}	Internal regulated output	I_{AVDD} = 0.1mA	3.0	3.3	3.6	V

DC ELECTRICAL CHARACTERISTICS (CONTINUE)

V_{CC}=24V, T_A=25°C, R_L=8Ω (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Logic Electrical Characteristics						
V_{IH}	High level input voltage	SDB, GAIN0, GAIN1, PBTL	2			V
V_{IL}	Low level input voltage	SDB, GAIN0, GAIN1, PBTL			0.8	V
V_{OL}	Low level output voltage	FAULTB, R_{PU}=100kΩ, V_{CC}=26V			0.8	V
I_{IH}	High level input current	SDB,GAIN0,GAIN1,PBTL,V_I=2V, V_{CC}=18V			50	μA
I_{IL}	Low level input current	SDB,GAIN0,GAIN1,PBTL, V_I=0.8V, V_{CC}=18V			5	μA

AC ELECTRICAL CHARACTERISTICS

V_{CC}=24V, T_A=25°C, R_L=8Ω (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_O	Output power	THD+N = 10%, f = 1kHz, V_{CC} = 13V		10		W
		THD+N = 10%, f = 1kHz, V_{CC} = 16V		15		
THD+N	Total harmonic distortion + noise	V_{CC}=24V, R_L=8Ω, f=1kHz, P_O=15W (half-power)		0.1		%
		V_{CC}=12V, R_L=8Ω, f=1kHz, P_O=5W (half-power)		0.11		
V_N	Output integrated noise	20Hz to 22kHz, A-weighted filter, Gain = 20dB, R_L=8Ω		130		μV
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1kHz, Gain = 20dB, A-weighted		102		dB
PSRR	Power supply ripple rejection	200mV_{P-P} ripple at 1kHz, Gain = 20dB, Inputs ac-coupled to AGND		-62		dB
X_{TALK}	Crosstalk	f=1kHz, V_O=1Vrms, Gain=20dB		-83		dB
f_{OSC}	Oscillator frequency		250	310		kHz
T_{SD}	Thermal trip point			170		°C
T_{SD_HY}	Thermal hysteresis			20		°C

TYPICAL PERFORMANCE CHARACTERISTICS

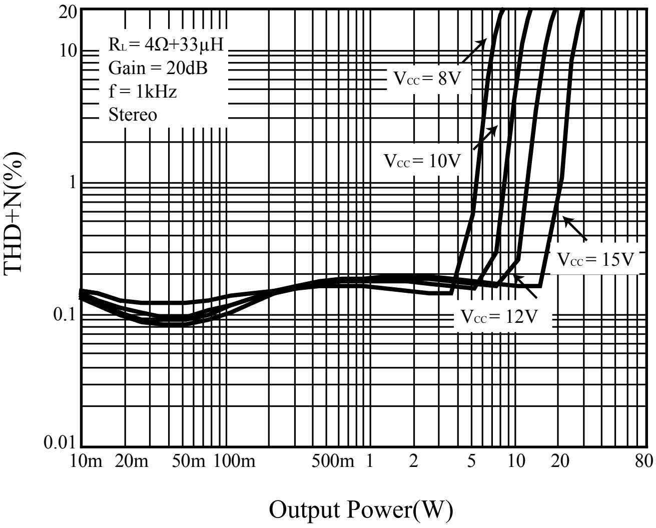


Figure 3 THD+N vs. Output Power

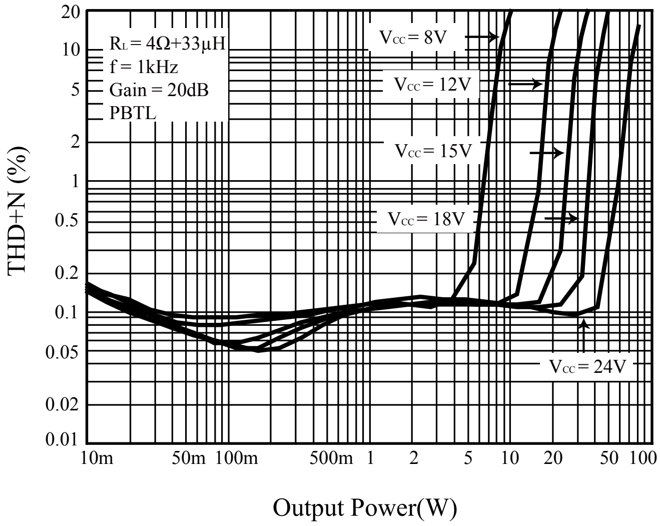


Figure 4 THD+N vs. Output Power

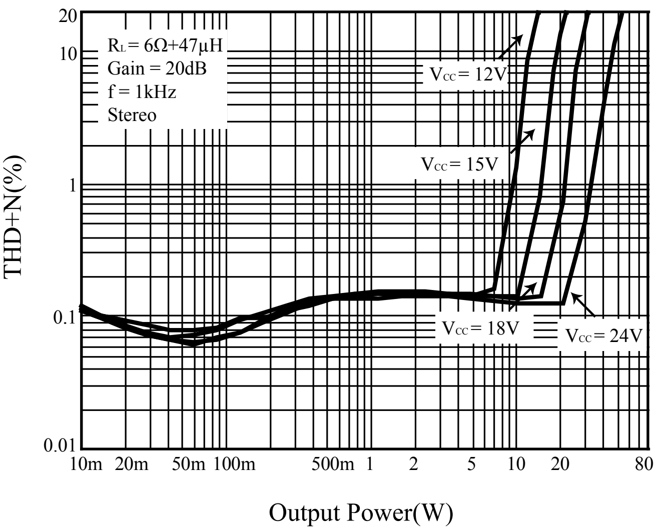


Figure 5 THD+N vs. Output Power

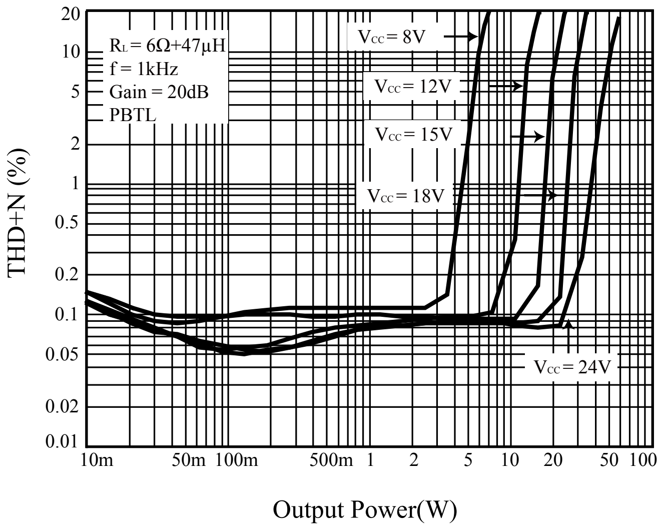


Figure 6 THD+N vs. Output Power

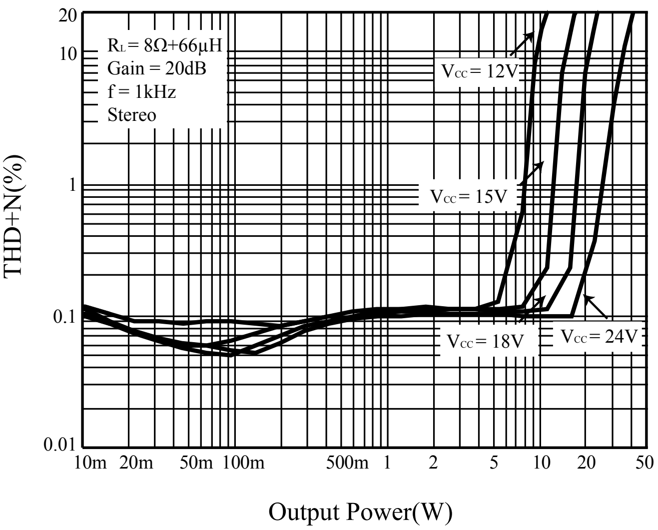


Figure 7 THD+N vs. Output Power

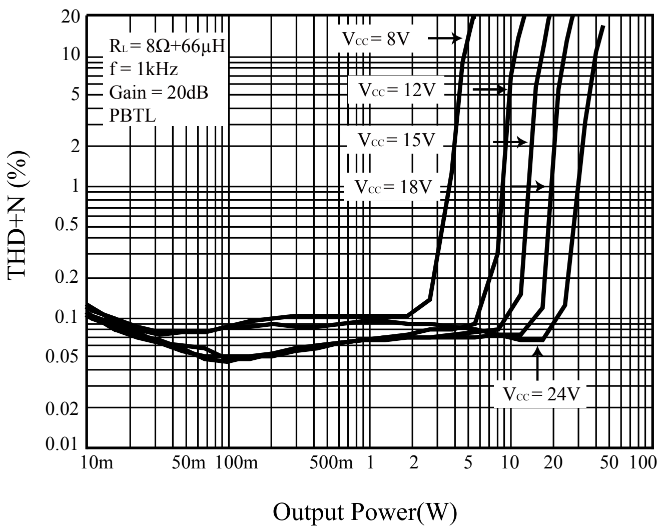


Figure 8 THD+N vs. Output Power

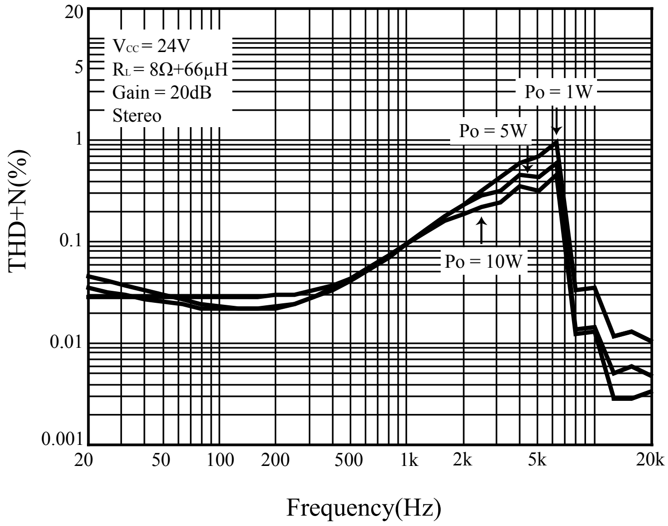


Figure 9 THD+N vs. Frequency

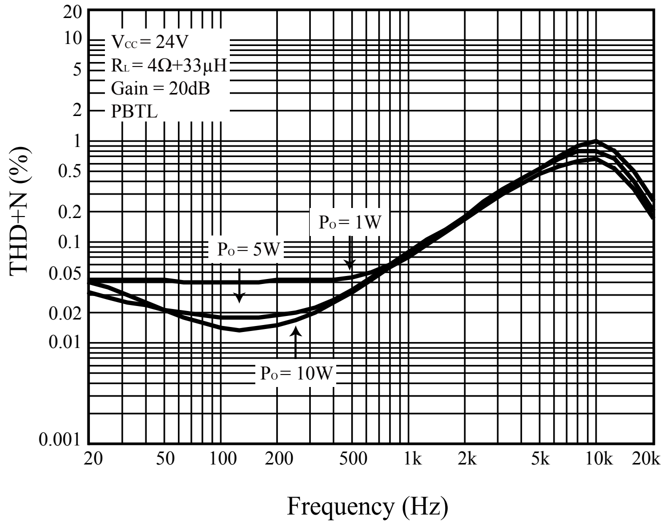


Figure 10 THD+N vs. Frequency

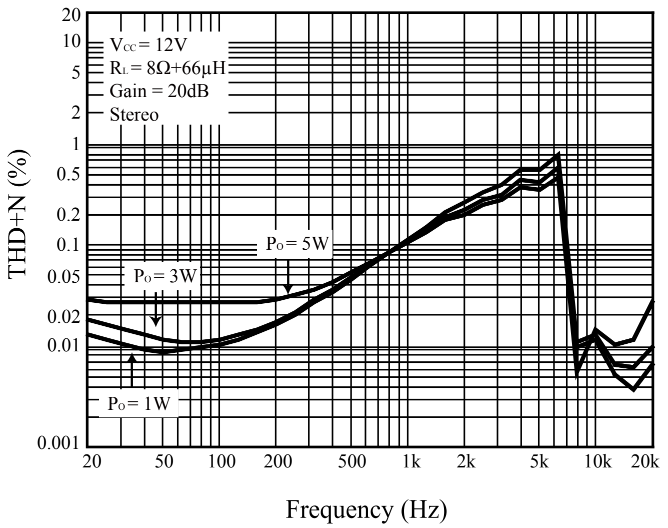


Figure 11 THD+N vs. Frequency

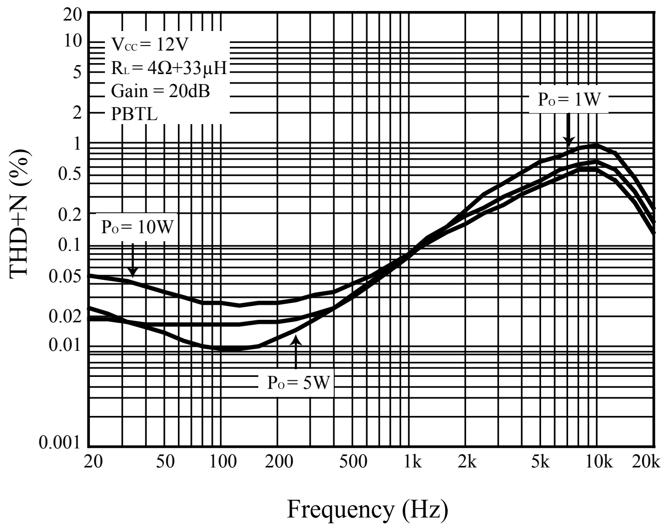


Figure 12 THD+N vs. Frequency

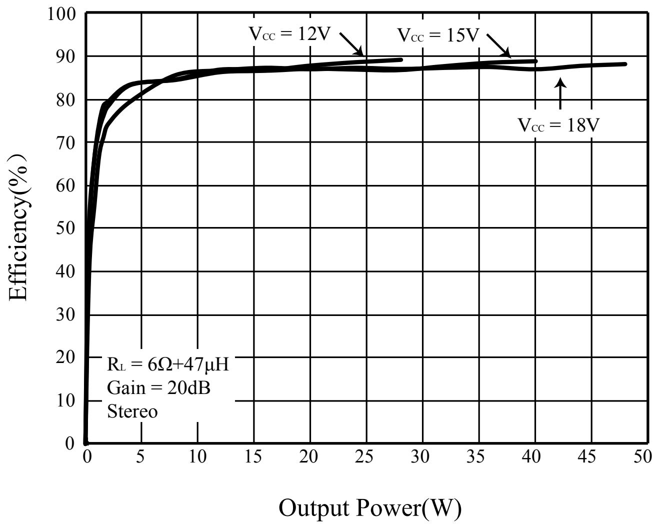


Figure 13 Efficiency vs. Output Power

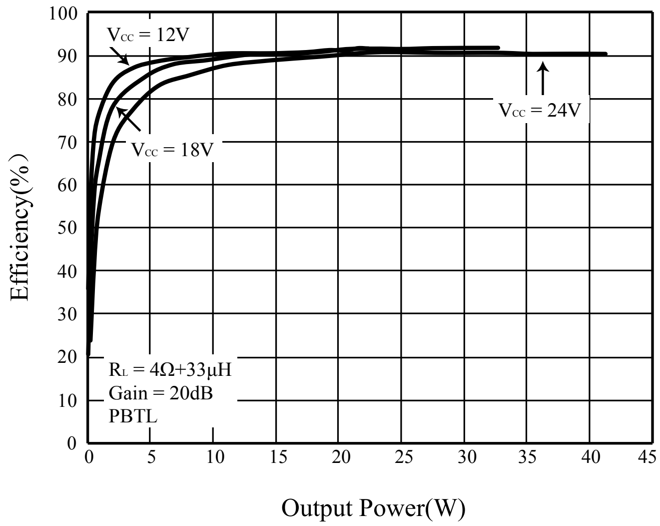


Figure 14 Efficiency vs. Output Power

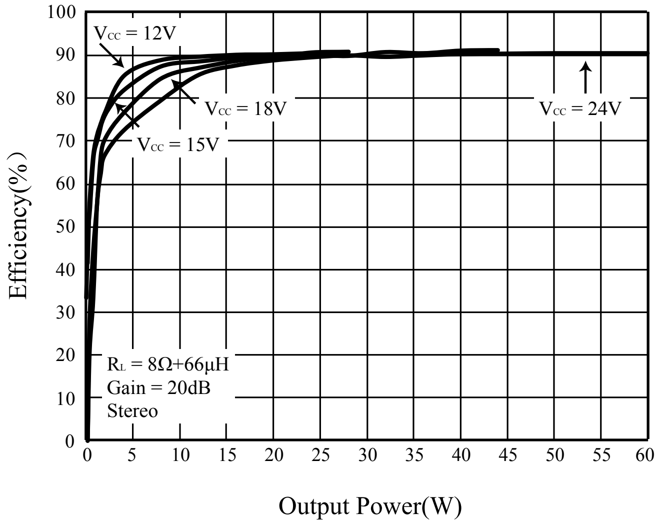


Figure 15 Efficiency vs. Output Power

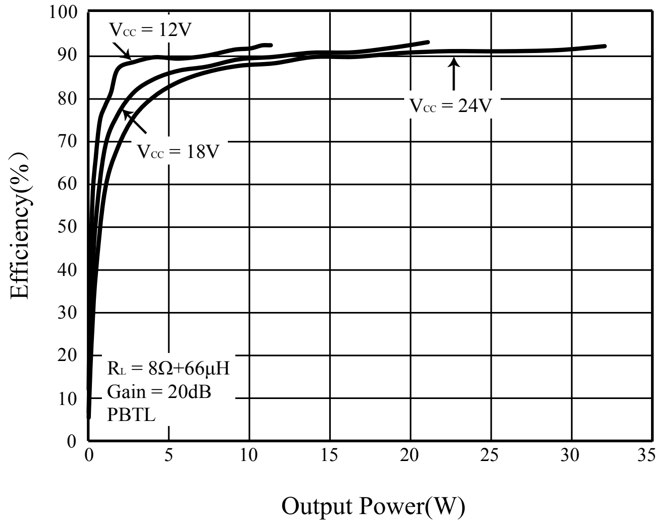


Figure 16 Efficiency vs. Output Power

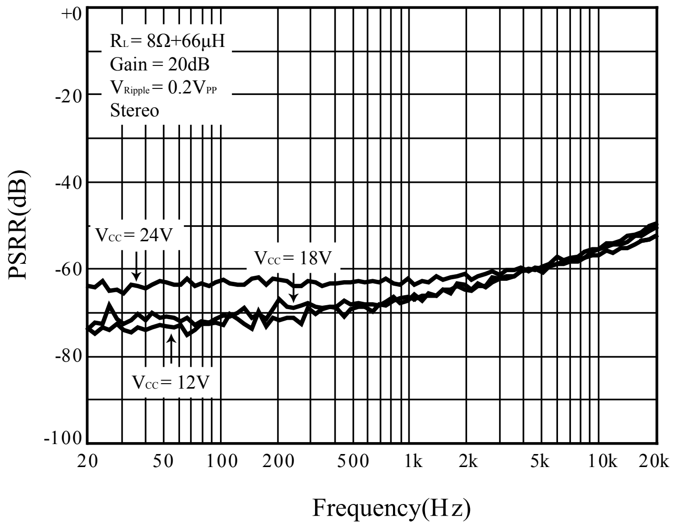


Figure 17 PSRR

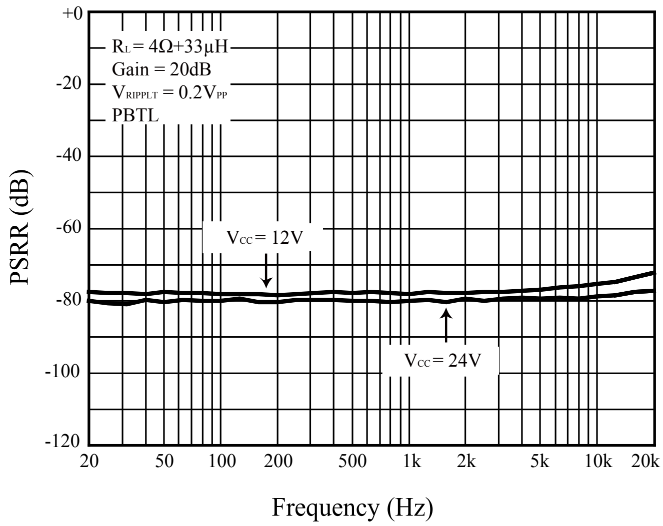


Figure 18 PSRR

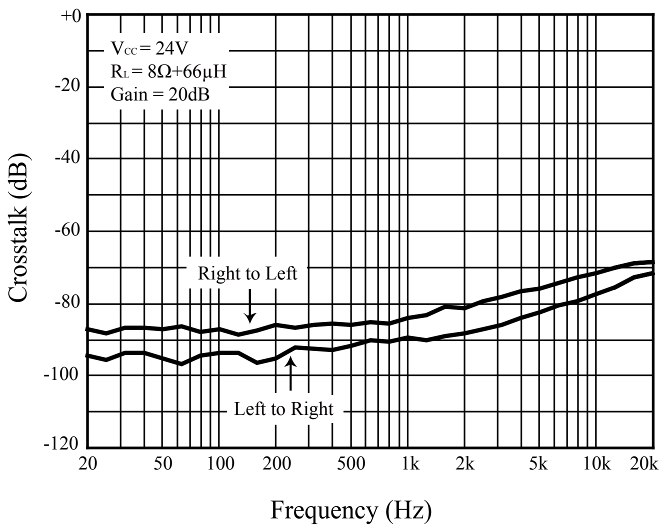


Figure 19 Crosstalk

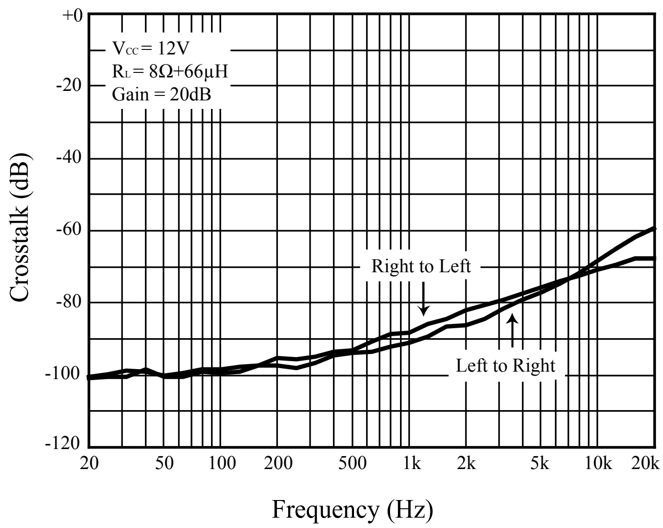
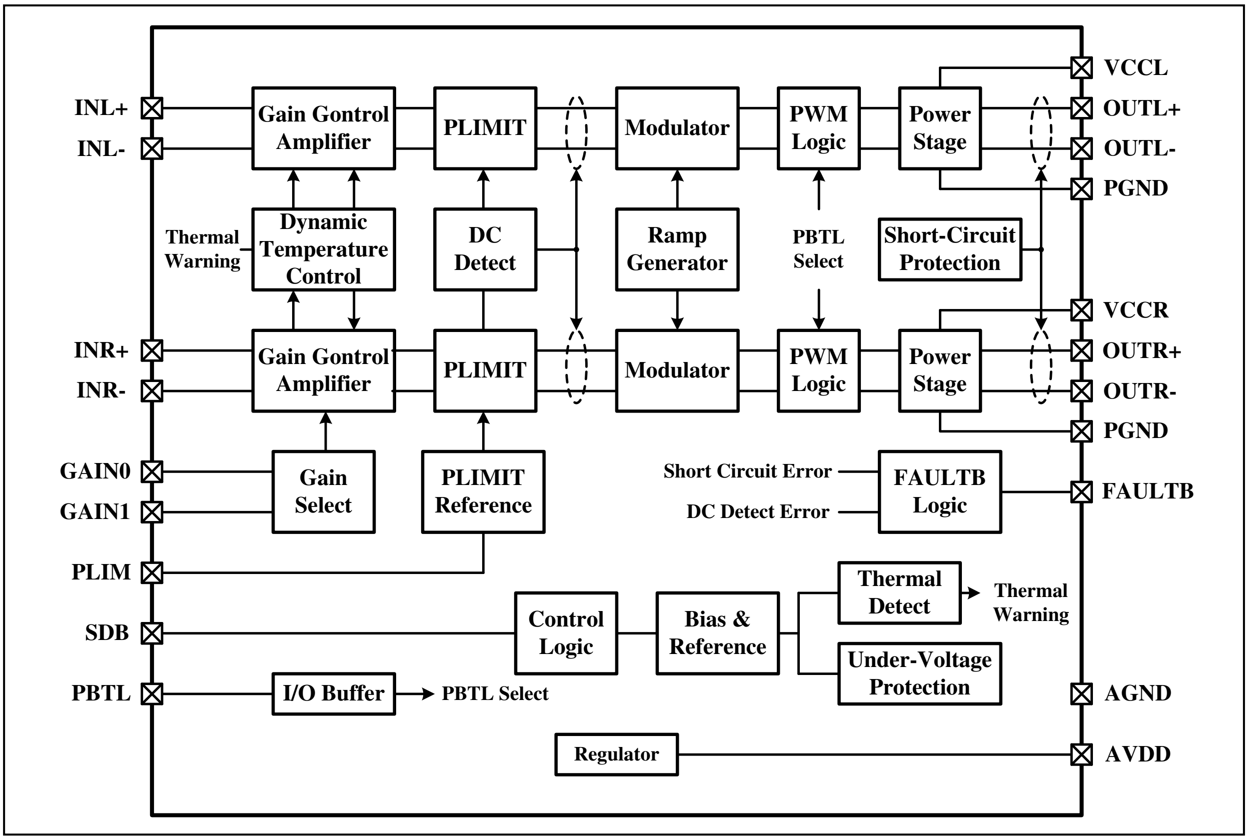


Figure 20 Crosstalk

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

GAIN SETTINGS

The gain of the IS31AP2110 is set by two input pins, GAIN0 and GAIN1. By varying input resistance in IS31AP2110, the various volume gains are achieved. The respective volume gain and input resistance are listed in Table 1. However, there is 20% variation in input resistance from production variation.

Table 1 Volume gain and input impedance

GAIN1	GAIN0	Volume Gain (dB)	Input Resistance, R_{IN} (kΩ)
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

SHUTDOWN (SDB) CONTROL

Pulling SDB pin low will let IS31AP2110 operate in low-current state for power conservation. The IS31AP2110 outputs will enter mute once SDB pin is pulled low, and regulator will also disable to save power. If let SDB pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

DC DETECTION

IS31AP2110 has dc detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 420ms, the dc detect error will occur and report to FAULTB pin. At the same time, loudspeaker drivers of right/left channel will disable and enter Hi-Z. This fault can't be cleared by cycling SDB, it is necessary to cycle the V_{CC} supply.

The minimum differential input voltages required to trigger the DC detect function are shown in Table 2. The input voltage must keep above the voltage listed in the table for more than 420msec to trigger the DC detect fault. The equivalent class-D output duty of the DC detect threshold is listed in Table 3. For 8V supply, DC detect fault will occur as output duty exceed 13% for more than 420msec.

Table 2 DC Detect Threshold

AV (dB)	V_{IN} (mV, differential)
20	104
26	52
32	26
36	16

Table 3 Output DC Detect Duty (for Either Channel)

V_{CC} (V)	Output Duty Exceeds
8	13%
12	8.7%
16	6.5%
24	4.3%

THERMAL PROTECTION

If the internal junction temperature is higher than 170°C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for IS31AP2110 returning to normal operation is about 150°C. The variation of protected temperature is about 10%. Thermal protection faults are not reported on the FAULTB pin.

SHORT-CIRCUIT PROTECTION

To protect loudspeaker drivers from over-current damage, IS31AP2110 has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to GND or to V_{CC}, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The short protection fault is reported on FAULTB pin as a low state. The latch can be cleared by reset SDB or power supply cycling.

The short circuit protection latch can have auto-recovery function by connect the FAULTB pin directly to SDB pin. The latch state will be released after 420ms, and the short protection latch will re-cycle if output overload is detected again.

UNDER-VOLTAGE DETECTION

When the AVDD voltage is lower than 2.7V or the V_{CC} voltage is lower than 7.5V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, IS31AP2110 return to normal operation.

OVER-VOLTAGE PROTECTION

When the V_{CC} is higher than 30V, loudspeaker will be disabled kept at low state. The protection status will be released as V_{CC} lower than 28.7V.

POWER LIMIT FUNCTION

The voltage at PLIM pin (pin 10) can used to limit the power of first gain control amplifier output. Add a resistor divider from AVDD to ground to set the voltage V_{PLIMIT} at the PLIMIT pin. The voltage V_{PLIM} sets a limit on the output peak-to-peak voltage. The maximum BTL output voltage of the gain control amplifier is limited to $2\times(1.55V–V_{PLIM})$. The Class-D BTL output voltage on loudspeaker is amplified by 9.95 of $2\times(1.55V–V_{PLIM})$.

For normal BTL operation (Stereo) and PBTL (Mono) operation:

$$P_{OUT} = \left[2\times\left|V_P\right|\times 9.95\right]^2 \div \left(2\times R_L\right)$$

for unclipped power (1)

Where:

- V_P is the peak voltage of gain control amplifier output,

if $(V_{IN}\times Gv/2) < (1.55V–V_{PLIM})$, then $V_P = (V_{IN}\times Gv/2)$.

If $(V_{IN}\times Gv/2) > (1.55V–V_{PLIM})$, then $V_P = (1.55V–V_{PLIM})$.

- V_{IN} is the input peak voltage.

- Gv is the gain of gain control amplifier, the four gain levels are 1V/V, 2V/V, 4V/V, 6.34V/V, corresponding to 20dB, 26dB, 32dB, 36dB overall gain.

- AVDD is the regulator output at pin 9, typical 3.3V.

- R_L is the load resistance.

- P_{OUT} (10% THD) = 1.25 x P_{OUT} (unclipped).

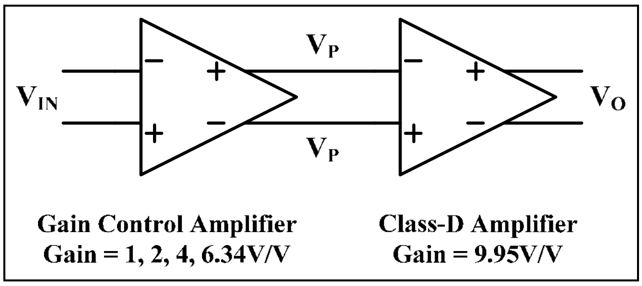


Figure 21 Gain Contribution of the Two Gain Stages

Table 4 PLIM Typical Operation

Test Conditions	Output P_O (W)	V_{PLIM}(V) @ THD+N=1%	V_{PLIM}(V) @ THD+N=10%	Output Voltage (V_{P-P})
V_{CC}=24V R_L=8Ω	25	0.54	0.65	40
	20	0.65	0.75	35.6
	15	0.77	0.85	30.8
	10	0.91	0.98	25.2
	5	1.1	1.15	17.8

Note: Connect PLIM pin to AVDD (>1.55V) or GND (either one) to disable power limit function.

PBTL (MONO) FUNCTION

IS31AP2110 provides the application of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin is tied high, the positive and negative outputs of left and right channel are synchronized and in phase. Apply the input signal to the RIGHT channel input in PBTL mode and let the LEFT channel input grounded, and place the speaker between the LEFT and RIGHT outputs. The output current capability is doubled of that in normal mode. See the application circuit example for PBTL (Mono) mode operation. For normal BTL (Stereo) operation, connect the PBTL pin to ground.

DYNAMIC TEMPERATURE CONTROL (DTC)

The DTC function is designed to protect the loudspeaker from over heating. As the junction temperature is higher than OT_W, the gain of amplifier will decrease step by step every 0.25s. Finally, as the junction temperature is lower than OT_R, the attenuated gain steps will be released step by step every 0.5s. If DTC can’t suppress the temperature and the temperature reach to the OT trip point (170°C), the amplifier will be shutdown. The OT hysteresis temperature equals to OT_R. Typically, OT_W is 160°C and OT_R is 145°C.

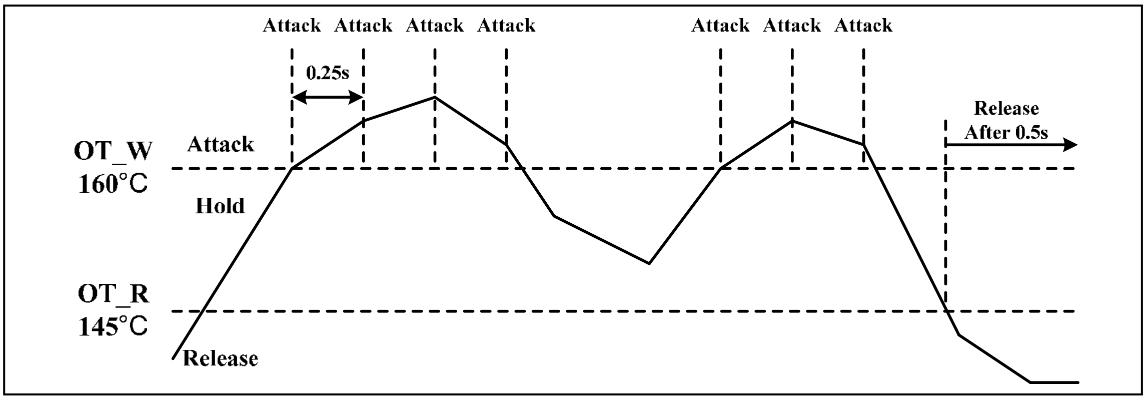


Figure 22 Dynamic Temperature Control Function

Input Capacitors (C_{IN})

The performance at low frequency (bass) is affected by the corner frequency (f_C) of the high-pass filter composed of input resistor (R_{IN}) and input capacitor (C_{IN}), determined in Equation (2). Typically, a 0.1μF or 1μF ceramic capacitor is suggested for C_{IN}. The resistance of input resistors is different at different gain setting. The respective gain and input resistance are listed in Table 1 (shown at GAIN SETTING). However, there is 20% variation in input resistance from production variation.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}} (Hz) \quad (2)$$

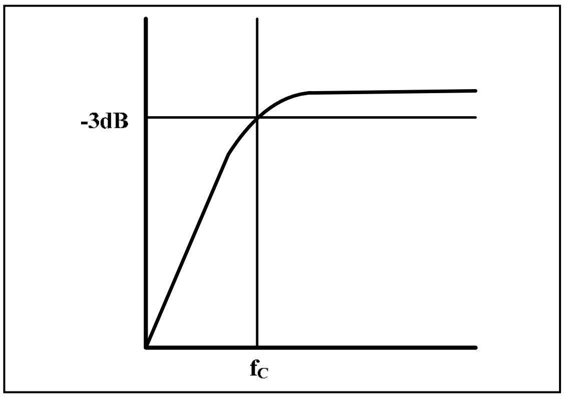


Figure 23 Corner Frequency

Ferrite Bead Selection

If the traces from the IS31AP2110 to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.

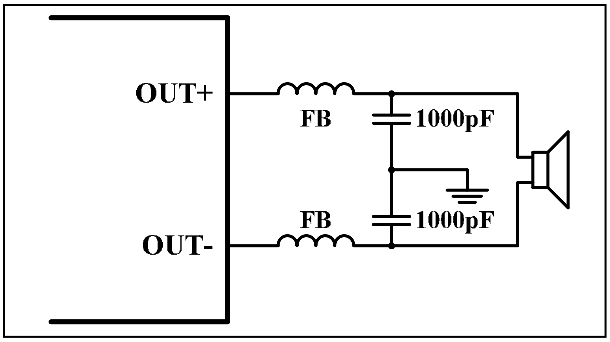


Figure 24 Typical Ferrite Bead Filter

Output LC Filter

If the traces from the IS31AP2110 to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 25 shows the typical output filter for 8Ω speaker with a cut-off frequency of 27kHz and Figure 26 shows the typical output filter for 4Ω speaker with a cut-off frequency of 27kHz.

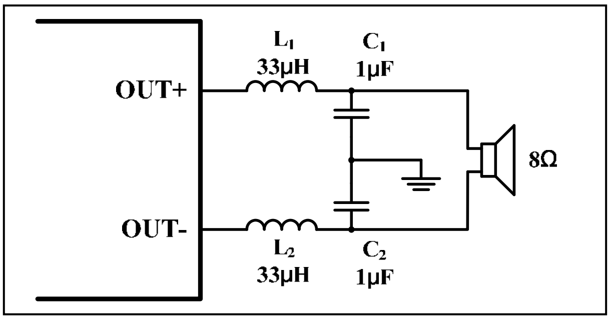


Figure 25 Typical LC Output Filter for 8Ω Speaker

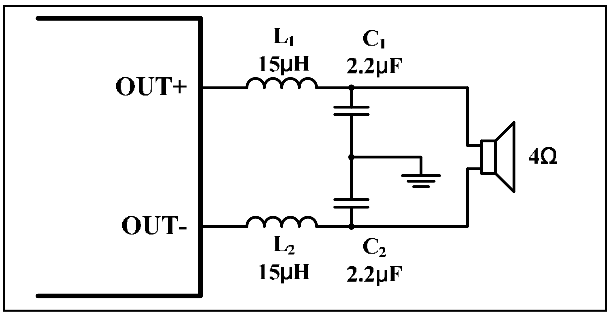


Figure 26 Typical LC Output Filter for 4Ω Speaker

Power Supply Decoupling Capacitor (C_S)

Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to VCCR/L and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1μF or 1μF as close as possible to the device VCCR/L leads works best. For low frequency noise filtering, a 100μF or greater capacitor (tantalum or electrolytic type) is suggested.

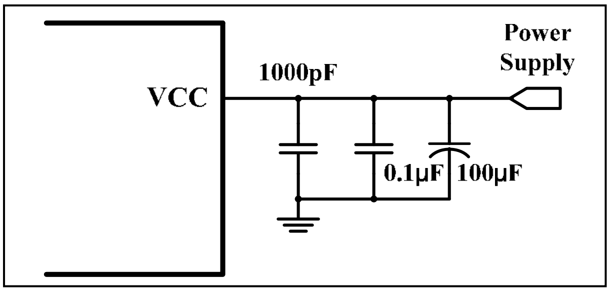


Figure 27 Recommended Power Supply Decoupling Capacitors

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

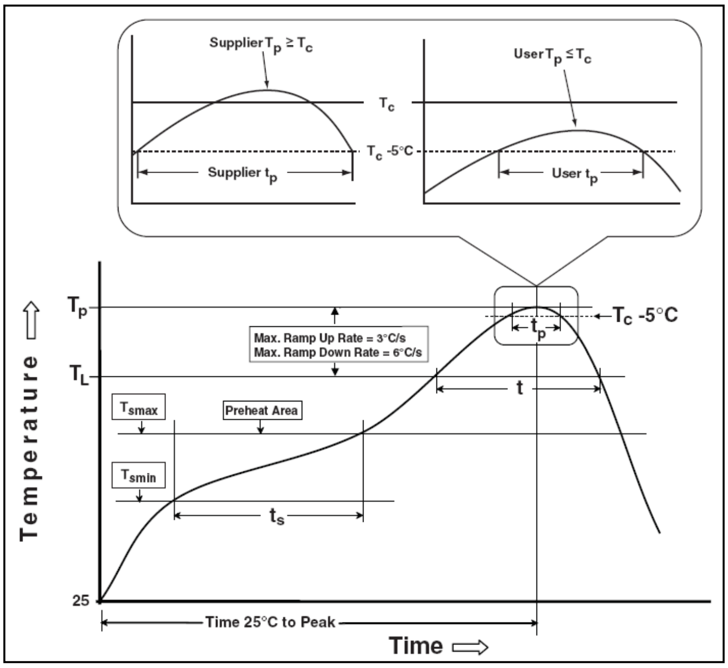
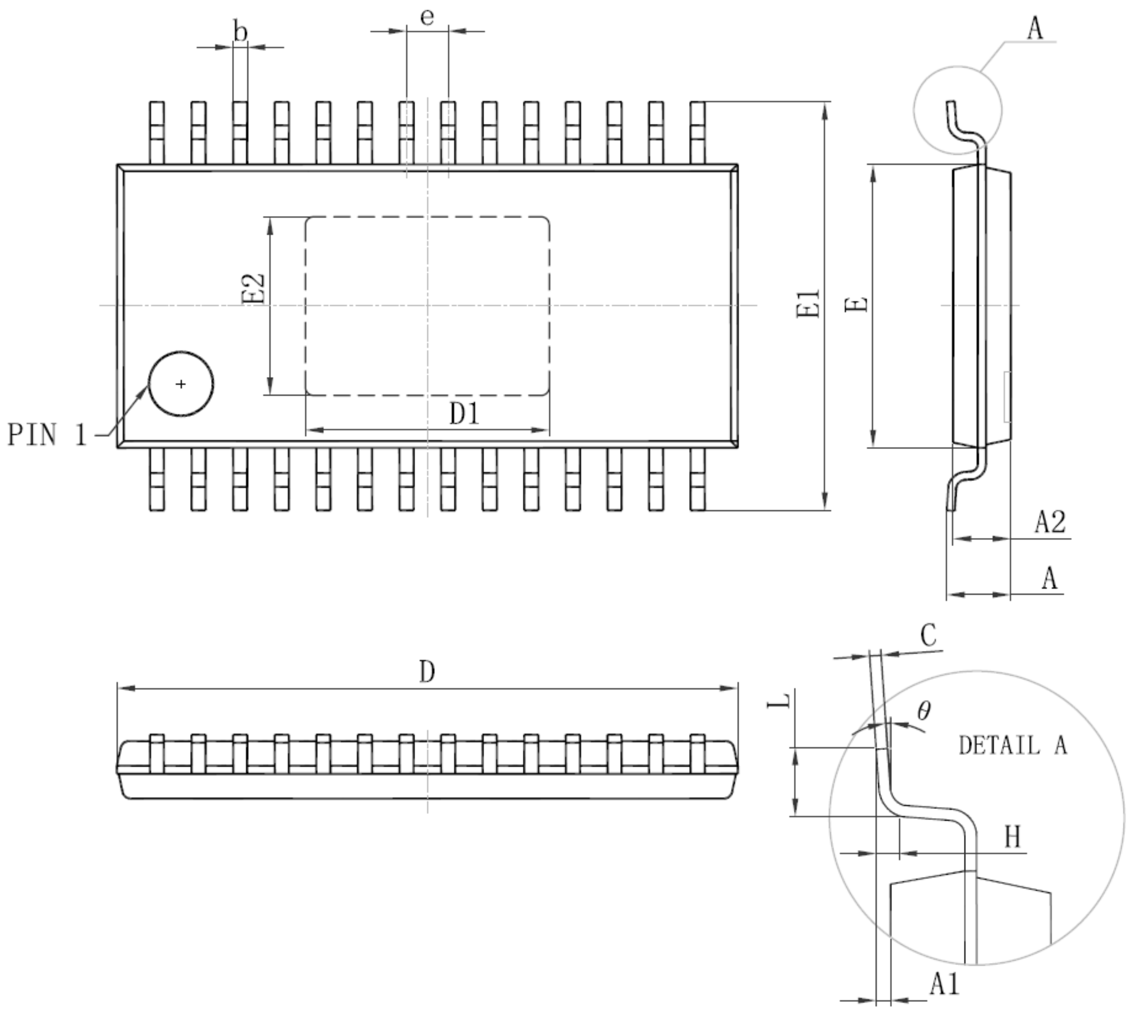


Figure 28 Classification Profile

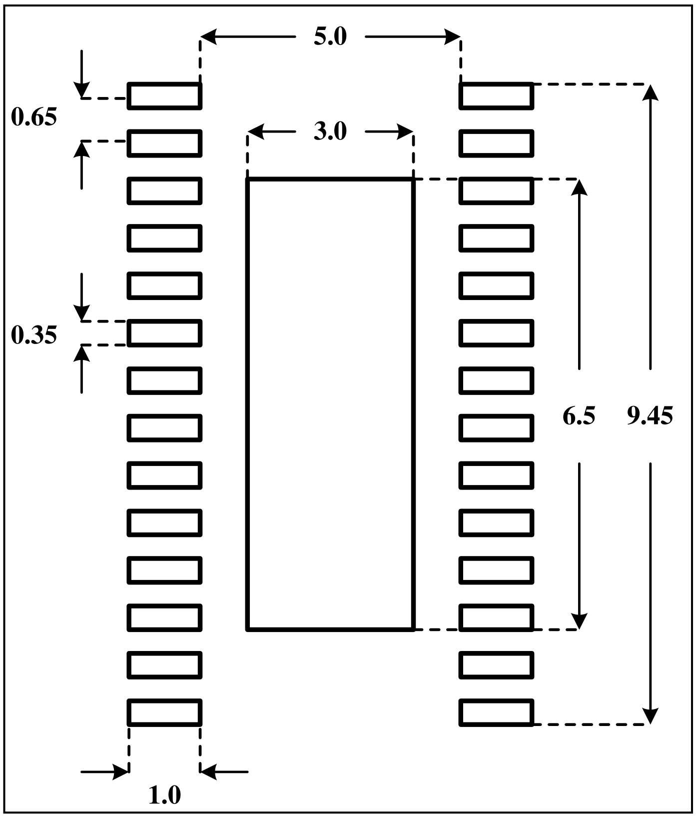
PACKAGE INFORMATION

eTSSOP-28



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	9.600	9.800	0.378	0.386
D1	3.710	3.910	0.146	0.154
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
E2	2.700	2.900	0.106	0.122
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.02	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2015.09.01
B	1. Update EC table 2. Add performance characteristics curves. 3. Add land pattern	2015.10.20