CY62148VN MoBL®

4 Mbit (512K x 8) Static RAM

Features

- Wide Voltage Range: 2.7V to 3.6V
- Ultra Low Active Power
- Low Standby Power
- TTL-compatible Inputs and Outputs
- Automatic Power Down when deselected
- CMOS for optimum Speed and Power
- Package available in a 32-Pin TSOP II and a 32-Pin SOIC Package

Functional Description

The CY62148VN is a high performance CMOS static RAM organized as 512K words by eight bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 99 percent when addresses are not toggling. The device can be put into standby mode when deselected ($\overline{CE}$ HIGH).

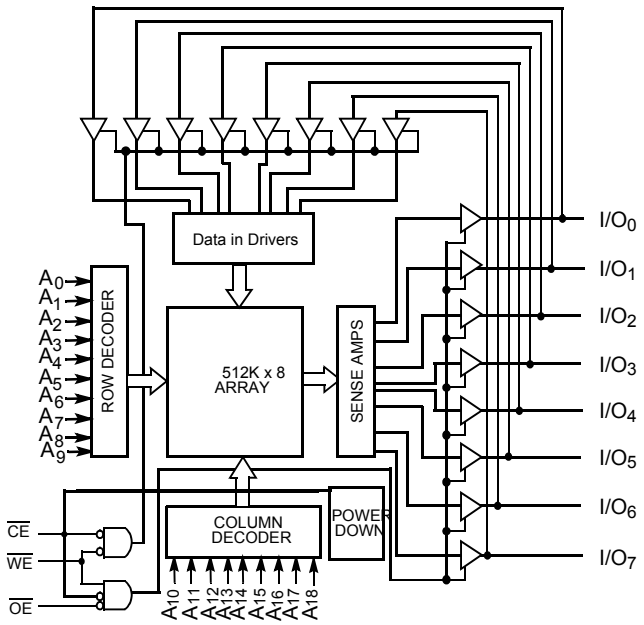
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

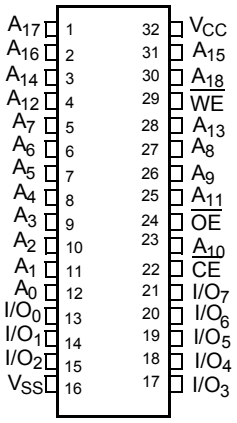
For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Logic Block Diagram



Pin Configuration

Figure 1. 32-Pin TSOP II/SOIC (Top View)



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation			
					Operating I_{CC}, (mA)		Standby I_{SB2}, (µA)	
	Min	Typ[1]	Max		Typ[1]	Max	Typ[1]	Max
CY62148VNLL	2.7	3.0	3.6	70	7	15	2	20

Note
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... 55°C to +125°C

Supply Voltage to Ground Potential.....–0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[2].....–0.5V to V_{CC} + 0.5V

DC Input Voltage[2] .....–0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	2.7V to 3.6V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		CY62148VN-70 Min.	CY62148VN-70 Typ.[1]	CY62148VN-70 Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{CC} = 2.7V	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	V_{CC} = 2.7V			0.4	V
V_{IH}	Input HIGH Voltage		V_{CC} = 3.6V	2.2		V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage		V_{CC} = 2.7V	–0.5		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	±1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1	+1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{RC} CMOS Levels	V_{CC} = 3.6V		7	15	mA
		I_{OUT} = 0 mA, f = 1 MHz CMOS Levels			1	2	mA
I_{SB1}	Automatic CE Power down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = f_{MAX}			2	20	µA
I_{SB2}	Automatic CE Power down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0	V_{CC} = 3.6V				

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.0V	6	pF
C_{OUT}	Output Capacitance		8	pF

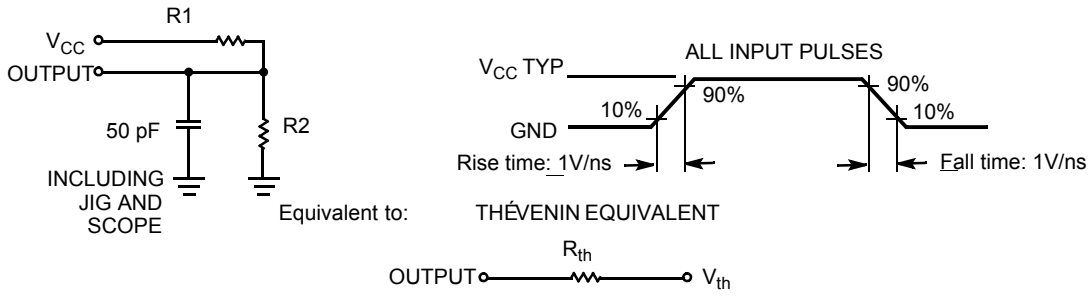
Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	SOIC	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, four-layer printed circuit board	TBD	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		TBD	TBD	°C/W

Note
2. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.

Figure 2. AC Test Loads and Waveforms



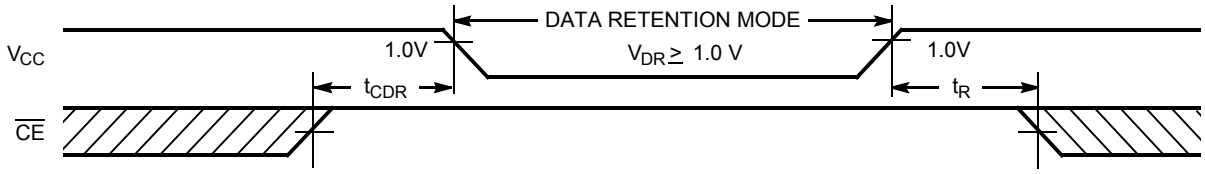
Parameters	3.0V	Unit
R1	1105	Ω
R2	1550	Ω
R_{TH}	645	Ω
V_{TH}	1.75V	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0		3.6	V
I_{CCDR}	Data Retention Current	V_{CC} = 1.0V, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$; No input may exceed V_{CC} + 0.3V		0.2	5.5	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time		0			ns
t_R[4]	Operation Recovery Time		t_{RC}			ns

Figure 3. Data Retention Waveform



Notes

3. Tested initially and after any design or process changes that may affect these parameters.
4. Full-device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 10$ µs or stable at $V_{CC(min.)} \geq 10$ µs.

Switching Characteristics

Over the Operating Range[5]

Parameter	Description	70 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		25	ns
t_{LZCE}	$\overline{CE}$ LOW and to Low Z[6]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		25	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power Up	0		ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power Down		70	ns
Write Cycle[8, 9]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	60		ns
t_{AW}	Address Setup to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{SD}	Data Setup to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	10		ns

Notes

5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle No. 1: Address Transition Controlled [10, 11]

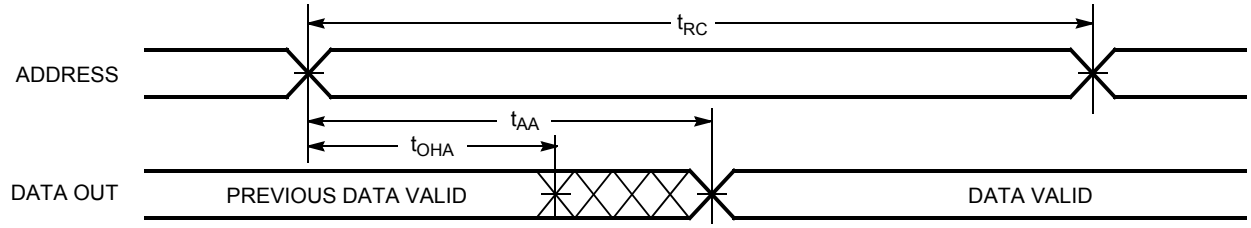


Figure 5. Read Cycle No. 2: $\overline{OE}$ Controlled [11, 12]

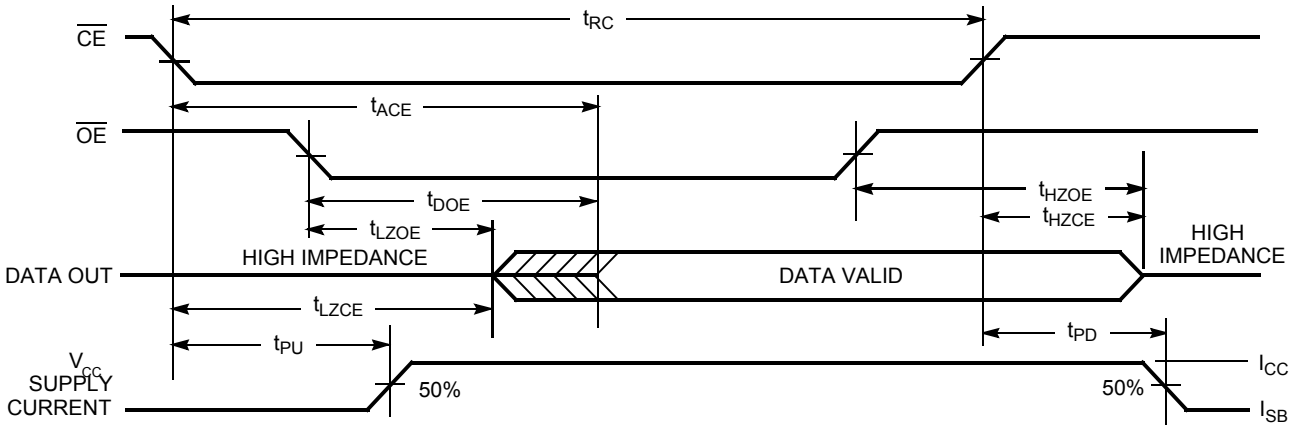
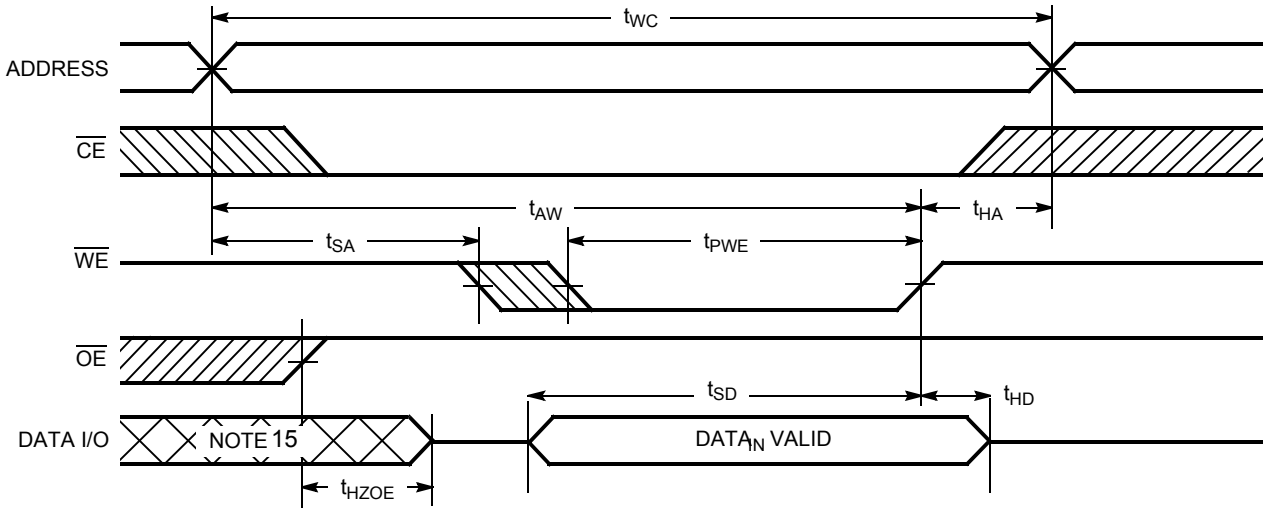


Figure 6. Write Cycle No 1: $\overline{WE}$ Controlled [8, 13, 14]



Notes
10. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid before or similar to $\overline{CE}$ transition LOW.
13. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle 2: $\overline{CE}$ Controlled [8, 13, 14]

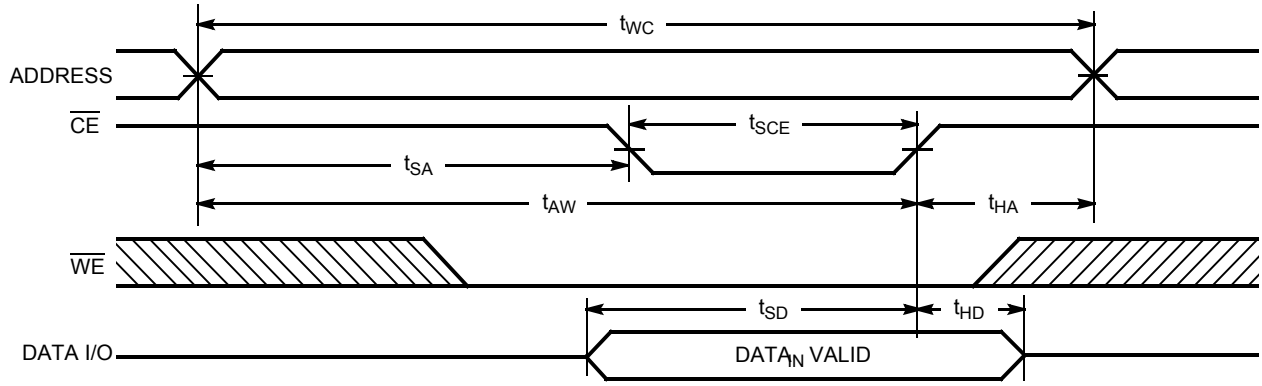
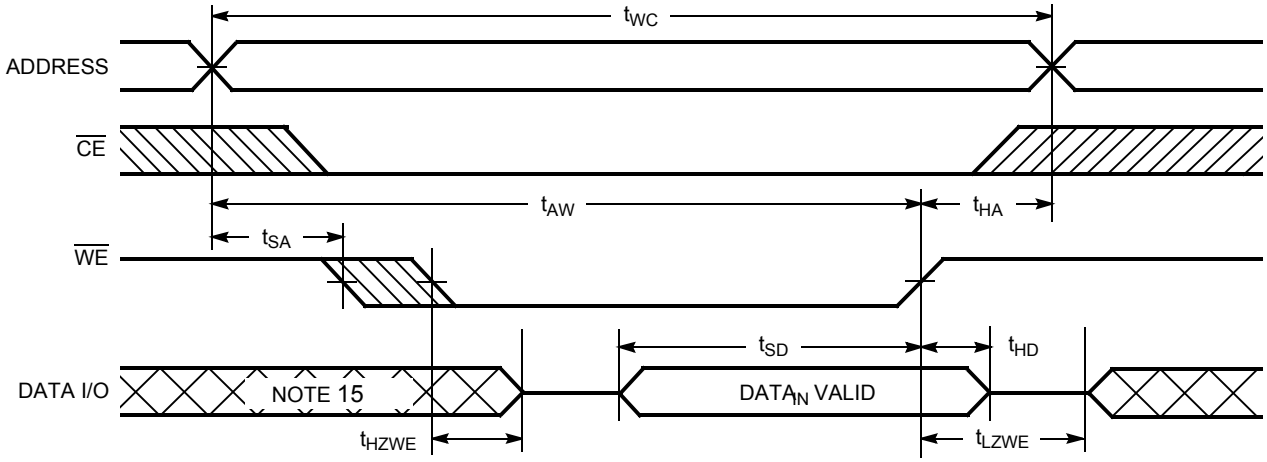
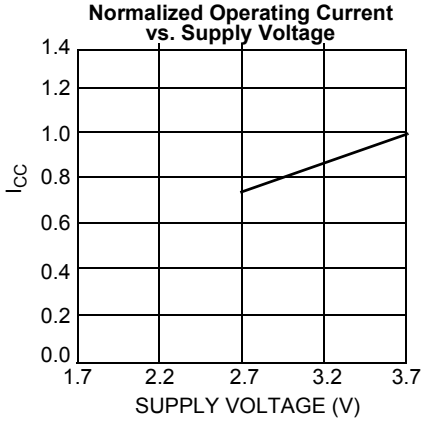


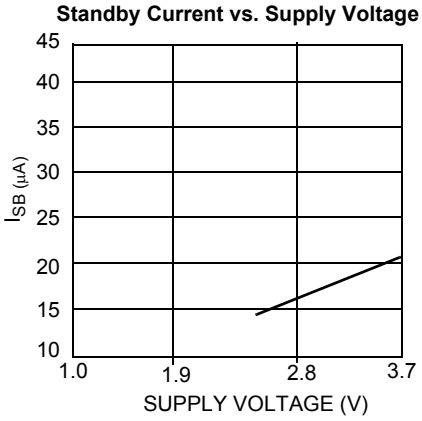
Figure 8. Write Cycle 3: $\overline{WE}$ controlled, $\overline{OE}$ LOW [14]

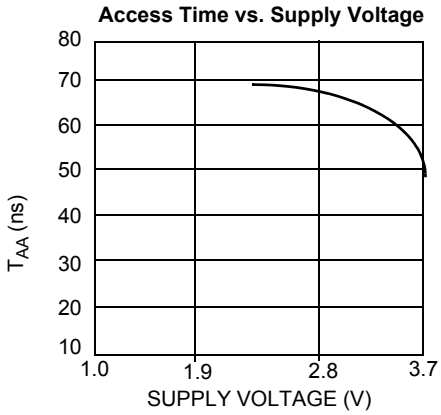


Note
15. During this period, the I/Os are in output state. Do not apply input signals.

Typical DC and AC Characteristics







Truth Table

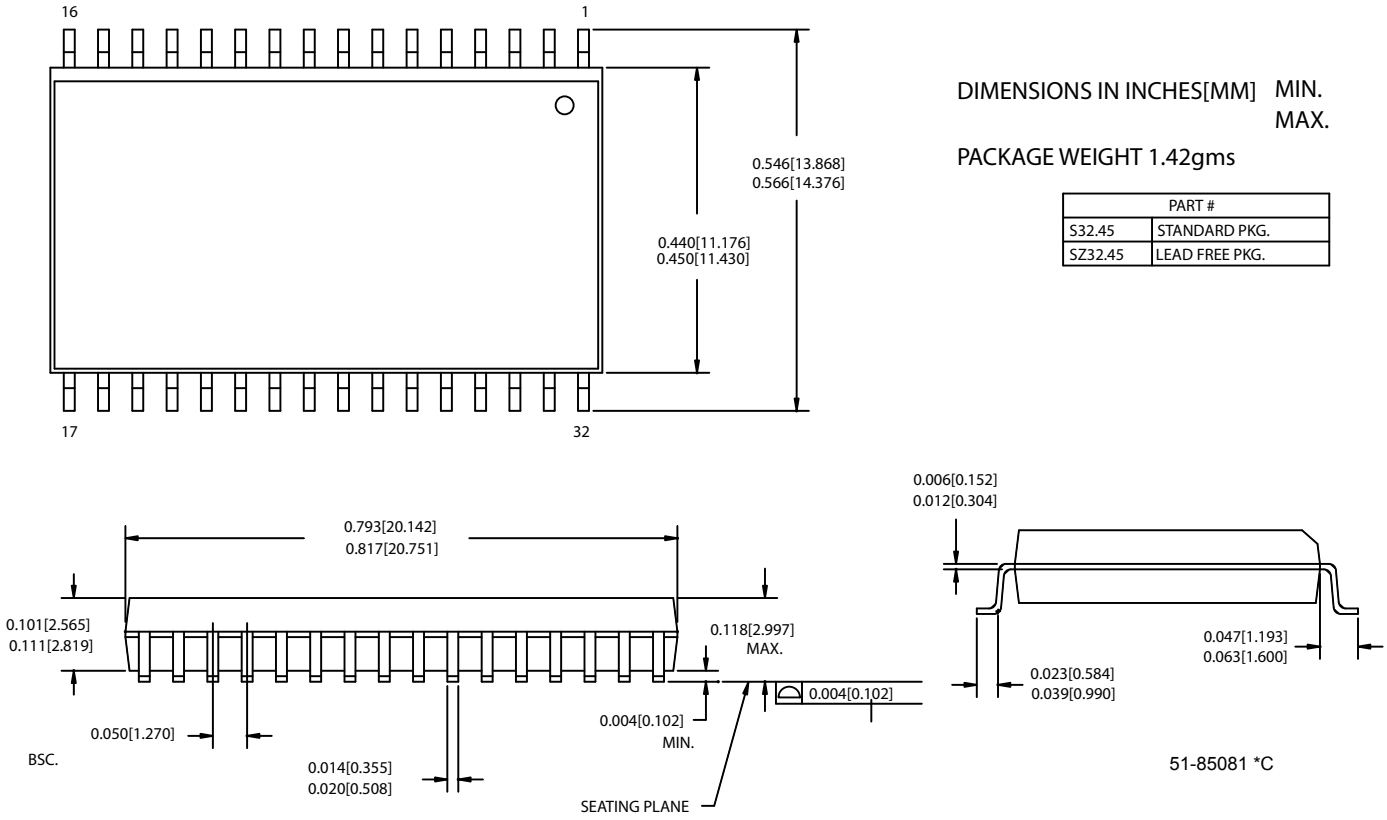
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High-Z	Deselect/Power down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62148VNLL-70ZSXI	51-85095	32-Pin TSOP II	Industrial
	CY62148VNLL-70SXI	51-85081	32-Pin (450-mil) Molded SOIC	

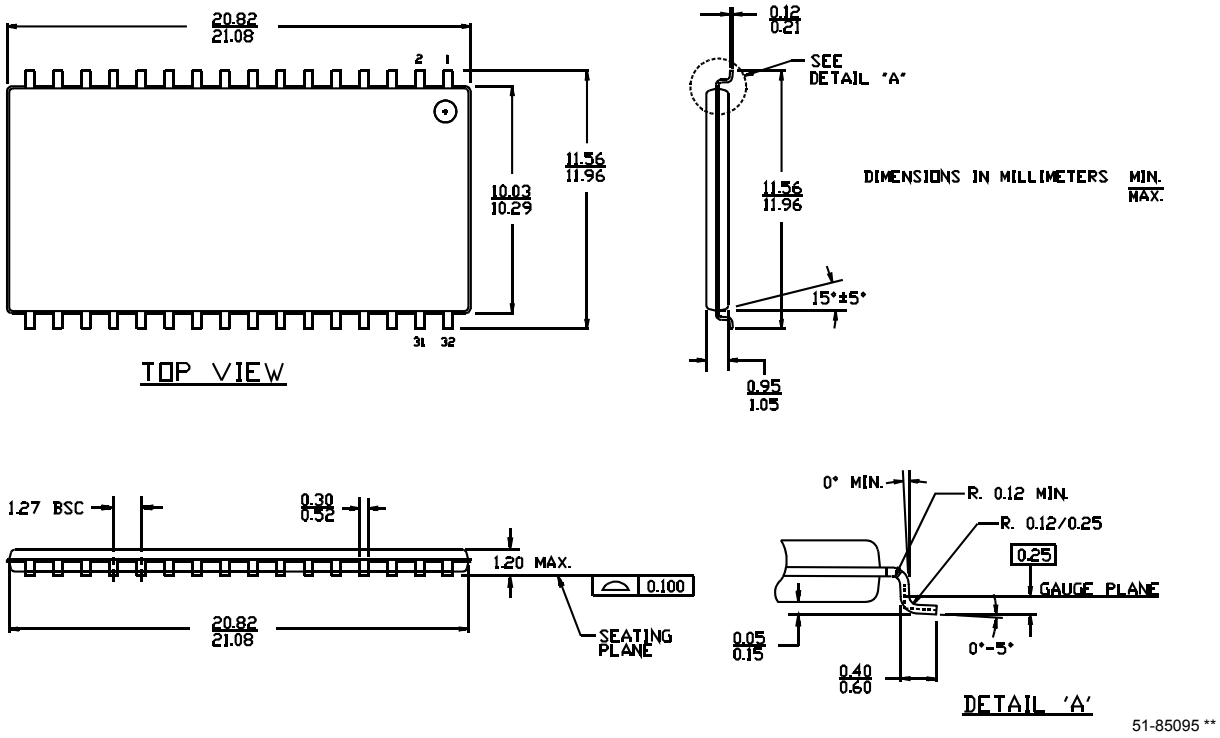
Package Diagrams

Figure 9. 32-Pin (450-mil) Molded SOIC, 51-85081



Package Diagrams (continued)

Figure 10. 32-Pin TSOP II, 51-85095



Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2761558	VKN	09/09/2009	New data sheet

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