# BT151-650LTF

SCR

Rev.01 - 07 February 2022

Product data sheet

## 1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a TO220 plastic package intended for use in applications requiring good bidirectional blocking voltage and high surge current capability and high junction temperature capability ($T_{j(max)}$ = 150 °C).

## 2. Features and benefits

- High junction operating temperature capability ($T_{j(max)}$ = 150 °C)
- High bidirectional blocking voltage capability
- Very high current surge capability
- High thermal cycling performance
- Planar passivated for voltage ruggedness and reliability

## 3. Applications

- Capacitive Discharge Ignition (CDI)
- Crowbar protection
- Inrush protection
- Motor control
- Voltage regulation

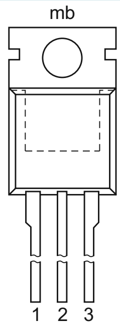
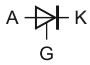
## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | - | 650 | V |
| $I_{T(RMS)}$ | RMS on-state current | half sine wave; $T_{mb}$ ≤ 135 °C; Fig. 1; Fig. 2; Fig. 3 | | - | - | 12 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 10 ms; Fig. 4; Fig. 5 | | - | - | 120 | A |
| | | half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 8.3 ms | | - | - | 132 | A |
| $T_j$ | junction temperature | | | - | - | 150 | °C |
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 7 | | 1.5 | - | 5 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 9 | | - | - | 20 | mA |
| $V_T$ | on-state voltage | $I_T$ = 12 A; $T_j$ = 25 °C; Fig. 10 | | - | - | 1.5 | V |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 436 V; $T_j$ = 150 °C; $R_{GK}$ = 100 Ω; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform | | 500 | - | - | V/µs |
| | | $V_{DM}$ = 436 V; $T_j$ = 150 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit | | 200 | - | - | V/µs |

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | K | cathode |  | <br>*sym037* |
| 2 | A | anode | | |
| 3 | G | gate | | |
| mb | A | mounting base; connected to anode | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package name | Orderable part number | Packing method | Small packing quantity | Package version | Package issue date |
|---|---|---|---|---|---|---|
| BT151-650LTF | TO220 | BT151-650LTFQ | Tube | 50 | SOT78 | 13-Jun-2008 |

## 7. Marking

**Table 4. Marking codes**

| Type number | Marking codes |
|---|---|
| BT151-650LTF | BT151<br>650LTF |

# 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | 650 | V |
| $V_{RRM}$ | repetitive peak reverse voltage | | | - | 650 | V |
| $I_{T(AV)}$ | average on-state current | half sine wave; $T_{mb}$ ≤ 135 °C; | | - | 7.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | half sine wave; $T_{mb}$ ≤ 135 °C; Fig. 1; Fig. 2; Fig. 3 | | - | 12 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 10 ms; Fig. 4; Fig. 5 | | - | 120 | A |
| | | half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 8.3 ms | | - | 132 | A |
| $I^2t$ | $I^2t$ for fusing | $t_p$ = 10 ms; sine wave | | - | 72 | $A^2s$ |
| $dI_T/dt$ | rate of rise of on-state current | $I_G$ = 10 mA | | - | 150 | A/µs |
| $I_{GM}$ | peak gate current | | | - | 2 | A |
| $P_{GM}$ | peak gate power | | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | | - | 1 | W |
| $T_{stg}$ | storage temperature | | | -40 | 150 | °C |
| $T_j$ | junction temperature | | | - | 150 | °C |

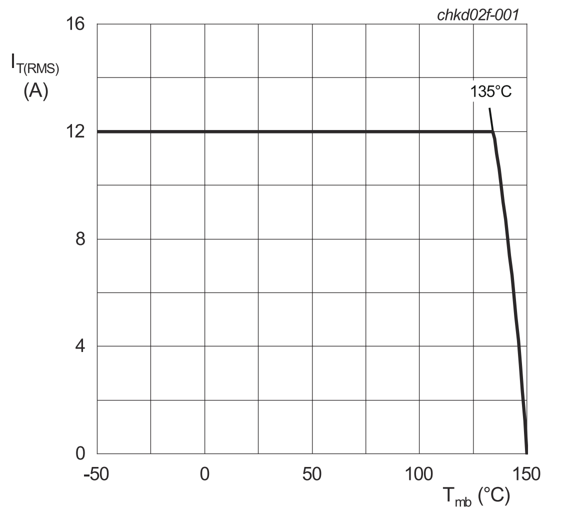
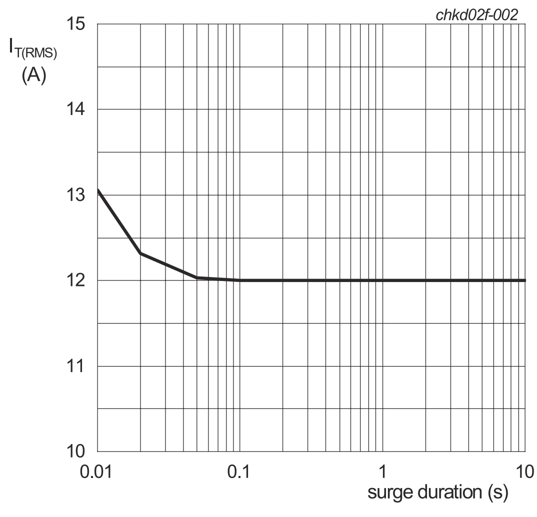
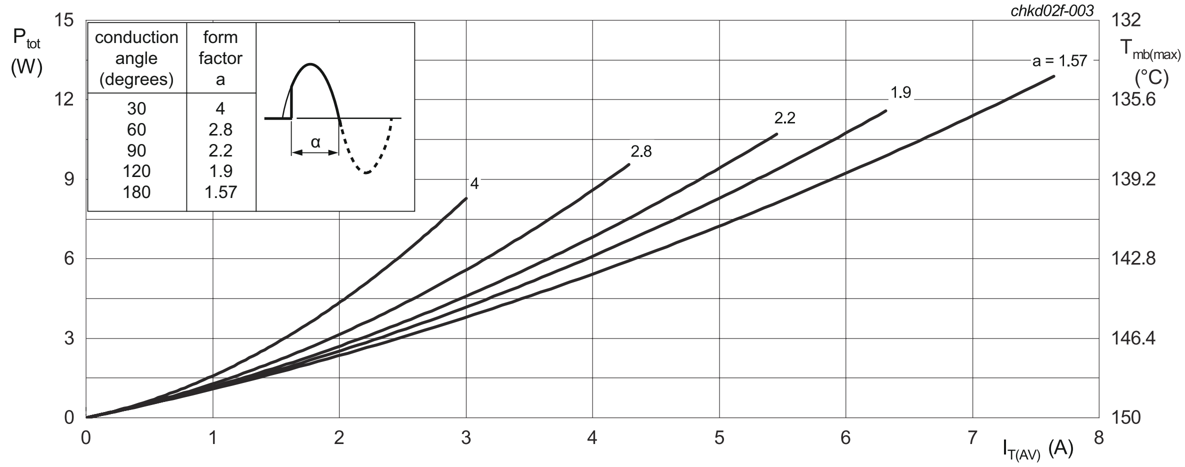



**Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values**




f = 50 Hz; $T_{mb}$ = 135 °C

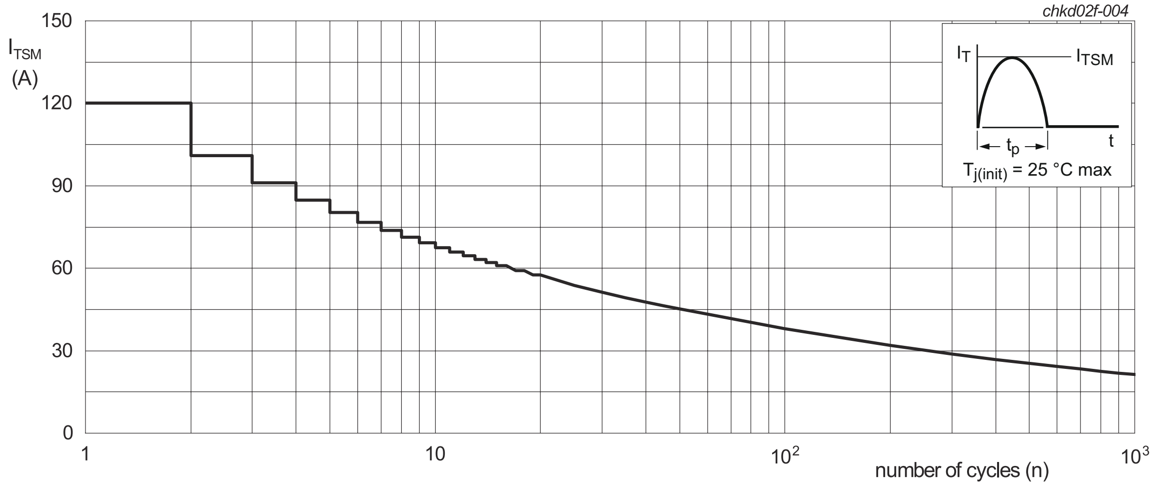
**Fig. 2. RMS on-state current as a function of surge duration; maximum values**




α = conduction angle

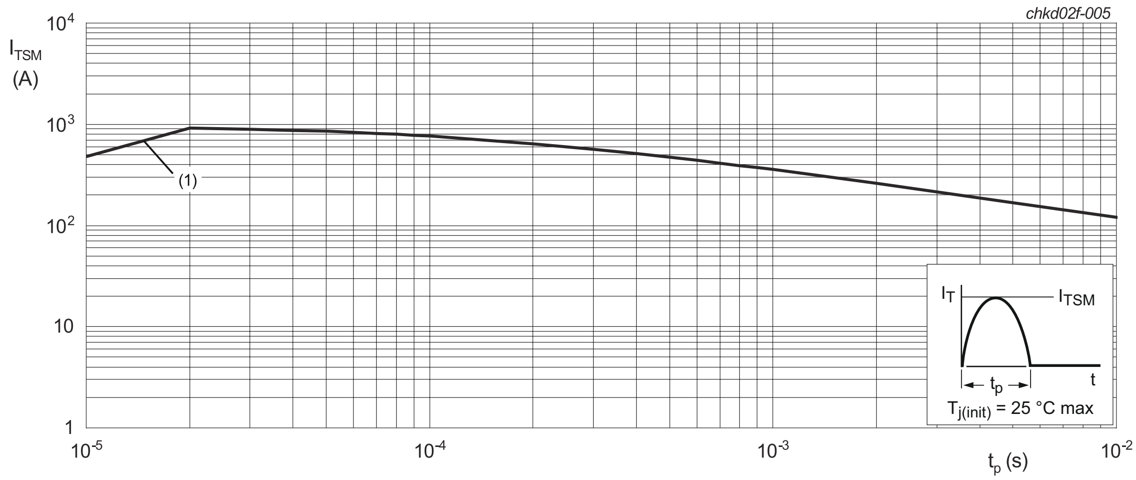
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

**Fig. 3. Total power dissipation as a function of average on-state current; maximum values**




f = 50 Hz

**Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**




$t_p \leq 10$ ms ;

(1) $dI_T/dt$ limit

**Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values**

# 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 6 | | - | - | 1.2 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | in free air | | - | 60 | - | K/W |

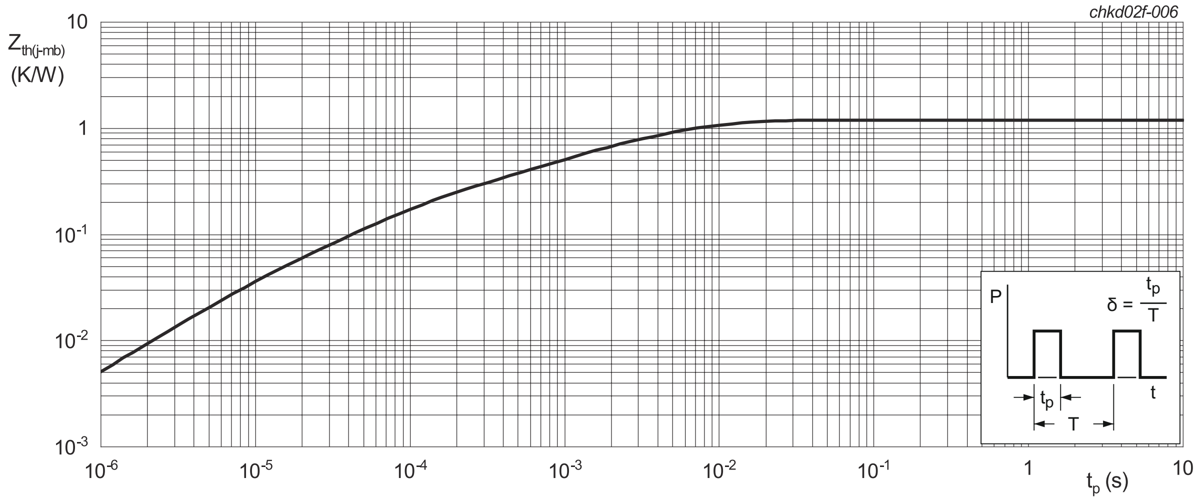



**Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 10. Characteristics

**Table 8. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 7 | | 1.5 | - | 5 | mA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_G$ = 0.1 A; $T_j$ = 25 °C; Fig. 8 | | - | - | 40 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 9 | | - | - | 20 | mA |
| $V_T$ | on-state voltage | $I_T$ = 12 A; $T_j$ = 25 °C; Fig. 10 | | - | - | 1.5 | V |
| $V_{GT}$ | gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 11 | | - | 0.8 | 1 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 150 °C | | 0.25 | 0.45 | - | V |
| $V_{GR}$ | gate reverse voltage | $I_{RG}$ = 100 mA | | 10 | - | - | V |
| $I_D$ | off-state current | $V_D$ = 650 V; $T_j$ = 25 °C | | - | - | 10 | µA |
| | | $V_D$ = 650 V; $T_j$ = 150 °C | | - | - | 2 | mA |
| $I_R$ | reverse current | $V_D$ = 650 V; $T_j$ = 25 °C | | - | - | 10 | µA |
| | | $V_D$ = 650 V; $T_j$ = 150 °C | | - | - | 2 | mA |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 436 V; $T_j$ = 150 °C; $R_{GK}$ = 100 Ω; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform | | 500 | - | - | V/µs |
| | | $V_{DM}$ = 436 V; $T_j$ = 150 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit | | 200 | - | - | V/µs |
| $t_{gt}$ | gate-controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = 600 V; $I_G$ = 20 mA; $(dI_G/dt)_M$ = 5 A/µs; $T_j$ = 25 °C | | | 2 | - | µs |
| $t_q$ | commutated turn-off time | $I_{TM}$ = 2 A; $t_p$ = 50 µs; $dV_D/dt$ = 5 V/µs; dI/dt = 30 A/µs | | | - | 12 | µs |

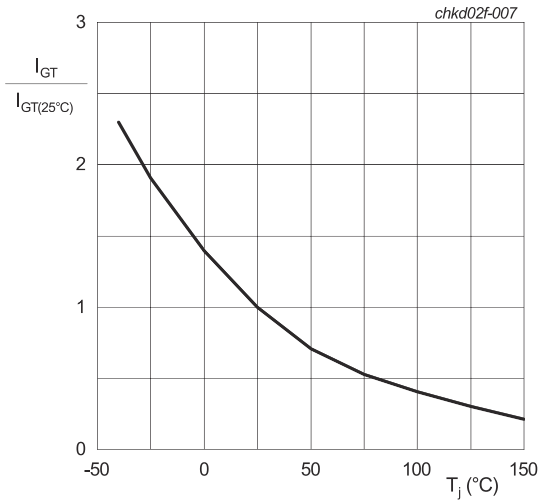



Fig. 7. Normalized gate trigger current as a function of junction temperature

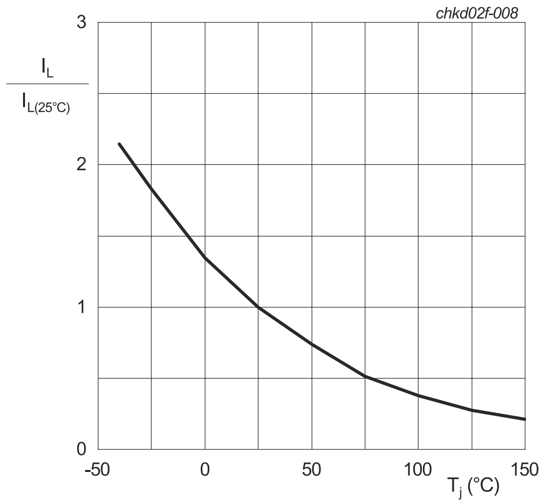



Fig. 8. Normalized latching current as a function of junction temperature

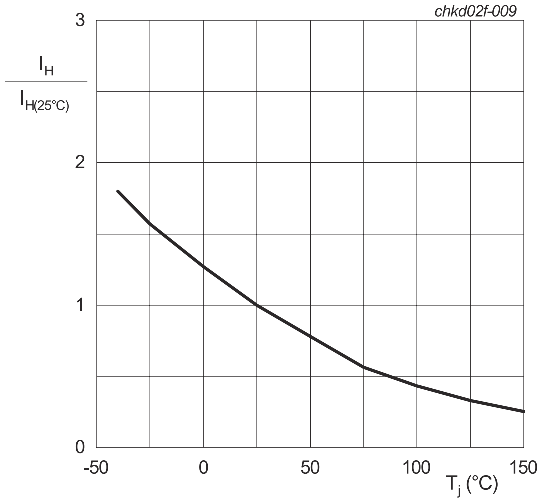
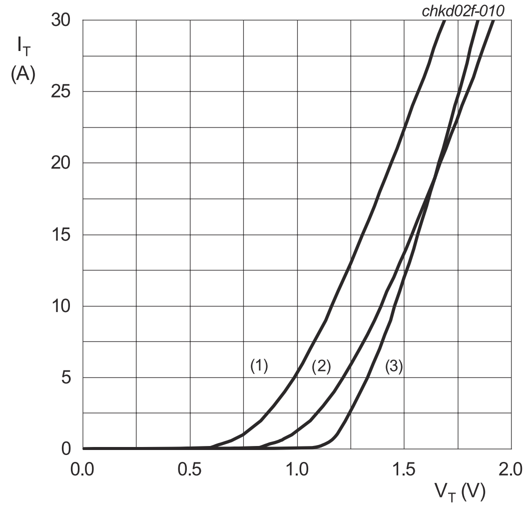



Fig. 9. Normalized holding current as a function of junction temperature




$V_o$ = 0.993 V; $R_s$ = 0.0368 Ω
(1) $T_j$ = 150 °C; typical values
(2) $T_j$ = 150 °C; maximum values
(3) $T_j$ = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

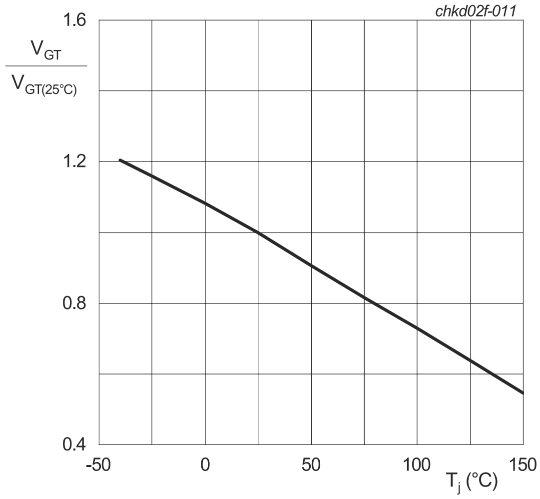
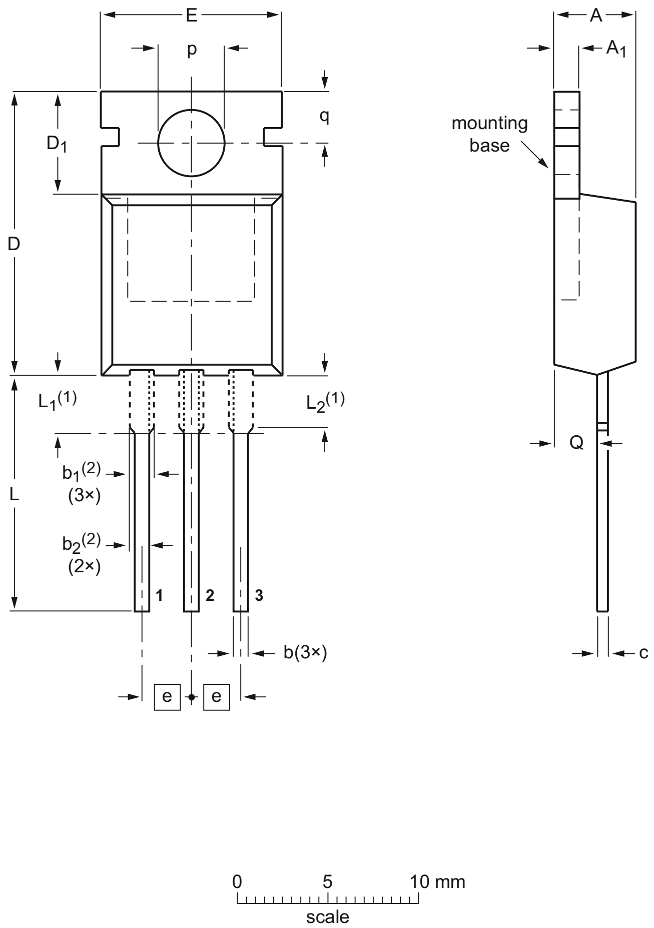



Fig. 11. Normalized gate trigger voltage as a function of junction temperature

# 11. Package outline

**Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB** **SOT78**

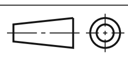



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$(2) | $b_2$(2) | c | D | $D_1$ | E | e | L | $L_1$(1) | $L_2$(1) max. | p | q | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.7<br>4.1 | 1.40<br>1.25 | 0.9<br>0.6 | 1.6<br>1.0 | 1.3<br>1.0 | 0.7<br>0.4 | 16.0<br>15.2 | 6.6<br>5.9 | 10.3<br>9.7 | 2.54 | 15.0<br>12.8 | 3.30<br>2.79 | 3.0 | 3.8<br>3.5 | 3.0<br>2.7 | 2.6<br>2.2 |

**Notes**

1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT78 | | 3-lead TO-220AB | SC-46 | |  | ~~08-04-23~~<br>08-06-13 |

# 12. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ween-semi.com.

## Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. WeEn Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local WeEn Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between WeEn Semiconductors and its customer, unless WeEn Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the WeEn Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, WeEn Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. WeEn Semiconductors takes no responsibility for the content in this document if provided by an information source outside of WeEn Semiconductors.

In no event shall WeEn Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, WeEn Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of WeEn Semiconductors.

**Right to make changes** — WeEn Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — WeEn Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an WeEn Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. WeEn Semiconductors and its suppliers accept no liability for inclusion and/or use of WeEn Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. WeEn Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using WeEn Semiconductors products, and WeEn Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the WeEn Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

WeEn Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using WeEn Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). WeEn does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific WeEn Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. WeEn Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without WeEn Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond WeEn Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies WeEn Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond WeEn Semiconductors' standard warranty and WeEn Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

# 13. Contents





For more information, please visit: http://www.ween-semi.com
For sales office addresses, please send an email to: salesaddresses@ween-semi.com
**Date of release: 07 February 2022**