74LV03

Quad 2-input NAND gate

Rev. 4 — 31 August 2017 Product data sheet

1 General description

The 74LV03 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT03.

The 74LV03 provides the 2-input NAND function.

The 74LV03 has open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF-state, i.e., when one input is LOW, the output may be pulled to any voltage between GND and $V_{O(max)}$. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

2 Features and benefits

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V @ V_{CC} = 3.3 V, T_{amb} = 25 °C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V @ V_{CC} = 3.3 V, T_{amb} = 25 °C
- Level shifter capability
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV03D	-40 °C to + 125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

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4 Functional diagram

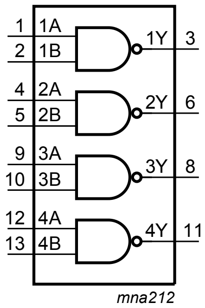

Figure 1. Logic symbol

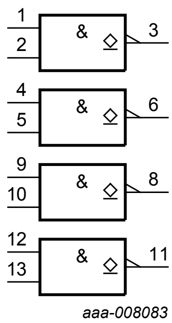

Figure 2. IEC logic symbol

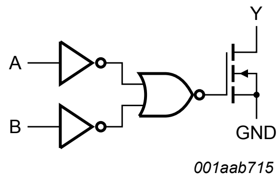

Figure 3. Logic diagram (one gate)

5 Pinning information

5.1 Pinning

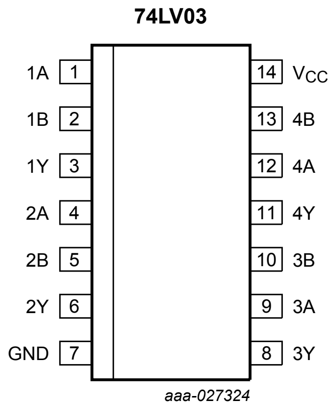

Figure 4. Pin configuration SO14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

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6 Functional description

Table 3. Function table [1]

Input		Output
nA	**nB**	**nY**
L	L	Z
L	H	Z
H	L	Z
H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
Z = high-impedance OFF-state.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V [1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±50	mA
I_O	output current	$V_O = -0.5$ V to (V_{CC} + 0.5 V)	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

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8 Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V	-	-	50	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

9 Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 μA; V_{CC} = 1.2 V	-	0	-	-	-	V
		I_O = 100 μA; V_{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 3.0 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 4.5 V	-	0	0.2	-	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	0.35	0.55	-	0.65	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	1.0	-	1.0	μA

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Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	
I_{OZ}	OFF-state output current	per input pin; V_{CC} = 2.0 V to 3.6 V; $V_I = V_{IL}$; $V_O = V_{CC}$ or GND; other inputs at V_{CC} or GND		-	-	±5.0	-	±10	μA
		per input pin; V_{CC} = 2.0 V to 3.6 V; $V_I = V_{IL}$; V_O = 6.0 V; other inputs at V_{CC} or GND	[2]	-	-	±10.0	-	±20	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V		-	-	20.0	-	40	μA
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC}$ - 0.6 V; V_{CC} = 2.7 V to 3.6 V		-	-	500	-	850	μA
C_I	input capacitance			-	3.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.
[2] The maximum operating output voltage ($V_{O(max)}$) is 6.0 V.

10 Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; For test circuit see Figure 6.

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	nA, nB to nY; see Figure 5	[2]						
		V_{CC} = 1.2 V		-	50	-	-	-	ns
		V_{CC} = 2.0 V		-	17	26	-	31	ns
		V_{CC} = 2.7 V		-	13	19	-	23	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	8	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	10	16	-	19	ns
		V_{CC} = 4.5 V to 5.5 V		-	-	13	-	16	ns
C_{PD}	power dissipation capacitance	C_L = 0 pF; $R_L = \infty\ \Omega$; V_I = GND to V_{CC}	[4]	-	4	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLZ} and t_{PZL}.
[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V).
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz,
f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in V
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

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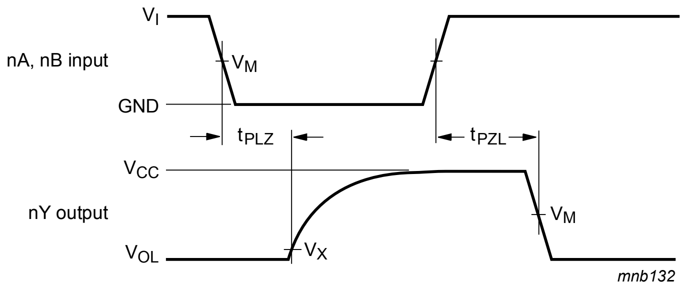
10.1 Waveforms and test circuit



Measurement points are given in Table 8

V_{OL} is a typical voltage output level that occurs with the output load.

Figure 5. Inputs nA and nB to output nY propagation delay times

Table 8. Measurement points

Supply voltage	Input	Output	
V_{CC}	V_M	V_X	V_M
≤ 2.7 V	0.5 × V_{CC}	V_{OL} + 0.1 V	0.5 × V_{CC}
2.7 V to 3.6 V	1.5 V	V_{OL} + 0.3 V	1.5 V
≥ 4.5 V	0.5 × V_{CC}	V_{OL} + 0.1 V	0.5 × V_{CC}

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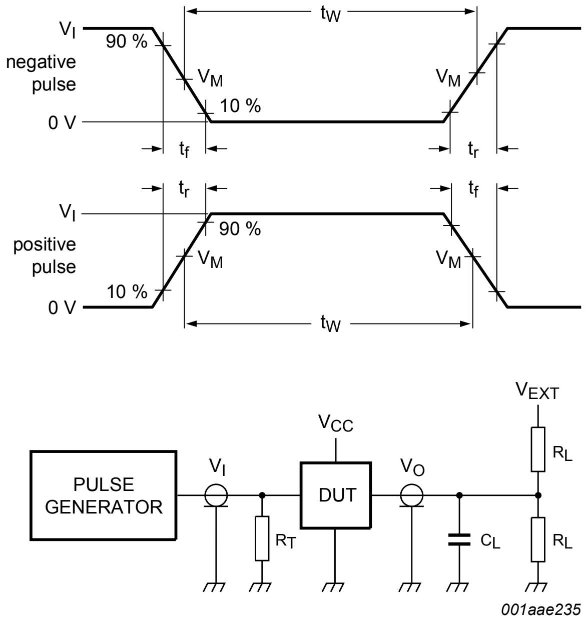

Test data is given in Table 9

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Figure 6. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLZ}, t_{PZL}
≤ 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	2 × V_{CC}
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	1 kΩ	2 × V_{CC}
≥ 4.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	2 × V_{CC}

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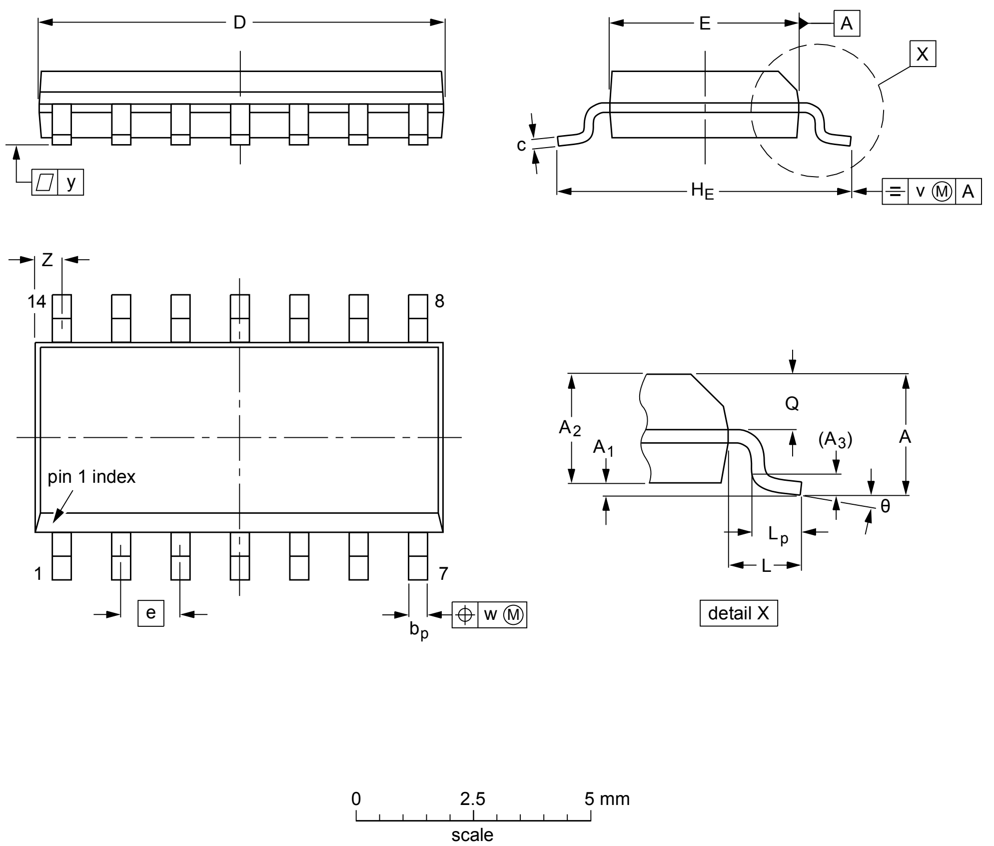
11 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Figure 7. Package outline SOT108-1 (SO14)

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12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV03 v.4	20170831	Product data sheet	-	74LV03 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74LV03 v.3	20030303	Product data sheet	ECN 853-1963 29494	74LV03 v.2
Modifications:	• Deleted DIL, SSOP and TSSOP package ordering and package outlines (discontinued options). • Corrected power dissipation formula.			
74LV03 v.2	19980420	Product specification	ECN 853-1963 19257	74LV03 v.1
74LV03 v.1	19970328	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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