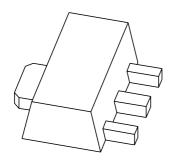
# **DISCRETE SEMICONDUCTORS**

# DATA SHEET



PBSS4540X 40 V, 5 A NPN low  $V_{CEsat}$  (BISS) transistor

Product specification Supersedes data of 2004 Jun 11





# 40 V, 5 A NPN low V<sub>CEsat</sub> (BISS) transistor

# **PBSS4540X**

## **FEATURES**

- High hFE and low VCEsat at high current operation
- High collector current capability: I<sub>C</sub> maximum 4 A
- High efficiency leading to less heat generation.

## **APPLICATIONS**

- Medium power peripheral drivers (e.g. fan and motor)
- Strobe flash units for DSC and mobile phones
- Inverter applications (e.g. TFT displays)
- · Power switch for LAN and ADSL systems
- Medium power DC-to-DC conversion
- · Battery chargers.

#### **DESCRIPTION**

NPN low V<sub>CEsat</sub> transistor in a medium power SOT89 (SC-62) package.

PNP complement: PBSS5540X.

## **MARKING**

TYPE NUMBER	MARKING CODE(1)
PBSS4540X	*1B

## Note

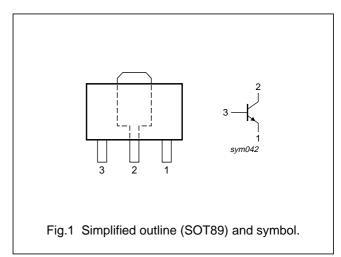
- 1. \* = p: made in Hong Kong.
  - \* = t: made in Malaysia.
  - \* = W: made in China.

## **QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	40	V
I <sub>C</sub>	collector current (DC)	4	Α
I <sub>CM</sub>	peak collector current	10	Α
R <sub>CEsat</sub>	equivalent on-resistance	71	mΩ

## **PINNING**

PIN	DESCRIPTION	
1	emitter	
2	collector	
3	base	



## **ORDERING INFORMATION**

TYPE NUMBER		PACKAGE		
TIPE NOMBER	NAME DESCRIPTION			
PBSS4540X	SC-62	SC-62 plastic surface mounted package; collector pad for good heat transfer; 3 leads		

# 40 V, 5 A NPN low $V_{CEsat}$ (BISS) transistor

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## **LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

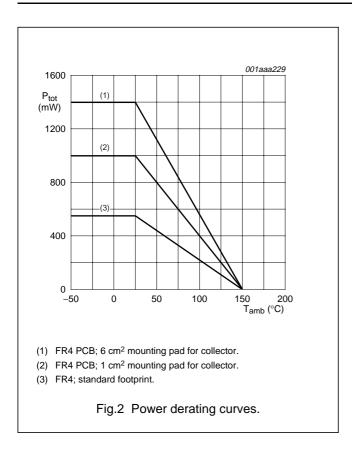
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT	
V <sub>CBO</sub>	collector-base voltage	open emitter		40	V	
V <sub>CEO</sub>	collector-emitter voltage	open base	_	40	V	
V <sub>EBO</sub>	emitter-base voltage	open collector	_	6	V	
I <sub>C</sub>	collector current (DC)		_	4	А	
I <sub>CRM</sub>	maximum repetitive collector current	notes 1 and 2	_	5	А	
I <sub>CM</sub>	peak collector current	$t_p \le 1 \text{ ms}$	_	10	А	
I <sub>B</sub>	base current (DC)		_	1	А	
I <sub>BM</sub>	peak base current	t <sub>p</sub> ≤ 1 ms	_	2	А	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C				
		notes 1 and 2	_	2.5	W	
		note 2	_	0.55	W	
		note 3	_	1	W	
		note 4	_	1.4	W	
		note 5	_	1.6	W	
T <sub>stg</sub>	storage temperature		-65	+150	°C	
Tj	junction temperature		_	150	°C	
T <sub>amb</sub>	operating ambient temperature		-65	+150	°C	

## **Notes**

- 1. Operated under pulsed conditions; pulse width  $t_p \le 10$  ms; duty cycle  $\delta \le 0.2$ .
- 2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
- Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm<sup>2</sup>.
- 4. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm<sup>2</sup>.
- 5. Device mounted on a 7 cm² ceramic printed-circuit board, 1 cm² single-sided copper and tin-plated. For other mounting conditions, see *"Thermal considerations for SOT89 in the General Part of associated Handbook"*.

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# 40 V, 5 A NPN low V<sub>CEsat</sub> (BISS) transistor

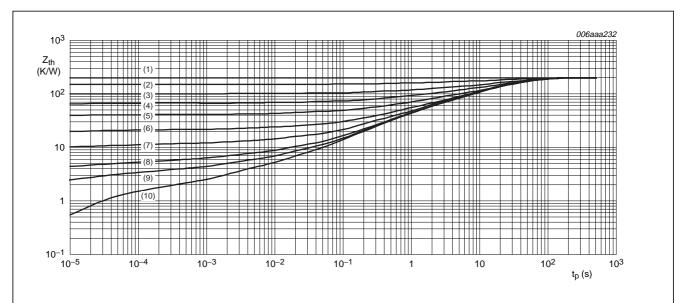
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## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-a)</sub>	from junction to ambient	in free air		
		notes 1 and 2	50	K/W
		note 2	225	K/W
		note 3	125	K/W
		note 4	90	K/W
		note 5	80	K/W
R <sub>th(j-s)</sub>	from junction to soldering point		16	K/W

#### **Notes**

- Operated under pulsed conditions; pulse width  $t_p \leq 10$  ms; duty cycle  $\delta \leq 0.2.$
- Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint. 2.
- Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm<sup>2</sup>.
- Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm<sup>2</sup>.
- 5. Device mounted on a 7 cm<sup>2</sup> ceramic printed-circuit board, 1 cm<sup>2</sup> single-sided copper and tin-plated. For other mounting conditions, see "Thermal considerations for SOT89 in the General Part of associated Handbook".



Mounted on FR4 printed-circuit board; standard footprint.

- (1)  $\delta = 1$ .
- (3)  $\delta = 0.5$ .
- (5)  $\delta = 0.2$ .
- (7)  $\delta = 0.05$ .
- (9)  $\delta = 0.01$ .

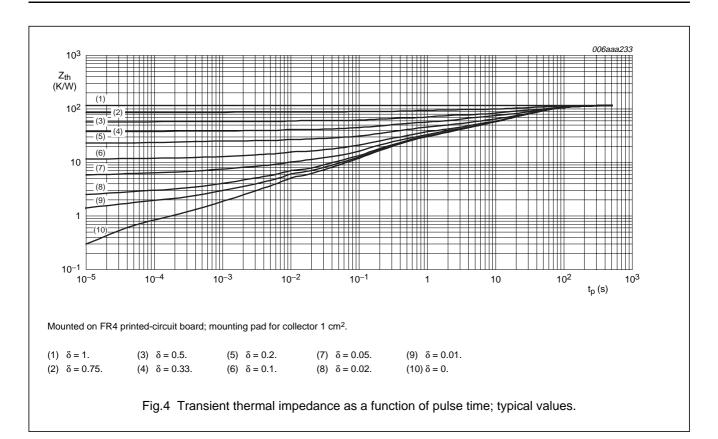
- (2)  $\delta = 0.75$ .
- (4)  $\delta = 0.33$ .

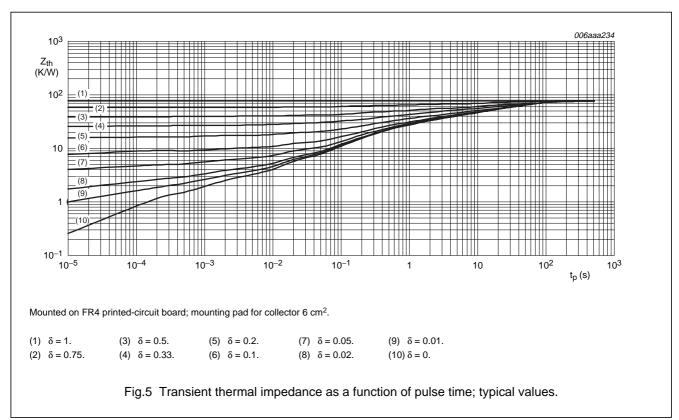
- (8)  $\delta = 0.02$ .
- (10)  $\delta = 0$ .

Fig.3 Transient thermal impedance as a function of pulse time; typical values.

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# 40 V, 5 A NPN low $V_{CEsat}$ (BISS) transistor

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# **CHARACTERISTICS**

 $T_{amb}$  = 25  $^{\circ}C$  unless otherwise specified.

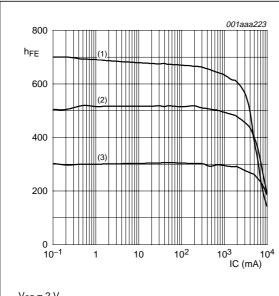
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>CBO</sub>	collector-base cut-off	V <sub>CB</sub> = 30 V; I <sub>E</sub> = 0 A	_	_	100	nA
	current	$V_{CB} = 30 \text{ V}; I_E = 0 \text{ A}; T_j = 150 ^{\circ}\text{C}$	_	_	50	μΑ
I <sub>CES</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 30 V; V <sub>BE</sub> = 0 V	_	_	0.1	μΑ
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A	_	_	100	nA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 2 V; I <sub>C</sub> = 0.5 A	300	_	_	
		V <sub>CE</sub> = 2 V; I <sub>C</sub> = 1 A; note 1	300	_	_	
		V <sub>CE</sub> = 2 V; I <sub>C</sub> = 2 A; note 1	250	_	_	
		V <sub>CE</sub> = 2 V; I <sub>C</sub> = 5 A; note 1	100	_	_	
V <sub>CEsat</sub> collector-emitte voltage	collector-emitter saturation	I <sub>C</sub> = 0.5 A; I <sub>B</sub> = 5 mA	_	_	90	mV
	voltage	I <sub>C</sub> = 1 A; I <sub>B</sub> = 10 mA	_	_	120	mV
		I <sub>C</sub> = 2 A; I <sub>B</sub> = 200 mA; note 1	_	_	150	mV
		I <sub>C</sub> = 4 A; I <sub>B</sub> = 200 mA; note 1	_	_	290	mV
		I <sub>C</sub> = 5 A; I <sub>B</sub> = 500 mA; note 1	_	_	355	mV
R <sub>CEsat</sub>	equivalent on-resistance	I <sub>C</sub> = 5 A; I <sub>B</sub> = 500 mA; note 1	_	40	71	mΩ
V <sub>BEsat</sub>	base-emitter saturation	I <sub>C</sub> = 4 A; I <sub>B</sub> = 200 mA; note 1	_	_	1.1	V
	voltage	I <sub>C</sub> = 5 A; I <sub>B</sub> = 500 mA; note 1	_	_	1.2	V
V <sub>BEon</sub>	base-emitter turn-on voltage	$V_{CE} = 2 \text{ V}; I_{C} = 2 \text{ A}$	_	_	1.1	V
f <sub>T</sub>	transition frequency	V <sub>CE</sub> = 10 V; I <sub>C</sub> = 0.1 A; f = 100 MHz	70	_	_	MHz
C <sub>c</sub>	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz	_	_	75	pF

## Note

1. Pulse test:  $t_p \le 300~\mu s;~\delta \le 0.02.$ 

# 40 V, 5 A NPN low V<sub>CEsat</sub> (BISS) transistor

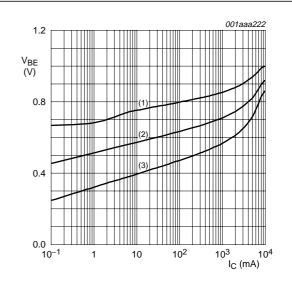
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 $V_{CE} = 2 V$ .

- (1)  $T_{amb} = 100 \, ^{\circ}C$ .
- (2)  $T_{amb} = 25 \, ^{\circ}C$ .
- (3)  $T_{amb} = -55 \, ^{\circ}C$ .

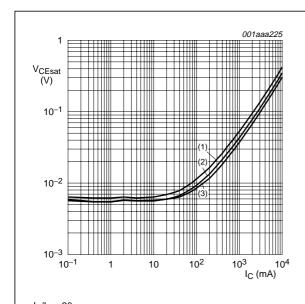
Fig.6 DC current gain as a function of collector current; typical values.



 $V_{CE} = 2 V$ .

- (1) T<sub>amb</sub> = 55 °C.
- (2)  $T_{amb} = 25 \, ^{\circ}C$ .
- (3)  $T_{amb} = 100 \, ^{\circ}C$ .

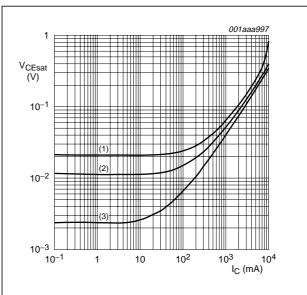
Fig.7 Base-emitter voltage as a function of collector current; typical values.



 $I_{\rm C}/I_{\rm B} = 20$ .

- (1) T<sub>amb</sub> = 100 °C.
- (2)  $T_{amb} = 25 \, ^{\circ}C$ .
- (3)  $T_{amb} = -55 \, ^{\circ}C$ .

Fig.8 Collector-emitter saturation voltage as a function of collector current; typical values.



 $T_{amb} = 25 \, ^{\circ}C.$ 

- (1)  $I_C/I_B = 100$ .
- (2)  $I_C/I_B = 50$ .
- (3)  $I_C/I_B = 10$ .

Fig.9 Collector-emitter saturation voltage as a function of collector current; typical values.

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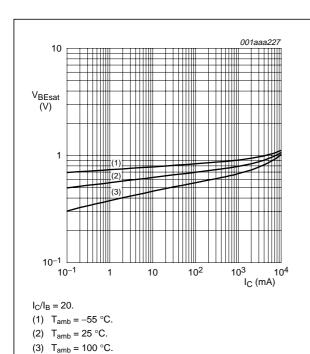
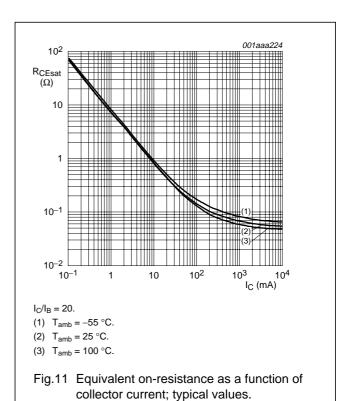
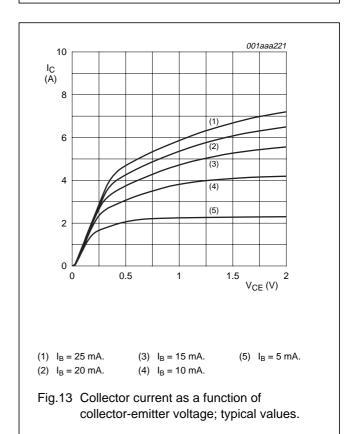


Fig.10 Base-emitter saturation voltage as a function of collector current; typical values.



10<sup>3</sup>  $\mathsf{R}_{\text{CE},\text{at}}$ 10<sup>2</sup> 10 10<sup>-1</sup> 10-2 10<sup>4</sup> I<sub>C</sub> (mA)  $10^{-1}$ 10<sup>2</sup> 10<sup>3</sup> 10  $T_{amb} = 25 \, ^{\circ}C.$ (1)  $I_C/I_B = 100$ . (2)  $I_C/I_B = 50$ . (3)  $I_C/I_B = 10$ . Fig.12 Equivalent on-resistance as a function of

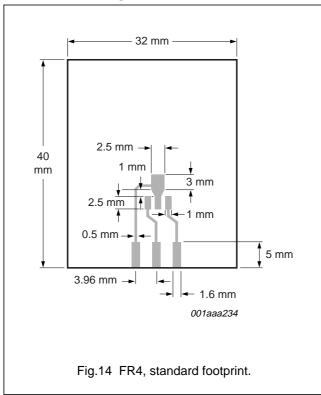
collector current; typical values.

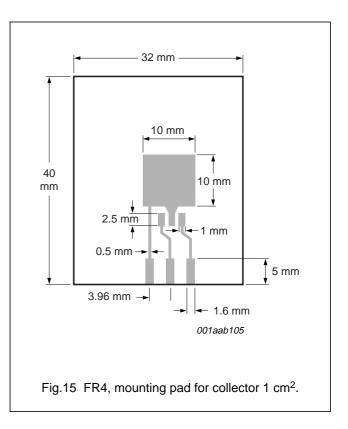


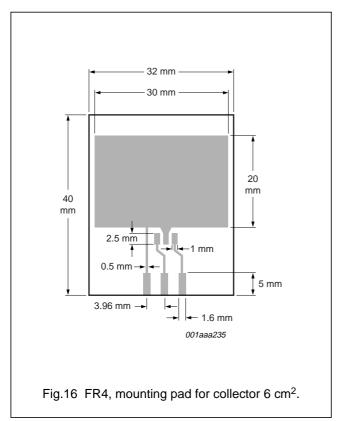
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# Reference mounting conditions







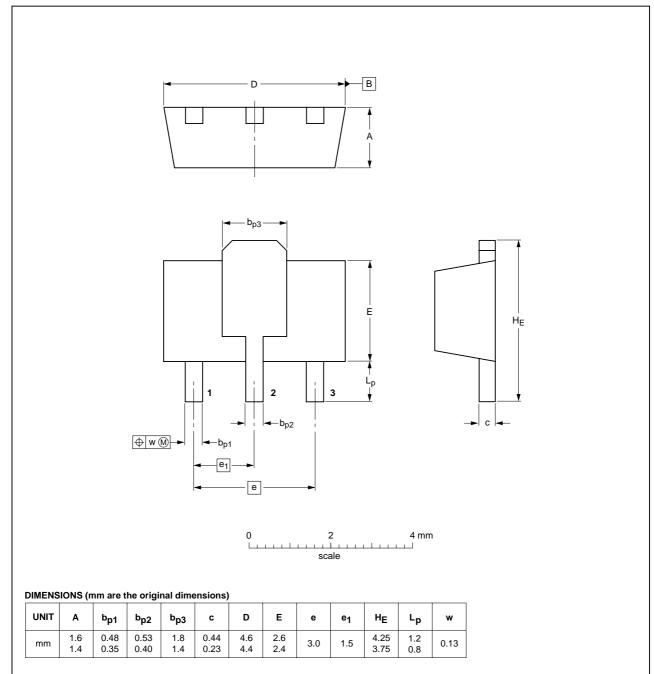
40 V, 5 A NPN low V<sub>CEsat</sub> (BISS) transistor

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# **PACKAGE OUTLINE**

## Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



OUTLINE	OUTLINE REFERENCES			EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT89		TO-243	SC-62			<del>99-09-13</del> 04-08-03

# 40 V, 5 A NPN low V<sub>CEsat</sub> (BISS) transistor

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