N-Channel Power MOSFET

600V, 4A, 0.9Ω

FEATURES

- Super-Junction technology
- High performance due to small figure-of-merit
- High ruggedness performance
- High commutation performance
- 100% UIL tested
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

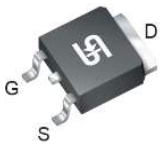
KEY PERFORMANCE PARAMETERS		
PARAMETER	**VALUE**	**UNIT**
V_{DS}	600	V
$R_{DS(on)}$ (max)	0.9	Ω
Q_g	9.6	nC

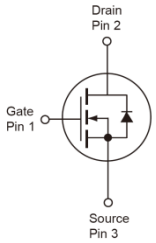
Pb-Free RoHS COMPLIANT HALOGEN FREE

APPLICATIONS

- Power Supply
- Lighting

TO-252 (DPAK)





Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	4	A
	T_C = 100°C		2.4	A
Pulsed Drain Current (Note 2)		I_{DM}	12	A
Total Power Dissipation @ T_C = 25°C		P_{DTOT}	36.8	W
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	42.3	mJ
Single Pulsed Avalanche Current (Note 3)		I_{AS}	1.3	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	3.4	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	62	°C/W

Thermal Performance Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	600	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	2	3.3	4	V
Gate Body Leakage	V_{GS} = ±30V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 600V, V_{GS} = 0V	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance (Note 4)	V_{GS} = 10V, I_D = 1.2A	$R_{DS(on)}$	--	0.69	0.9	Ω
Dynamic (Note 5)						
Total Gate Charge	V_{DS} = 380V, I_D = 4A, V_{GS} = 10V	Q_g	--	9.6	--	nC
Gate-Source Charge		Q_{gs}	--	2.0	--	
Gate-Drain Charge		Q_{gd}	--	4.5	--	
Input Capacitance	V_{DS} = 100V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	315	--	pF
Output Capacitance		C_{oss}	--	46.4	--	
Gate Resistance	F = 1MHz, open drain	R_g	--	3.2	--	Ω
Switching (Note 6)						
Turn-On Delay Time	V_{DD} = 380V, R_{GEN} = 25Ω, I_D = 4A, V_{GS} = 10V,	$t_{d(on)}$	--	18	--	ns
Turn-On Rise Time		t_r	--	10	--	
Turn-Off Delay Time		$t_{d(off)}$	--	36.4	--	
Turn-Off Fall Time		t_f	--	8	--	
Source-Drain Diode						
Forward Voltage (Note 4)	I_S = 4A, V_{GS} = 0V	V_{SD}	--	--	1.4	V
Reverse Recovery Time	V_R = 100V, I_S = 4A dI_F/dt = 100A/μs	t_{rr}	--	185.5	--	ns
Reverse Recovery Charge		Q_{rr}	--	1.38	--	μC

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. L = 50mH, I_{AS} = 1.3A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%.
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

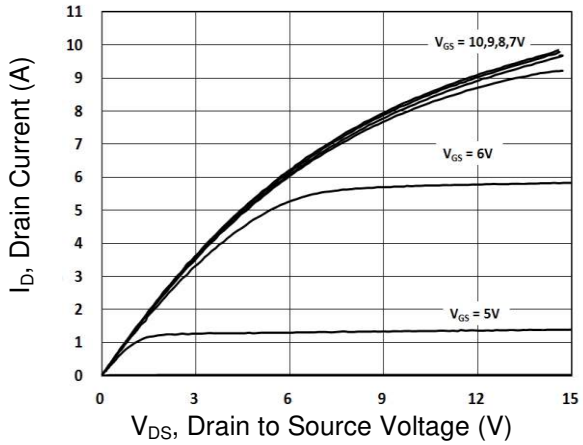
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM60NB900CP ROG	TO-252 (DPAK)	2,500pcs / 13” Reel

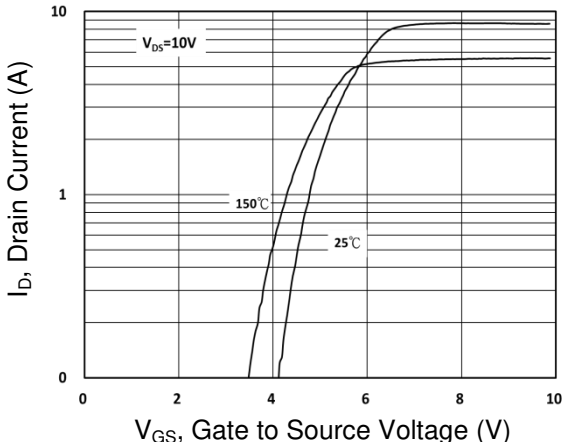
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

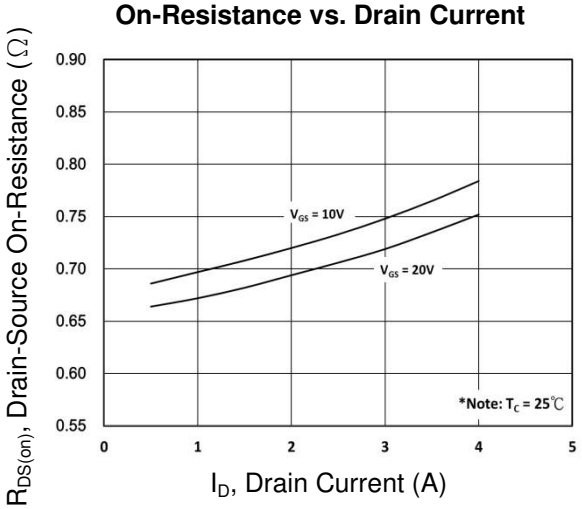
Output Characteristics



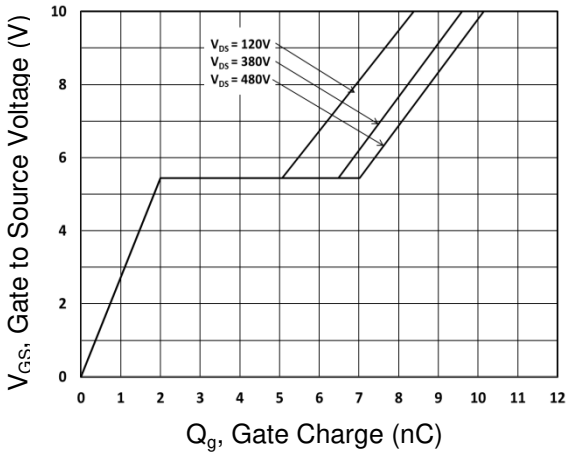
Transfer Characteristics



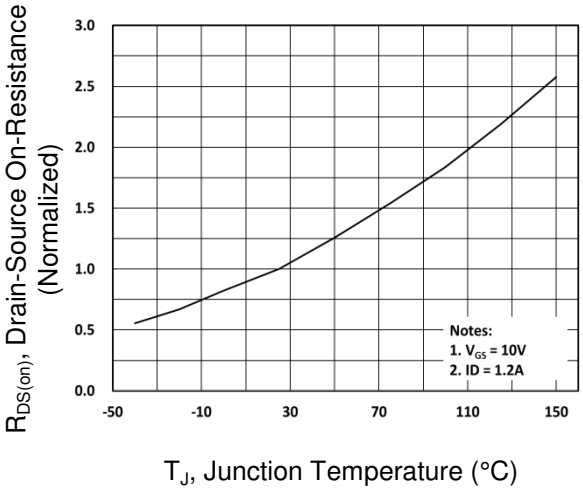
On-Resistance vs. Drain Current



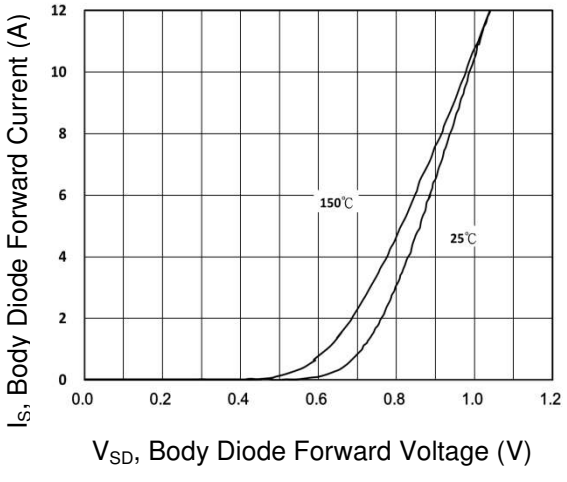
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



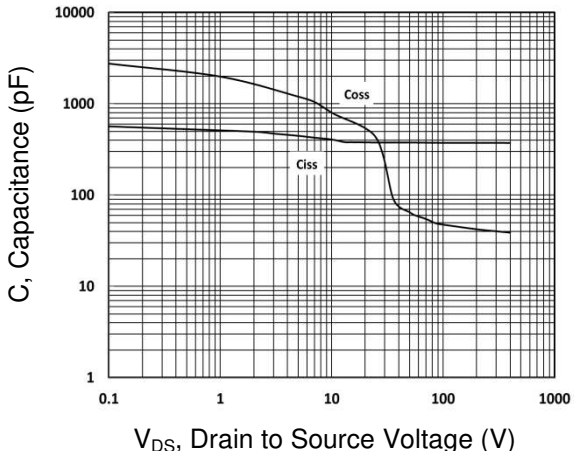
Source-Drain Diode Forward Current vs. Voltage



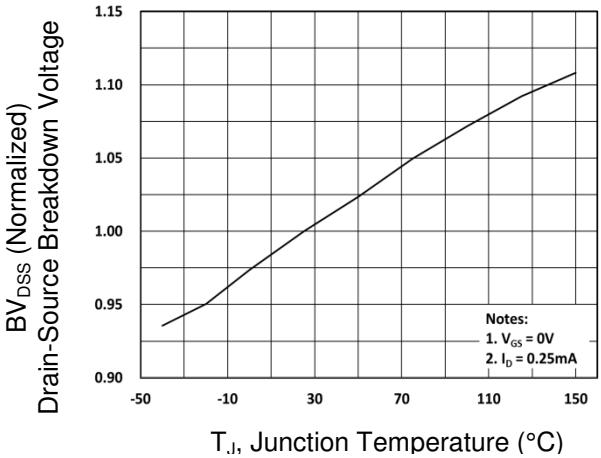
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

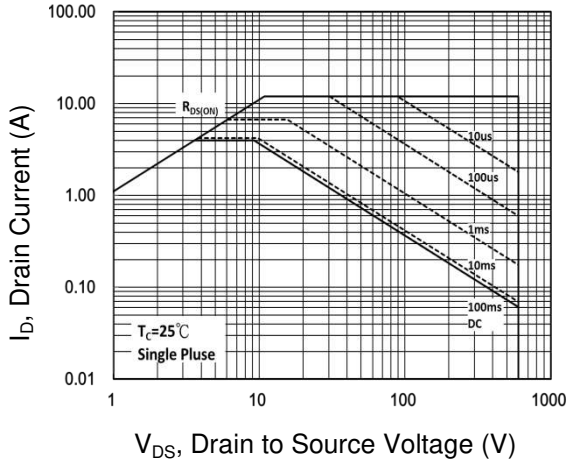
Capacitance vs. Drain-Source Voltage



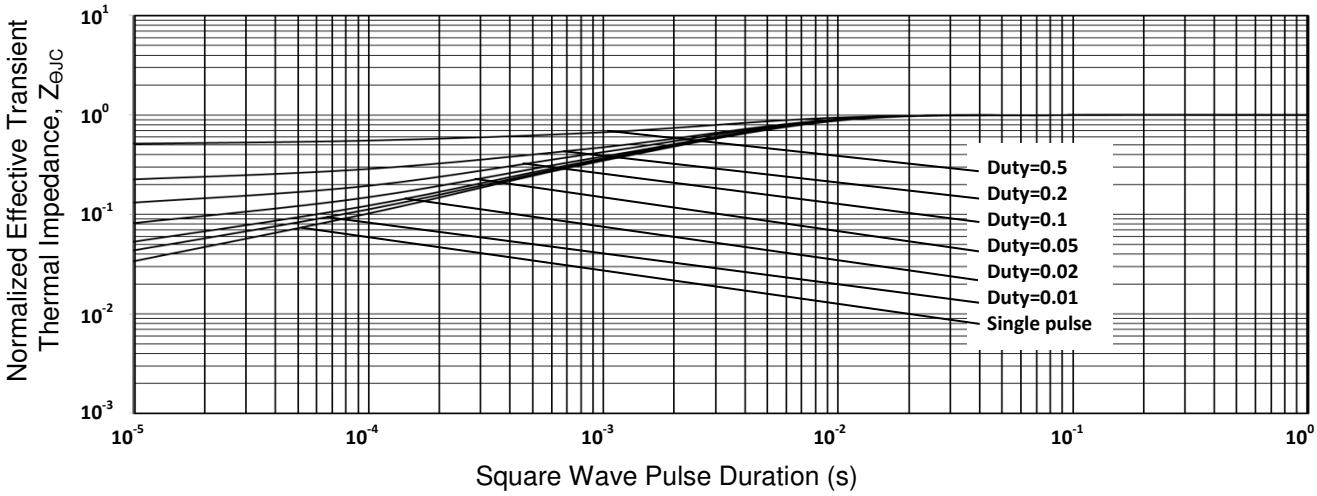
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area

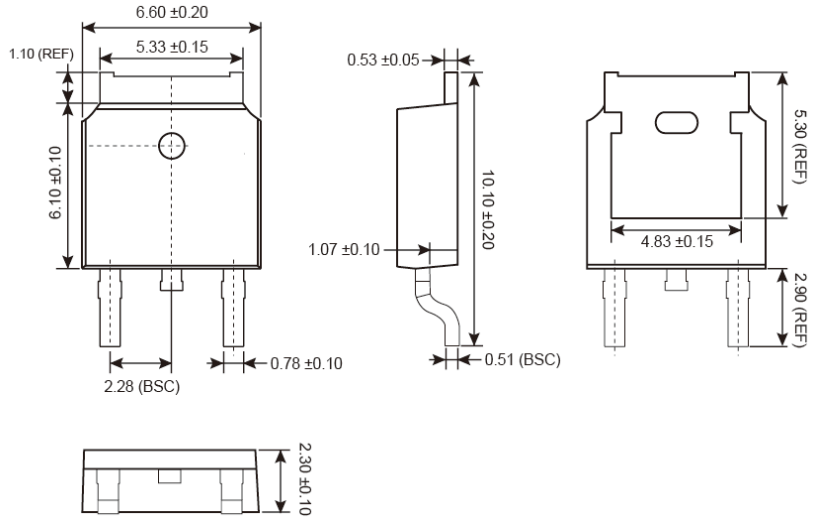


Normalized Thermal Transient Impedance, Junction-to-Case

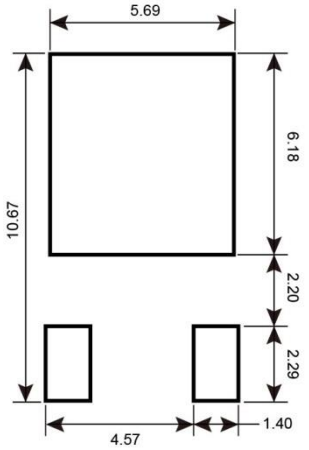


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

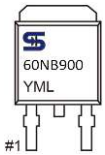
TO-252 (DPAK)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

M = Month Code for Halogen Free Product

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

L = Lot Code (1~9, A~Z)

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