User's Guide

TPS56C230 Buck Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS56C230EVM evaluation module as well as for the TPS56C230 dc/dc converter. Also included are the performance specifications, schematic, layout and the list of materials for the TPS56C230EVM.

Table of Contents

Trademarks

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1 Introduction

The TPS56C230 is a synchronous buck converter designed to provide up to a 12-A output. The input voltage is rated for 4.5 V to 18 V. The TPS56C230 uses a proprietary D-CAP3™ control mode. It provides a fast transient response with no external compensation, and supports low ESR output capacitors. A MODE pin is used to set Forced Continuous Conduction Mode (FCCM) or Advanced Eco-mode operation. Rated input voltage and output current range for the evaluation module are given in Table 1-1. The high-side and low-side switching MOSFETs are integrated inside the TPS56C230 package along with the gate-driver circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS56C230 to achieve high efficiencies and helps keep the junction temperature low at high output currents. An external divider allows for an adjustable output voltage. Additionally, the TPS56C230 provides adjustable soft start and undervoltage lockout inputs and an open drain power good output.

The TPS56C230EVM evaluation module (EVM) is a single, synchronous buck converter providing 1.2 V at 12 A from 4.5 V to 18 V input. This user's guide describes the TPS56C230EVM performance.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE (V_{IN}) Range	OUTPUT CURRENT (I_{OUT}) Range
TPS56C230EVM	4.5 V to 18 V	0 A to 12 A

2 Performance Specification Summary

A summary of the TPS56C230EVM performance specifications is provided in Table 2-1. Specifications are given for an input voltage of 12 V and an output voltage of 1.2 V, unless otherwise specified. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. TPS56C230EVM Performance Specifications Summary

SPECIFICATIONS	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} Input voltage			4.5	12	18	V
V_{IN} start voltage				Internal UVLO		V
V_{IN} stop voltage				Internal UVLO		V
Output voltage setpoint				1.2		V
Output current range	V_{IN} = 4.5 V to 18 V		0		12	A
Line regulation	I_{OUT} = 6 A, V_{IN}= 4.5 V to 17 V			± 0.05%		
Load regulation	V_{IN} = 12 V, I_{OUT} = 0 to 12 A			-0.02%, +0.25%		
Load transient response	I_{OUT} = 1.2 A to 10.8 A	Voltage change		-38		mV
		Recovery time		75		µs
	I_{OUT} = 10.8 A to 1.2 A	Voltage change		48		mV
		Recovery time		50		µs
Loop bandwidth	V_{IN} = 12 V, I_{OUT} = 6 A			126.5		kHz
Phase margin	V_{IN} = 12 V, I_{OUT} = 6 A			72.5		degree
Input ripple voltage	V_{IN} = 12 V, I_{OUT} = 12 A			290		mVPP
Output ripple voltage	V_{IN} = 12 V, I_{OUT} = 12 A			16		mVPP
Output rise time	Soft start pin floating			1.5		ms
Maximum efficiency	TPS56C230EVM, V_{IN} = 12 V, I_{OUT} = 4 A			89.75%		

3 Modifications

The evaluation module is designed to provide access to the features of the TPS56C230. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R4 (R_{TOP}) and R6 (R_{BOT}). R6 is fixed at 10.0 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R4. Changing the value of R4 can change the output voltage above the 0.6 V reference voltage V_{REF}. The value of R4 for a specific output voltage can be calculated using Equation 1.

$$R_{(TOP)} = \frac{R_{(BOT)} \cdot (V_{OUT} - V_{REF})}{V_{REF}} \quad (1)$$

3.2 Mode Selection

TPS56C230 has a MODE pin to select the operation mode. The device reads the voltage on MODE pin during start-up and latches onto one of the MODE options listed below in Table 3-1.

Table 3-1. Mode Pin Resistor Settings

VOLTAGE ON MODE	R9/10/11/12 (kΩ)	R13/14/15/16 (kΩ)	OPERATION	FREQUENCY (kHz)
(0~10%)*VCC	330	15	Eco-mode	500
(10~20%)*VCC	180	33	FCCM	500

Change the position of the jumper on J4 to modify the MODE configuration before start up.

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS56C230EVM evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, line regulation, load transient response, output voltage ripple, input voltage ripple, start-up and power-off.

4.1 Input/Output Connections

The TPS56C230EVM is provided with input/output connectors and test points as shown in Table 4-1. A power supply capable of supplying greater than 5 A must be connected to J1 through a pair of 20-AWG wires or better. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 12 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP3 provides a place to monitor the V_{IN} input voltages with TP8 providing a convenient ground reference. TP5 is used to monitor the output voltage with TP11 as the ground reference.

Table 4-1. Connection and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	V_{IN} input connector. (see Table 1-1 for V_{IN} range)
J2	V_{OUT} output connector. 1.2 V at 12 A maximum.
J3	Soft start selection. Remove the shunt to set the soft start time as internal default value.
J4	MODE selection. Refer to Section 3.2.
J5	EN control. Shunt EN to GND to disable. Shunt EN to the other side to enable.
TP1	VCC
TP2	V_{IN} terminal
TP3	V_{IN} test point
TP4	V_{OUT} terminal
TP5	V_{OUT} test point
TP6	SW node test point
TP7	Test point between voltage divider network and output. Used for loop response measurements.
TP8~11	GND test point
TP12	PGOOD test point
TP13~15	GND test point
TP16	EN test point

4.2 Efficiency

Figure 4-1 shows the efficiency for the TPS56C230EVM in 500kHz/Eco mode. The ambient temperature is 25 °C.

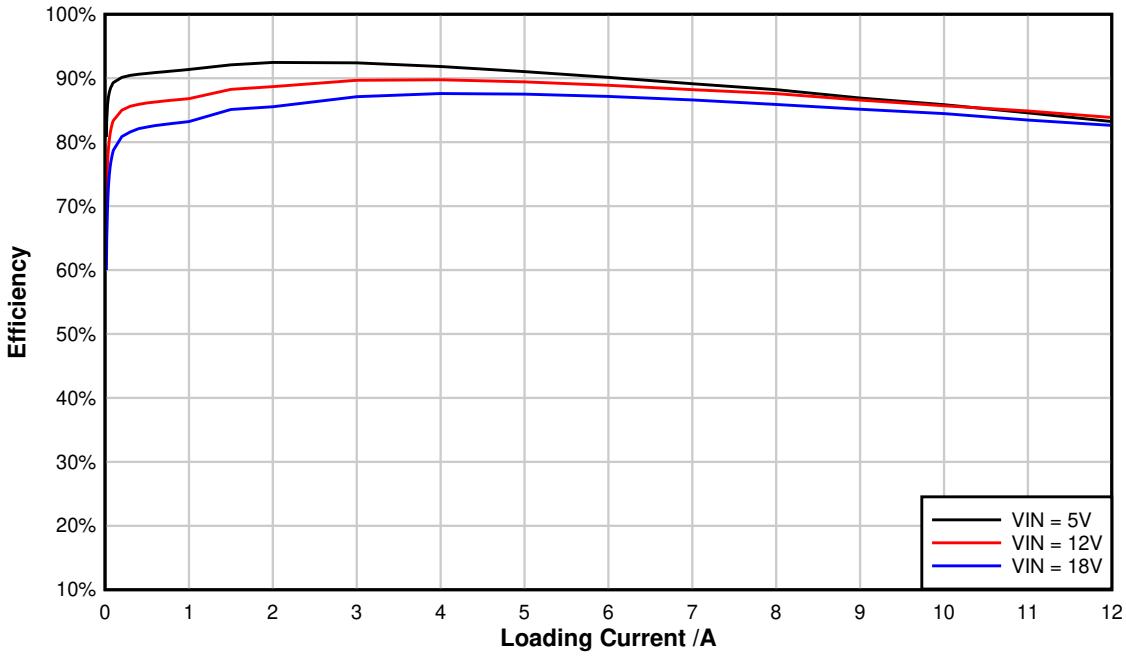

Figure 4-1. TPS56C230EVM Efficiency at 500-kHz/Eco mode

Figure 4-2 shows the efficiency at light loads for the TPS56C230EVM using a semi-log scale. The ambient temperature is 25 °C.

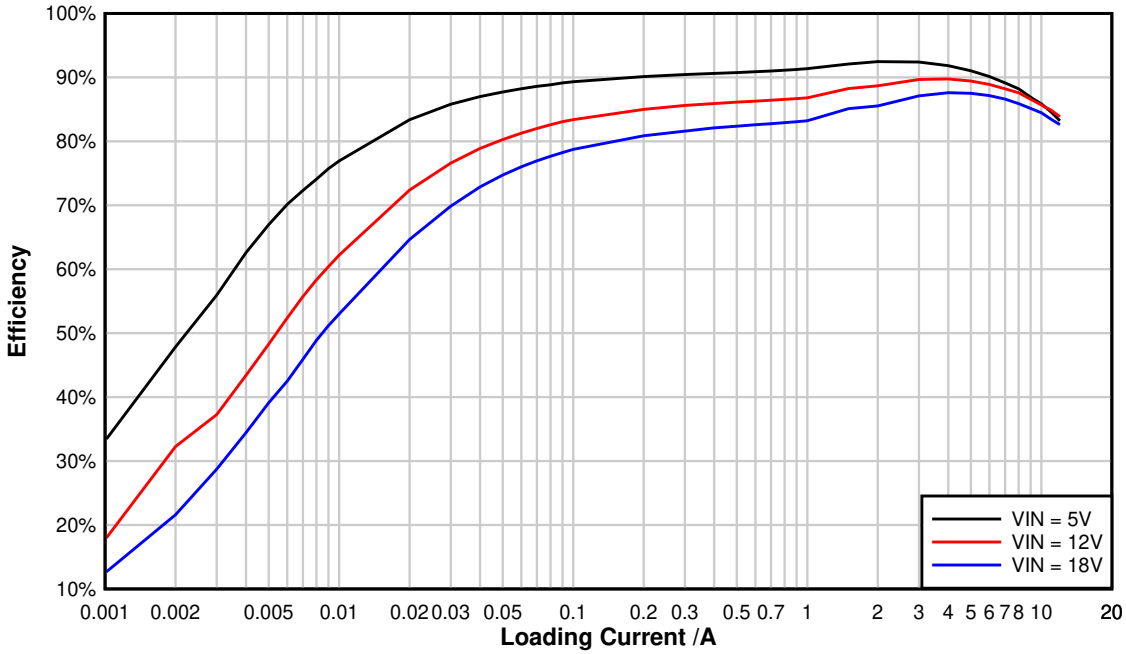

Figure 4-2. TPS56C230EVM Light Load Efficiency at 500-kHz/Eco Mode

The efficiency may be lower at higher ambient temperature, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

4.3 Output Voltage Load Regulation

Figure 4-3 shows the load regulation for the TPS56C230EVM. Measurement is given for an ambient temperature of 25 °C.

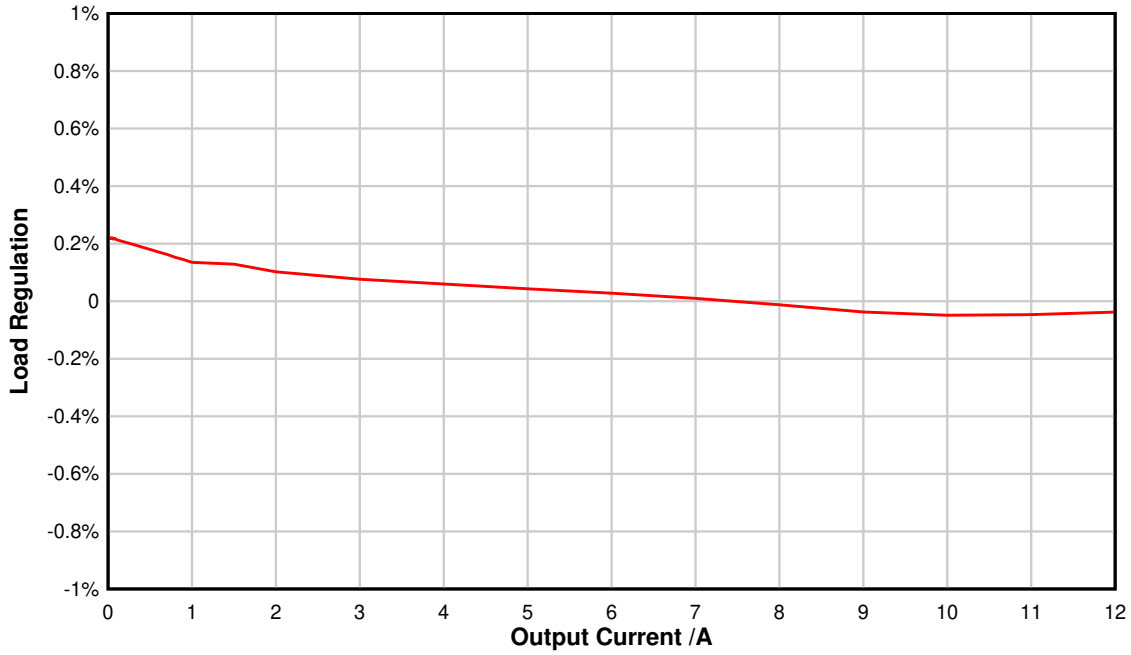

Figure 4-3. TPS56C230EVM Load Regulation, V_{IN} = 12 V

4.4 Output Voltage Line Regulation

Figure 4-4 shows the line regulation for the TPS56C230EVM. Measurement is given for an ambient temperature of 25 °C.

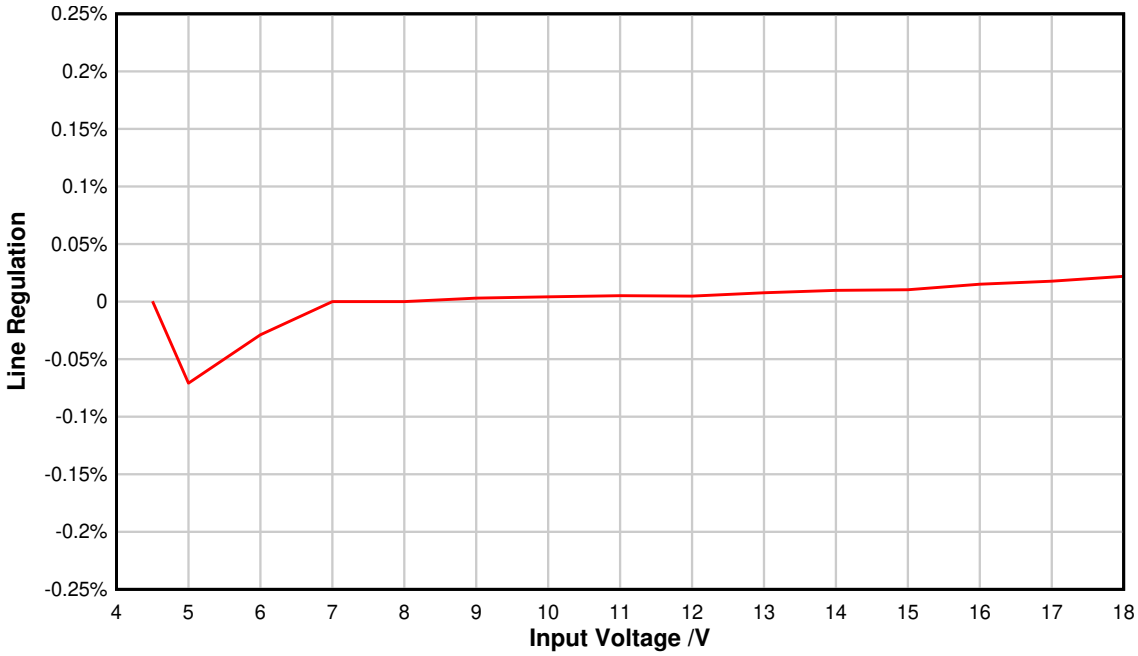

Figure 4-4. TPS56C230EVM Line Regulation

4.5 Load Transient Response

The TPS56C230EVM response to load transient is shown in Figure 4-5. The current steps and slew rates are indicated in the following figures . Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

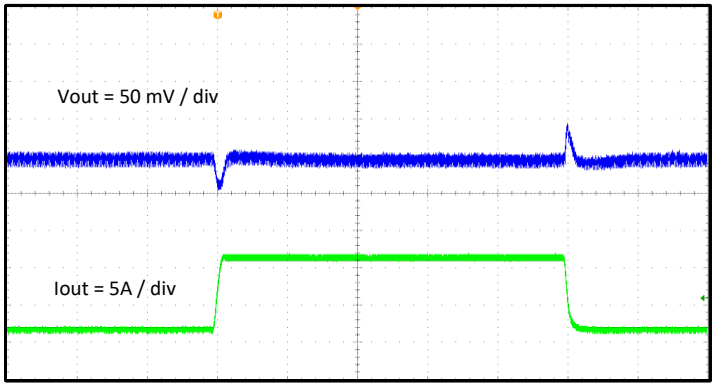

Figure 4-5. TPS56C230EVM Load Transient Response

4.6 Output Voltage Ripple

Figure 4-6, Figure 4-7, Figure 4-8 show the TPS56C230EVM output voltage ripple. The load currents are 10 mA, 800 mA, and 12 A. V_{IN} = 12 V. The ripple voltage is measured directly across TP5 and TP11.

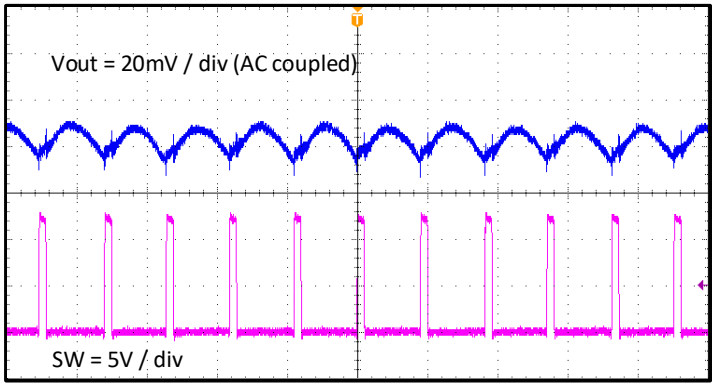

Figure 4-6. TPS56C230EVM Output Ripple, 10-mA Load

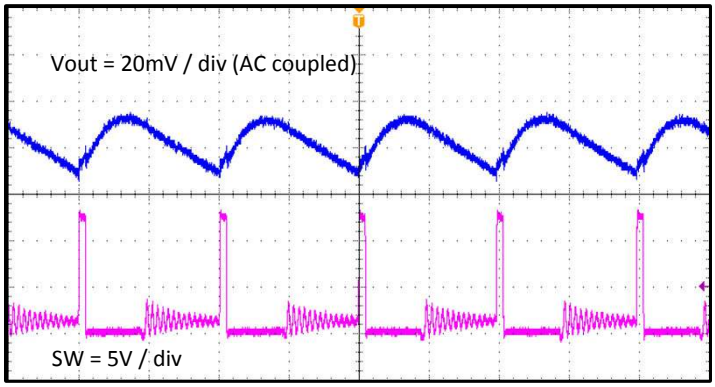

Figure 4-7. TPS56C230EVM Output Ripple, 800-mA Load

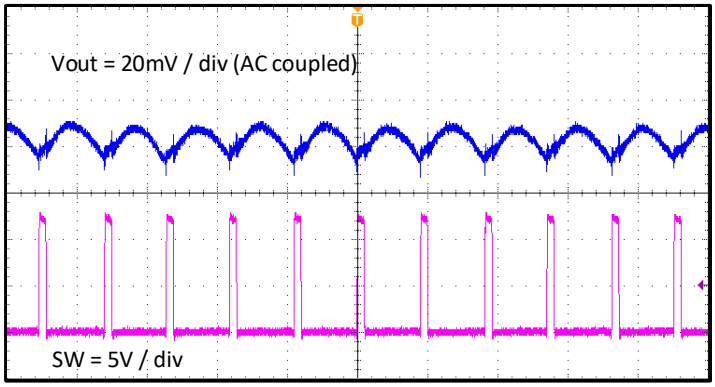

Figure 4-8. TPS56C230EVM Output Ripple, 12-A Load

4.7 Input Voltage Ripple

Figure 4-9, Figure 4-10 and Figure 4-11 show the TPS56C230EVM input voltage ripple at 500 kHz Eco-mode. The load currents are 10 mA, 800 mA and 12 A. The ripple voltage is measured directly across TP3 and TP8.

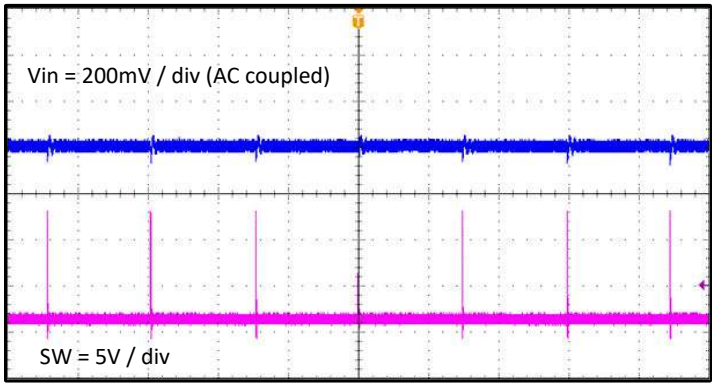

Figure 4-9. TPS56C230EVM Input Ripple, 10-mA Load

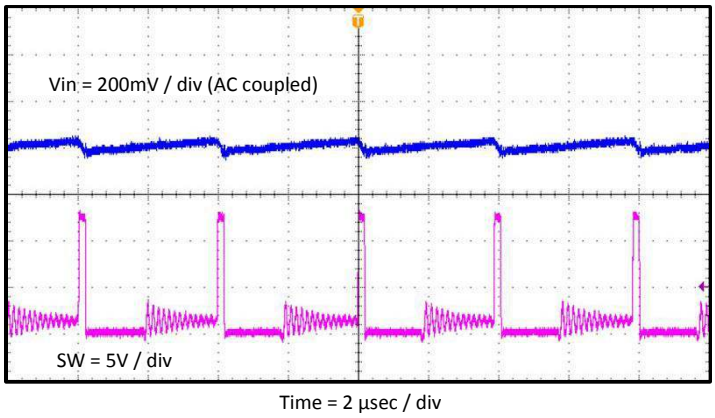

Figure 4-10. TPS56C230EVM Input Ripple, 800-mA Load

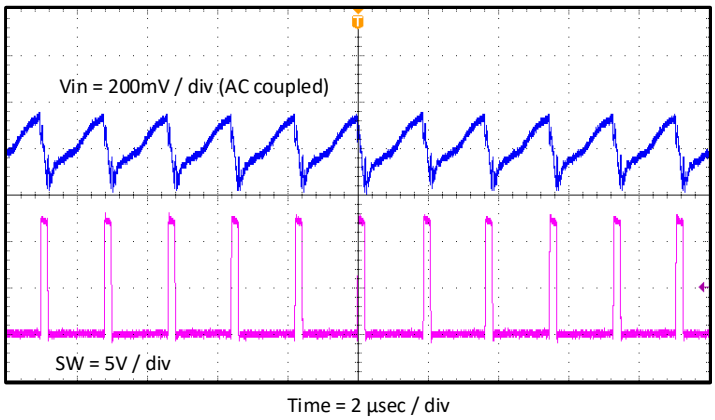

Figure 4-11. TPS56C230EVM Input Ripple, 12-A Load

4.8 Loop Characteristics

Figure 4-12 shows the TPS56C230EVM loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 12 A.

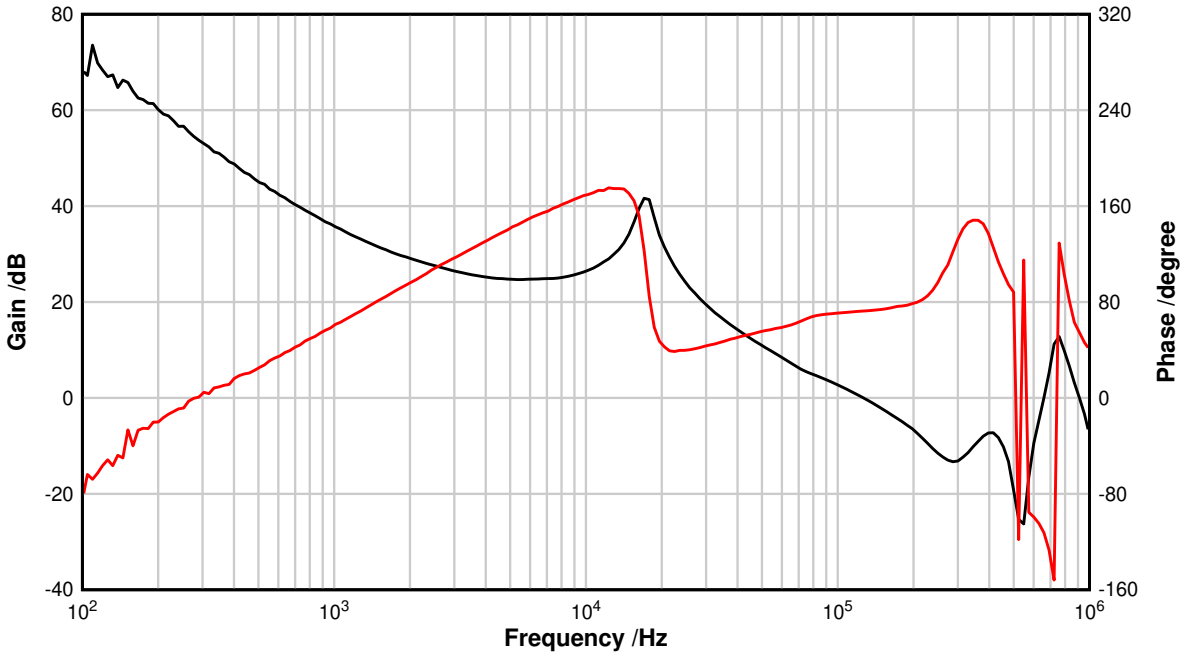

Figure 4-12. TPS56C230EVM Loop Response

4.9 Start-Up

Figure 4-13 and Figure 4-14 show the start-up waveforms for the TPS56C230EVM. In Figure 4-13, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold. In Figure 4-14, the input voltage is initially applied and the output is inhibited by using a jumper at J5 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 1.2 V. The input voltage for these plots is 12 V and the load is 1 Ω.

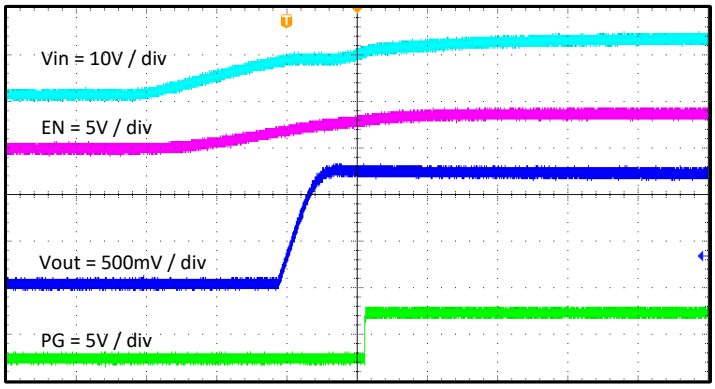

Figure 4-13. TPS56C230EVM Start-Up Relative to V_{IN}

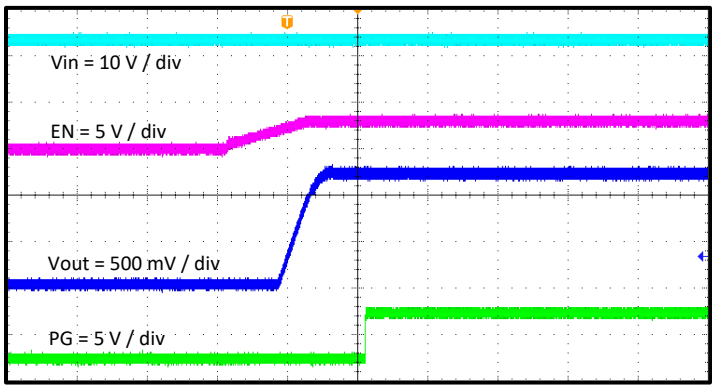

Figure 4-14. TPS56C230EVM Start-Up Relative to Enable

4.10 Shut-Down

Figure 4-15 and Figure 4-16 show the shutdown waveforms for the TPS56C230EVM. The input voltage for these plots is 12V and the load is 1Ω.

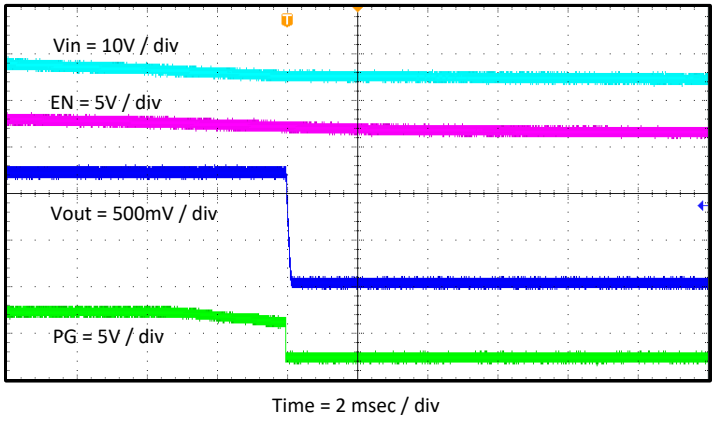

Figure 4-15. Shutdown Relative to V_{IN}

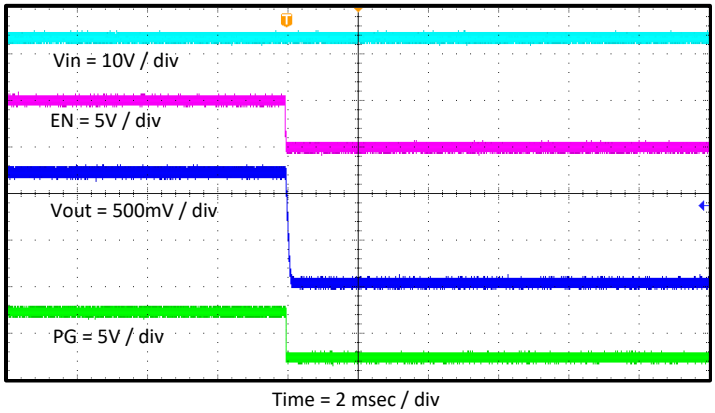

Figure 4-16. Shutdown Relative to Enable

5 Board Layout

This section provides a description of the TPS56C230EVM, board layout and layer illustrations.

5.1 Layout

The board layout for the TPS56C230EVM is shown in Figure 5-1 through Figure 5-5. The top and bottom layers are 2-oz copper thickness. Internal layers are 1-oz copper thickness.

The top layer contains the main power traces for VIN, VOUT and ground. Also on the top layer are connections for the pins of the TPS56C230 and a large area filled with ground. Most of the signal traces are located on the bottom left side, surrounding by a ground plane with an island for quiet analog ground that is connected to the main power ground at a single point. The internal layer-1 and internal layer-2 are dedicated ground planes. The bottom layer is another ground copper area with additional SW, VIN and VOUT copper fill. Ground traces on different layers are connected to each other with multiple vias placed on the board.

The input decoupling capacitors are located as close to the IC as possible. Critical analog circuits, such as the voltage set point divider, EN resister, SS capacitor, Mode resistor, VCC and AGND pin are terminated to quiet analog ground island on the top layer. The input and output connectors, test points and all of the components are located on the top side. The bottom layer is a ground plane along with the switching node copper fill, VIN and VOUT copper fill and the feedback trace from the point of regulation to the top of the resistor divider network.

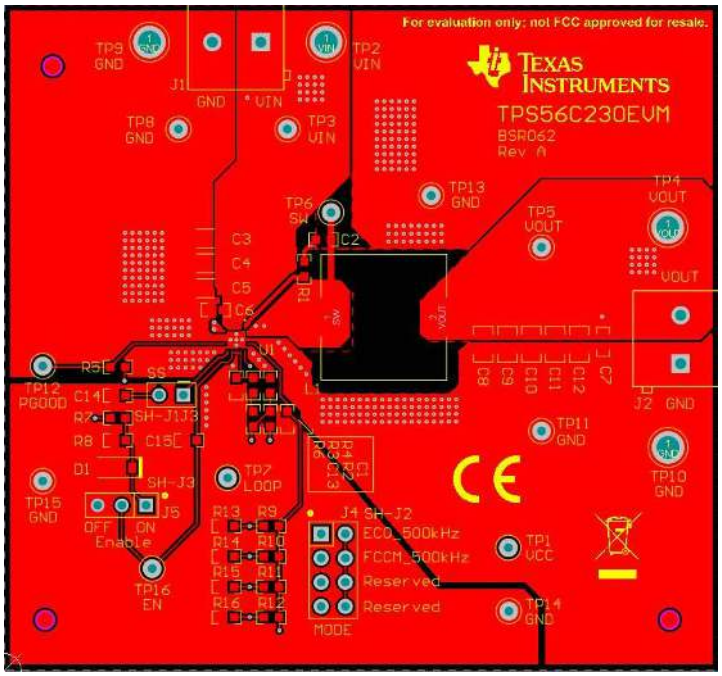

Figure 5-1. TPS56C230EVM Top-Side Assembly

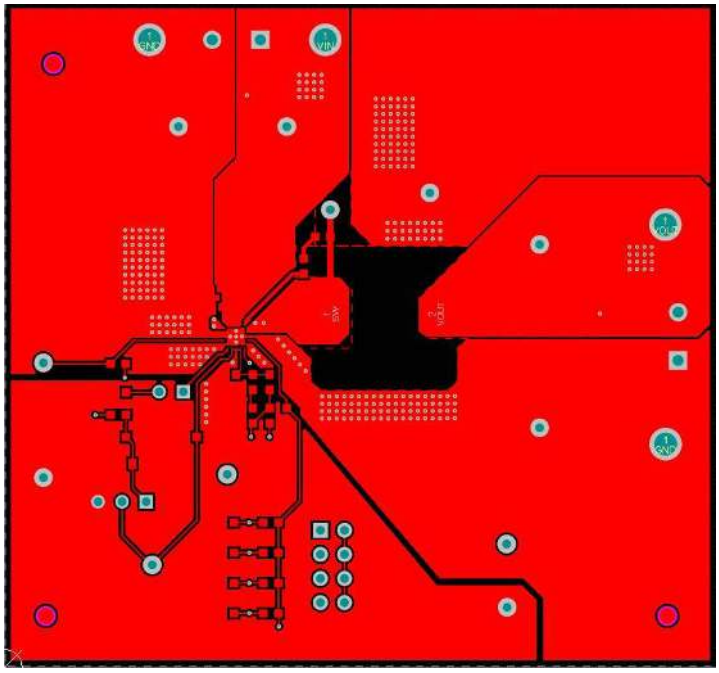

Figure 5-2. TPS56C230EVM Top-Side Layout

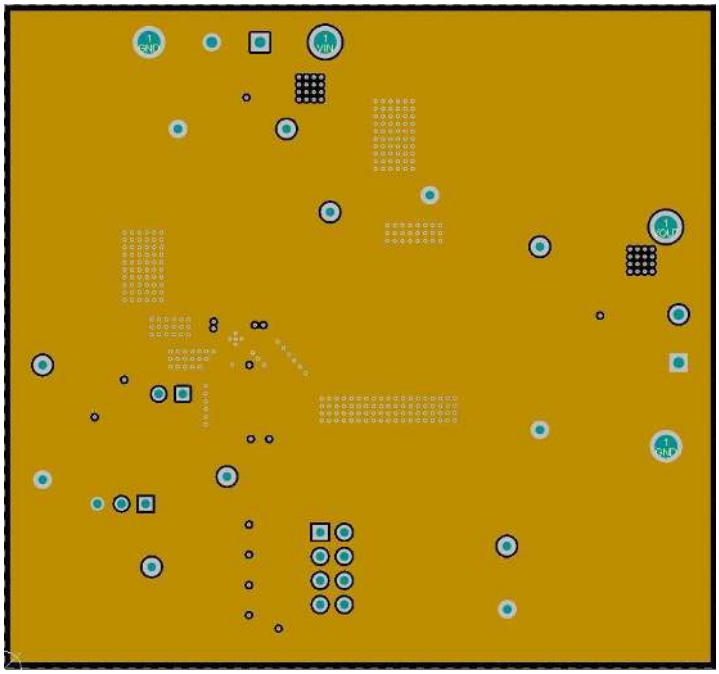

Figure 5-3. TPS56C230EVM Internal Layer-1 Layout

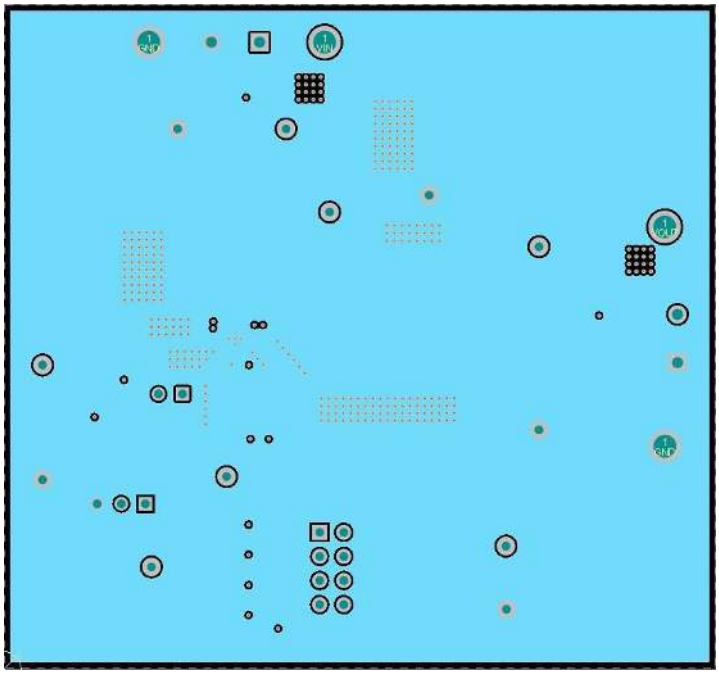

Figure 5-4. TPS56C230EVM Internal Layer-2 Layout

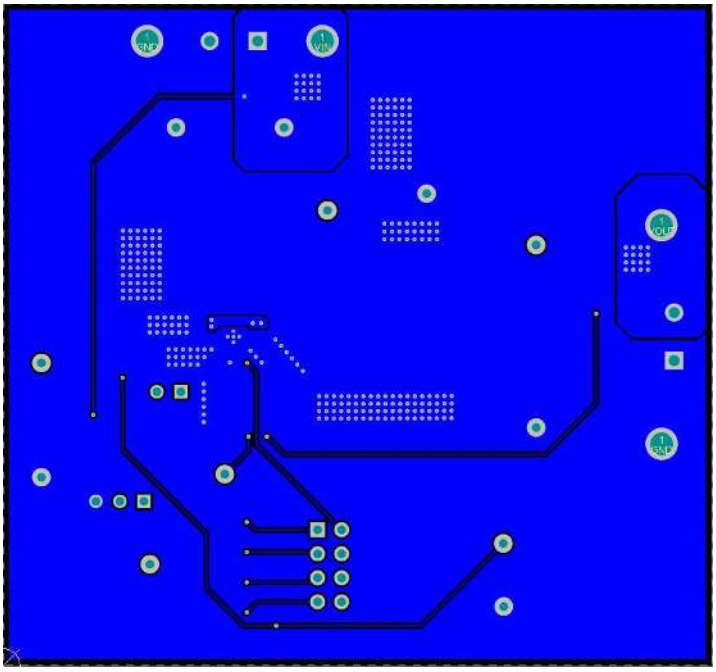

Figure 5-5. TPS56C230EVM Bottom Side Layout

6 Schematic, List of Materials, and Reference

6.1 Schematic

Figure 6-1 shows the schematic for TPS56C230EVM.

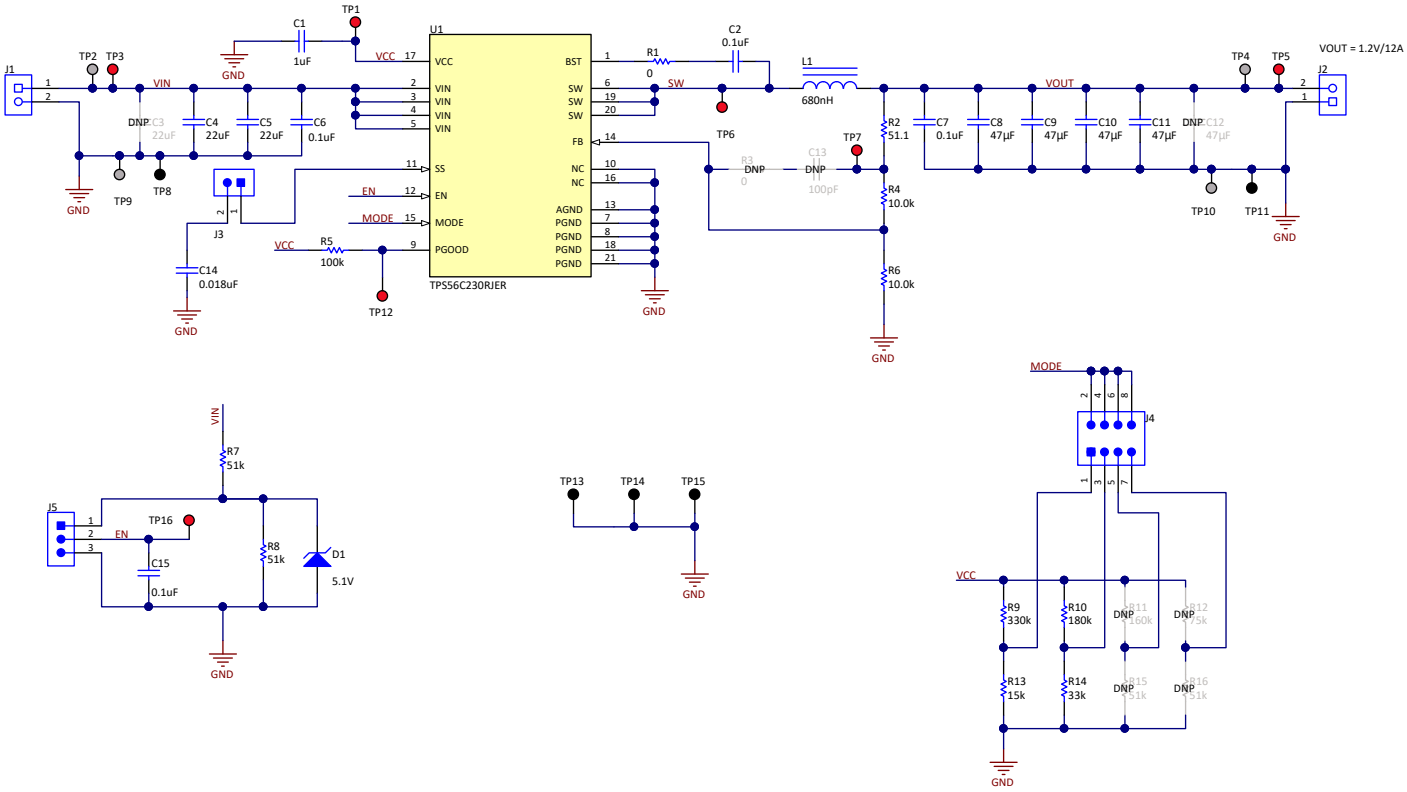

Figure 6-1. TPS56C230EVM Schematic

6.2 List of Materials

Table 6-1 presents the list of materials for the TPS56C230EVM.

Table 6-1. TPS56C230EVM List of Materials

DES	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
!PCB1	1	Printed circuit board	BSR062	Any
C1	1	Capacitor ceramic, 1 µF, 25 V, ±10%, X5R, 0603	C1608X5R1E105K080AC	TDK
C2, C6, C7, C15	4	Capacitor ceramic, 0.1 µF, 50 V, ±10%, X7R, 0603	C1608X7R1H104K080AA	TDK
C4, C5	2	Capacitor ceramic, 22 µF, 35 V, ±20%, X5R, 1206	C3216X5R1V226M160AC	TDK
C8, C9, C10, C11	4	Capacitor ceramic, 47 µF, 10 V, ±20%, X5R, 0805	GRM21BR61A476ME15L	MuRata
C14	1	Capacitor ceramic, 0.018 µF, 16 V, ±10%, X7R, 0603	GRM188R71C183KA01D	MuRata
D1	1	Diode, Zener, 5.1 V, 500 mW, SOD-123	MMSZ5231B-7-F	Diodes Inc.
H1, H2, H3, H4	4	Bumpon, hemisphere, 0.44 X 0.20, clear	SJ-5303 (CLEAR)	3M
J1, J2	2	Terminal block, 5.08 mm, 2x1, brass, TH	ED120/2DS	On-Shore Technology
J3	1	Header, 100 mil, 2x1, tin, TH	PEC02SAAN	Sullins Connector Solutions
J4	1	Header, 100 mil, 4x2, tin, TH	PEC04DAAN	Sullins Connector Solutions
J5	1	Header, 100 mil, 3x1, tin, TH	PEC03SAAN	Sullins Connector Solutions
L1	1	Inductor, shielded drum core, powdered iron, 680 nH, 17.5 A, 0.0018 ohm, SMD	744373770068	Wurth Elektronik
R1	1	Resistor, 0 Ω, 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW06030000Z0EA	Vishay-Dale
R2	1	Resistor, 51.1 Ω, 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060351R1FKEA	Vishay-Dale
R4, R6	2	Resistor, 10.0 kΩ, 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060310K0FKEA	Vishay-Dale
R5	1	Resistor, 100 kΩ, 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW0603100KFKEA	Vishay-Dale
R7, R8	2	Resistor, 51 kΩ, 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060351K0JNEA	Vishay-Dale
R9	1	Resistor, 330 kΩ, 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW0603330KJNEA	Vishay-Dale
R10	1	Resistor, 180 kΩ, 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW0603180KJNEA	Vishay-Dale
R13	1	Resistor, 15 kΩ, 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060315K0JNEA	Vishay-Dale
R14	1	Resistor, 33 kΩ, 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060333K0JNEA	Vishay-Dale
SH-J1, SH-J2, SH-J3	3	Shunt, 100 mil, gold plated, black	SNT-100-BK-G	Samtec
TP1, TP3, TP5, TP6, TP7, TP12, TP16	7	Test point, miniature, red, TH	5000	Keystone
TP2, TP4, TP9, TP10	4	Terminal, turret, TH, triple	1598-2	Keystone
TP8, TP11, TP13, TP14, TP15	5	Test point, miniature, black, TH	5001	Keystone
U1	1	4.5-V to 18-V Input, 12-A Synchronous Step-Down Voltage Regulator, RJE0020B (VQFN-20)	TPS56C230RJER	Texas Instruments
C3	0	Capacitor ceramic, 22 µF, 35 V, ±20%, X5R, 1206	C3216X5R1V226M160AC	TDK
C12	0	Capacitor ceramic, 47 µF, 10 V, ±20%, X5R, 0805	GRM21BR61A476ME15L	MuRata
C13	0	Capacitor ceramic, 100 pF, 25 V, ±10%, X7R, 0603	06033C101KAT2A	AVX
FID1, FID2, FID3	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
R3	0	Resistor, 0 Ω, 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW06030000Z0EA	Vishay-Dale
R11	0	Resistor, 160 kΩ, 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW0603160KJNEA	Vishay-Dale
R12	0	Resistor, 75 kΩ, 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060375K0JNEA	Vishay-Dale
R15, R16	0	Resistor, 51 kΩ, 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060351K0JNEA	Vishay-Dale

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2019) to Revision B (June 2021)	Page
• Updated user's guide title	2
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2

Changes from Revision * (January 2019 September 2019) to Revision A ()	Page
• Added updated List of Materials	18

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