CY28506

PowerPC™ Spread Spectrum Clock Generator

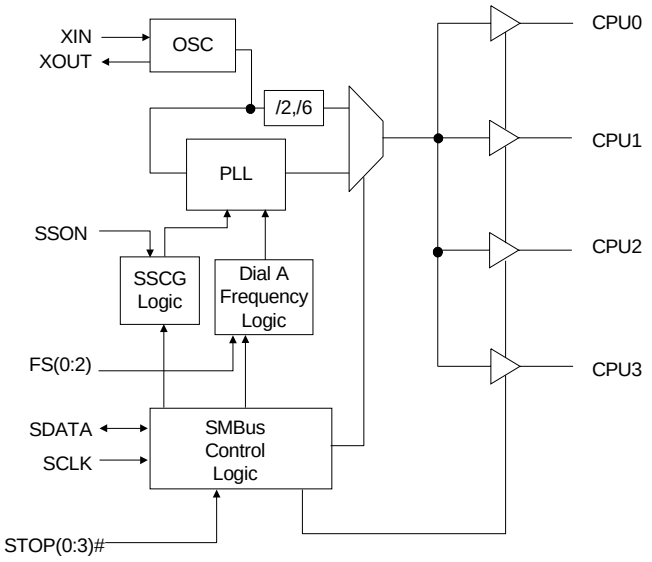
Features

- **Precision clock generation**
- **Low Clock Skew: 100 ps**
- **Low Cycle to Cycle Jitter: 125 ps**
- **Dial-a-Frequency™ capabilities**
- **Cypress Spread Spectrum for best EMI reduction**
- **All four CPUs have independent hardware enable.**
- **SMBus compatible programmability.**
- **28 Pin SSOP Package**

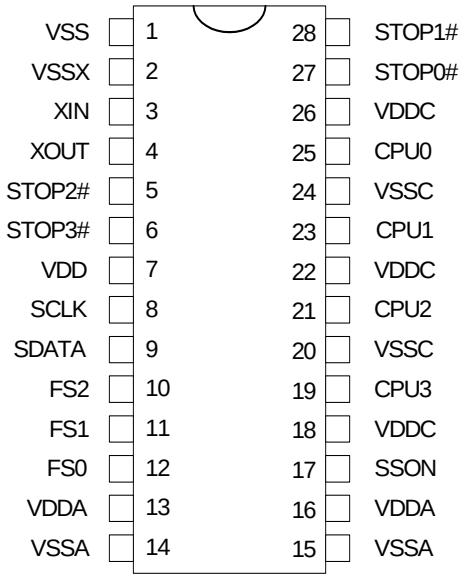
Table 1. Frequency Table

FS2	FS1	FS0	CPU(0:3)
0	0	0	100.0 MHz
0	0	1	133.3 MHz
0	1	0	150.0 MHz
0	1	1	166.7 MHz
1	0	0	Three-State
1	0	1	XIN/2
1	1	0	XIN/6
1	1	1	PWRDN

Block Diagram



Pin Configuration



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Pin Description

Pin	Name	PWR	I/O	Description
3	XIN	V_{DD}	I	Oscillator Buffer Input. Connect to a crystal or to an external clock.
4	XOUT	V_{DD}	O	Oscillator Buffer Output. Connect to a crystal. Do not connect when an external clock is applied at XIN.
25, 23, 21, 19	CPU(0:3)	V_{DDC}	O	1.8V Host bus clock outputs
12	FS0	V_{DD}	PD	Frequency select 0. See*Table 1*. Not latched.
11	FS1	V_{DD}	PD	Frequency select 1. See*Table 1*. Not latched.
10	FS2	V_{DD}	PD	Frequency select 2. See *Table 1*. Not latched.
17	SSON	V_{DD}	PU	0 = Spread OFF, 1 = Spread ON. Not latched.
27	STOP0#	V_{DD}	PU	CPU0 stop clock control input. When this signal is at a logic LOW level (0), CPU0 clock stops at a logic LOW level. Using this pin to start and stop CPU0 clock ensures synchronous (no short or long clocks) transitioning of this clock.
28	STOP1#	V_{DD48}	PU	CPU1 stop clock control input. When this signal is at a logic LOW level (0), CPU1 clock stops at a logic LOW level. Using this pin to start and stop CPU1 clock ensures synchronous (no short or long clocks) transitioning of this clock.
5	STOP2#	V_{DD48}	PU	CPU2 stop clock control input. When this signal is at a logic LOW level (0), CPU2 clock stops at a logic LOW level. Using this pin to start and stop CPU2 clock ensures synchronous (no short or long clocks) transitioning of this clock.
6	STOP3#	V_{DD}	PU	CPU3 stop clock control input. When this signal is at a logic LOW level (0), CPU3 clock stops at a logic LOW level. Using this pin to start and stop CPU3 clock ensures synchronous (no short or long clocks) transitioning of this clock.
9	SDATA	V_{DD}	PU	Serial data input pin. Conforms to the SMBus specification of a Slave Receive/Transmit device. This pin is an input when receiving data. It is an open drain output when acknowledging or transmitting data.
8	SCLK	V_{DD}	PU	Serial clock input pin. Conforms to the SMBus specification.
18, 22, 26	VDDC			1.8V Power for CPU output buffers
20, 24	VSSC			Ground for CPU output buffers
13, 16	VDDA			3.3V Analog Power Supply
14, 15	VSSA			Analog Power Ground
7, 11	VDD			3.3V Common Power Supply
1	VSS			Common Ground pins.
2	VSSX			Common Ground pins.

Byte 0: Frequency Select Register

Bit	@Pup	Pin#	Name	Description
7	0	-	SWEN	If this bit is programmed to a “1”, the FS frequency and SS operation will be derived from the register values in bits (0:6) for selecting the frequency and Spread Spectrum. If this bit is programmed to a “0”, the FS mode and SS mode will be derived from the hardware pins on FS(0:2) and SSON. When reading this register, if bit3 = 1, then the software register is read back and enabled, and when reading bit3 = 0, then the hardware values are read back and enabled.
6	H/W Setting	17	SSON	Spread Spectrum Enable: 0 = off, 1 = on. Value is the H/W setting at power-up, then can be over-written via this bit.
5	0		SSMode	Spread Spectrum Mode Select: 0 = down spread, 1 = center spread (see *Table 3*)
4	0		S1	Spread Spectrum Table Select 1. (see*Table 3*)
3	0		S0	Spread Spectrum Table Select 0. (see *Table 3*)
2	H/W Setting	10	FS2	For selecting frequencies in table 1; when SWEN = 1, FS0 = FS1 = FS0 = 1 does not get decoded.
1	H/W Setting	11	FS1	For selecting frequencies in table 1; when SWEN = 1, FS0 = FS1 = FS0 = 1 does not get decoded.
0	H/W Setting	12	FS0	For selecting frequencies in table 1; when SWEN = 1, FS0 = FS1 = FS0 = 1 does not get decoded.

Byte 1: CPU Clock Register

Bit	@Pup	Pin#	Name	Description
7	1	19	CPU3 Dual Drive	1 = high output drive. 0 = low output drive
6	1	21	CPU2 Dual Drive	1 = high output drive. 0 = low output drive
5	1	23	CPU1 Dual Drive	1 = high output drive. 0 = low output drive
4	1	25	CPU0Dual Drive	1 = High output drive. 0 = low output drive
3	1	19	CPU3 Enable	1 = output enabled (running). 0 = output disabled asynchronously in a low state
2	1	21	CPU2 Enable	1 = output enabled (running). 0 = output disabled asynchronously in a low state
1	1	23	CPU1 Enable	1 = output enabled (running). 0 = output disabled asynchronously in a low state
0	1	25	CPU0 Enable	1 = output enabled (running). 0 = output disabled asynchronously in a low state

Byte 2: Dial-a-Frequency™ Control Register N

Bit	@Pup	Pin#	Name	Description
7	0			Reserved
6	0		N6, MSB	These bits are for the PLL’s internal N register. This access allows the user to modify the CPU frequency at very high resolution (accuracy).
5	0		N5	
4	0		N4	
3	0		N3	
2	0		N2	
1	0		N1	
0	0		N0, LSB	

Byte 3: Dial-a-Frequency Control Register R

Bit	@Pup	Pin#	Name	Description
7	0			Reserved
6	0		R5, MSB	These bits are for programming the PLL's internal register. This access allows the user to modify the CPU frequency at very high resolution (accuracy)
5	0		R4	
4	0		R3	
3	0		R2	
2	0		R1	
1	0		R0, LSB	
0	0		DAFEN	0 = Hardware FS(0:2) selected, 1 = Dial-a-Frequency registered selected

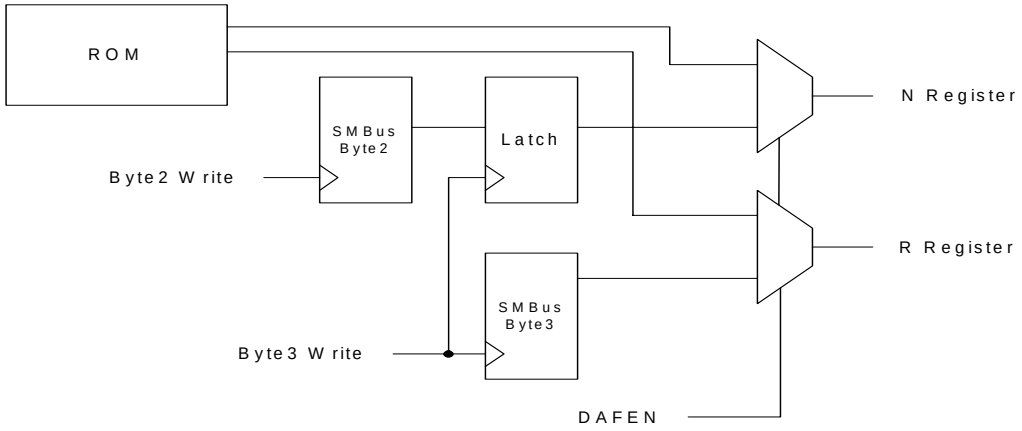


Figure 1. Dial-a-Frequency ™ Feature[1]

Table 2. P is a PLL Constant that Depends on the Frequency Selection prior to Accessing the Dial-a-Frequency Feature

FS(2:0)	P
XXX	96016000

Table 3. Spread Spectrum Clock Generation (SSCG)

Mode Byte0, Bit6	SST1 Byte0, Bit5	SST0 Byte0, Bit4	% Spread
0	0	0	–0.5% Lexmark
0	0	1	–1.0% Lexmark
0	1	0	–0.5% Linear
0	1	1	–1.0% Linear
1	0	0	±0.25% Lexmark
1	0	1	±0.5% Lexmark
1	1	0	±0.25% Linear
1	1	1	±0.5% Linear

Note:
1. The SMBus controlled Dial-a-Frequency feature is available in this device via Byte 2 and byte 3.

CPU Clock Timing

All clocks can be individually enabled or stopped via the 2-wire SMBus control interface. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stop and on transitions from stopped to running when the specific STOP pin is sampled internally

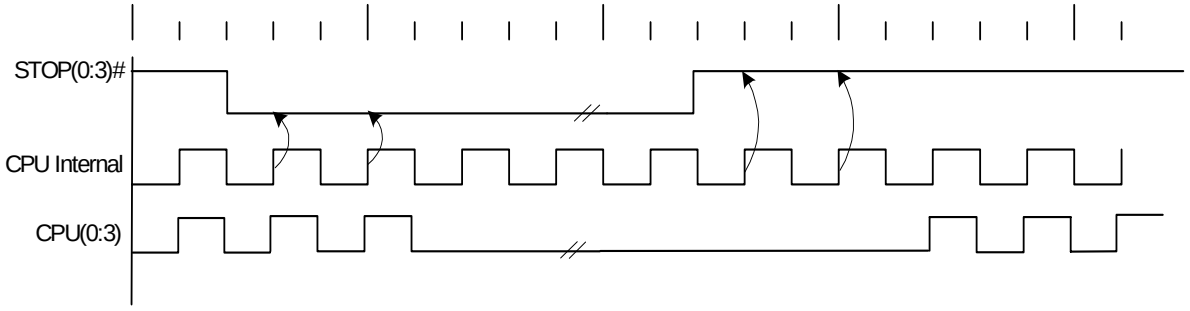


Figure 2. CPU Assertion and Deassertion Timing Waveform

Maximum Ratings

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: ..... –65°C to + 150°C

Operating Temperature: ..... 0°C to +70°C

Maximum ESD protection 2000V

Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters (V_{DD} = VDDA= 3.3±5%, V_{DDC} = 1.8±5%, T_A = 0°C to +70°C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL1}	Input Low Voltage	Applicable to SSON#, STOP(0:3)#, FS(0:2)			1.0	Vdc
V_{IH1}	Input High Voltage		2.0			Vdc
V_{IL2}	Input Low Voltage	Applicable to SDATA and SCLK			0.8	Vdc
V_{IH2}	Input High Voltage		2.1			Vdc
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			0.4	Vdc
V_{OH}	Output High Voltage	I_{OH} = –1 mA			1.4	Vdc
Ioz	Three-State Leakage Current				10	µA
Idd3.3V	Dynamic Supply Current	CPU frequency set at 166 MHz[2]		46	60	mA
Idd1.8V	Dynamic Supply Current	CPU frequency set at 166 Hz[2]		48	60	mA
I_{pup}	Internal Pull-up Device Current	Input @ V_{SS}			–25	µA
I_{pdwn}	Internal Pull-down Device Current	Input @ V_{DD}			10	µA
Cin	Input Pin Capacitance				5	pF
Cout	Output Pin Capacitance				6	pF
Lpin	Pin Inductance				7	nH
Cxtal	Crystal Pin Capacitance	Measured from the Xin or Xout to V_{SS}	27	36	45	pF

Note:

2. All outputs loaded as per loading specified in the loading *Table 4*.

AC Parameters (V_{DD}= V_{DDA}= 3.3±5%, V_{DDC} = 1.8±5%, T_A = 0°C to +70°C)

Parameter	Description	100 MHz		133 MHz		150 MHz		166 MHz		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Crystal											
TDC	Xin Duty Cycle	45	55	45	55	45	55	45	55	%	3, 5, 9
TPeriod	Period	69.8413	71.0	69.8413	71.0	69.8413	71.0	69.8413	71.0	ns	3, 5, 9
VHIGH	Xin High Voltage	0.7Vdd	Vdd	0.7Vdd	Vdd	0.7Vdd	Vdd	0.7Vdd	Vdd	V	
VLOW	Xin Low Voltage	0	0.3Vdd	0	0.3Vdd	0	0.3Vdd	0	0.3Vdd	V	
Tr/Tf	Xin Rise and Fall Times	-	10.0	-	10.0	-	10.0	-	10.0	ns	11
TCCJ	Xin Cycle to Cycle Jitter	-	500	-	500	-	500	-	500	ps	2, 7, 9 @50%V_{DD}
Txs	Crystal Startup Time	-	30	-	30	-	30	-	30	µs	8, 10
CPU											
TDC	CPU(0:3) Duty Cycle	45	55	45	55	45	55	45	55	%	2, 6
TPeriod	CPU(0:3) Period	10.00	10.03	7.50	7.53	6.66	6.69	6.00	6.03	ns	2, 6
Tr/Tf	Rise and Fall times	0.450	0.820	0.450	0.820	0.450	0.820	0.450	0.820	ns	2, 4
TSKEW	CPU(0:3) to CPU(0:3) Clock Skew		100		100		100		100	ps	2,6,7
TCCJ	CPU(0:3) Cycle to Cycle Jitter		125		125		125		125	ps	2, 6, 7

Notes:

3. This parameter is measured as an average over a 1 us duration, with a crystal center frequency of 14.31818MHz
4. Probes are placed on the pins and measurements are acquired between 0.4V and 1.4V.
5. This is required for the duty cycle on the REF clock out to be as specified. The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within data sheet specifications.
6. Probes are placed on the pins, and measurements are acquired at 0.9V.
7. This measurement is applicable with Spread ON or spread OFF.
8. The time specified is measured from when all VDD's reach their respective supply rail (3.3V and 1.8V) till the frequency output is stable and operating within the specifications
9. When Xin is driven from and external clock source.
10. When Crystal meets minimum 40-ohm device series resistance specification.
11. Measured between 0.2Vdd and 0.7Vdd

Table 4. Sign Loading Table

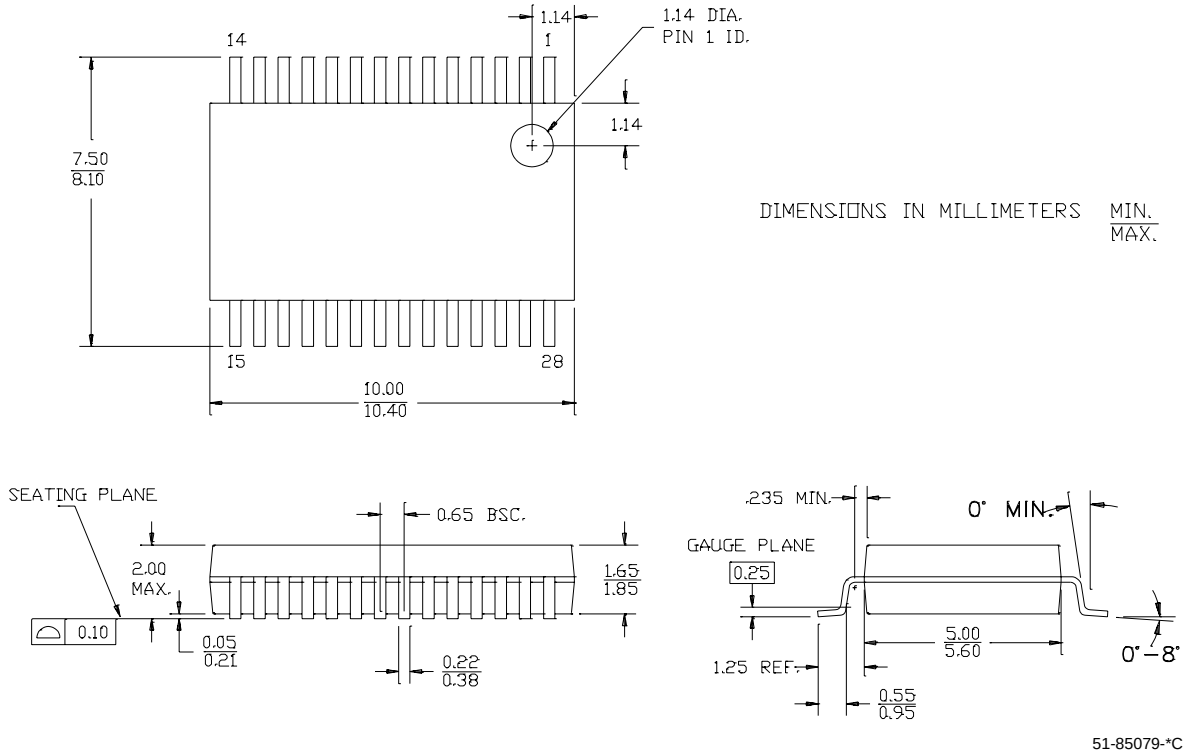
Clock Name	Max. Load (in pF)
CPU(0:3)	20

Ordering Information

Part Number	Package Type	Product Flow
CY28506OC	28-Pin SSOP	Commercial, 0° to 70°C
CY28506OCT	28-Pin SSOP - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

28-Lead (5.3 mm) Shrunk Small Outline Package O28



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**	111133	02/21/02	DMG	New data sheet