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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E40RC-FS1000-C

Overview:

- 4.0-inch TFT: 480x480 (77x80)
- MIPI/DSI Interface
- 16.7M colors
- CTP I2C Interface
- White LED back-light
- Transmissive/ Normally Black
- Capacitive Touch Panel
- 1000 NITS
- Controller: ST7701S
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit and backlight unit. The resolution of the 4.0" TFT-LCD contains 480x480 pixels and can display up to 16.7M colors.

Features

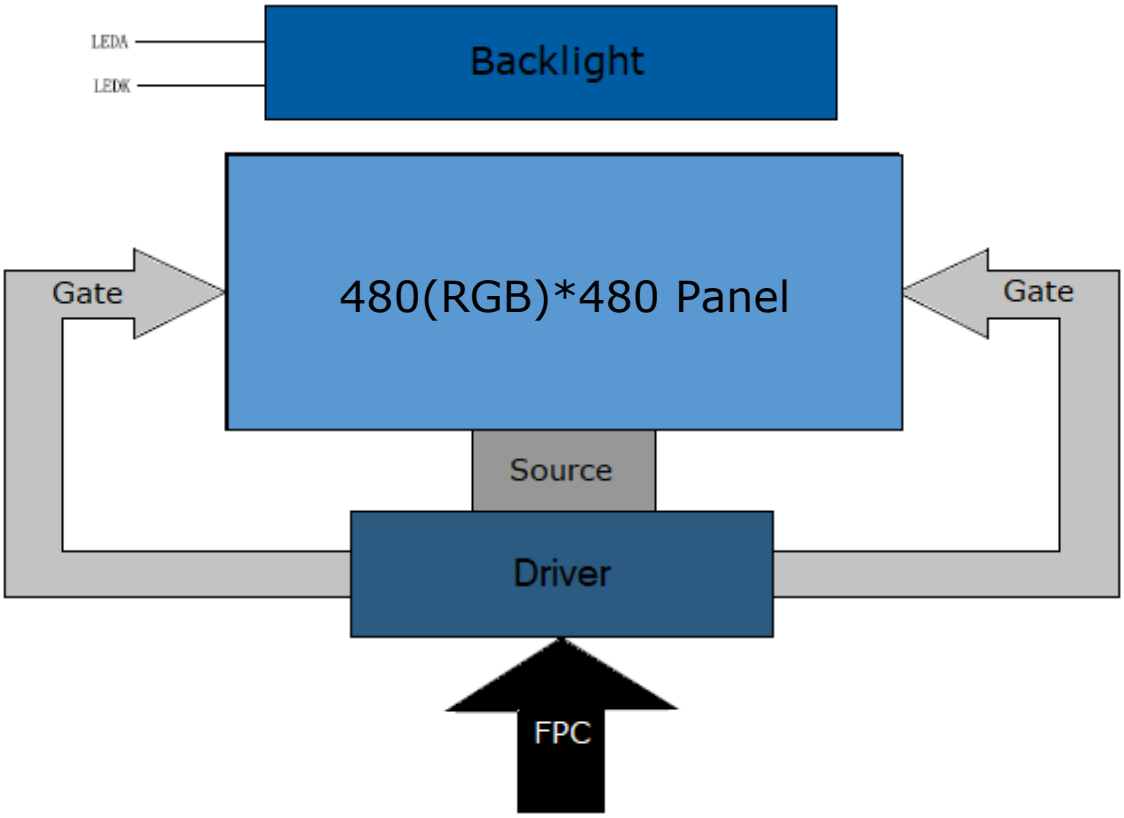
Low Input Voltage: 3.3V (TYP)
Display Colors: 16.7M colors
TFT Interface: MIPI/DSI
CTP Interface: I2C

General Information Items	Specification Main Panel	Unit	Note
TFT Display Area (AA)	71.86(H) x 70.18(V) (3.95 inch)	mm	-
Driver Element	TFT active matrix	-	-
Display Colors	16.7M	colors	-
Display Resolution	480(RGB)x480	pixels	-
TFT Pixel Arrangement	RGB stripe	-	-
Pixel Pitch	0.1497(H)*0.1462(V)	mm	-
Viewing Angle	ALL	o'clock	-
TFT Controller IC	ST7701S	-	-
LCM Interface	2-lane MIPI	-	-
Display Mode	Transmissive/Normally Black	-	-
CTP Structure	G+G	-	-
CTP Controller IC	GT911	-	-
CTP Slave Address	0x5D(7bit) or 0x14(7bit)	-	-
Touch Mode	Five points and Gestures	-	-
Operating Temperature	-30～+85	℃	-
Storage Temperature	-40～+90	℃	-

Mechanical Information

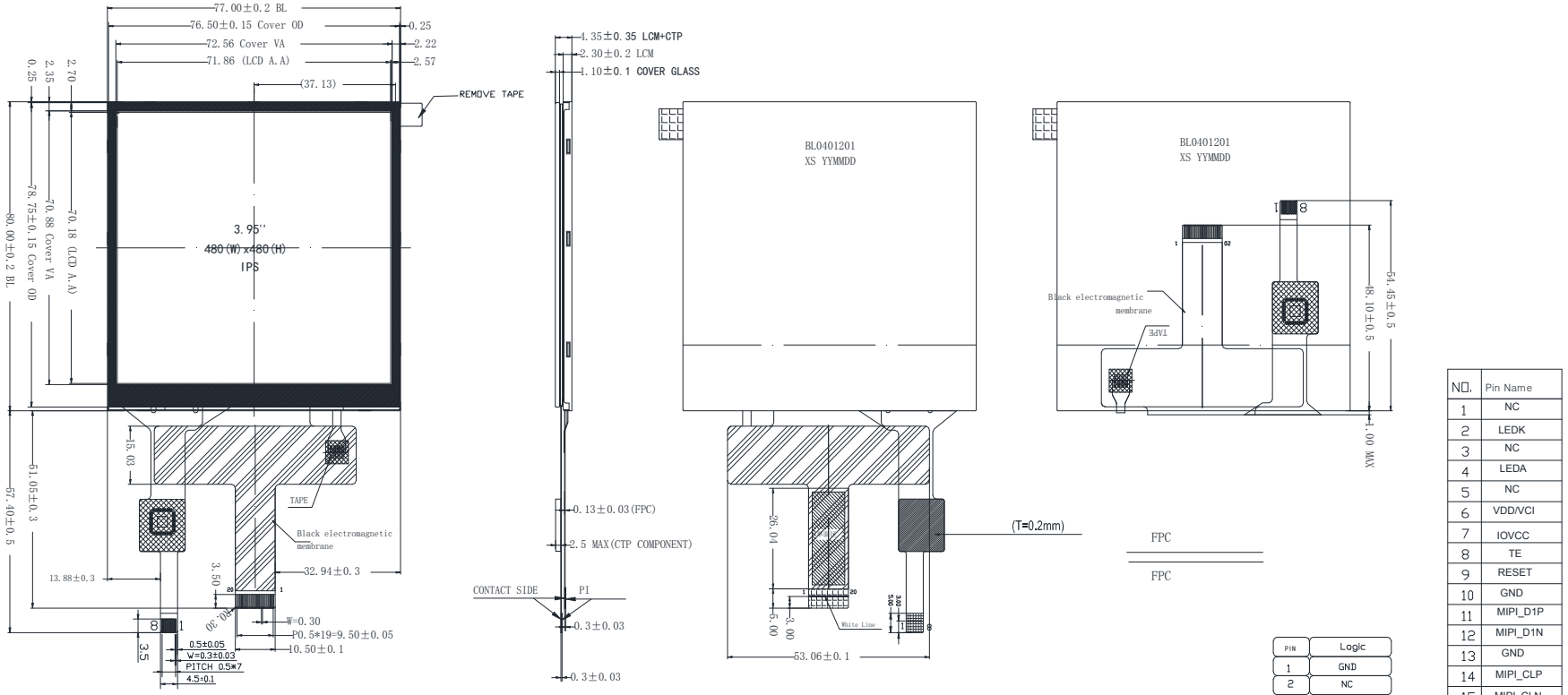
Item		Min	Typ.	Max	Unit	Note
Module Size	Height (H)		77		mm	-
	Vertical (V)		80		mm	-
	Depth (D)		4.35		mm	-
Weight			TBD		g	-

1. Block Diagram



2. Outline Dimensions

ReV.	Revision content description	Date
V0	FIRST	2019.02.20

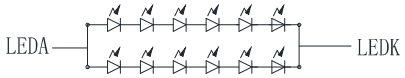


NO.	Pin Name
1	NC
2	LEDK
3	NC
4	LEDA
5	NC
6	VDD/VCI
7	IOVCC
8	TE
9	RESET
10	GND
11	MIPI_D1P
12	MIPI_D1N
13	GND
14	MIPI_CLP
15	MIPI_CLN
16	GND
17	MIPI_D0P
18	MIPI_D0N
19	GND
20	GND

PIN	Logic
1	GND
2	NC
3	VDD
4	SCL
5	SDA
6	INT
7	RST
8	GND

NOTES:

1. DISPLAY TYPE:3.5", TFT-LCD, 16.7M COLORS
2. DISPLAY MODE: NORMALLY BLACK
3. VIEWING DIRECTION: ALL
4. LCM DRIVER IC: ST7701S(COG)
5. LCM Interface: MIPI
6. Touch Mode: Multi-touch
7. Touch Driver: GT911
8. Touch Interfac: I2C
9. Touch and LCM Bonding technology: Optical Bonding
10. VDD/VCI: 3.3V;IOVCC:1.8~3.3V
11. OPERATING TEMP: -30°C TO 85°C
    STORAGE TEMP: -40°C TO 90°C
12. BACK LIGHT: LED WHITE, 12 LED, 40mA,18.6±0.3V
13. Contrast Ratio:
14. LCM Brightness: cd/m2
15. RoHS COMPLIANT.



CIRCUIT DIAGRAM

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	DRAWING NAME	E40RC-FS1000-N	
TOLERANCE UNLESS OTHERWISE SPECIFIED X.X±0.3 X.XX±0.2	Drawn		Unit
	Checked		mm
Scale 1:1	Approve		Page 1/1

3. Input TFT Terminal Pin Assignment

Recommended TFT Connector: FH19C-20S-0.5SH(10) | Recommended CTP Connector: FH12-8S-0.5SH(55)

NO.	Symbol	Description	I/O
1	NC	--	--
2	LEDK	Cathode pin of backlight	P
3	NC	--	--
4	LEDA	Anode pin of backlight	P
5	NC	--	--
6	VDD/VCI	Supply voltage (3.3V)	P
7	IOVCC	I/O power supply voltage	P
8	TE	Tearing effect output. Leave pin open when not used.	O
9	RESET	External reset input. Initializes the chip with low input. Execute a power on reset after applying power.	I
10	GND	Ground	P
11	MIPI_D1P	MIPI DSI differential data pair (DSI-Dn+/-)	I/O
12	MIPI_D1N		I/O
13	GND	Ground	P
14	MIPI_CLP	MIPI DSI differential clock pair (DSI-CLK+/-)	I
15	MIPI_CLN		I
16	GND	Ground	P
17	MIPI_D0P	MIPI DSI differential data pair (DSI-Dn+/-)	I/O
18	MIPI_D0N		I/O
19	GND	Ground	P
20	GND	Ground	P

I: Input, O: Output, P: Power

3.1 CTP

NO.	Symbol	Description	I/O
1	GND	Ground	P
2	NC	No connection	
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I
6	INT	External interrupt to the host	I
7	RST	External reset, low is active	I
8	GND	Ground	P

4. LCD Optical Characteristics

4.1 Optical Specifications

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Contrast Ratio		CR	Normal Viewing Angle θ=0	640	800	--	--	(2)
Response Time	Rising	TR+TF		--	25	35	ms	(4)
	Falling							
Uniformity		S(%)		55	60	--	%	(5)
Color Filter Chromaticity	White	W_X		0.269	0.309	0.349	--	(5)(6)
		W_Y		0.310	0.350	0.390		
	Red	R_X		0.571	0.611	0.651		
		R_Y		0.323	0.363	0.403		
	Green	G_X		0.277	0.317	0.357		
		G_Y		0.530	0.570	0.610		
	Blue	B_X		0.110	0.150	0.190		
		B_Y		0.060	0.100	0.140		
Viewing Angle	Hor.	ΘL	CR>10	70	80	--	degree	(1)(6)
		ΘR		70	80	--		
	Ver.	ΘT		70	80	--		
		ΘB		70	80	--		
Option View Direction		ALL						(1)

4.2 Measuring Conditions

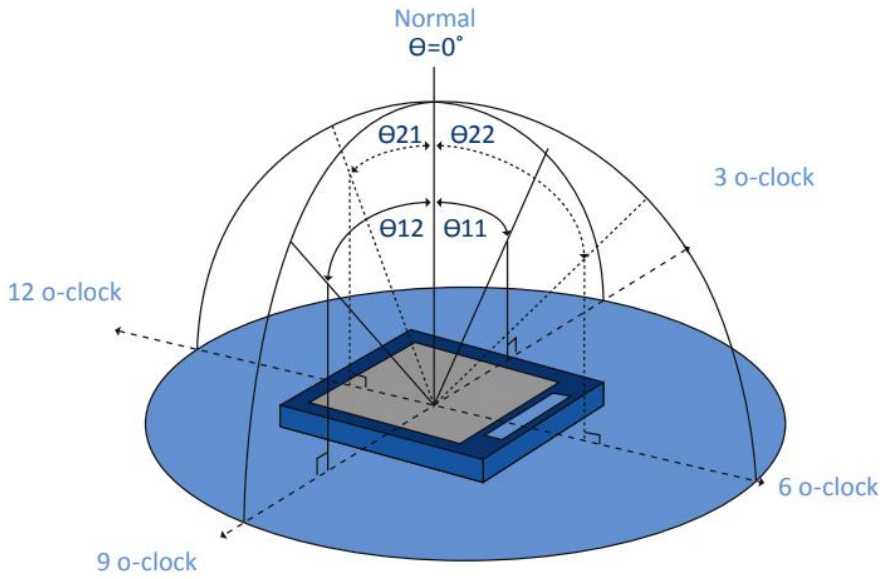
Measuring surrounding: dark room

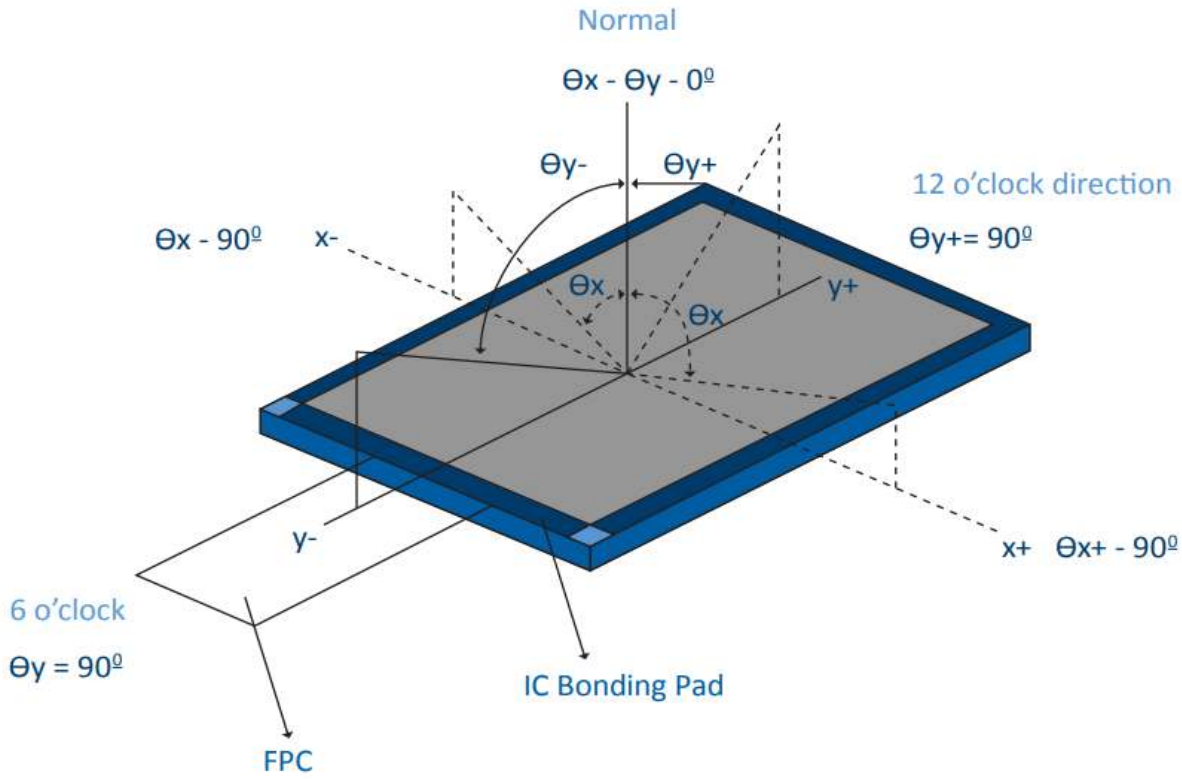
Ambient temperature: 25±2˚C

15 min. warm-up time

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.

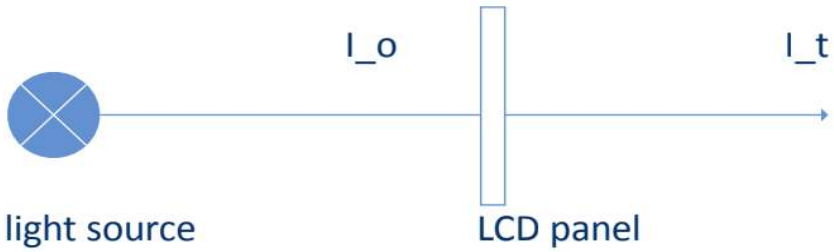




(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving.

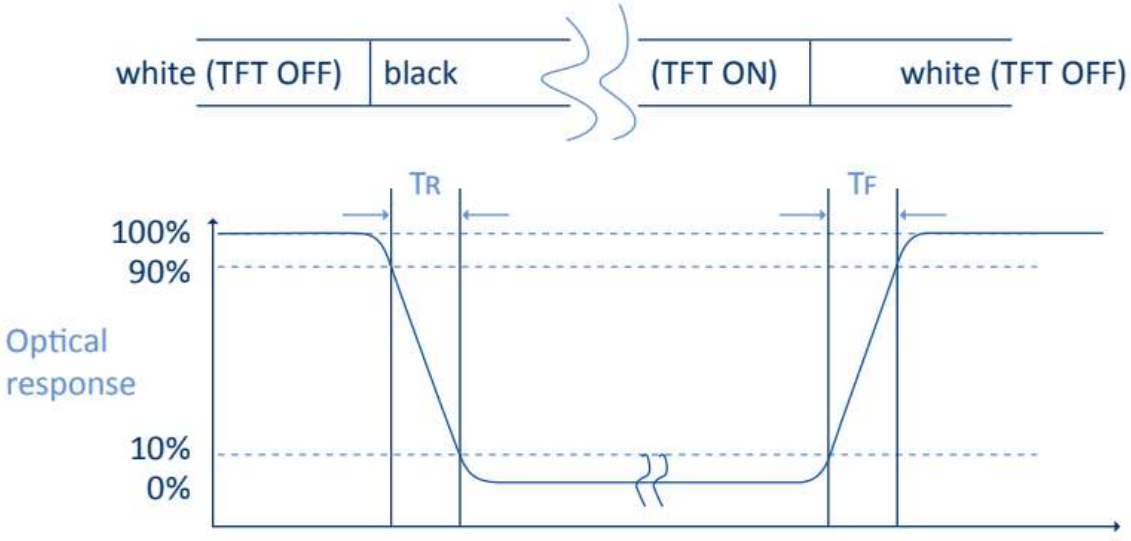


The transmittance is defined as:

$$Tr = \frac{It}{Io}\ x\ 100\%$$

Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut: Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

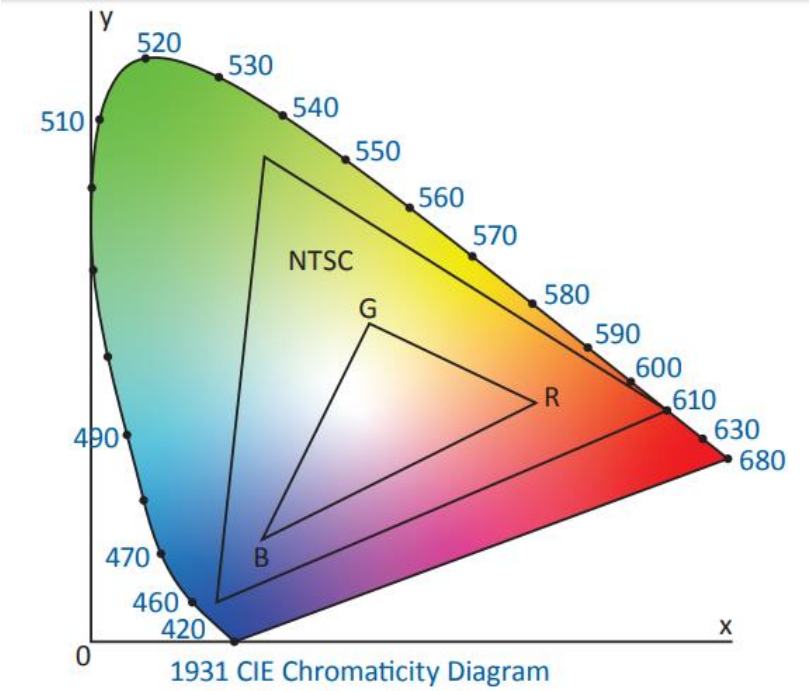
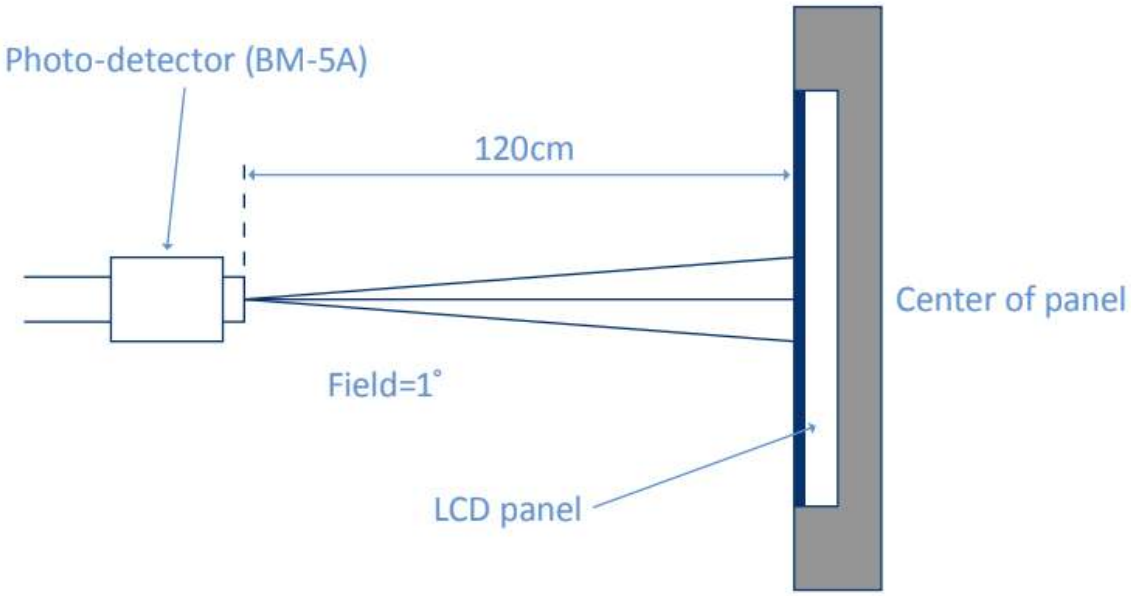


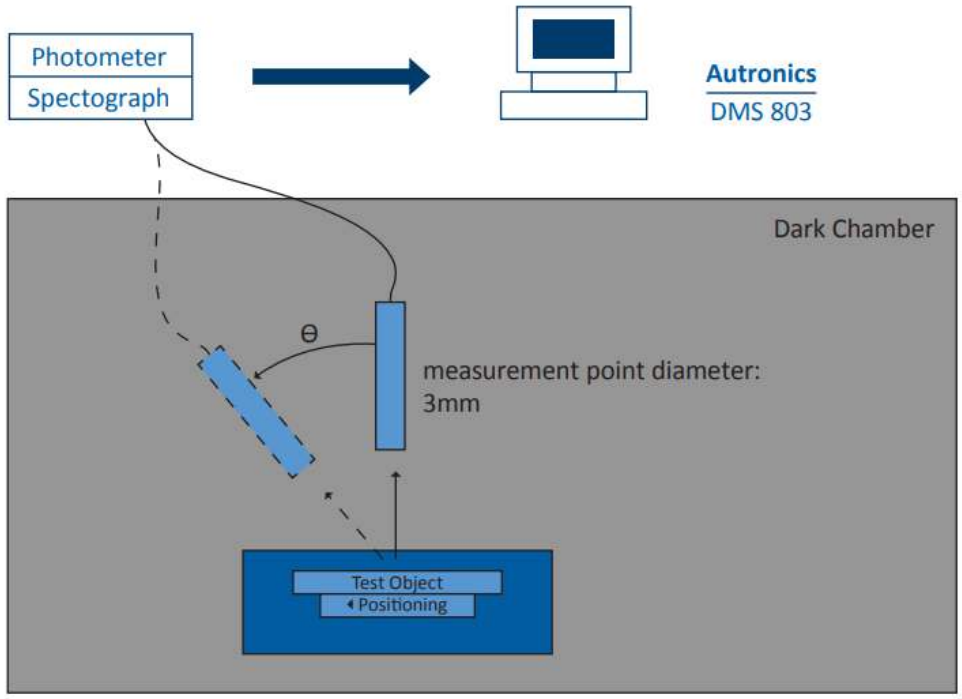
Fig. 1931 CIE chromacity diagram

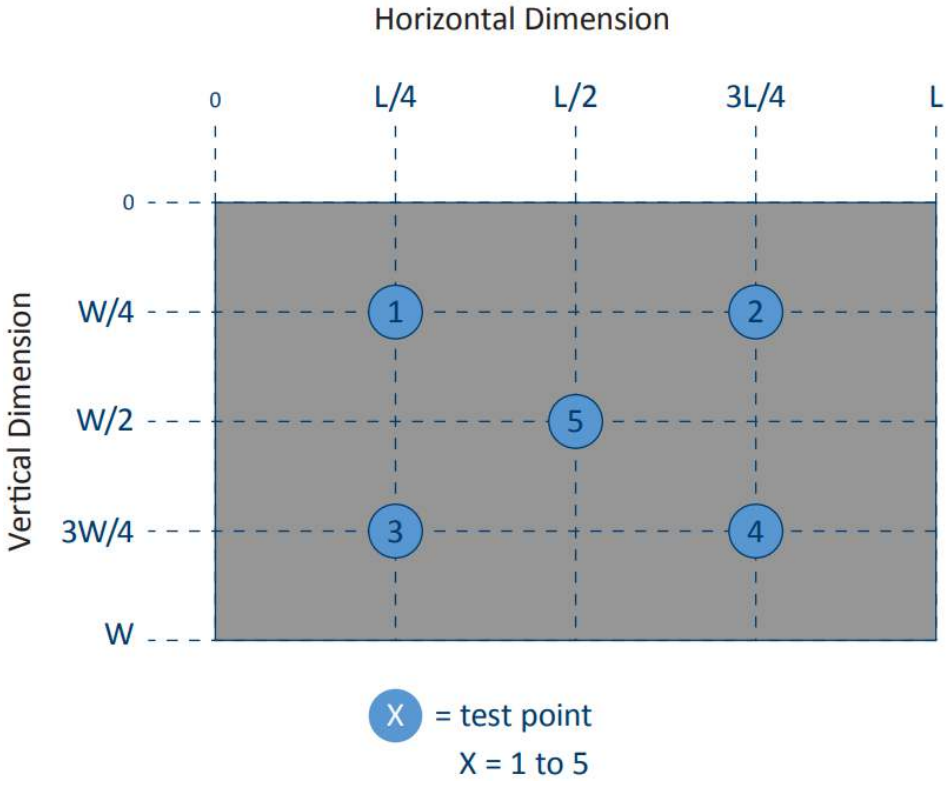
$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:



(6) Optical Measurement Setup Continued:
The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.





5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

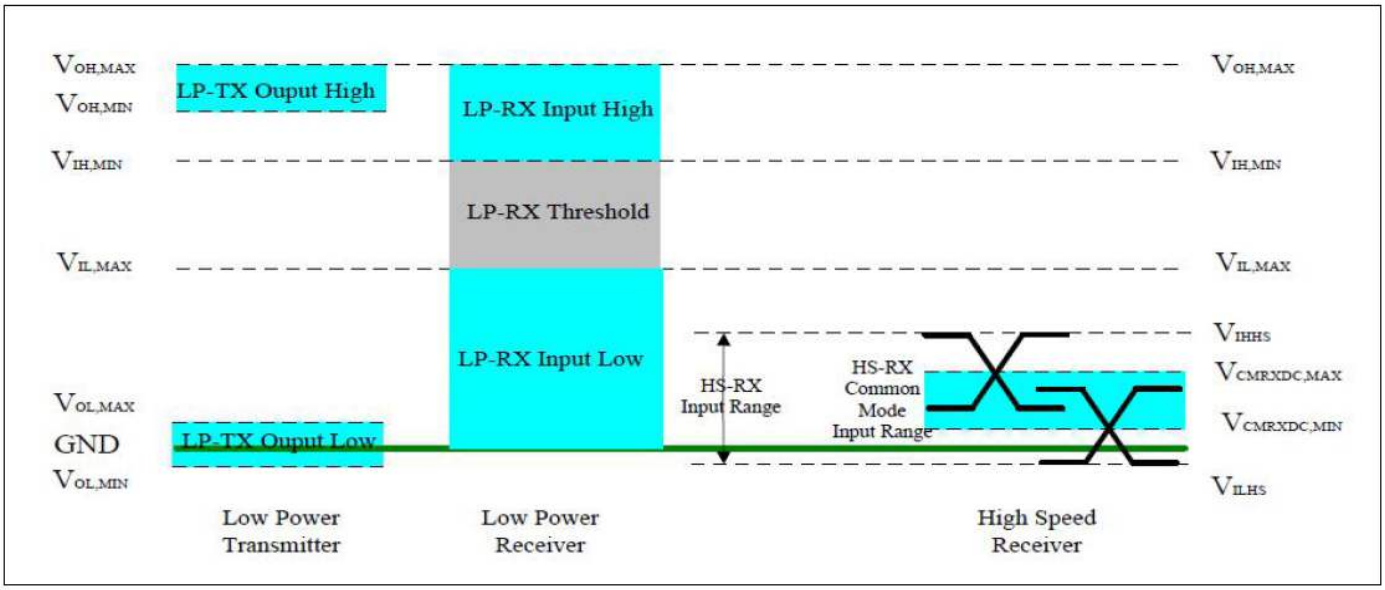
Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VCI	-0.3	4.6	V
Digital Interface Supply Voltage	IOVCC	-0.3	4.6	V
Operating Temperature	TOP	-30	+85	℃
Storage Temperature	TST	-40	+90	℃

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	3.6	V	
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3	V	
Normal Mode Current	IDD	--	30	--	mA	
Differential Input High Threshold Voltage	VIT+	--	0	50	mV	MIPI_CLK MIPI_Data
Differential Input Low Threshold Voltage	VIT-	-50	0	--	mV	
Single-ended Receiver Input Operation Voltage Range	VIR	0.5	--	1.2	V	

5.3 MIPI DC Electrical Characteristics



Characteristics	Symbol	Min	Typ.	Max	Unit
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	VLPH	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single ended input low voltage	VILHS	-40	--	--	mV
Single ended input high voltage	VIHHS	--	--	460	mV
Common mode voltage	VCMRXDC	70	--	330	mV
Differential input impedance	ZID	80	100	125	Ω
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	VI	-50	--	1350	mV
Logic 0 input threshold	VIL	0	--	550	mV
Logic 1 input threshold	VIH	880	--	1350	mV
Output low level	VOL	-50	--	50	mV
Output high level	VOH	1.1	1.2	1.3	V

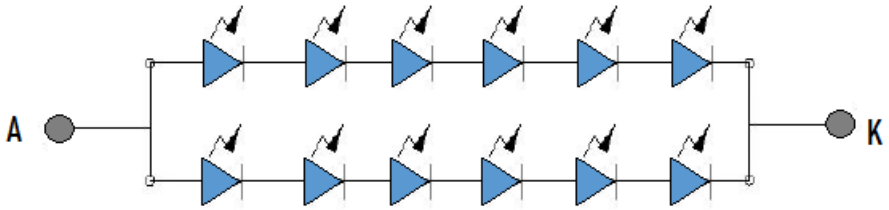
5.4 LED Backlight Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	35	40	--	mA	
Forward Voltage	VF	--	18.6	--	V	
LCM Luminance	LV	900	950	--	cd/m2	Note 3
LED lifetime	Hr	--	50000	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

The back-light system is edge-lighting type with 12 chips White LED

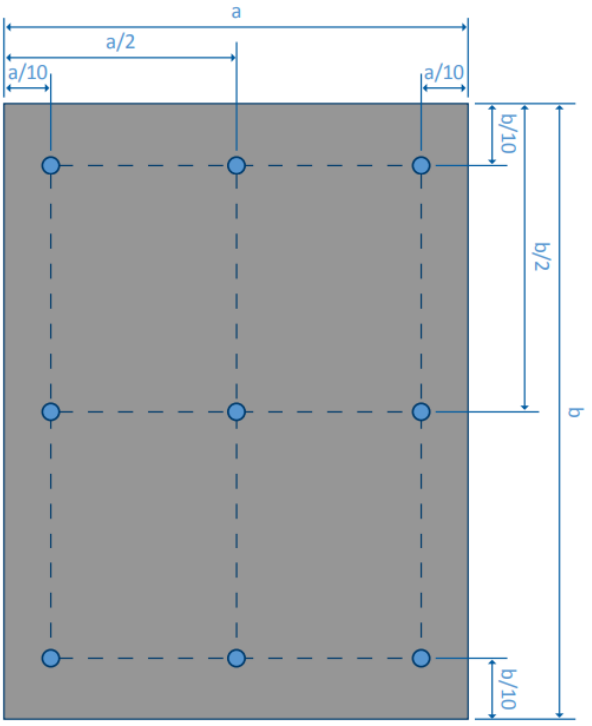
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.



Backlight LED Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

6. MIPI Interface AC Characteristics

6.1 High Speed Mode

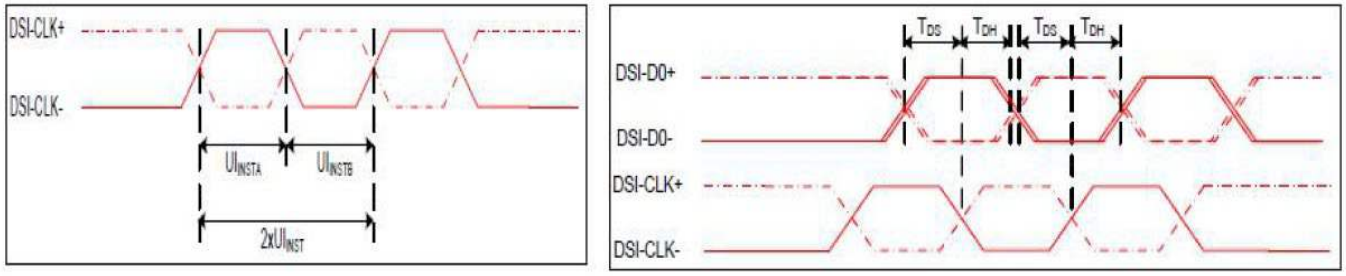


Figure 6.1: DSI Clock Channel Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Note
DSI-CLK+/-	2xUIINSTA	Double UI Instantaneous	4	25	ns	
DSI-CLK+/-	UIINSTA UIINSTB	UI Instantaneous Halves	2	12.5	ns	UI=UIINSTA=UIINSTB
DSI-Dn+/-	tDS	Data to clock setup time	0.15	--	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	--	UI	

Table 6.1: MIPI Interface High Speed Mode Timing Characteristics

6.2 Low Power Mode

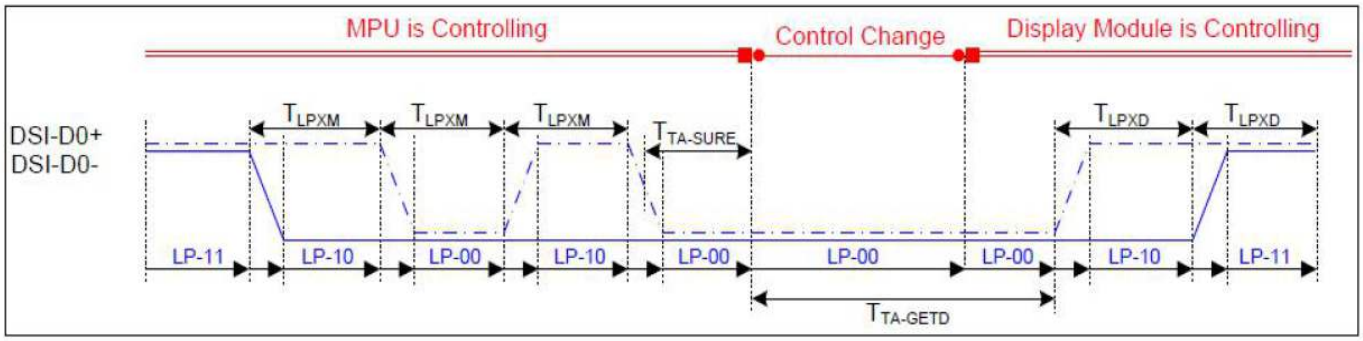


Figure 6.2: Bus Turnaround (BTA) from Display Module to MPU Timing Diagram

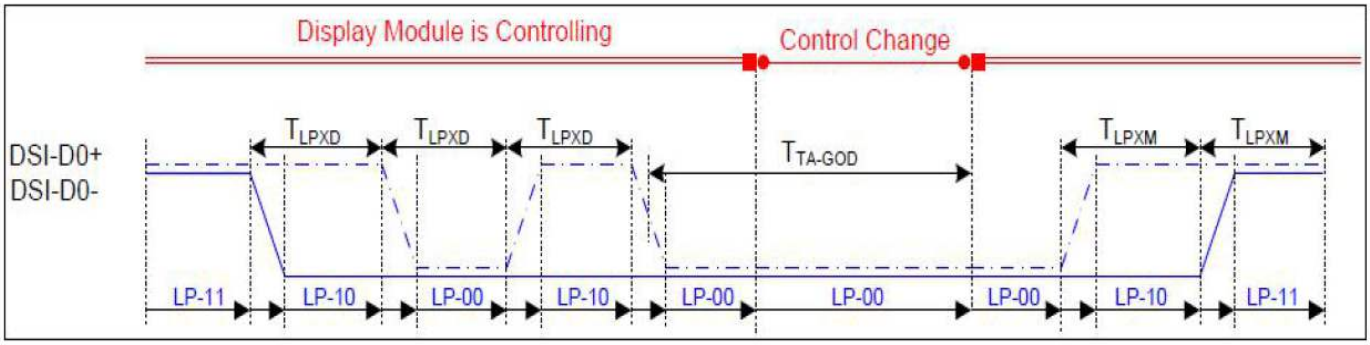


Figure 6.3: Buss Turnaround (BTA) from MPU to Display Module Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Note
DSI-D0+/-	TLPXM	Length of LP-00, LP_01, LP-10 or LP-11 periods MPU-> Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00, LP_01, LP-10 or LP-11 periods MPU-> Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU starts driving	TLPXD	2xTLPXD	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	5xTLPXD		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	4xTLPXD		ns	Output

Table 6.2: MIPI Interface Low Power Mode Timing Characteristics

6.3 Bursts Mode

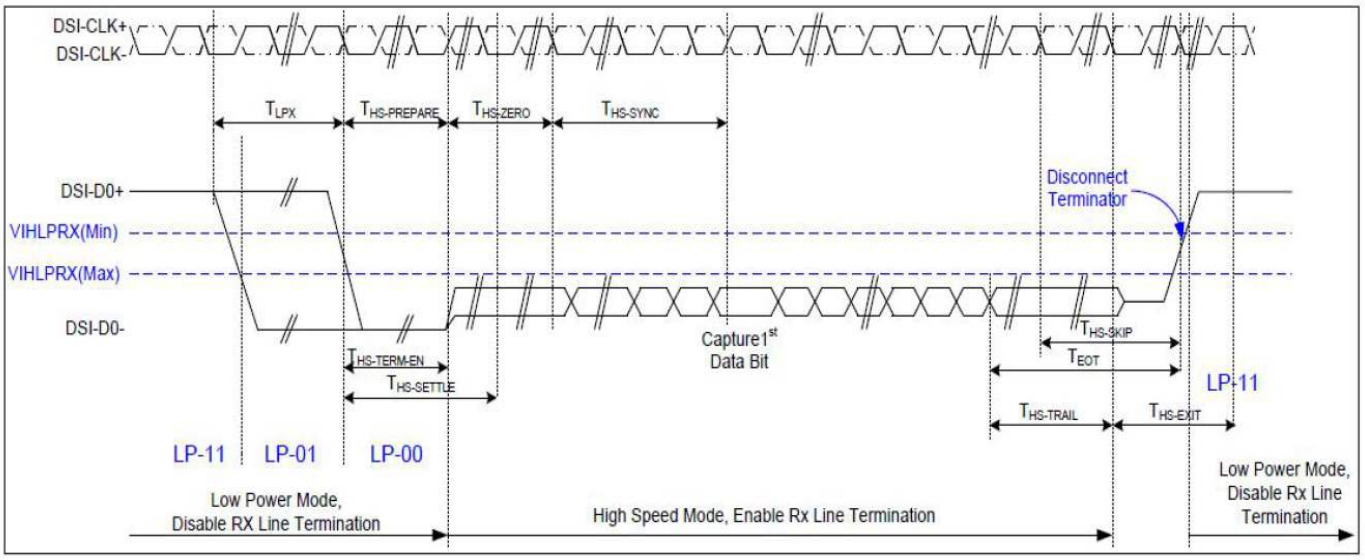


Figure 6.4: Data Lanes Low Power Mode to/from High Speed Mode Timing Diagram

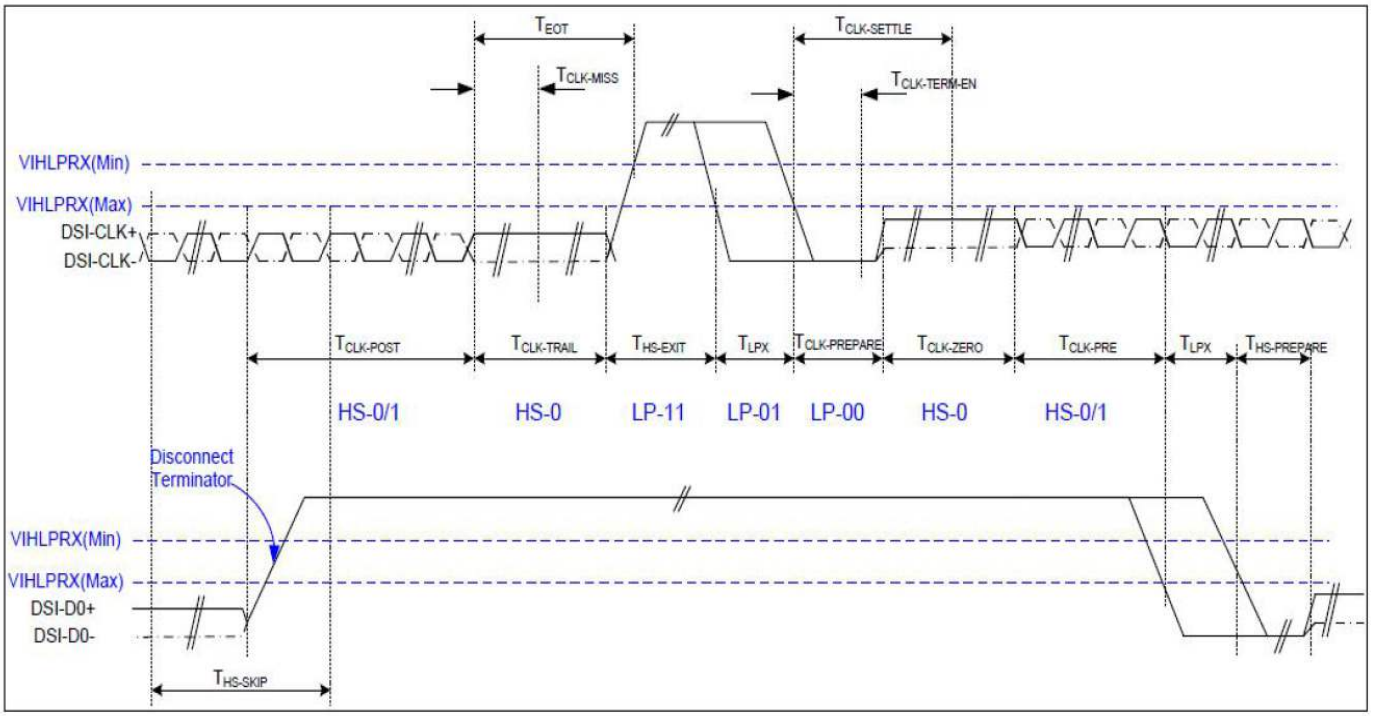


Figure 6.5: Clock Lanes High Speed Mode to/from Low Power Mode Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Note
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	--	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4UI	85+6UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	--	35+4UI	ns	Input
DSI-Dn+/-	THS-PREPARE+ THS-ZERO	THS-PREPARE+time to drive HS-0 before the sync sequence	140+10UI	--	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	--	ns	Input
DSI-Dn+/-	THS-TRIAL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4UI	--	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transitioned to LP mode	60+52UI	--	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	--	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	--	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for Hs transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time out at clock ands display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE+ TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	--	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	--	ns	Input
DSI-CLK+/-	TEOT	Time from start of TCLK-TRAIL period to start of LP-11 state	--	105+12 UI	ns	Input

Table 6.3: Bursts Mode LP to/from HS Mode Timing Characteristics

6.4 Reset Timing

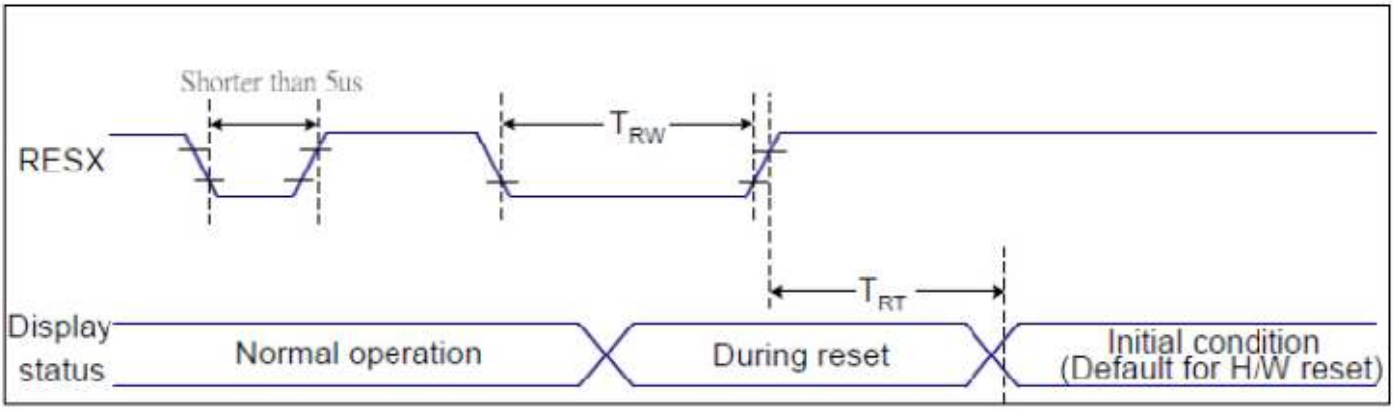


Figure 6.6: Reset Timing Diagram

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

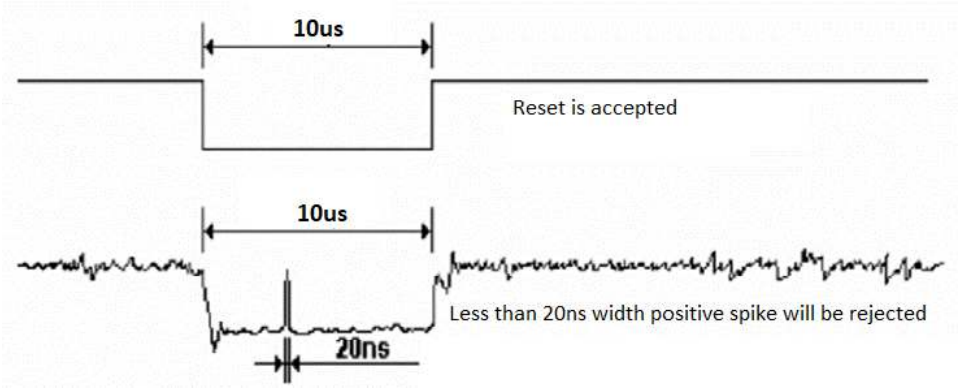
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. CTP Electrical Characteristics

7.1 Absolute Maximum Rating

Characteristics	Symbol	Min	Max	Unit
Power Supply Voltage	VDD	2.66	3.47	V
I/O Digital Voltage	VDDIO	--	--	V
Operating Temperature	TOP	-20	+70	℃
Storage Temperature	TST	-30	+80	℃

Table 7.1: CTP Absolute Maximum Rating Characteristics

NOTE: If used beyond the absolute maximum ratings, GT911 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the conditions not within the electrical characteristics, it may affect the reliability of the device.

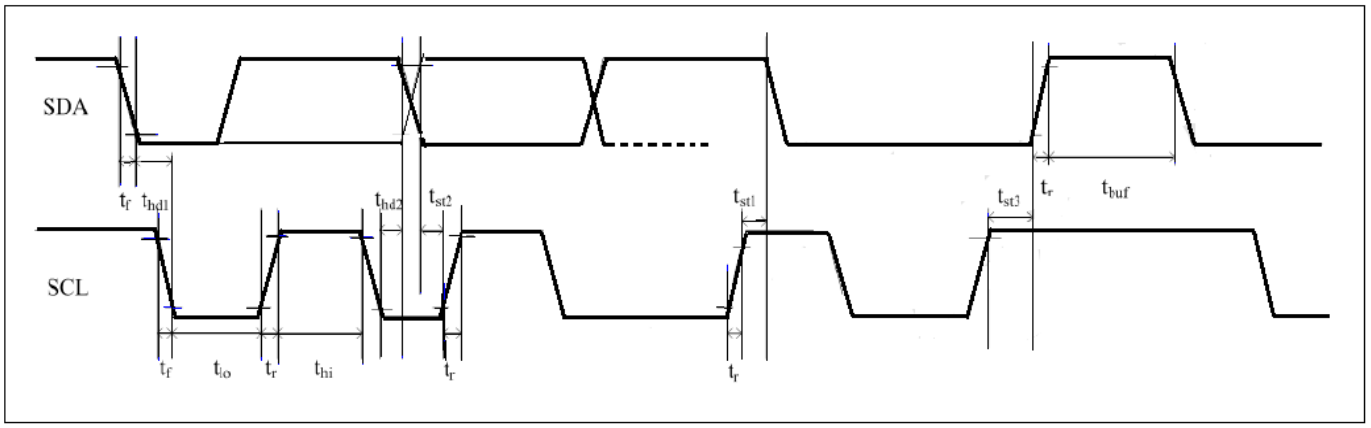
7.2 DC Electrical Characteristics (Ta=25˚C)

Characteristics	Symbol	Min	Typ.	Max	Unit
Power Supply Voltage	VDD	2.66	3.3	3.47	V
Doze Mode Operating Current	Io	--	0.78	--	mA
Normal Operation Mode Current Consumption	Iopr	--	8	--	mA
Green Mode Current Consumption	Imon	--	3.3	--	mA
Sleep Mode Current Consumption	Isip	70	--	120	uA
Level Input Voltage	VIH	0.75VDD	--	VDD+0.3	V
	VIL	-0.3	--	0.25VDD	V
Level Output Voltage	VOH	0.85VDD	--	--	V
	VOL	--	--	0.15VDD	V

Table 7.2: CTP DC Electrical Characteristics

7.3 I2C Interface Characteristics

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is recommended that transmission rate be kept at or below 400kbps. The figure shown below is the I2C timing:



Parameter	Symbols	Condition	Min	Max	Units
SCL low period	t_{lo}		1.3		us
SCL high period	t_{hi}		0.6		us
SCL setup time for start condition	t_{st1}		0.6		us
SCL setup time for stop condition	t_{st3}		0.6		us
SCL hold time for start condition	t_{hd1}		0.6		us
SDA setup time	t_{st2}		0.1		us
SDA hold time	t_{hd2}		0		us

Table 7.3: I2C AC Characteristics, 1.8V interface voltage, 400kbps transmission rate, 2k pull-up resistor

Parameter	Symbols	Condition	Min	Max	Units
SCL low period	t_{lo}		1.3		us
SCL high period	t_{hi}		0.6		us
SCL setup time for start condition	t_{st1}		0.6		us
SCL setup time for stop condition	t_{st3}		0.6		us
SCL hold time for start condition	t_{hd1}		0.6		us
SDA setup time	t_{st2}		0.1		us
SDA hold time	t_{hd2}		0		us

Table 7.4: I2C AC Characteristics, 3.3V interface voltage, 400kbps transmission rate, 2k pull-up resistor

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. The configuration methods and timings are shown below:

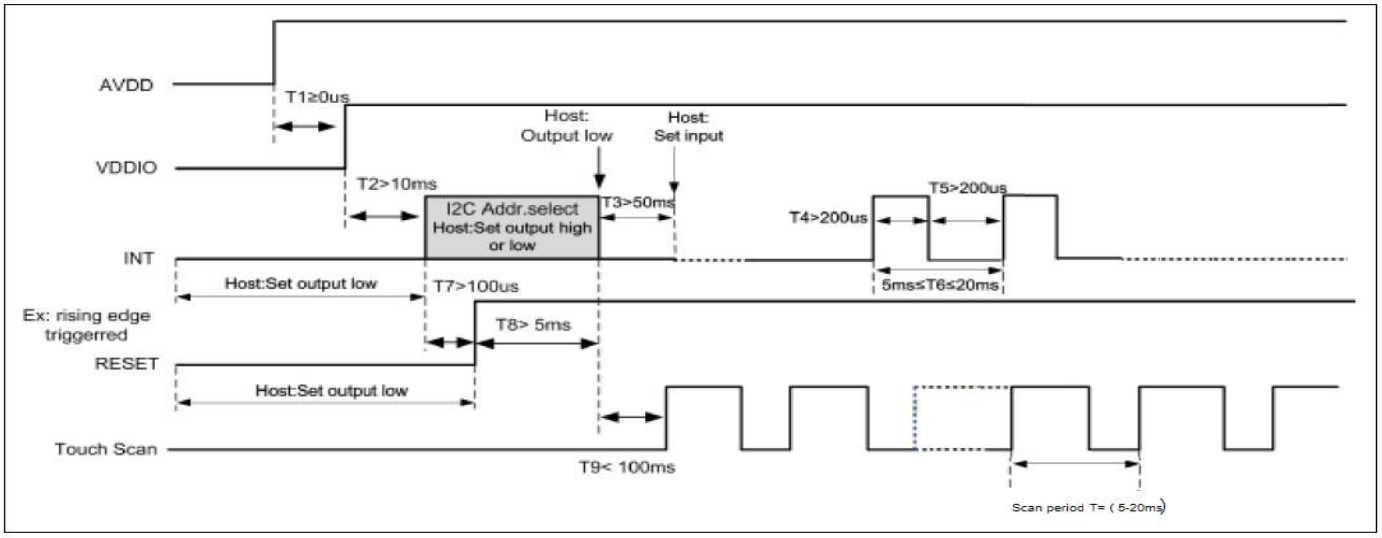


Figure 7.1: I2C Power on Timing

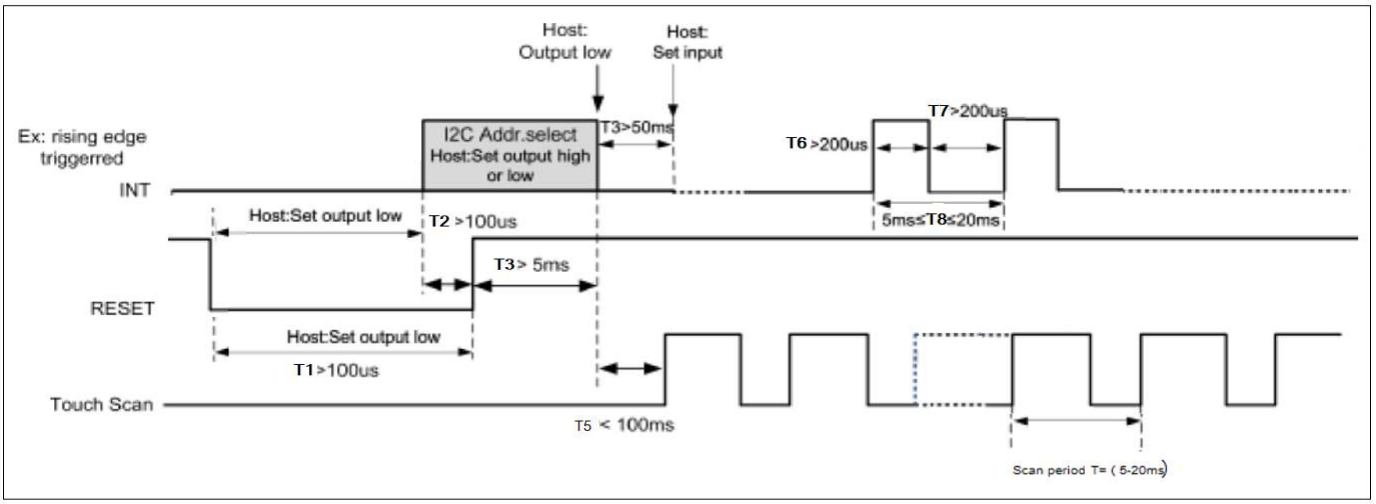


Figure 7.2: I2C Host Resetting Timing

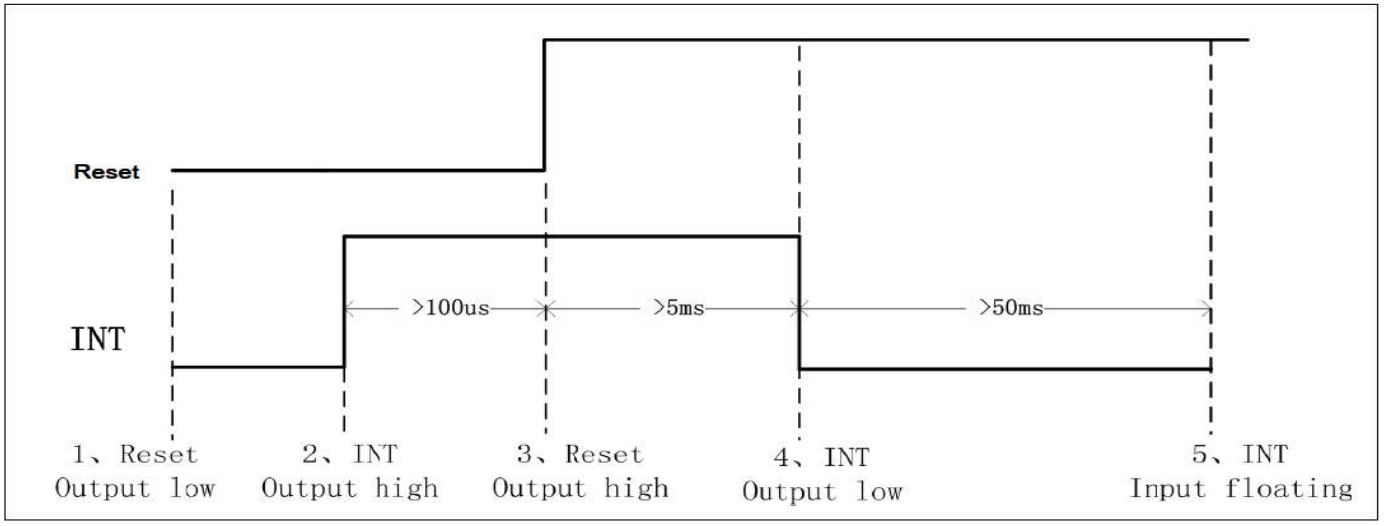


Figure 7.3: Setting Slave Address to 0x28/0x29 Timing

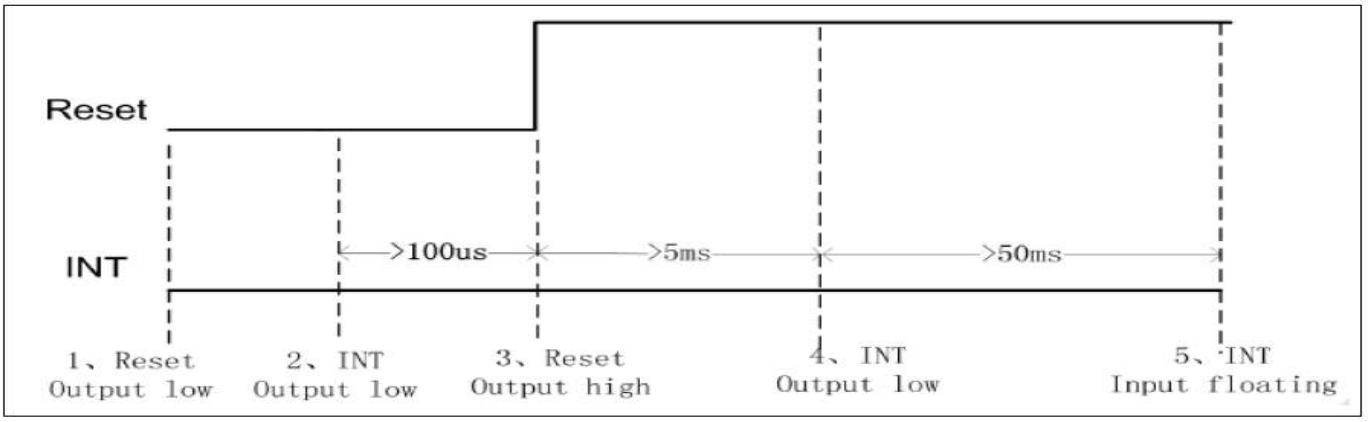


Figure 7.4: Setting Slave Address to 0xBA/0xBB Timing

Data Transmission *(ex. 0xBA/0xBB)*

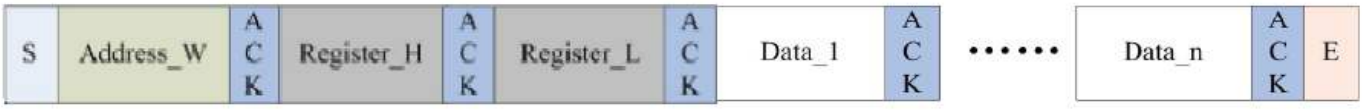
Communication is always initiated by the host. Valid start condition is signaled by pulling SDA line from high to low when SCL is high. Data flow or address is transmitted after the start condition.

All slave devices connected to I2C bus should detect the 8-bit address issued after start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely not 0xBA or 0xBB, GT911 will stay in an idle state.

For data bytes on SDA, each of the 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is high. When communication is completed the host will issue the stop condition. Stop condition implies the transition of SDA line from low to high when SCL is high.

Writing Data to GT911

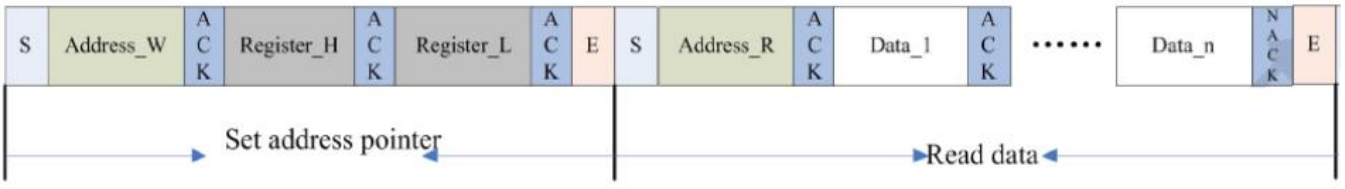
The diagram displays the timing sequence of the host writing data onto GT911. First the host issues a start condition. The host sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates write operation) to the slave device. After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register)



The location of the register address pointer will automatically add 1 every write operation. When the host needs to perform write operations on a group of registers of continuous addresses it can write continuously. The write operation is terminated when the host issues the stop condition.

Reading Data from GT911

The diagram below is the timing sequence of the host reading data from GT911. The host issues the start condition and sends 0xBA (Address bits and R/W bit, R/W bit as 0 indicates write operation) to the slave device. After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.



The host issues the start condition once again and sends 0xBB (read operation). After receiving ACK, the host starts to read the data. GT911 also supports continuous read operation. When receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

8. Cautions and Handling Precautions

8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

8.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.