Texas Instruments

UCC3976/7 Dual Evaluation Module

User's Guide

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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UCC3976/7 Dual Evaluation Module

Power Supply Control Products

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1 Introduction

1.1 UCC3976/7 Dual Evaluation Module Design Note

The UCC3976/7 dual evaluation modules are dc/ac inverter modules used to drive a cold cathode fluorescent lamp (CCFL) with a piezoelectric transformer (PZT). This evaluation module (EVM) consists of two separate circuits. One is a half-bridge circuit using the UCC3976 controller. The other is a push-pull circuit using the UCC3977 controller.

The principle of operation for the inverter is explained in the application section of the UCC3975/6/7 data sheet. This design note explains the design procedures for the two circuits. Section 2 describes the half-bridge design, while Section 3 describes the push-pull design.

2 Half-Bridge Design With the UCC3976 Controller

A schematic for the UCC3976 EVM is given in Figure 1. Recommended parts lists are provided in Table 1. The evaluation board components can be modified depending on the application require ments.

This EVM is designed for a 400-V cold-cathode fluorescent lamp (CCFL) with a 12-V input voltage. The input voltage range changes for lamps that have different voltage requirements.

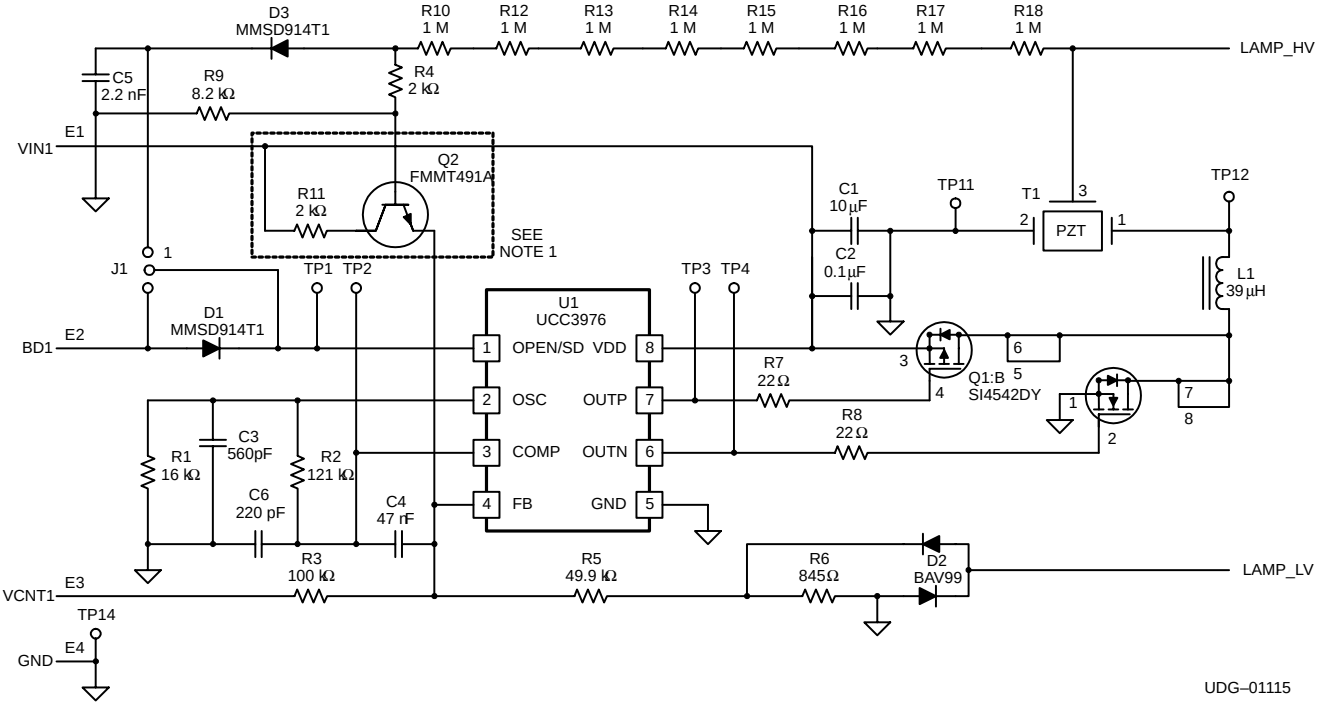

Figure 1. Evaluation Module Schematic for UCC3976

2.1 Half-Bridge Inductor Selection

The inductor and the capacitor from the primary side of a PZT form a low-pass filter, which should pass the resonant frequency required by the PZT and attenuate higher harmonic components. The resonant frequency formed by the LC filter can be calculated by equation 1.

$$f = \frac{1}{2\pi\sqrt{L \times C_{IN}}} \quad (1)$$

where C_{IN} is the primary capacitance of the PZT.

In the EVM, the inductance value is 39 μH while the input capacitance of the PZT is 105 nF. The resulting LC resonant frequency is around 78 kHz. The resonant frequency of the PZT, which is also the operating frequency, is around 55 kHz. Therefore the LC circuit passes the 55 kHz fundamental, yet attenuates higher harmonics.

If the external inductance is too low, a non-sinusoidal primary waveform results, since higher order harmonics are allowed through the filter. A low value inductor also increases circulating currents and results in lower efficiency. If the inductance is too large, it causes attenuation of the input voltage to the PZT and increases its gain requirements.

2.2 Frequency Range Setting

The VCO frequency range is programmed with external components R1, R2, and C3. The frequency is determined by the voltage decay from 1.7 V to 0.7 V at the OSC pin. When the voltage reaches 0.7 V, an internal current source charges OSC back to 1.7 V. The decay time is determined by the value of C3 and the discharge currents generated in R1 and R2. An accurate NPO capacitor is recommended for C3 and 1% resistors are recommended for R1 and R2. The output frequency range can be calculated by equation 2:

$$f\left(V_{COMP}\right) = \frac{\left[\frac{R1+R2}{R1\times R2\times C3}\right]}{2 \times 1n\left[\frac{1.7\ V\times(R1+R2)-V_{COMP}\times R1}{\left(0.7\ V-V_{COMP}\right)\times R1+0.7\ V\times R2}\right]} \quad (2)$$

With C3 set at 560 pF, R1 at 16 kΩ, and R2 at 121 kΩ, the frequency range is 51 kHz to 71 kHz, which gives sufficient operation range.

2.3 Analog Dimming of the Lamp

For analog dimming, enable the open-lamp detection by connecting pin 1 to pin 2 of jumper J1 and ground BD1. Lamp intensity is controlled with the signal VCNT1.

Referring to Figure1, the RMS lamp current becomes:

$$I_{LAMP} = \frac{\left[1.5\ V \times (R3 + R5) - V_{CNT} \times R5\right]\pi}{\sqrt{2} \times R3 \times R6} \quad (3)$$

Zero volts on VCNT1 commands full current while 3 V commands minimum current. For the initially configured EVM, maximum current is 6 mA and minimum current is 2 mA. R6 is selected to be 845 Ω using equation 3 and setting VCNT1 to 1.5 V and lamp current to 4 mA. With R3 set to 100 kΩ, R5 is calculated to be 50 kΩ using equation 3 and setting VCNT1 to 0 V and lamp current to 6 mA. The control-voltage to lamp-current equation for the EVM is:

$$I_{LAMP}(mA) = 6.0 - 1.33 \times V_{CNT} \quad (4)$$

Figure 2 shows the normal operation waveforms. The waveforms were take at V_{IN} = 12 V and I_{LAMP} = 5 mA.

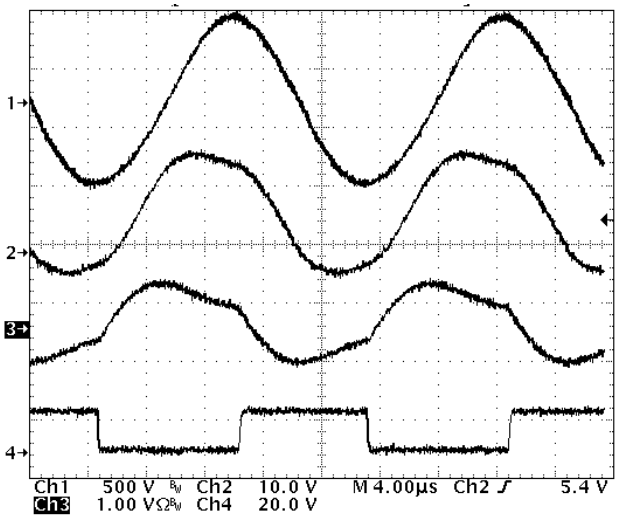

Figure 2. Half-Bridge Operation Waveform
CH1: Lamp Voltage; CH2: Primary Voltage; CH3: Primary Current; CH4: OUTN

2.4 Open-Lamp Voltage Programming

It is necessary to suspend power-stage operation if an open lamp occurs, because the piezoelectric transformer has high gain. The open-lamp detection circuit is composed of voltage divider R10, R12 through R18, R4, R9, D3, and C5. Resistors R10 and R12 through R18 are multiple series 1-MΩ resistors to stand off high voltage. A 1.5-V comparator at the OPEN pin shuts down the inverter if an open lamp is triggered. The RMS secondary voltage at which an open lamp shutdown occurs can be calculated by equation 5.

$$V_{OPEN} = \frac{\left(1.5\ V + V_{DIODE}\right) \times \left[R10 + \sum_{I=12}^{18} R_I + R9 + R4\right]}{\sqrt{2} \times (R9 + R4)}\,RMS \quad (5)$$

With R10 and R12 through R18 at 1 M each, R12 at 2 kΩ, and R9 at 8.2 kΩ, the RMS value of open lamp threshold voltage at the secondary is 1220 VRMS.

The value of capacitor C5 should be large enough to filter the sinusoid waveform into dc. For this board, 2.2 nF was chosen. If C5 is too large, it will take extra time for the OPEN/SD to climb to 1.5 V when the output voltage hits the open-lamp threshold, which results in a higher output voltage than the set value.

The open-lamp level should be set high enough to avoid tripping during normal operation. Open-lamp detection is disabled for burst-dimming mode by connecting pin 3 to pin 2 of J1. Connect pin 1 to pin 2 of J1 to enable open lamp and shutdown for analog dimming application.

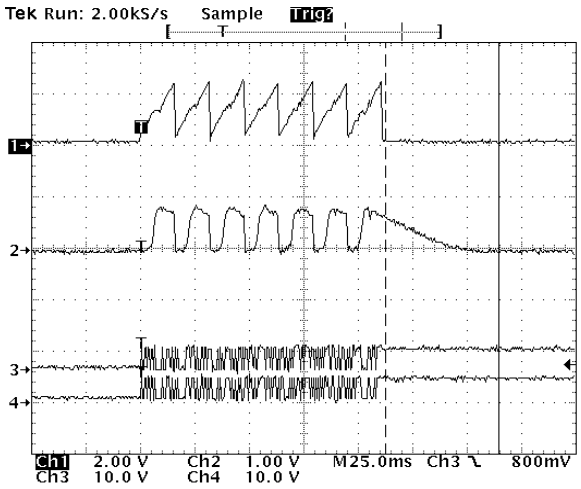

Figure 3. COMP Pin and SD/OPEN Pin During Open Lamp Start-Up
CH1: COMP; CH2: OPEN/SD; CH 3&4: OUTP/OUTN

2.5 Shutdown

The OPEN/SD pin is used for both open-lamp detection and commanded shutdown. When a voltage higher than 2.5 V is applied to OPEN/SD through D1, the part enters the shutdown or sleep mode where the oscillator is inactive and both outputs are high. In this mode, the part draws little current at the VDD pin and the OPEN/SD pin.

2.6 No-Lock

If the part fails to achieve regulation before reaching minimum frequency (Comp >2.2 V), it causes an internal retry counter to increment and then attempt another start-up. If the application does not operate normally after 7 attempts, the controller enters an error-induced shutdown state removing power to the load. Figure 4 shows the waveforms at no lock. Under low input-voltage conditions, the PZT is unable to ignite the lamp at full current. The waveforms in Figure 4 were taken at 4-V input voltage and 0-V VCNT1.

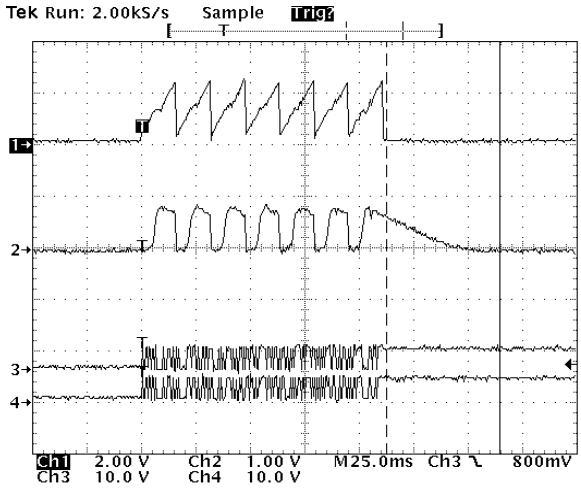

Figure 4. COMP Pin and SD/OPEN Pin During No-Lock Start-Up
CH1: COMP; CH2: OPEN/SD; CH3 & 4: OUTP/OUTN

2.7 System Efficiency and Frequency Range

Efficiencies and operating frequencies using analog dimming techniques are shown in Figure 5 and Figure 6 using a 400-V lamp. The maximum efficiency can be as high as 89%.

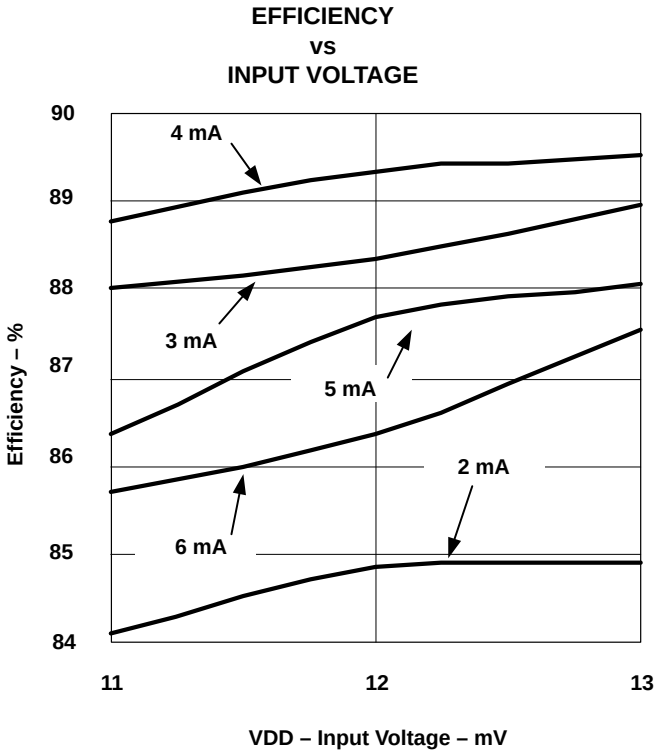

Figure 5

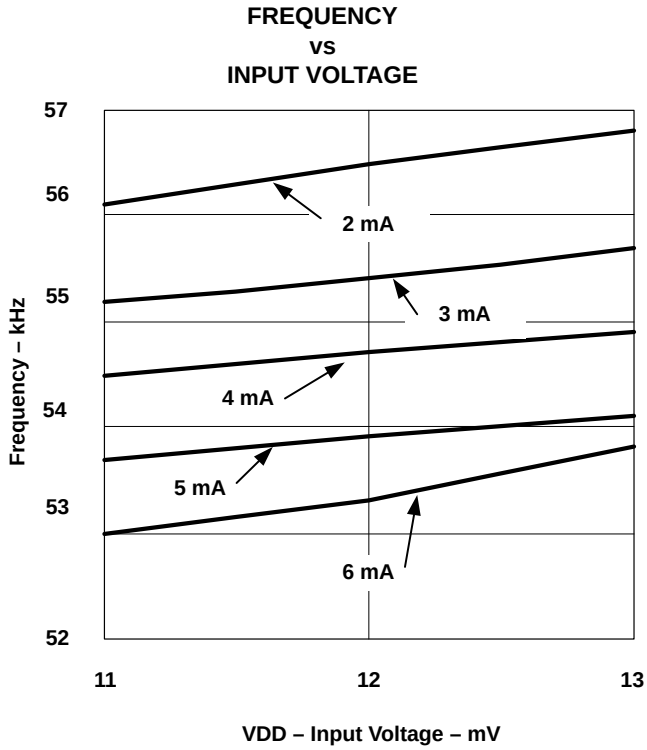

Figure 6

2.8 Burst Dimming

The UCC3976 is primarily intended for analog dimming applications. Burst dimming can be implemented at the OPEN/SD pin at the cost of open-lamp detection.

Connect pin 2 to pin 3 of J1 to disable the open-lamp detection circuit during burst dimming mode.

To implement burst dimming on the EVM, VCNT1 should be grounded to set maximum lamp brightness. A low-frequency 0-V to 5-V square wave applied to BD1 modulates the lamp current between zero and full intensity at the desired frequency. A low-frequency repetition rate of greater than 120 Hz is recommended to avoid visible flicker. Applying 5 V at BD1 forces the lamp current to zero, where 0 V at BD1 forces maximum lamp current. The duty cycle of the square wave determines the lamp brightness as a percent of rated lamp current.

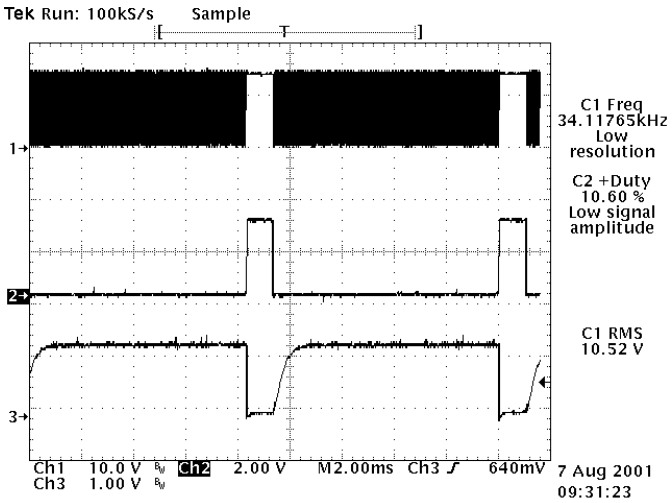

Figure 7. Burst Dimming
CH1: OUTP; CH2: OPEN/SD; CH3: COMP

2.9 Clamp Circuit (Optional)

There is also a clamp circuit to limit the maximum secondary voltage. This circuit is typically not needed since the CCFL strikes or the open lamp circuit triggers before destructive levels are reached.

If R11 and Q2 are added to the board, the peak clamp voltage for the EVM is given by equation 6:

$$V_{CLAMP} = \frac{\left(1.5\ V + V_{BE}\right) \times \left[R10 + \sum_{t=12}^{18} R_I + R9 + R4\right]}{R9}\ PEAK \quad (6)$$

The peak clamped voltage for the evaluation board is 2200 V.

Figure 8 shows the waveforms when clamp circuit is active.

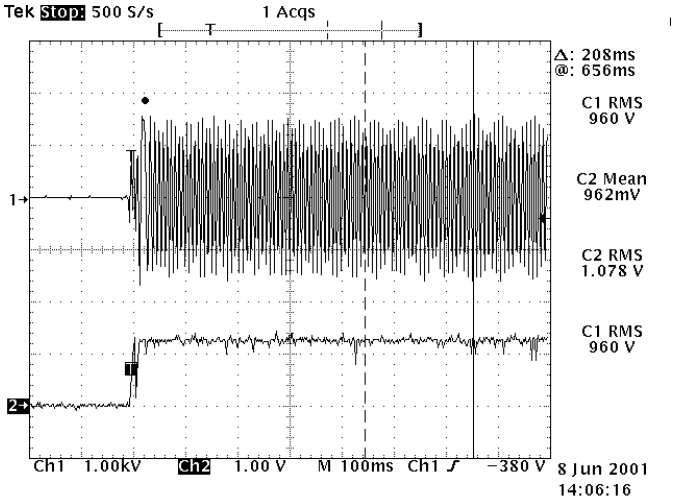

Figure 8. Clamp Circuit During Open-Lamp Start-Up
CH1: Lamp Voltage; CH 2: Comp

3 Push-Pull Design With the UCC3977 Controller

A complete schematic for the UCC3977 EVM is given in Figure 9. Recommended part lists are provided in Table 2. The evaluation board components can be modified depending on the application requirements.

The frequency-range, open-lamp voltage programming, no-lock, shutdown, analog-dimming setting, and the clamp circuit are all designed with the same values as the UCC3976 half-bridge circuit.

A supply between 4 VDC and 8 VDC is required for this board to operate a 520-V cold-cathode fluorescent lamp (CCFL) from 2 mA to 6 mA.

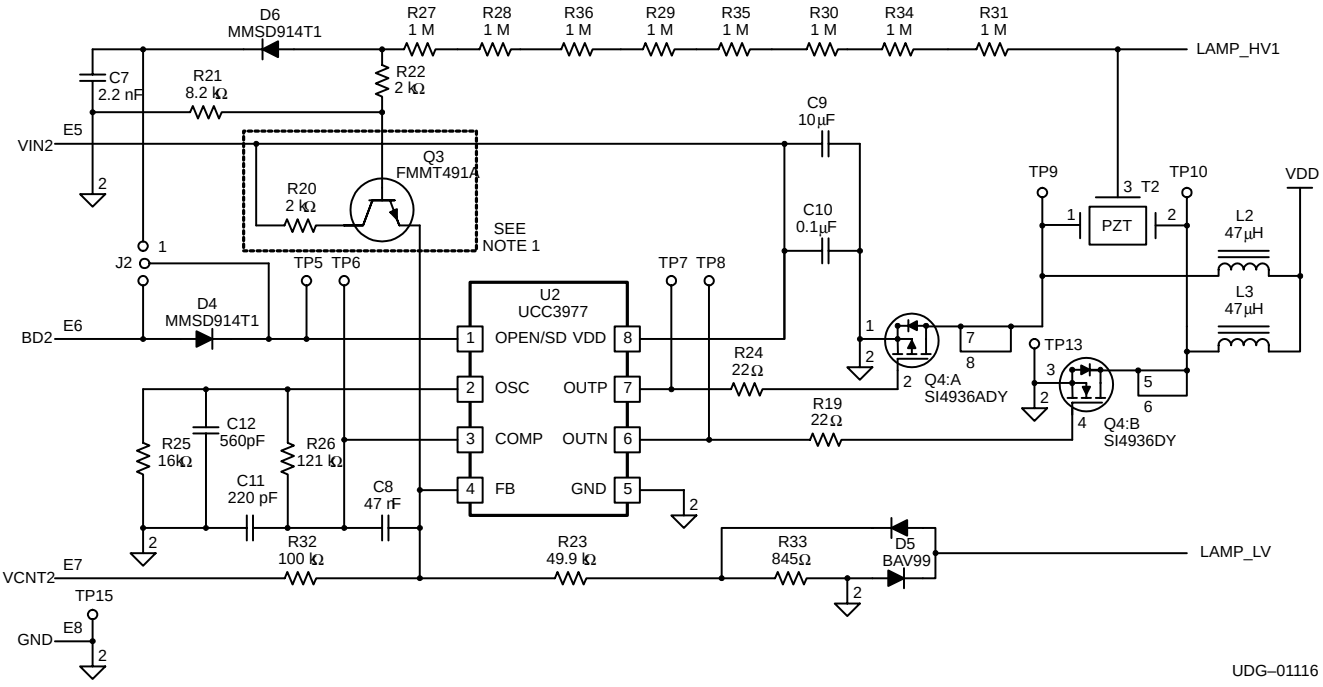

Figure 9. Evaluation Module Schematic for UCC3977

3.1 Push-Pull Inductor Selection

The push-pull topology requires a different approach for calculating the external inductor values. Referring to Figure 1, Q4A and Q4B are driven out of phase at 50% duty cycle. When Q4A is on, current is ramped up in L2 as shown in Figure 10. During the next switch cycle Q4B is turned on, Q4A is turned off, and the energy stored in L2 is transferred through the piezoelectric transformer (returning to ground through L3). L2 resonates with the piezoelectric primary capacitance forming a half sinusoid at Q4A's drain and across the transformer. In order to achieve zero-voltage switching, the drain voltage must return to ground before the next switching cycle. This dictates that the LC resonant frequency must be greater than the switching frequency.

$$L < \frac{1}{4 \times \pi^2 \times f^2 \times C_P} \quad (7)$$

In the EVM with a 55-kHz switching frequency and 105-nF piezoelectric transformer, L2 and L3 must be less than 80 µH for zero-voltage switching, so 47-µH inductors are used.

Figure 10 shows the normal operation waveforms, which were taken at V_{IN} = 4 V and I_{LAMP} = 5 mA.

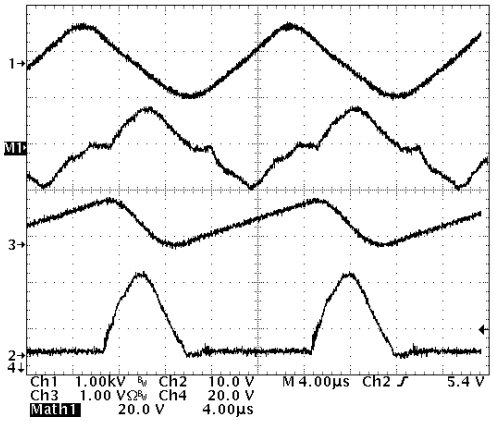

Figure 10. Push-Pull Operation Waveform
CH1: Lamp Voltage; M1: Primary Voltage; CH2: Voltage of P to GND; CH3: Current Through L1

3.2 System Efficiency

Efficiencies and operating frequencies using analog-dimming techniques are shown in Figure 11 and Figure 12 using a 520-V lamp. The maximum efficiency can be as high as 88%.

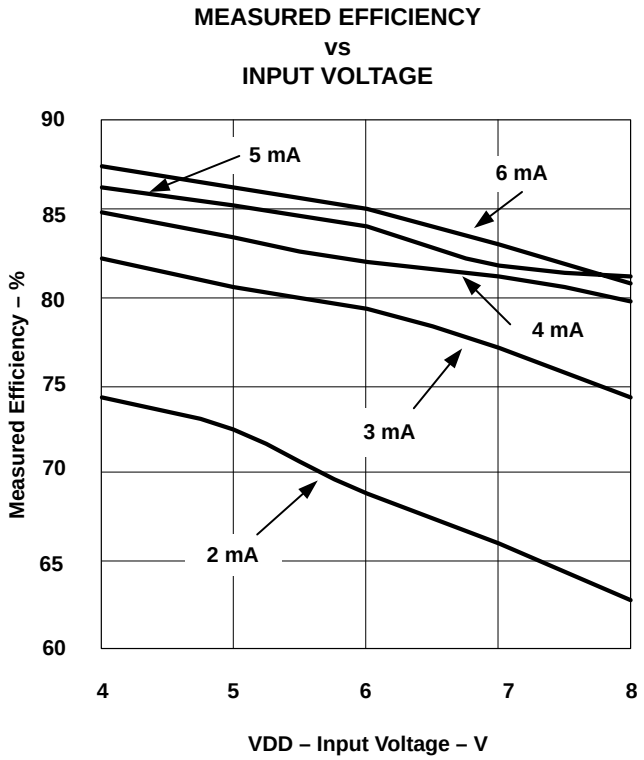

Figure 11

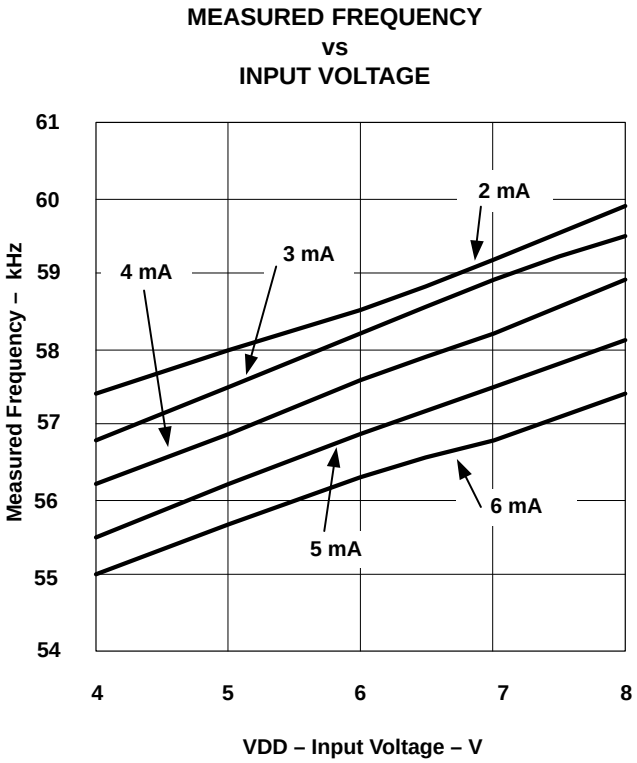

Figure 12

3.3 Evaluation Module Component Placement

Figure 13 shows the component placement for the EVM. Pin numbers and component polarities are also shown. The top part is for a half-bridge circuit with UCC3976 and the bottom one is for a push-pull circuit with UCC3977. Table 1 lists the parts values of the UCC3976/7 EVM as initially configured. These values can be modified to meet the application requirements.

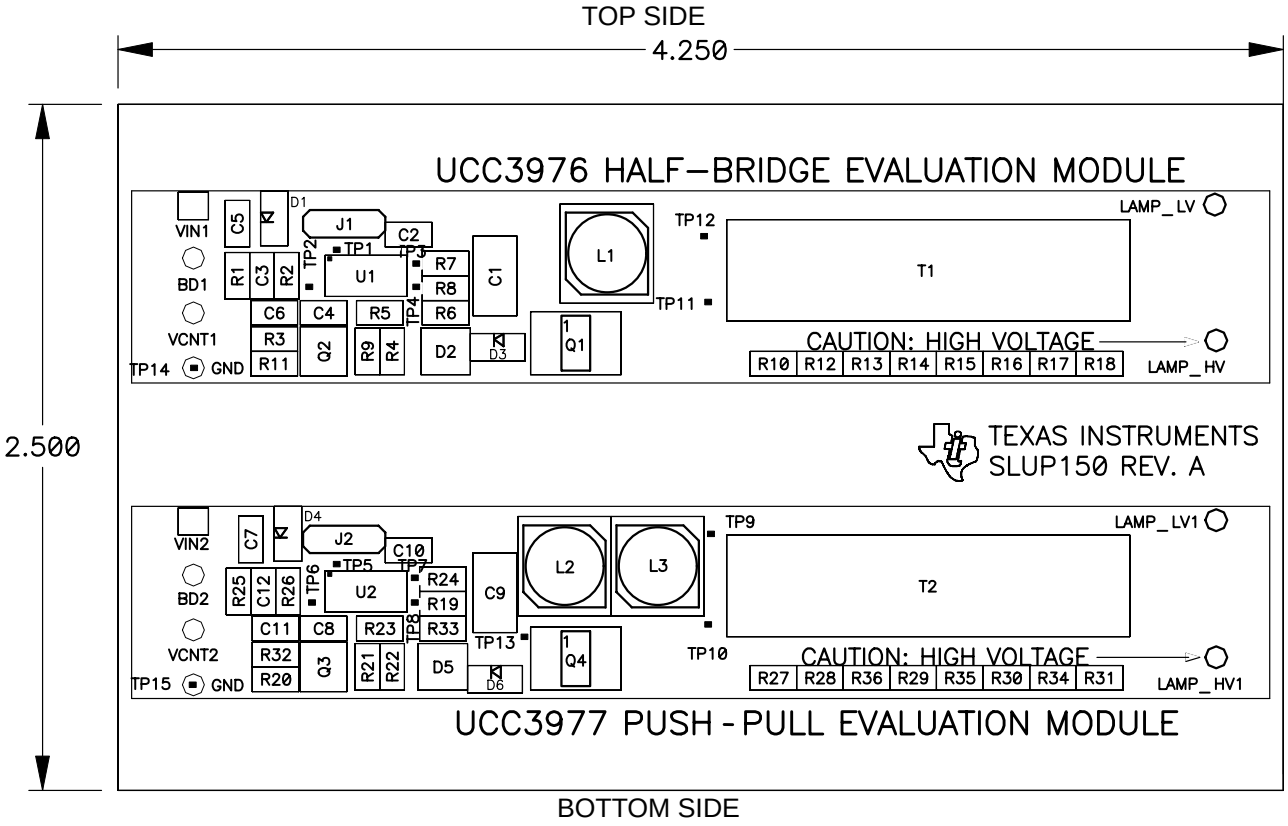

Figure 13. Parts Placement for the UCC3976/7 Dual Evaluation Module

Table 1. UCC3976/7 Evaluation Board List of Materials

	Reference	Qty	Description	Manufacturer	Part Number
Capacitor	C1, C9	2	Ceramic, X7R, 10 μF, 25 V, 20%, 1812	Taiyo Yuden	TMK432BJ106MM–T
	C2, C10	2	Ceramic, X7R, 0.1 μF, 16 V, 10%, 0805	Vishay	VJ0805Y104KXJAT
	C3, C12	2	Ceramic, NPO, 560 pF, 25 V, 5%, 0805	Vishay	VJ0805A561JXXAT
	C4, C8	2	Ceramic, X7R, 47 nF, 16 V, 10%, 0805	Vishay	VJ0805Y473KXJAT
	C5, C7	2	Ceramic, X7R, 2.2 nF, 16 V, 10%, 0805	Vishay	VJ0805Y222KXJAT
	C6, C11	2	Ceramic, X7R, 220 pF, 16 V, 10%, 0805	Vishay	VJ0805Y221KXJAT
Resistor	R1, R25	2	Metal film, 16 kΩ, 0.125 Ω, 1%, 0805	Vishay	CRCW08051602F
	R2, R26	2	Metal film, 121 kΩ, 0.125 Ω, 1%, 0805	Vishay	CRCW08051213F
	R3, R32	2	Metal film, 100 kΩ, 0.125 Ω, 1%, 0805	Vishay	CRCW08051003F
	R4, R22	2	Metal film, 2 kΩ, 0.125 Ω, 1%, 0805	Vishay	CRCW08052001F
	R5, R23	2	Metal film, 49.9 kΩ, 0.125 Ω, 1%, 0805	Vishay	CRCW08054992F
	R6, R33	2	Metal film, 845 Ω, 0.125 Ω, 1%, 0805	Vishay	CRCW08058450F
	R7, R8, R19, R24	4	Metal film, 22 Ω, 0.125 Ω, 1%, 0805	Vishay	CRCW080522R1F
	R9,R21	2	Metal film, 8.2 kΩ, 0.125 Ω, 1%, 0805	Vishay	CRCW08058201F
	R10, R12–R18, R27–R31, R34–R36	16	Metal film, 1 MΩ, 0.125 Ω, 1%, 0805	Vishay	CRCW08051004F
	R11, R20	0	Not used, 0805	Vishay	CRCW08052001F
Diode	D1, D3, D4, D6	4	Diode, 100 V, 0.2 A, SOD–123	Motorola	MMSD914T1
	D2, D5	2	Dual diode, 70 V, 0.15 A, SOT–23	Motorola	BAV99LT1
Inductor	L1 **	1	39 μH, D75C	Toko	646CY–390M
	L2, L3 **	2	47 μH, D75C	Toko	646CY–470M
MOSFET	Q1 **	1	Dual, (N/P channel), SO–8	Vishay	Si4542DY
	Q2, Q3	0	Not used, SOT–23	Zetex	FMMT491A
	Q4 **	1	Dual, (N/N channel), SO–8	Vishay	Si4936ADY
Transformer	T1, T2	2	Transformer, piezoelectric, 35 X 8.5 X 3.1 mm	Panasonic	EFTU14R0M02
IC	U1 **	1	Backlight controller, 8-Pin TSSOP	TI	UCC3976
	U2 **	1	Backlight controller, 8-Pin TSSOP	TI	UCC3977
PCB	—	1	FR4, .032, SMOBC, see fab	Any	SLUP150.R–A
Jumper	J1, J2	2	Header, 25mil	Sullins	PTC36SAAN
	Shorts Jumper	2	Shorts jumper, N/A	Sullins	STC02SYAN
Terminal	TP1, TP2, TP5, TP6, TP9, TP10, TP11, TP12	7	PCB black PK100, N/A	William Hughes	200–203

4 Appendix

4.1 Layout Consideration to Avoid Oscillations Due to Output Capacitance

There is a very small capacitance in a PZT output, (about 15 pF for a Panasonic PZT). For a CCFL system, there are many parasitic capacitances from the lamp to ground along the length of the lamp. These parasitic capacitances influence resonant operation and contribute to the output voltage. If the wires to the lamp are long and these parasitic capacitances are not constant, output voltage can jitter and an output voltage envelope appears, as shown in Figure 14 trace 1. Due to the nonlinear characteristics of CCFL, small lamp voltage changes result in large current changes, as shown in Figure 14 trace 2.

If these types of oscillations occur, the high voltage wire to the lamp should be shortened and the parasitic capacitance should be kept constant. Putting a shield around the lamp and letting the ground return wire run along the shield also helps.

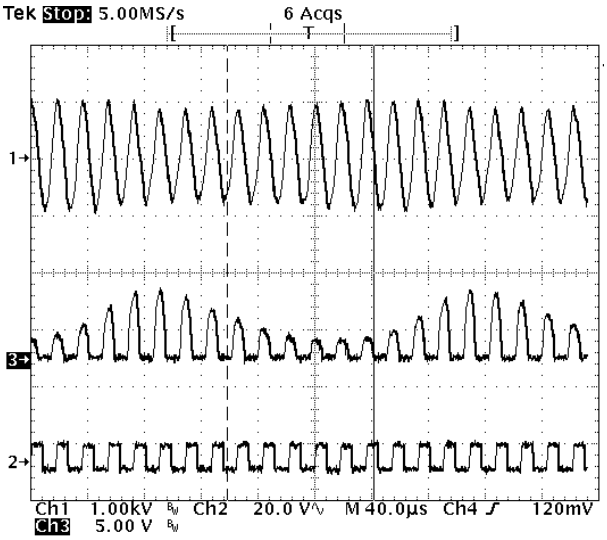

Figure 14. Envelope
CH1: Lamp Voltaage, CH2: Drive Signal, CH3: Lamp Current

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