

# FDS6064N3

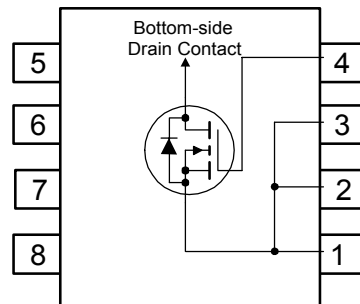
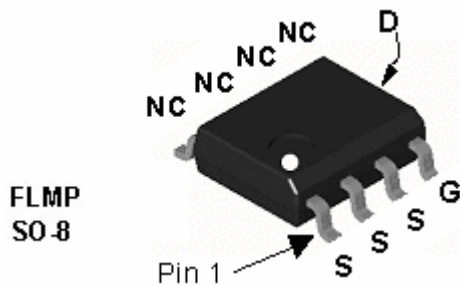
## 20V N-Channel PowerTrench® MOSFET

### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for "low side" synchronous rectifier operation, providing an extremely low  $R_{DS(ON)}$  in a small package.

### Applications

- Synchronous rectifier
- DC/DC converter
- FLMP SO-8 package: Enhanced thermal performance in industry-standard package size



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Rated	Units
V <sub>DSS</sub>	Drain-Source Voltage	20	V
V <sub>GSS</sub>	Gate-Source Voltage	± 8	
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	23	A
	– Pulsed	60	
P <sub>D</sub>	Power Dissipation (Note 1a)	3.0	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	–55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	0.5	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6064N3	FDS6064N3	13"	12mm	2500 units

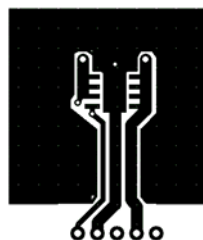
## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		11		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>On Characteristics (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.4	0.6	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 23\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 22\text{ A}$ $V_{GS} = 1.8\text{ V}, I_D = 18\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 23\text{ A}, T_J = 125^\circ\text{C}$		3.4 3.8 4.9 4.5	4 5 7 8	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 23\text{ A}$		179		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$		7191		pF
$C_{oss}$	Output Capacitance	$f = 1.0\text{ MHz}$		1403		pF
$C_{rss}$	Reverse Transfer Capacitance			703		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		1.2		$\Omega$
<b>Switching Characteristics (Note 2)</b>						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A}, V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		22	35	ns
$t_r$	Turn–On Rise Time			22	35	ns
$t_{d(off)}$	Turn–Off Delay Time			153	245	ns
$t_f$	Turn–Off Fall Time			77	123	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 23\text{ A}, V_{GS} = 4.5\text{ V}$		70	98	nC
$Q_{gs}$	Gate–Source Charge			10		nC
$Q_{gd}$	Gate–Drain Charge			15		nC
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				2.5	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.5\text{ A}$ (Note 2)		0.6	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 23\text{ A}, d_i/d_t = 100\text{ A}/\mu\text{s}$		43		nS
$Q_{rr}$	Diode Reverse Recovery Charge			55		nC

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 40°C/W when mounted on a 1in<sup>2</sup> pad of 2 oz copper



b) 85°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

Typical Characteristics

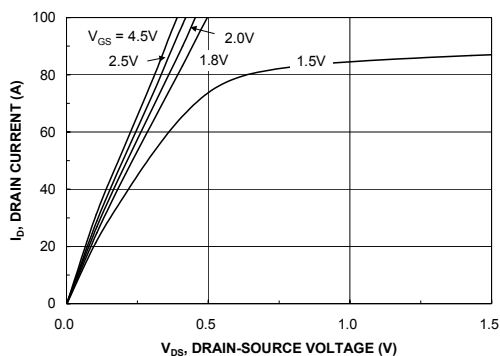


Figure 1. On-Region Characteristics.

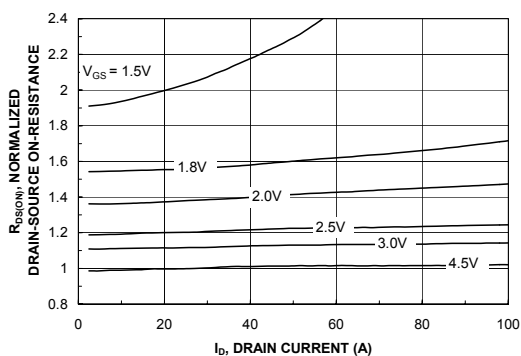


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

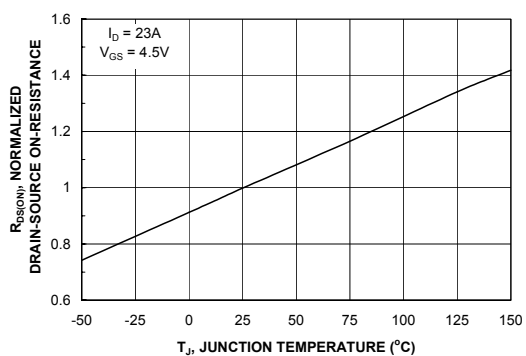


Figure 3. On-Resistance Variation with Temperature.

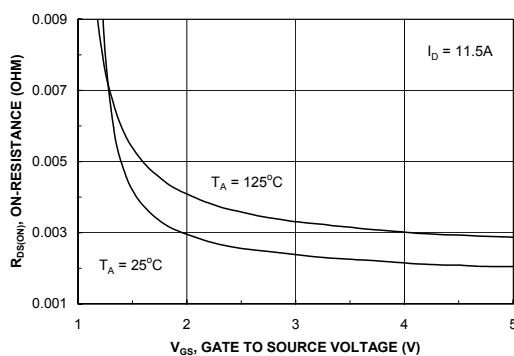


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

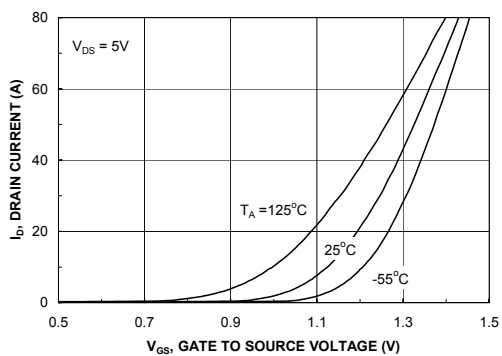


Figure 5. Transfer Characteristics.

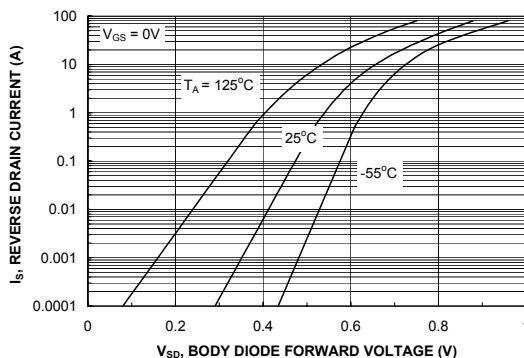
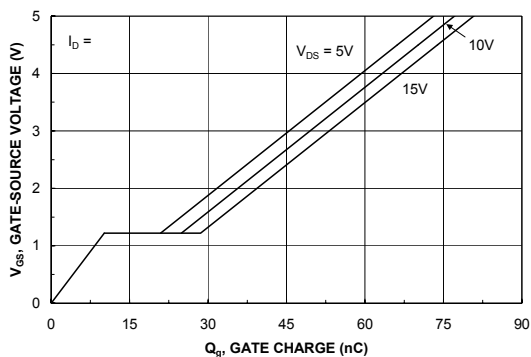
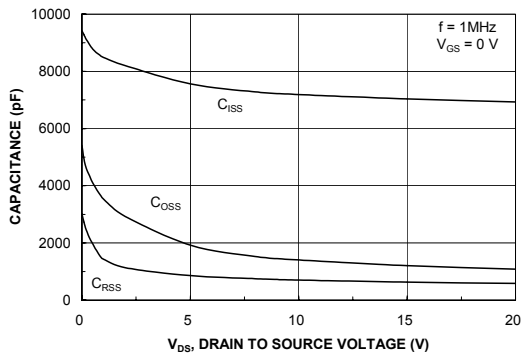


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

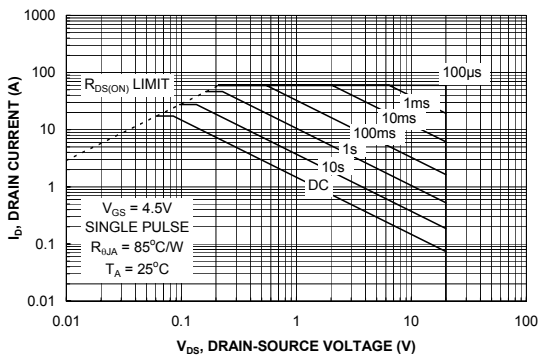
## Typical Characteristics



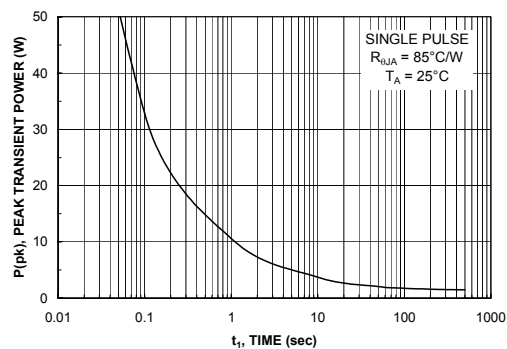
**Figure 7. Gate Charge Characteristics.**



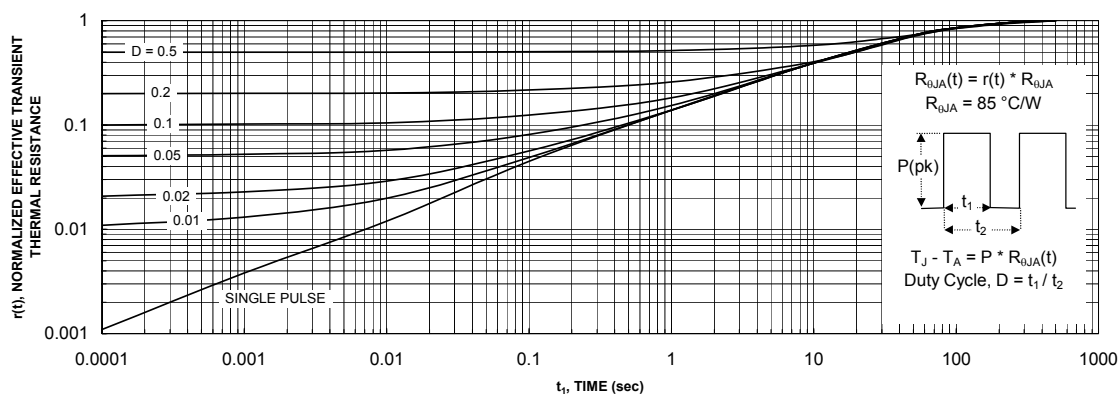
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



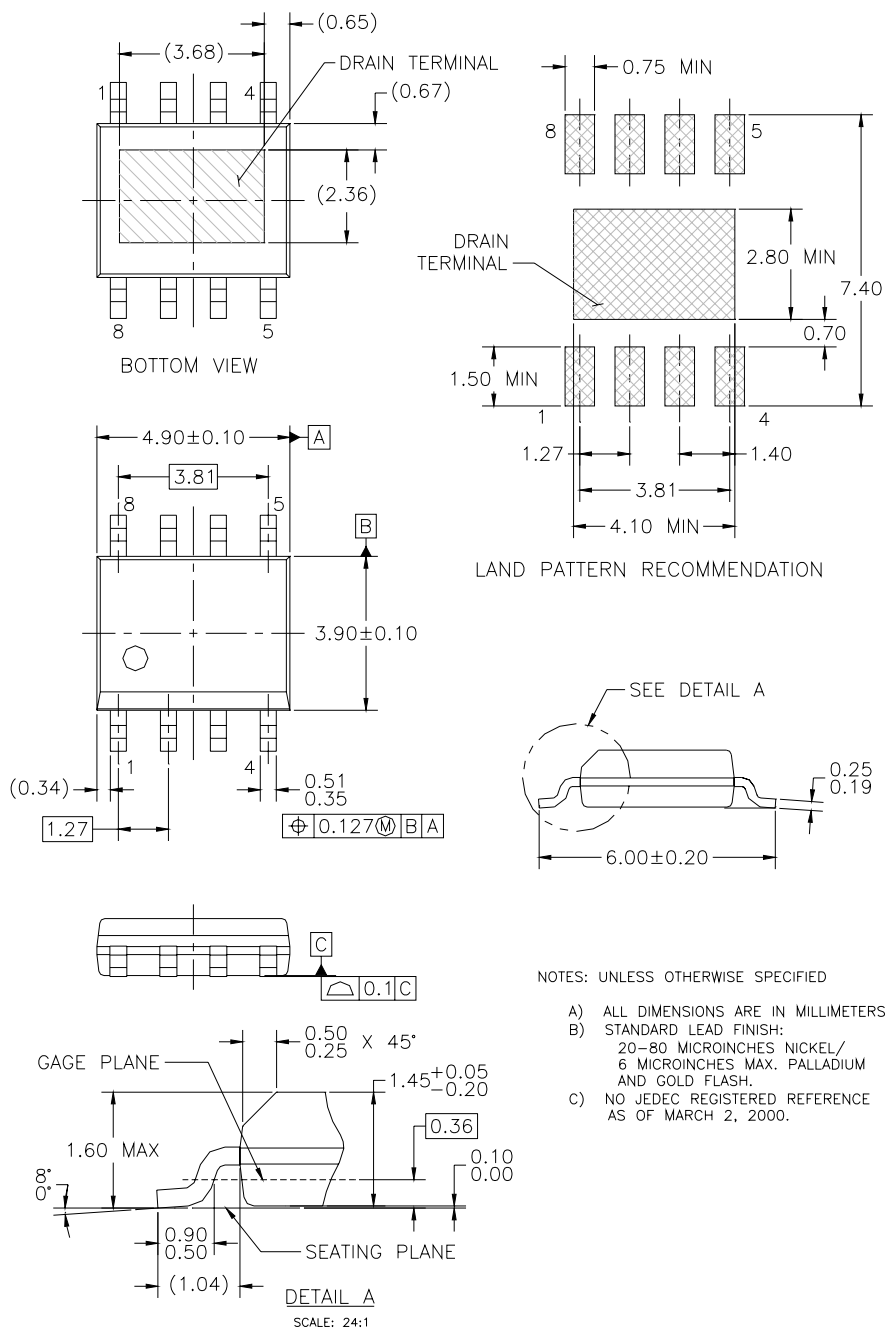
**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

### Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) STANDARD LEAD FINISH:  
20-80 MICROINCHES NICKEL/  
6 MICROINCHES MAX. PALLADIUM  
AND GOLD FLASH.
- C) NO JEDEC REGISTERED REFERENCE  
AS OF MARCH 2, 2000.

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