Wideband Distributed Amplifier
30 kHz - 50 GHz

Features

- Wide Frequency Range: 30 kHz - 50 GHz
- 14.5 dB Gain
- 3 - 8 V DC, 200 mA
- 20.5 dBm P1dB @ 21 GHz
- Integrated Power Detector with a Detector Reference Voltage Generator
- 50 Ω Input and Output Match
- Lead-Free 5 mm 12-Lead AQFN Package
- RoHS* Compliant

Applications

- Instrumentation and Communication Systems

Description

MAAM-011275 is an easy-to-use, wideband amplifier that operates from 30 kHz to 50 GHz. The amplifier provides 14.5 dB gain, 20.5 dBm output power and 4 dB noise figure. It is matched to 50 Ω with typical return loss better than 10 dB.

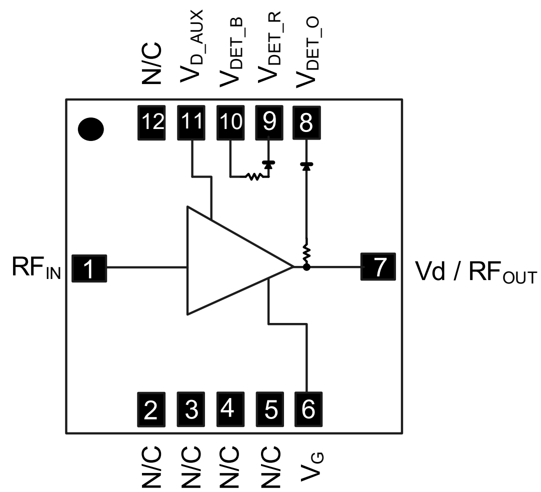
MAAM-011275 is suitable for a wide range of applications in instrumentation and communication systems.

Ordering Information[1,2]

Part Number	Package
MAAM-011275-TR0500	500 Piece Reel
MAAM-011275-SB1	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

Functional Schematic



Pin Configuration[3,4]

Pin #	Pin Name	Description
1	RF_{IN}	RF Input
2,3,4,5,12	N/C	Not Connected
6	V_{G1}	Gate Voltage 1
7	RF_{OUT}/V_{DD}	RF Output
8	DET_{OUT}	Output Detector
9	DET_{REF}	Reference Detector
10	DET_{BIAS}	Detector Bias
11	V_{DAUX}	Auxiliary Drain Voltage

3. MACOM recommends connecting unused package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: T_C = 25 °C, V_{DD} = 7 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	5 GHz 20 GHz 45 GHz	dB	13 13 11	15 15 14	—
Gain Flatness	1 - 50 GHz	dB	—	±1	—
Input Return Loss	1 - 50 GHz	dB	—	10	—
Output Return Loss	1 - 50 GHz	dB	—	10	—
P1dB	21 GHz	dBm	—	20.5	—
P3dB	5 GHz 20 GHz 45 GHz	dB	23 22 17	24.5 23.5 19	—
Output IP3	P_{IN} = -4 dBm / tone, 21 GHz tone spacing = 2 MHz	dBm	—	29	—
Noise Figure	26 GHz 40 GHz	dB	—	3.2 6.5	—
Drain Current[5]	Quiescent bias	mA	—	200	—

5. Set by adjusting VG1 as outlined in operating conditions on page 3.

Absolute Maximum Ratings[6,7]

Parameter	Absolute Maximum
Input Power	17 dBm
Drain Supply Voltage	10 V
V_{G1}	-4 V < V_{G1} < 0 V
V_{G2}	-3.5 V < V_{G2} < +4 V
Drain Supply Current	340 mA
Junction Temperature[8,9]	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Operating at nominal conditions with $T_J \leq$ +150°C will ensure MTTF > 1 x 10^6 hours.
9. Junction Temperature (T_J) = $T_A + \Theta_{JC}$ * ((V * I) - (P_{OUT} - P_{IN}))
Typical thermal resistance (Θ_{JC}) = 15.6 °C/W.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

Operating Conditions

The recommended biasing conditions are V_{DD} = 7 V and I_{DSQ} = 200 mA, with I_{DSQ} set by adjusting V_{G1} after correctly setting V_{DD} (refer to turn on sequence). To maintain the best performance MACOM recommends using an active bias circuit for constant I_{DD}.

It is noted that any biasing arrangement used, including active biasing, must be able to source at least 10 mA into the V_{G1} port. This is because the V_{G1} port contains a resistive divider with a total resistance to ground of 244 Ω. For the recommended I_{DSQ} of 200 mA obtained at a V_{G1} voltage of around 2.5 V, 10 mA of V_{G1} current (I_{G1}) is expected. These values of V_{G1} and I_{G1} will vary slightly between devices.

For biasing V_{DD}, apply V_{DD} through a bias tee connected to the RF_{OUT}/V_{DD} port and connect an external DC block to the RF_{IN} port. This provides wide band performance of 40 MHz to 50 GHz (depending on the bandwidth of the bias tee).

2 bypass capacitors of 100 pF and 1 µF should be connected to V_{DAUX}. This provides for improved gain flatness below 2 GHz down to 30 kHz when required.

The 100 pF capacitor can be a single layer capacitor or an SMT device on the PCB. Although it should be positioned as closely to the device as practically possible, the frequency response is not particularly sensitive to this. The 1 µF capacitor can be placed further away on the PCB.

Data in this datasheet was measured using 100 pF (C1) and 1 µF (C3) capacitors on V_{DAUX}.

Operating the MAAM-011275

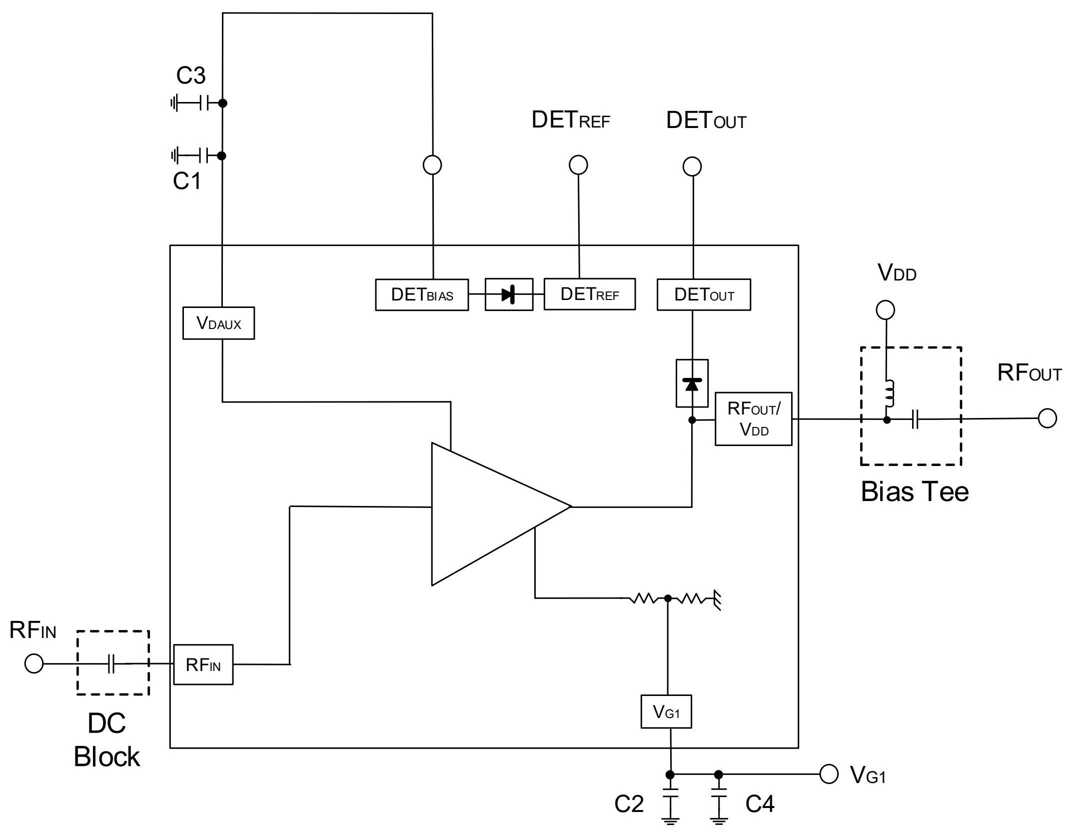
Turn-on

1. Apply V_{G1} (-4 V).
2. Increase V_{DD} to +7 V.
3. Set I_{DSQ} by adjusting V_{G1} more positive. (typically -2.5 V for I_{DSQ} = 200 mA).
4. Apply RF_{IN} signal.

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_{G1} to -4 V.
3. Decrease V_{DD} to 0 V.

Application Schematic

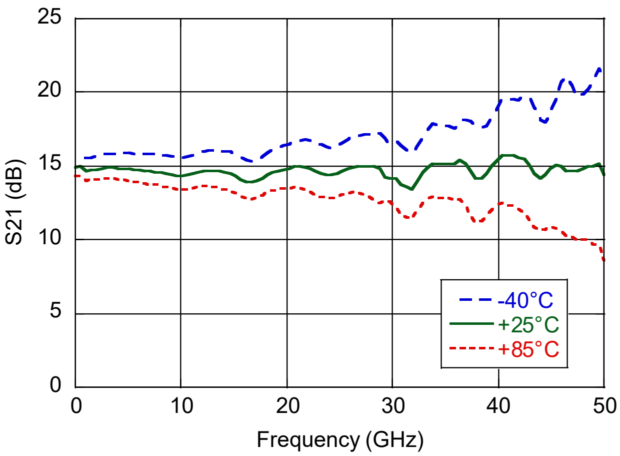


Component List

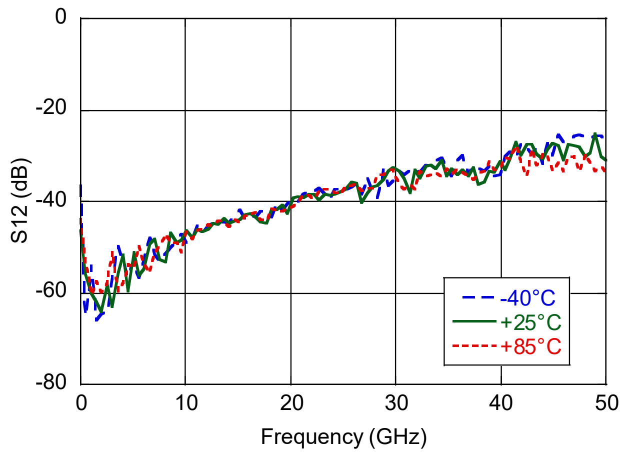
Part	Value	Size
C1, C2	0.01 µF	0402
C3, C4	1 µF	0603

Typical Performance Curves: V_{DD} = 7 V, I_{DSQ} = 200 mA

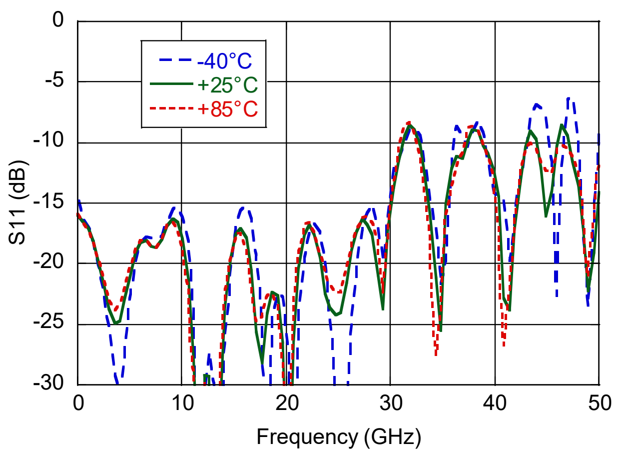
Gain



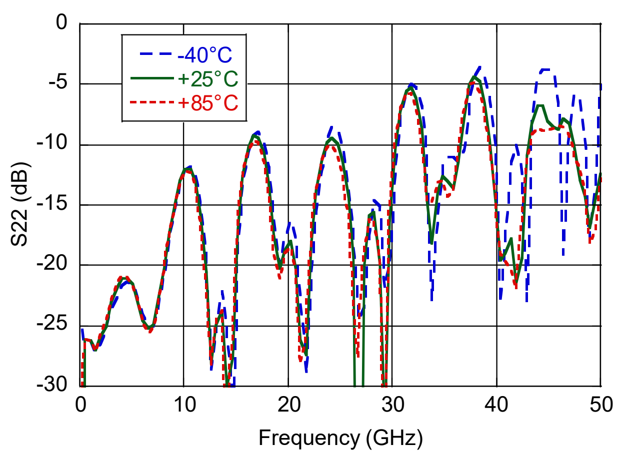
Reverse Isolation



Input Return Loss

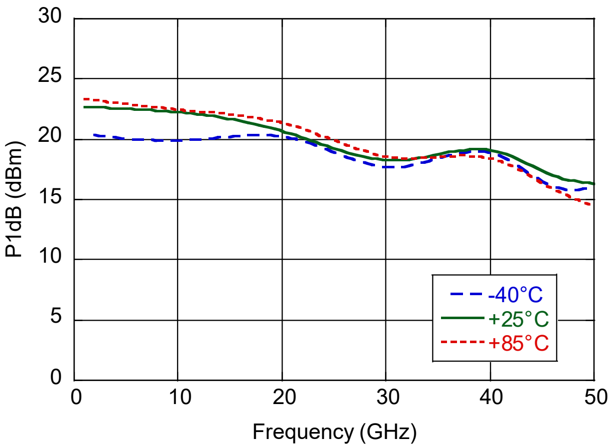


Output Return Loss

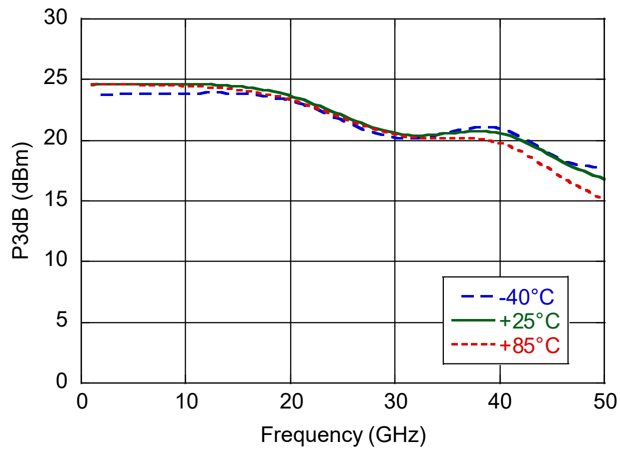


Typical Performance Curves: V_{DD} = 7 V, I_{DSQ} = 200 mA

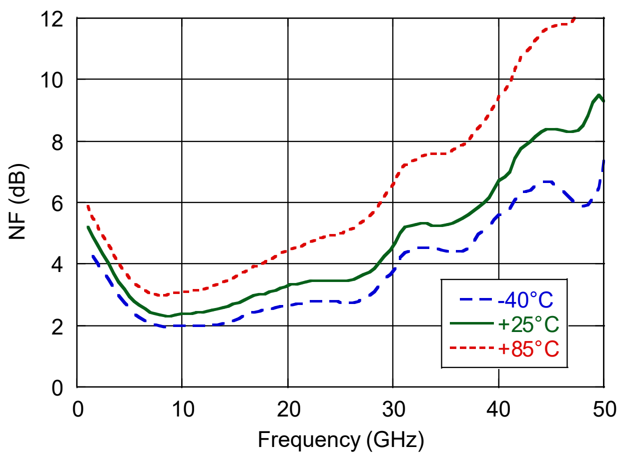
Output P1dB



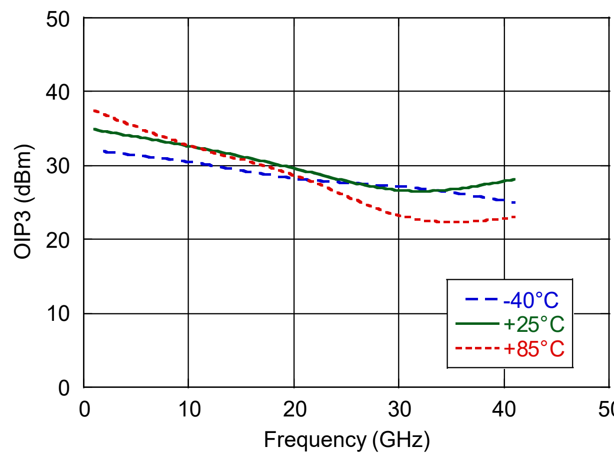
Output P3dB



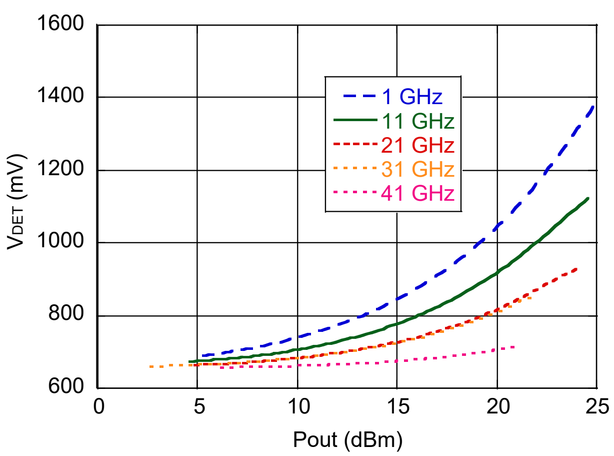
Noise Figure



OIP3 @ Pin = -4 dBm

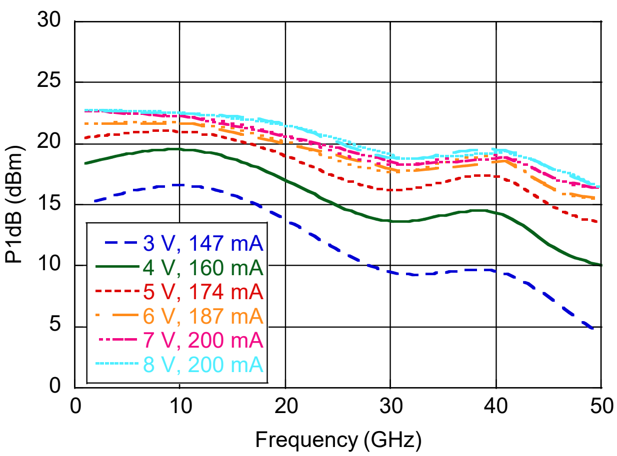


Detector Voltage @ +25°C

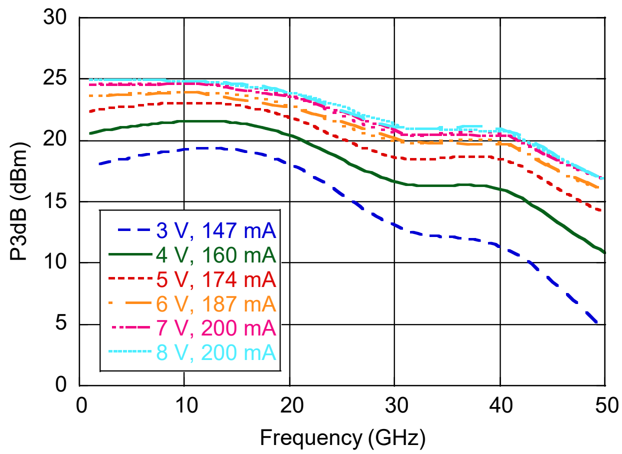


Typical Performance Curves: T_A = +25°C

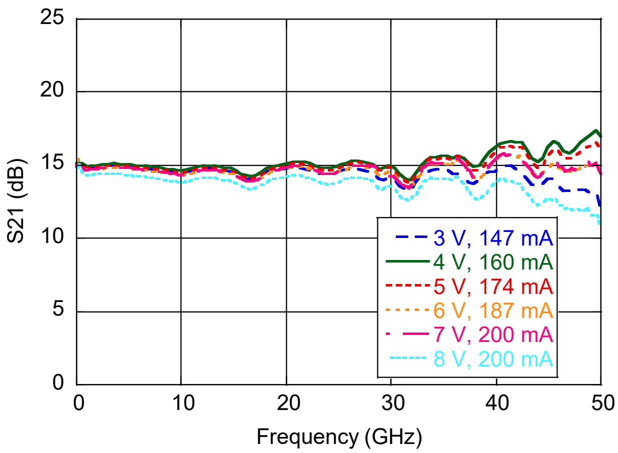
Output P1dB vs. V_{DD}



P3dB vs. V_{DD}

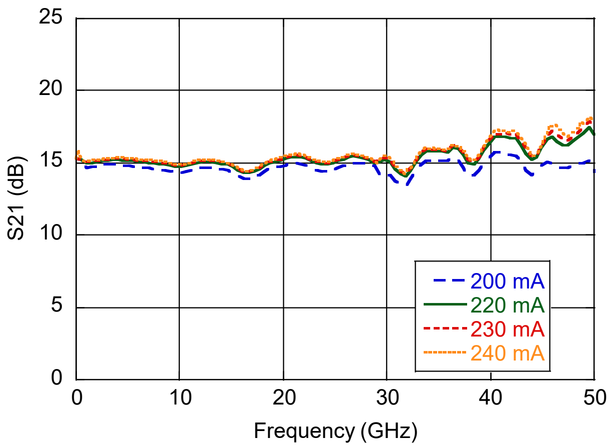


Gain vs. V_{DD}

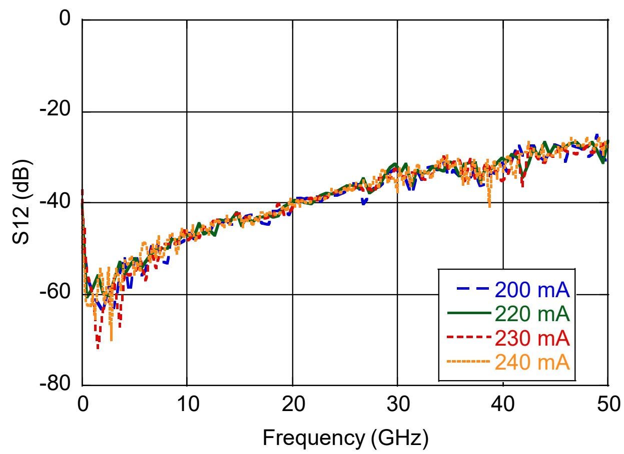


Typical Performance Curves: V_{DD} = 7 V, T_A = +25°C

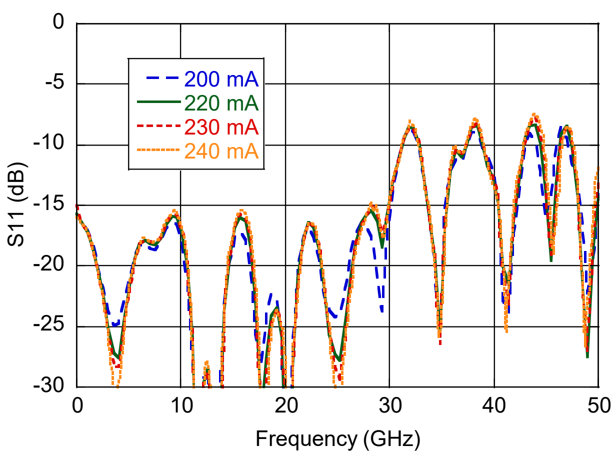
Gain vs. I_{DD}



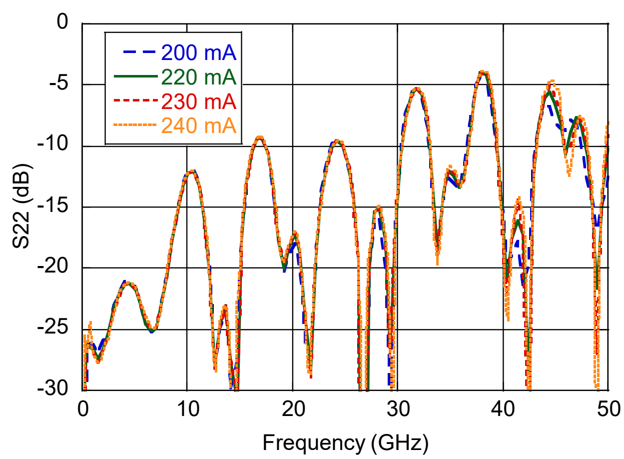
Reverse Isolation vs. I_{DD}



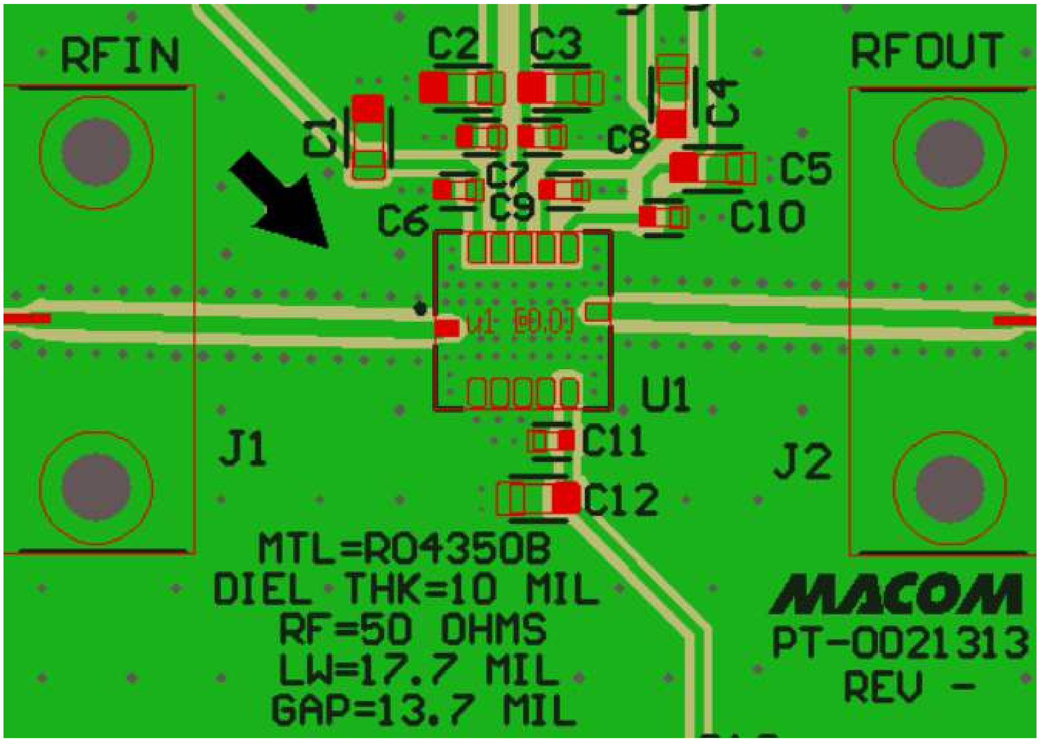
Input Return Loss vs. I_{DD}



Output Return Loss vs. I_{DD}



Recommended PCB Layout



Evaluation Board Parts List

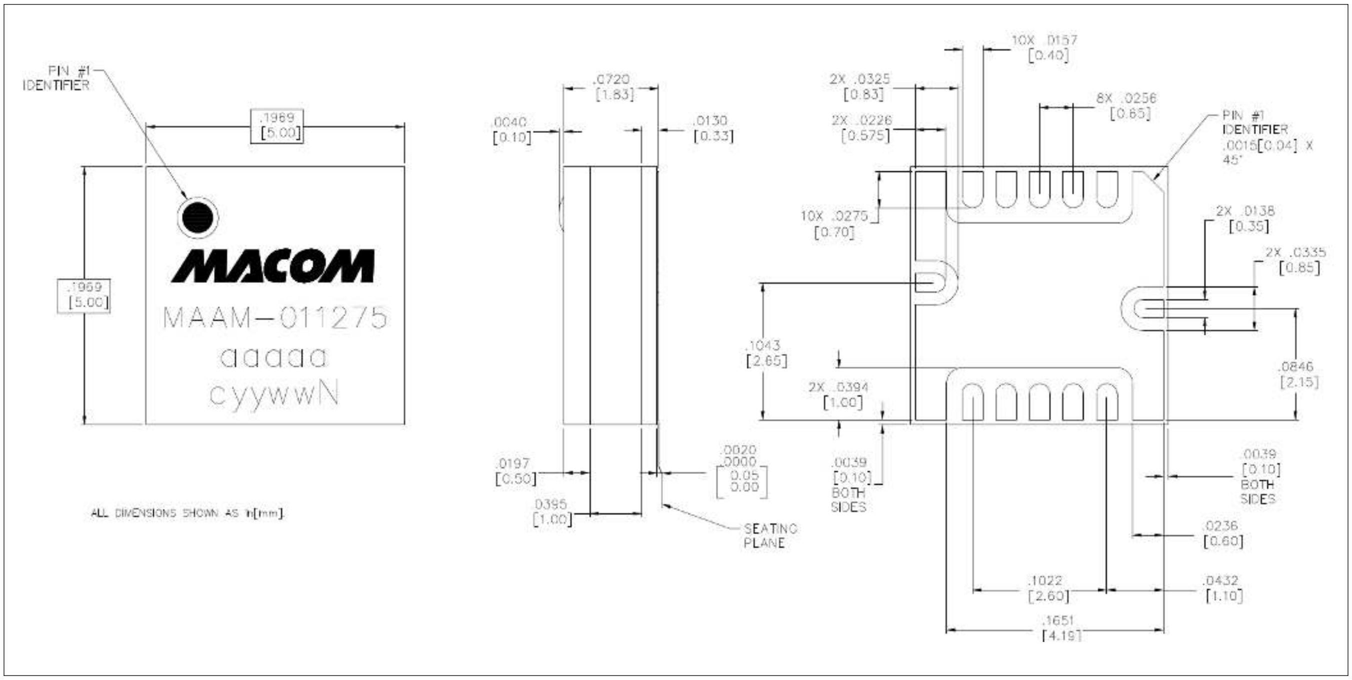
Part	Value	Case Style
C2, C12	1 µF	0603
C7, C11	0.01 µF	0402

Evaluation PCB Specifications[10,11]

Top Layer: 1 oz Copper Cladding
Dielectric Layer: Rogers RO4350B 10 mil
Bottom Layer: 1 oz Copper Cladding
Finished overall thickness: *12.8* mil

10. PCB finish is ENEPIG. The vias located under the device are 8 mil in diameter and filled with thermally conductive material, capped over and planarized
11. Evaluation board should be mounted on a heat sink.

Lead-Free 5 mm 12-Lead AQFN [12 - 16]



12. All units in in(mm), unless otherwise noted, with a tolerance of .xxxx = ±.0005 in and .xxx = ±.005 in.
13. Lead finish: NiPdAu plating
14. Marking: line 2 part number; line 3 wafer lot number; line 4 c = country of origin (T = Thailand), yyww = date code, N = Nickel/Palladium/ Gold plating
15. Reference Application Note S2083 for lead-free solder reflow recommendations.
16. Meets JEDEC moisture sensitivity level 3 requirements.