

MF1444-04

# **S1D15711 Series**

## NOTICE

---

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

©SEIKO EPSON CORPORATION 2003, All rights reserved.

All other product names mentioned herein are trademarks and/or registered trademarks of their respective companies.

# Contents

1. DESCRIPTION .....	1
2. FEATURES .....	1
3. BLOCK DIAGRAM .....	2
4. PIN ASSIGNMENT .....	3
5. PIN DESCRIPTION .....	7
6. FUNCTION DESCRIPTION .....	11
7. COMMAND DESCRIPTION .....	27
8. ABSOLUTE MAXIMUM RATINGS .....	40
9. DC CHARACTERISTICS .....	41
10. TIMING CHARACTERISTICS .....	46
11. MICROPROCESSOR (MPU) INTERFACE: REFERENCE .....	53
12. CONNECTION BETWEEN LCD DRIVERS: REFERENCE .....	54
13. LCD PANEL WIRING: REFERENCE .....	55
14. CAUTIONS .....	56

## 1. DESCRIPTION

The S1D15711 Series is a single-chip dot matrix liquid crystal display driver that can be connected directly to a microprocessor bus. Eight-bit parallel or serial display data transmitted from the microprocessor is stored in the internal display data RAM, and the chip generates liquid crystal drive signals, independently of the microprocessor.

It has a on-chip  $9 \times 200$ -bits display data RAM, and there is a one-to-one correspondence between the dot pixel on the liquid crystal panel pixels and internal RAM bit. This feature ensures implementation of highly free display.

The S1D15711 Series incorporate 9 common and 200 segment driver circuits. A single chip can drive a  $9 \times 200$  dots display. Further, display capacity can be extended by designing two chips in a master/slave configuration.

The S1D15711 Series can read and write RAM data with the minimum current consumption because it does not require any external operation clock. Also it incorporates a LCD power supply featuring a very low current consumption, a LCD drive power voltage regulator resistor and a display clock CR oscillator circuit. This allows the display system of a high-performance for handy equipment to be realized at the minimum power consumption and minimum component configuration.

## 2. FEATURES

- Direct display of RAM data using the display data RAM  
RAM bit data "1" .... goes on.  
"0" .... goes off (at display normal rotation).
- RAM capacity  
 $9 \times 200 = 1,800$  bits
- Liquid crystal drive circuits

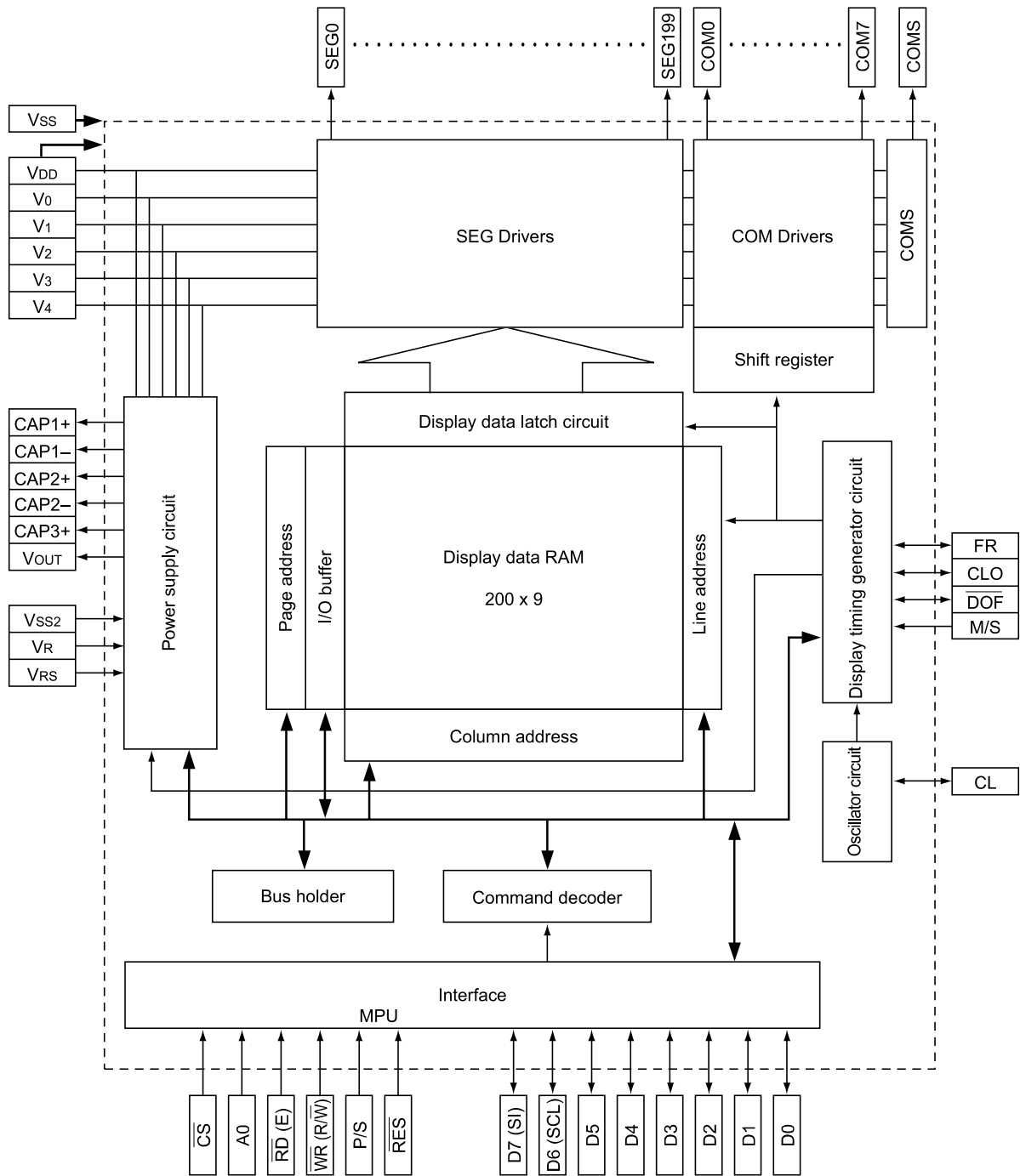
9 common outputs and 200 segment outputs

- High-speed 8-bit MPU interface (Both the 80 and 68 series MPUs can directly be connected.)/serial interface enabled
- Abundant command functions  
Display Data Read/Write, Display ON/OFF, Display Normal Rotation/Reversal, Page Address Set, Display Start Line Set, column address set, Power Supply Save Display All Lighting ON/OFF, LCD Bias Set, Read Modify Write, Segment Driver Direction Select, Electronic Control, V<sub>0</sub> Voltage Adjusting Built-in Resistance Ratio Set, Static Indicator, n Line Alternating Current Reversal Drive, and Common Output State Selection
- Built-in power supply circuit for low power supply liquid crystal drive  
Booster circuit (Boosting magnification - double, triple, quadruple, boosting reference power supply external input enabled)
- High accuracy alternating current voltage adjusting circuit (Temperature gradient:  $-0.05\%/^{\circ}\text{C}$ )  
Built-in V<sub>0</sub> voltage adjusting resistor, built-in V<sub>1</sub> to V<sub>4</sub> voltage generation split resistors, built-in electronic control function, and voltage follower
- Built-in CR oscillator circuit (external clock input enabled)
- Power supplies  
Logic power supply:  $V_{DD} - V_{SS} = 1.8$  to  $5.5$  V  
Boosting reference power supply:  $V_{DD} - V_{SS} = 1.8$  to  $5.0$  V  
Liquid crystal drive power supply:  $V_0 - V_{DD} = 4.5$  to  $9.0$  V
- Wide operating temperature range  $-40$  to  $+85^{\circ}\text{C}$
- CMOS process
- Shipping form: Bare chip
- No light-resistant and radiation-resistant design are provided.

### Series specification

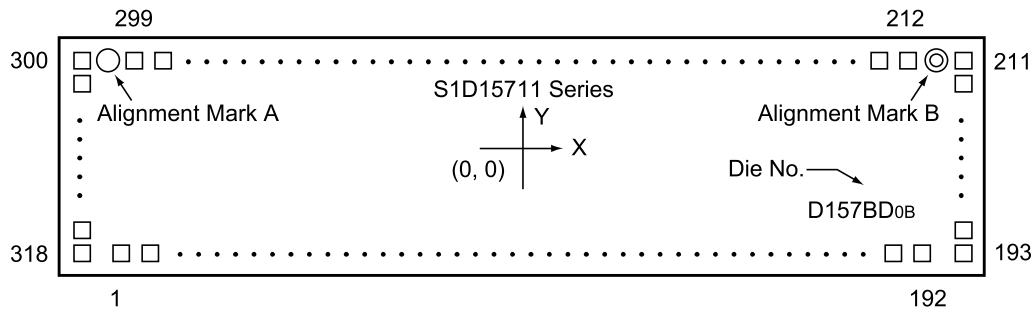
Product name	Duty	Bias	SEG Dr	COM Dr	VREG temperature gradient	Shipping form	Bump height
S1D15711D00B000	1/9	1/5, 1/6	200	9	$-0.1\%/^{\circ}\text{C}$	Bare chip	17.0 $\mu\text{m}$ Typ.
S1D15711D00C000	1/9	1/5, 1/6	200	9	$-0.1\%/^{\circ}\text{C}$	Bare chip	22.5 $\mu\text{m}$ Typ.

### 3. BLOCK DIAGRAM



### 4. PAD ASSIGNMENT

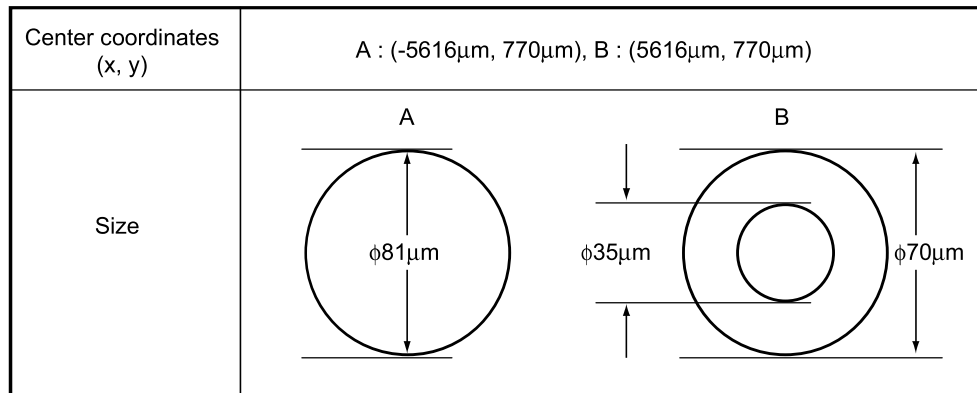
#### Chip Specification



#### Chip Outline, Bump

Item	Size		Unit
	X	Y	
Chip size	11.92	× 1.85	mm
Chip thickness	0.625		mm
Bump pitch	60 (Min.)		μm
Bump size	PAD No.1	85 × 74	μm
	PAD No.2 to 189	41 × 85	μm
	PAD No.190	85 × 74	μm
	PAD No.191 to 210	85 × 45	μm
	PAD No.211	85 × 74	μm
	PAD No.212 to 299	85 × 85	μm
	PAD No.300	85 × 74	μm
	PAD No.301 to 318	85 × 45	μm
Bump height	17 (Typ.) or 22.5 (Typ.)		μm

#### Alignment Marks



## Pad Central Coordinates

Unit:  $\mu\text{m}$ 

Pad No.	Pin Name	X	Y	Pad No.	Pin Name	X	Y	Pad No.	Pin Name	X	Y
1	NC	-5807	-776	51	SEG46	-2726	-770	101	SEG96	266	-770
2	NC	-5658	-770	52	SEG47	-2666		102	SEG97	326	
3	NC	-5598		53	SEG48	-2606		103	SEG98	386	
4	NC	-5539		54	SEG49	-2547		104	SEG99	445	
5	SEG0	-5479		55	SEG50	-2487		105	SEG100	505	
6	SEG1	-5419		56	SEG51	-2427		106	SEG101	565	
7	SEG2	-5359		57	SEG52	-2367		107	SEG102	625	
8	SEG3	-5299		58	SEG53	-2307		108	SEG103	685	
9	SEG4	-5239		59	SEG54	-2247		109	SEG104	745	
10	SEG5	-5180		60	SEG55	-2188		110	SEG105	804	
11	SEG6	-5120		61	SEG56	-2128		111	SEG106	864	
12	SEG7	-5060		62	SEG57	-2068		112	SEG107	924	
13	SEG8	-5000		63	SEG58	-2008		113	SEG108	984	
14	SEG9	-4940		64	SEG59	-1948		114	SEG109	1044	
15	SEG10	-4880		65	SEG60	-1888		115	SEG110	1104	
16	SEG11	-4821		66	SEG61	-1829		116	SEG111	1163	
17	SEG12	-4761		67	SEG62	-1769		117	SEG112	1223	
18	SEG13	-4701		68	SEG63	-1709		118	SEG113	1283	
19	SEG14	-4641		69	SEG64	-1649		119	SEG114	1343	
20	SEG15	-4581		70	SEG65	-1589		120	SEG115	1403	
21	SEG16	-4521		71	SEG66	-1529		121	SEG116	1463	
22	SEG17	-4461		72	SEG67	-1469		122	SEG117	1523	
23	SEG18	-4402		73	SEG68	-1410		123	SEG118	1582	
24	SEG19	-4342		74	SEG69	-1350		124	SEG119	1642	
25	SEG20	-4282		75	SEG70	-1290		125	SEG120	1702	
26	SEG21	-4222		76	SEG71	-1230		126	SEG121	1762	
27	SEG22	-4162		77	SEG72	-1170		127	SEG122	1822	
28	SEG23	-4102		78	SEG73	-1110		128	SEG123	1882	
29	SEG24	-4043		79	SEG74	-1051		129	SEG124	1941	
30	SEG25	-3983		80	SEG75	-991		130	SEG125	2001	
31	SEG26	-3923		81	SEG76	-931		131	SEG126	2061	
32	SEG27	-3863		82	SEG77	-871		132	SEG127	2121	
33	SEG28	-3803		83	SEG78	-811		133	SEG128	2181	
34	SEG29	-3743		84	SEG79	-751		134	SEG129	2241	
35	SEG30	-3684		85	SEG80	-692		135	SEG130	2300	
36	SEG31	-3624		86	SEG81	-632		136	SEG131	2360	
37	SEG32	-3564		87	SEG82	-572		137	SEG132	2420	
38	SEG33	-3504		88	SEG83	-512		138	SEG133	2480	
39	SEG34	-3444		89	SEG84	-452		139	SEG134	2540	
40	SEG35	-3384		90	SEG85	-392		140	SEG135	2600	
41	SEG36	-3325		91	SEG86	-333		141	SEG136	2659	
42	SEG37	-3265		92	SEG87	-273		142	SEG137	2719	
43	SEG38	-3205		93	SEG88	-213		143	SEG138	2779	
44	SEG39	-3145		94	SEG89	-153		144	SEG139	2839	
45	SEG40	-3085		95	SEG90	-93		145	SEG140	2899	
46	SEG41	-3025		96	SEG91	-33		146	SEG141	2959	
47	SEG42	-2965		97	SEG92	27		147	SEG142	3019	
48	SEG43	-2906		98	SEG93	86		148	SEG143	3078	
49	SEG44	-2846		99	SEG94	146		149	SEG144	3138	
50	SEG45	-2786	▼	100	SEG95	206	▼	150	SEG145	3198	▼

Unit:  $\mu\text{m}$ 

Pad No.	Pin Name	X	Y	Pad No.	Pin Name	X	Y	Pad No.	Pin Name	X	Y
151	SEG146	3258	-770	201	SEG191	5807	-40	251	VDD	704	770
152	SEG147	3318		202	SEG192		40	252	P/S	583	
153	SEG148	3378		203	SEG193		120	253	C86	463	
154	SEG149	3437		204	SEG194		200	254	Vss	342	
155	SEG150	3497		205	SEG195		280	255	Vss	221	
156	SEG151	3557		206	SEG196		360	256	M/S	100	
157	SEG152	3617		207	SEG197		440	257	VDD	-20	
158	SEG153	3677		208	SEG198		520	258	VDD	-141	
159	SEG154	3737		209	SEG199		601	259	TEST4	-318	
160	SEG155	3796		210	NC		681	260	TEST5	-495	
161	SEG156	3856		211	NC	▼	776	261	TEST6	-671	
162	SEG157	3916		212	NC	5411	770	262	Vss	-792	
163	SEG158	3976		213	NC	5291		263	Vss	-913	
164	SEG159	4036		214	NC	5170		264	Vss	-1033	
165	SEG160	4096		215	NC	5049		265	TEST7	-1210	
166	SEG161	4155		216	TEST0	4928		266	TEST8	-1387	
167	SEG162	4215		217	TEST1	4808		267	TEST9	-1564	
168	SEG163	4275		218	Vss	4687		268	TEST10	-1741	
169	SEG164	4335		219	Vss	4566		269	VOUT	-1861	
170	SEG165	4395		220	TEST2	4446		270	VOUT	-1982	
171	SEG166	4455		221	TEST3	4325		271	Vss	-2103	
172	SEG167	4515		222	FR	4204		272	Vss	-2223	
173	SEG168	4574		223	CLO	4084		273	VR	-2344	
174	SEG169	4634		224	DOF	3963		274	V0	-2465	
175	SEG170	4694		225	RES	3842		275	V1	-2586	
176	SEG171	4754		226	CS	3721		276	V2	-2706	
177	SEG172	4814		227	Vss	3601		277	V3	-2827	
178	SEG173	4874		228	Vss	3480		278	V4	-2948	
179	SEG174	4933		229	CL	3359		279	VDD	-3068	
180	SEG175	4993		230	WR, R/W	3239		280	VDD	-3189	
181	SEG176	5053		231	RD, E	3118		281	VDD2	-3310	
182	SEG177	5113		232	VDD	2997		282	VDD2	-3430	
183	SEG178	5173		233	VDD	2877		283	VOUT	-3551	
184	SEG179	5233		234	A0	2756		284	VOUT	-3672	
185	SEG180	5292		235	D7	2635		285	CAP2+	-3793	
186	SEG181	5352		236	D6	2514		286	CAP2+	-3913	
187	SEG182	5412		237	D5	2394		287	CAP2-	-4034	
188	SEG183	5472		238	D4	2273		288	CAP2-	-4155	
189	NC	5532	▼	239	D3	2152		289	CAP1+	-4275	
190	NC	5807	-770	240	D2	2032		290	CAP1+	-4396	
191	NC	5592	-770	241	D1	1911		291	CAP1-	-4517	
192	NC	5651	-776	242	D0	1790		292	CAP1-	-4637	
193	NC	5807	-681	243	D7	1670		293	CAP3+	-4758	
194	SEG184		-601	244	VDD	1549		294	CAP3+	-4879	
195	SEG185		-520	245	VDD	1428		295	VOUT	-5000	
196	SEG186		-440	246	VDD2	1307		296	VOUT	-5120	
197	SEG187		-360	247	VDD2	1187		297	NC	-5241	
198	SEG188		-280	248	VDD2	1066		298	NC	-5362	
199	SEG189		-200	249	VDD2	945		299	NC	-5482	▼
200	SEG190	▼	-120	250	VDD	825	▼	300	NC	-5807	776





## 5. PIN DESCRIPTION

### Power Supply Pin

Pin name	I/O	Description	Number of pins												
VDD	Power supply	Commonly used with the MPU power supply pin Vcc.	10												
VSS	Power supply	0 V pin connected to the system ground (GND)	11												
VDD2	Power supply	Boosting circuit reference power supply for liquid crystal drive	6												
V0, V1, V2 V3, V4	Power supply	<p>Multi-level power supply for liquid crystal drive. The voltage specified according to liquid crystal cells is impedance-converted by a split resistor or operation amplifier (OP amp) and applied. The potential needs to be specified based on VSS to establish the relationship of dimensions shown below:</p> $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ <p>Master operation When the power supply is ON, the following voltages are applied to V1 to V4 from the built-in power supply circuit. The selection of the voltages is determined using the LCD bias set command.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tbody> <tr> <td>V1</td> <td><math>4/5 \cdot V_0</math></td> <td><math>5/6 \cdot V_0</math></td> </tr> <tr> <td>V2</td> <td><math>3/5 \cdot V_0</math></td> <td><math>4/6 \cdot V_0</math></td> </tr> <tr> <td>V3</td> <td><math>2/5 \cdot V_0</math></td> <td><math>2/6 \cdot V_0</math></td> </tr> <tr> <td>V4</td> <td><math>1/5 \cdot V_0</math></td> <td><math>1/6 \cdot V_0</math></td> </tr> </tbody> </table>	V1	$4/5 \cdot V_0$	$5/6 \cdot V_0$	V2	$3/5 \cdot V_0$	$4/6 \cdot V_0$	V3	$2/5 \cdot V_0$	$2/6 \cdot V_0$	V4	$1/5 \cdot V_0$	$1/6 \cdot V_0$	1 each
V1	$4/5 \cdot V_0$	$5/6 \cdot V_0$													
V2	$3/5 \cdot V_0$	$4/6 \cdot V_0$													
V3	$2/5 \cdot V_0$	$2/6 \cdot V_0$													
V4	$1/5 \cdot V_0$	$1/6 \cdot V_0$													

### LCD Power Supply Circuit Pin

Pin name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP1– pin.	2
CAP1–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.	2
CAP2+	O	Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP2– pin.	2
CAP2–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP2+ pin.	2
CAP3+	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1– pin.	2
VOUT	I/O	Boosting output pin. Connects a capacitor between the pin and VDD2.	6
VR	I	<p>Voltage adjusting pin. Applies voltage between V0 and VSS using a split resistor.</p> <p>Valid only when the V0 voltage adjusting internal resistor is not used V0 resistance ratio set command (D2, D1, D0) = (1, 1, 1) To use a resistor for adjusting the V0 voltage, open the circuit.</p>	1

**System Bus Connecting Pins**

Pin name	I/O	Description	Number of pins															
D7 to D0 (SI) (SCL)	I/O	An 8-bit bidirectional data bus is used to connect an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S=LOW), D7: Serial data entry pin (SI) D6: Serial clock input pin (SCL) In this case, D0 to D5 are set to high impedance. When Chip Select is in the non-active state, D0 to D7 are set to high impedance.	9															
A0	I	Normally the lowest order bit of the MPU address bus is connected to discriminate data / commands. A0=HIGH: Indicates that D0 to D7 are display data. A0=LOW: Indicates that D0 to D7 are control data.	1															
RES	I	Initialized by setting $\overline{\text{RES}}$ to LOW. $\overline{\text{RES}}$ signal level. Reset operation is performed at the $\overline{\text{RES}}$ signal level.	1															
CS	I	Chip Select signal. When $\overline{\text{CS}}$ =LOW, this signal becomes active and the input/output of data/commands is enabled.	1															
$\overline{\text{RD}}$ (E)	I	<ul style="list-style-type: none"> <li>When the 80 series MPU is connected, active LOW is set. Pin that connects the <math>\overline{\text{RD}}</math> signal of the 80 series MPU. When this signal is LOW, the S1D15711 Series data bus is set in the output state.</li> <li>When the 68 series MPU is connected, active HIGH is set. 68 series MPU enable clock input pin</li> </ul>	1															
$\overline{\text{WR}}$ (R/W)	I	<ul style="list-style-type: none"> <li>When the 80 series MPU is connected, active LOW is set. Pin that connects the <math>\overline{\text{WR}}</math> signal of the 80 series MPU. The data bus signal is latched on the leading edge of the <math>\overline{\text{WR}}</math> signal.</li> <li>When the 68 series MPU is connected, Read/write control signal input pin R/W=HIGH: Read operation R/W=LOW: Write operation</li> </ul>	1															
C86	I	MPU interface switching pin C86=HIGH: 68 series MPU interface C86=LOW: 80 series MPU interface	1															
P/S	I	Switching pin for parallel data entry/serial data entry P/S=HIGH: Parallel data entry P/S=LOW: Serial data entry According to the P/S state, the following table is given. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>P/S</th> <th>Data/command</th> <th>Data</th> <th>Read/write</th> <th>Serial clock</th> </tr> </thead> <tbody> <tr> <td>HIGH</td> <td>A0</td> <td>D0 to D7</td> <td><math>\overline{\text{RD}}</math>, <math>\overline{\text{WR}}</math></td> <td></td> </tr> <tr> <td>LOW</td> <td>A0</td> <td>SI (D7)</td> <td>Write-only</td> <td>SCL (D6)</td> </tr> </tbody> </table> <p>When P/S=LOW, D0 to D5 are set to high impedance. D0 to D5 can be HIGH, LOW, or "OPEN". <math>\overline{\text{RD}}</math>(E) and <math>\overline{\text{WR}}</math> (R/W) are fixed to HIGH or LOW. For the serial data entry, RAM display data cannot be read.</p>	P/S	Data/command	Data	Read/write	Serial clock	HIGH	A0	D0 to D7	$\overline{\text{RD}}$ , $\overline{\text{WR}}$		LOW	A0	SI (D7)	Write-only	SCL (D6)	1
P/S	Data/command	Data	Read/write	Serial clock														
HIGH	A0	D0 to D7	$\overline{\text{RD}}$ , $\overline{\text{WR}}$															
LOW	A0	SI (D7)	Write-only	SCL (D6)														

Pin name	I/O	Description	Number of pins																												
CL	I	Pin that selects the validity/invalidity of the built-in oscillator circuit for display clocks. CL=HIGH: Built-in oscillator circuit valid The display clock can also be input from outside the CL Pin. To stop the external clock, fix the CL Pin to LOW. When the S1D15711 Series is used for the master/slave configuration, fix the slave side to LOW.	1																												
M/S	I	Pin that selects the master/slave operation for the S1D15711 Series. The liquid crystal display system is synchronized by outputting the timing signal required for the liquid crystal display for the master operation and inputting the timing signal required for the liquid crystal display for the slave operation. M/S=HIGH: Master operation M/S=LOW: Slave operation According to the M/S and CL states, the following table is given. <table border="1" data-bbox="483 724 1252 888"> <thead> <tr> <th>M/S</th> <th>CL</th> <th>Oscillator circuit</th> <th>Power supply circuit</th> <th>CLO</th> <th>FRS</th> <th>DOF</th> </tr> </thead> <tbody> <tr> <td>HIGH</td> <td>HIGH</td> <td>Valid</td> <td>Valid</td> <td>Output</td> <td>Output</td> <td>Output</td> </tr> <tr> <td></td> <td>LOW</td> <td>Invalid</td> <td>Valid</td> <td>Output</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>LOW</td> <td>LOW</td> <td>Invalid</td> <td>Invalid</td> <td>Input</td> <td>Input</td> <td>Input</td> </tr> </tbody> </table>	M/S	CL	Oscillator circuit	Power supply circuit	CLO	FRS	DOF	HIGH	HIGH	Valid	Valid	Output	Output	Output		LOW	Invalid	Valid	Output	Output	Output	LOW	LOW	Invalid	Invalid	Input	Input	Input	1
M/S	CL	Oscillator circuit	Power supply circuit	CLO	FRS	DOF																									
HIGH	HIGH	Valid	Valid	Output	Output	Output																									
	LOW	Invalid	Valid	Output	Output	Output																									
LOW	LOW	Invalid	Invalid	Input	Input	Input																									
CLO	I/O	Display clock I/O pin According to the M/S and CLS states, the following table is given. When the S1D15711 Series is used for the master/slave configuration, each CLO pin is connected. <table border="1" data-bbox="483 1041 751 1171"> <thead> <tr> <th>M/S</th> <th>CLS</th> <th>CL</th> </tr> </thead> <tbody> <tr> <td>HIGH</td> <td>HIGH</td> <td>Output</td> </tr> <tr> <td></td> <td>LOW</td> <td>Output</td> </tr> <tr> <td>LOW</td> <td>LOW</td> <td>Input</td> </tr> </tbody> </table>	M/S	CLS	CL	HIGH	HIGH	Output		LOW	Output	LOW	LOW	Input	1																
M/S	CLS	CL																													
HIGH	HIGH	Output																													
	LOW	Output																													
LOW	LOW	Input																													
FR	I/O	Liquid crystal alternating current signal I/O pin M/S=HIGH: Output M/S=LOW: Input When the S1D15711 Series is used for the master/slave configuration, each FR pin is connected.	1																												
DOF	I/O	Liquid crystal display blanking control pin M/S=HIGH: Output M/S=LOW: Input When the S1D15711 Series is used for the master/slave configuration, each DOF pin is connected.	1																												

**Liquid Crystal Drive Pin**

Pin name	I/O	Description	Number of pins																										
SEG0 to SEG199	O	Output pins for the LCD segment drive. Contents of the display RAM and FR signal are combined to select a desired level among V <sub>0</sub> , V <sub>2</sub> , V <sub>3</sub> and V <sub>SS</sub> . <table border="1" style="margin-left: 20px;"> <thead> <tr> <th rowspan="2">RAM data</th> <th rowspan="2">FR</th> <th colspan="2">Output voltage</th> </tr> <tr> <th>Display normal operation</th> <th>Display reversal</th> </tr> </thead> <tbody> <tr> <td>HIGH</td> <td>HIGH</td> <td>V<sub>0</sub></td> <td>V<sub>2</sub></td> </tr> <tr> <td>HIGH</td> <td>LOW</td> <td>V<sub>SS</sub></td> <td>V<sub>3</sub></td> </tr> <tr> <td>LOW</td> <td>HIGH</td> <td>V<sub>2</sub></td> <td>V<sub>0</sub></td> </tr> <tr> <td>LOW</td> <td>LOW</td> <td>V<sub>3</sub></td> <td>V<sub>SS</sub></td> </tr> <tr> <td>Power save</td> <td>—</td> <td>V<sub>SS</sub></td> <td></td> </tr> </tbody> </table>	RAM data	FR	Output voltage		Display normal operation	Display reversal	HIGH	HIGH	V <sub>0</sub>	V <sub>2</sub>	HIGH	LOW	V <sub>SS</sub>	V <sub>3</sub>	LOW	HIGH	V <sub>2</sub>	V <sub>0</sub>	LOW	LOW	V <sub>3</sub>	V <sub>SS</sub>	Power save	—	V <sub>SS</sub>		200
RAM data	FR	Output voltage																											
		Display normal operation	Display reversal																										
HIGH	HIGH	V <sub>0</sub>	V <sub>2</sub>																										
HIGH	LOW	V <sub>SS</sub>	V <sub>3</sub>																										
LOW	HIGH	V <sub>2</sub>	V <sub>0</sub>																										
LOW	LOW	V <sub>3</sub>	V <sub>SS</sub>																										
Power save	—	V <sub>SS</sub>																											
COM0 to COM7	O	Output pins for the LCD common drive. Scan data and FR signal are combined to select a desired level among V <sub>0</sub> , V <sub>1</sub> , V <sub>4</sub> and V <sub>SS</sub> . <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Scanning data</th> <th>FR</th> <th>Output voltage</th> </tr> </thead> <tbody> <tr> <td>HIGH</td> <td>HIGH</td> <td>V<sub>SS</sub></td> </tr> <tr> <td>HIGH</td> <td>LOW</td> <td>V<sub>0</sub></td> </tr> <tr> <td>LOW</td> <td>HIGH</td> <td>V<sub>1</sub></td> </tr> <tr> <td>LOW</td> <td>LOW</td> <td>V<sub>4</sub></td> </tr> <tr> <td>Power save</td> <td>—</td> <td>V<sub>DD</sub></td> </tr> </tbody> </table>	Scanning data	FR	Output voltage	HIGH	HIGH	V <sub>SS</sub>	HIGH	LOW	V <sub>0</sub>	LOW	HIGH	V <sub>1</sub>	LOW	LOW	V <sub>4</sub>	Power save	—	V <sub>DD</sub>	8								
Scanning data	FR	Output voltage																											
HIGH	HIGH	V <sub>SS</sub>																											
HIGH	LOW	V <sub>0</sub>																											
LOW	HIGH	V <sub>1</sub>																											
LOW	LOW	V <sub>4</sub>																											
Power save	—	V <sub>DD</sub>																											
COMS	O	Indicator dedicated COM output pin Set to OPEN when not used When COMS is used for the master/slave configuration, the same signal is output to both the master and slave.	2																										

**Test Pin**

Pin name	I/O	Description	Number of pins
TEST 1 to TEST 10	I	Pins for testing IC chips. Use care to keep these pins free from loads like capacity and set them to OPEN.	11

Total : 291 pins

## 6. FUNCTION DESCRIPTION

### MPU Interface

#### Selection of interface type

The S1D15711 Series transfers data through 8-bit bidirectional data buses (D7 to D0) or serial data input (SI). By setting the polarity of the P/S pin to either HIGH or LOW, the 8-bit parallel data entry or serial data entry can be selected as listed in Table 1.

Table 1

P/S	$\overline{\text{CS}}$	A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	C86	D7	D6	D5 to D0
HIGH: Parallel data entry	$\overline{\text{CS}}$	A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	C86	D7	D6	D5 to D0
LOW: Serial data entry	$\overline{\text{CS}}$	A0	—	—	—	SI	SCL	(HZ)

Fix — to HIGH or LOW . HZ indicates the high impedance state.

#### Parallel interface

When the parallel interface is selected (P/S=HIGH), the S1D15711 Series can directly be connected to the MPU bus of either the 80 or 68 series MPU by setting the C86 pin to HIGH or LOW as listed in Table 2.

Table 2

C86	$\overline{\text{CS}}$	A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D7 to D0
HIGH: 68 series MPU bus	$\overline{\text{CS}}$	A0	E	$\overline{\text{R/W}}$	D7 to D0
LOW: 80 series MPU bus	$\overline{\text{CS}}$	A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D7 to D0

In addition, the data bus signal can be identified according to the combinations of the A0,  $\overline{\text{RD}}$  (E),  $\overline{\text{WR}}$  ( $\overline{\text{R/W}}$ ) signals as listed in Table 3.

Table 3

Common	68 series	80 series		Function
		$\overline{\text{RD}}$	$\overline{\text{WR}}$	
A0	R/W			
1	1	0	1	Display data read
1	0	1	0	Display data write
0	0	1	0	Control data write (command)

**Serial interface**

When the serial interface is selected (P/S=LOW), the serial data entry (SI) and serial clock input(SCL) can be accepted with the chip in the non-active state ( $\overline{CS}$ =LOW). The serial interface consists of an 8-bit shift register and a 3-bit counter. Serial data is fetched from the serial data entry pin in the order of D7, D6, ..., and D0 on the leading edge of the serial clock and converted into 8-bit

parallel data on the leading edge of the 8th serial clock, then processed.

Whether to identify that the serial data entry is display data or command is judged by the A0 input, and A0=HIGH indicates display data and A0=LOW indicates the command. After the chip is set to the non-active state, the A0 input is read and identified at the timing on the  $8 \times n$ -th leading edge of the serial clock. Fig. 1 shows the signal chart of the serial interface.

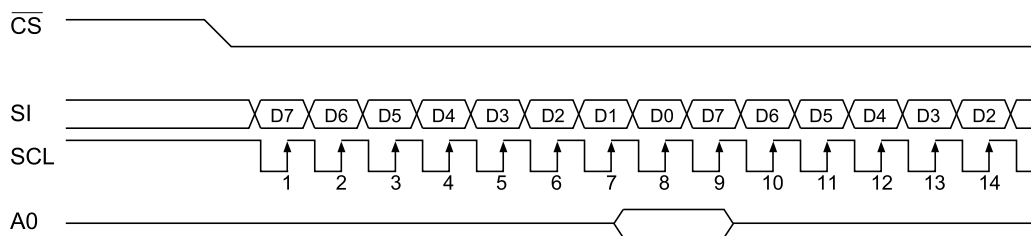


Fig. 1

- When the chip is in the non-active state, both the shift register and counter are reset to the initial state.
- Cannot be read for the serial interface.
- For the SCL signal, pay careful attention to the terminating reflection of lines and external noise. The operation confirmation using actual equipment is recommended.

**Chip select**

The S1D15711 Series has a chip select pins  $\overline{CS}$  and enables the MPU interface or serial interface only when  $\overline{CS}$ =LOW.

When Chip Select is in the non-active state, D0 to D7 are in the high impedance state and the A0,  $\overline{RD}$ , and  $\overline{WR}$  inputs become invalid. When the serial interface is selected, the shift register and counter are reset.

**Display data RAM and internal register access**

Since the S1D15711 Series access viewed from the MUP side satisfies the cycle time and does not require the wait time, high-speed data transfer is enabled.

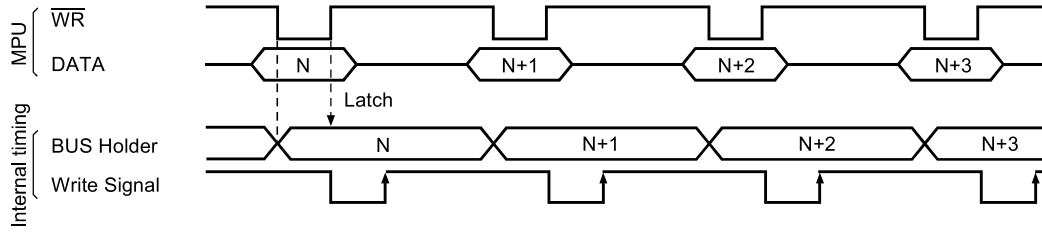
The S1D15711 Series performs a kind of inter-LSI pipeline processing through the bus holder attached to the internal data bus when it performs the data transfer with the MPU.

For example, when data is written on the display data RAM, the data is first held in the bus holder and written

on the display data RAM up to the next data write cycle. Further, when the MPU reads the contents of display data RAM, the read data at the first data read cycle (dummy) is held in the bus holder and read on the system bus from the bus holder up to the next data read cycle. The read sequence of the display data RAM is restricted. When the address is set, note that the specified address data is not output to the subsequent read instruction and output at the second data read. Therefore single dummy read is required after the address set and write cycle. Fig. 2 shows this relationship.

**Function description**

- Write



- Read

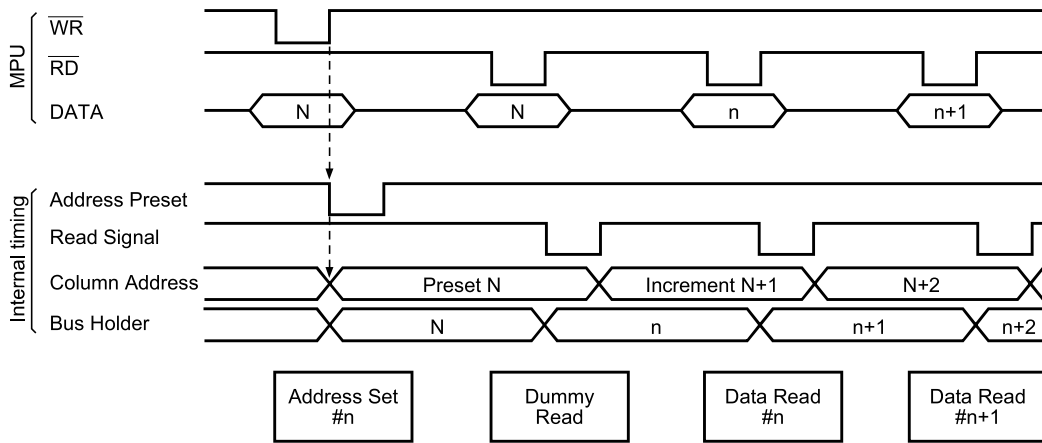


Fig. 2





**Column address circuit**

As shown in Fig. 5, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented by +1 at every input of display data read/write command. This allows the MPU to access the display data continuously.

After the last column address C7H is accessed, the column address returns to 00H. Since the page address is not automatically incremented, for example, the page address and the column address needs to be re-specified respectively to shift from the column C7H of page 0 to the column 00H of page 1.

Furthermore, as shown in Table 4, the AD command (segment driver direction select command) can be used to reverse the correspondence between the display data RAM column address and segment output. This allows constraints on IC layout to be minimized at the time of LCD module assembling.

Table 4

SEG output	SEG0	SEG199
ADC "0"	0 (H)→ Column Address→ C7 (H)	
(D0) "1"	C7 (H)← Column Address ← 0 (H)	

**Line address circuit**

When displaying contents of the display data RAM, the line address circuit is used for specifying the corresponding addresses. See Figure 4. Using the display start line address set command, the top line is normally selected (when the common output state is normal, COM0 is output. And, when reversed outputs COM7). For the display area of 9 lines is secured starting from the specified display start line address in the address incrementing direction.

Dynamically changing the line address using the display start line address set command enables screen scrolling and page change.

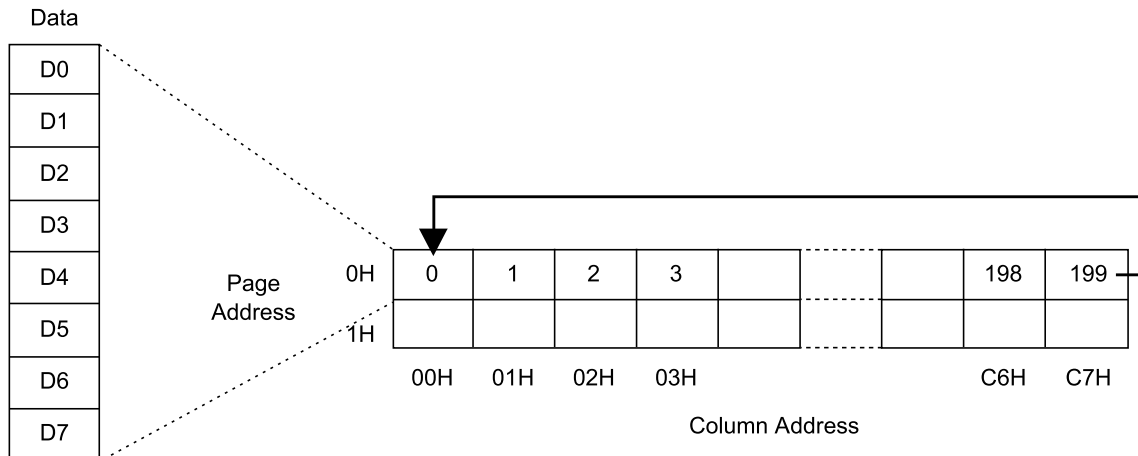


Fig. 5

**Display data latch circuit**

The display data latch circuit is a latch that temporarily stores the display data output from the display data RAM to the liquid crystal drive circuit.

Since the Display Normal Rotation/Reversal, Display ON/OFF, and Display All Lighting ON/OFF commands control the data in this latch, the data within the display data RAM is not changed.

**Oscillator Circuit**

This oscillator circuit is a CR type oscillator and generates display clocks. The oscillator circuit is valid only when M/S=HIGH and CL=HIGH.

When CL=LOW, the oscillation is stopped and the display clocks can be entered from the CL pin.

**Display Timing Generator Circuit**

This display timing generator circuit generates timing signals from the display clocks to the line address circuit and the display latch circuit. It latches the display data

to the display data latch circuit and outputs it to the segment drive output pin by synchronizing to the display clocks. The read operation of display data to the liquid crystal drive circuit is completely independent of the access to the display data RAM from the MPU. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.

The circuit also generates the internal common timing, liquid crystal alternating current signal (FR) from the display clocks.

As shown in Fig. 6, the FR normally generates the drive waveforms in the 2-frame alternating current drive system to the liquid crystal drive circuit.

When the S1D15711 Series is used for the multiple chip configuration, the slave side needs to supply the display timing signals (FR, CLO, and  $\overline{DOF}$ ) from the master side.

Table 5 shows the state of FR, CLO, or  $\overline{DOF}$ .

Table 5

Operation mode		FR	CLO	$\overline{DOF}$
Master (M/S=HIGH)	Built-in oscillator circuit valid (CL=HIGH)	Output	Output	Output
	Built-in oscillator circuit invalid (Input an external clock from the CL pin.)	Output	Output	Output
Slave (M/S=LOW)	(Fix the CL pin to LOW.)	Input	Input	Input

**2-frame alternating current drive waveforms**

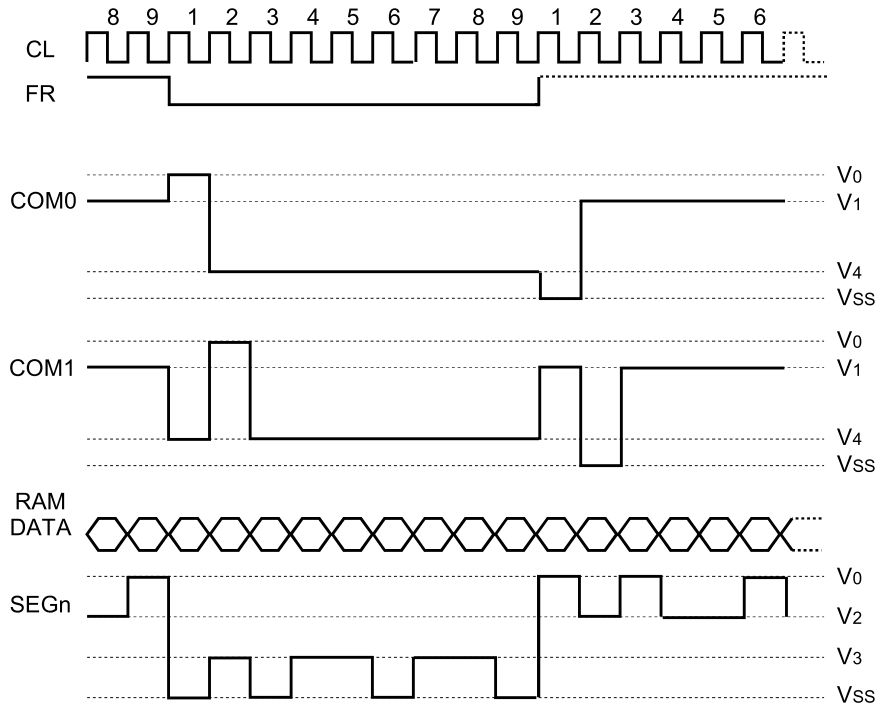


Fig. 6

### Common Output State Selection Circuit

The S1D15711 Series can set the scanning direction of the COM output using the common output state selection command (see Fig. 6). Therefore the IC assignment restrictions at LCD module assembly are reduced.

Table 6

State	COM scanning direction
Normal rotation	COM 0 → COM 7
Reversal	COM 7 → COM 0

### Liquid Crystal Drive Circuit

This liquid crystal drive circuit is 209 sets of multiplexers that generate quadruple levels for liquid crystal drive. It outputs the liquid crystal drive voltage that corresponds to the combinations of the display data, COM scanning signal, and FR signal.

Fig. 6 shows examples of the SEG and COM output waveforms.

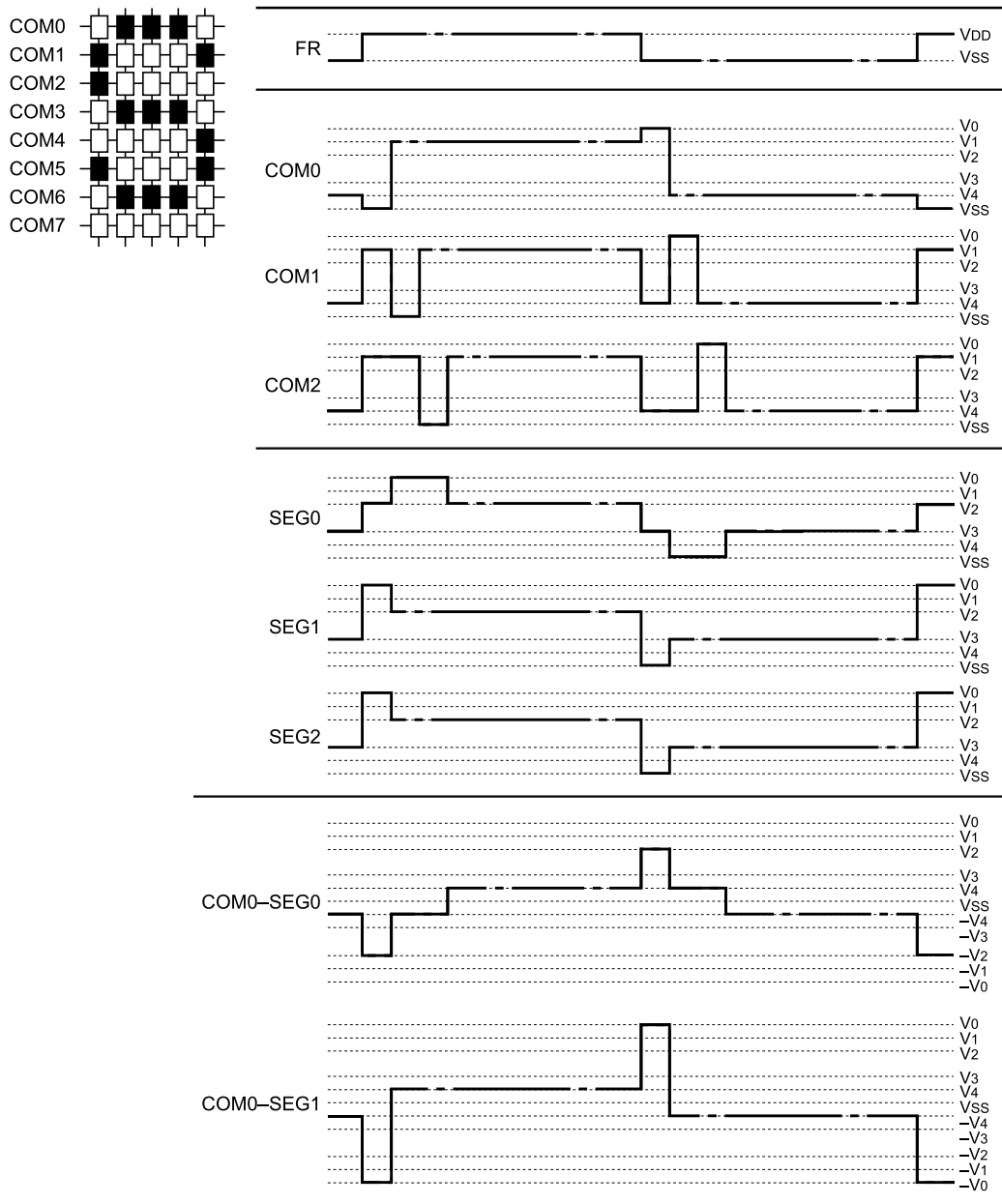


Fig. 7

**Power Supply Circuit**

This power supply circuit is a low power supply consumption one that generates the voltage required for the liquid crystal drive and consists of a boosting circuit, voltage adjusting circuit, and voltage follower circuit. It is valid only at master operation.

The power supply circuit ON/OFF controls the boosting

circuit, voltage adjusting circuit, and voltage follower circuit using the power supply control set command, respectively.

Therefore, it can also use the partial functions of the external power supply and built-in power supply together. Table 7 lists the functions that control 3-bit data using the power control set command and Table 8 lists the reference combinations.

Table 7 Description of controlling bits using the power control set command

Item	State	
	“1”	“0”
D2 Boosting circuit control bit	ON	OFF
D1 Voltage adjusting circuit (V adjusting circuit) control bit	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 8 Reference combinations

Status of use	D2	D1	D0	Boosting circuit	V adjusting circuit	V/F circuit	External voltage input	Boosting system pin
① Built-in power supply used	1	1	1	O	O	O	VDD2	Used
② V adjusting circuit and V/F circuit only	0	1	1	X	O	O	VOUT, VDD2	OPEN
③ V/F circuit only	0	0	1	X	X	O	V0, VDD2	OPEN
④ External power supply only	0	0	0	X	X	X	V1 to V4	OPEN

- The boosting system pin indicates the CAP1+, CAP1-, CAP2+, CAP2-, or CAP3- pin.
- Although the combinations other than those listed in the above table are also possible, they cannot be recommended because they are not actual use methods.

**Boosting circuit**

The boosting circuit incorporated in the S1D15711 Series enables the quadruple boosting, triple boosting, and double boosting of the VDD2 ↔ VSS potential.

For the quadruple boosting, the VDD2 ↔ VSS potential is quadruple-boosted to the positive side and output to the VOUT pin by connecting the capacitor C1 between CAP1+ and CAP1-, between CAP2+ and CAP2-, between CAP1+ and CAP3+, and between VDD2 and VOUT.

For the triple boosting, the VDD2 ↔ VSS potential is

triple-boosted to the positive side and output to the VOUT pin by connecting the capacitor C1 between CAP1+ and CAP1-, between CAP2+ and CAP2-, and between VDD2 and VOUT and strapping both CAP3- and VOUT pins.

For the double boosting, the VDD2 ↔ VSS potential is doubly boosted to the positive side and output to the VOUT pin by connecting the capacitor C1 between CAP1+ and CAP1-, and between VDD2 and VOUT, setting CAP2+ to OPEN, and VOUT and strapping CAP2-, CAP3+, and VOUT pins.

Fig. 8 shows the relationships of boosting potential.

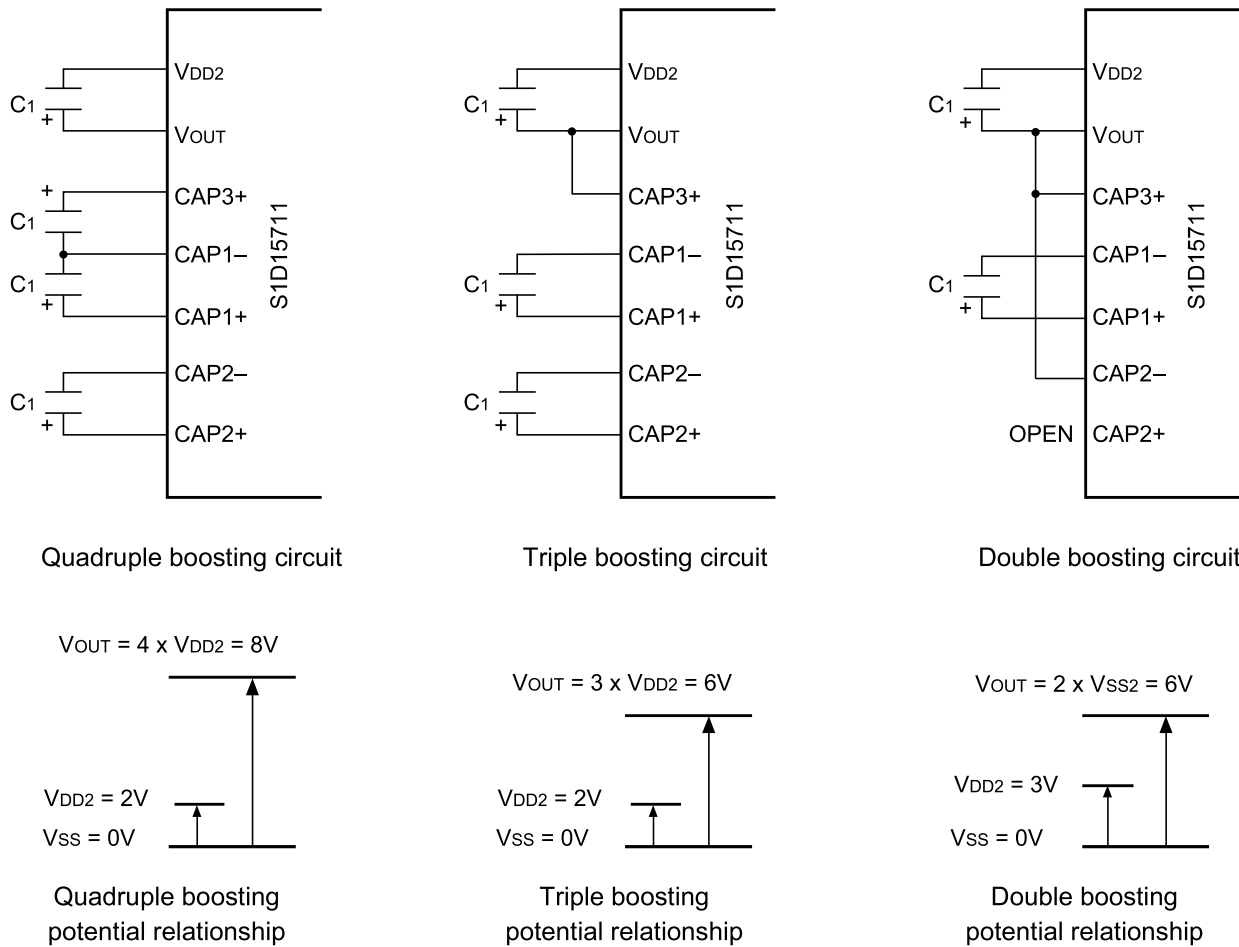


Fig. 8

- Set the VDD2 voltage range so that the voltage of the VOUT pin cannot exceed the absolute maximum ratings.

**Voltage adjusting circuit**

The boosting voltage generated in VOUT outputs the liquid crystal drive voltage V0 through the voltage adjusting circuit.

Since the S1D15711 Series incorporates a high-accuracy constant power supply, 64-step electronic volume function, and V0 voltage adjusting resistor, a high-accuracy voltage adjusting circuit can eliminate and save parts.

- (A) When using the V0 voltage adjusting internal resistor  
 The liquid crystal power supply voltage V5 can be controlled and the depth of liquid crystal display can be adjusted only by the command with the use of V0 voltage adjusting built-in resistor and the electronic volume function without any external resistor.

The V0 voltage can be obtained according to Expression A-1 within the range of  $|V_0| < |V_{OUT}|$ .

$$\begin{aligned}
 V_0 &= \left(1 + \frac{Rb}{Ra}\right) \cdot V_{EV} \\
 &= \left(1 + \frac{Rb}{Ra}\right) \cdot \left(1 - \frac{\alpha}{200}\right) \cdot V_{REG} \quad \text{(Expression A-1)} \\
 \therefore V_{EV} &= \left(1 - \frac{\alpha}{200}\right) \cdot V_{REG}
 \end{aligned}$$

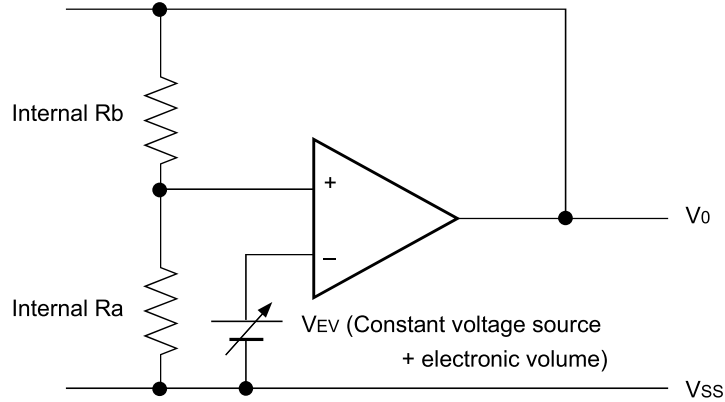


Fig. 9

VREG is a constant voltage source within an IC, and the value at Ta=25°C is constant as listed in Table 9.

Table 9

Device	Temperature gradient	Unit	VREG	Unit
Internal power supply	-0.1	[%/°C]	1.2	[V]

$\alpha$  indicates an electronic volume command value. Setting data in a 5-bit electronic volume register enters one state among 32 states. Table 10 lists the values of  $\alpha$  based on the setup of the electronic volume register.

Table 10

D4	D3	D2	D1	D0	$\alpha$
0	0	0	0	0	31
0	0	0	0	1	30
0	0	0	1	0	29
		⋮			⋮
1	1	1	0	1	2
1	1	1	1	0	1
1	1	1	1	1	0

Rb/Ra indicates the Vo voltage adjusting internal resistance ratio and can be adjusted into seven steps using the Vo voltage adjusting internal resistance ratio set command. The reference values of the (1+Rb/Ra) ratio are obtained as listed in Table 11 by setting 3-bit data in the Vo voltage adjusting internal resistance ratio register.

Table 11 (Reference values)

Register			Ratio of 1+ Rb/Ra
D2	D1	D0	
0	0	0	5.2
0	0	1	5.4
0	1	0	5.7
0	1	1	6.0
1	0	0	6.3
1	0	1	6.6
1	1	0	7.0
1	1	1	External resistor mode

For the internal resistance ratio, a manufacturing dispersion of up to  $\pm 3\%$  should be taken into account. When not within the tolerance, adjust the Vo voltage by externally mounting Ra and Rb.

Figs. 10 show the Vo voltage reference values per temperature gradient device based on the values of the Vo voltage adjusting internal resistance ratio register and electronic volume register at Ta=25°C.

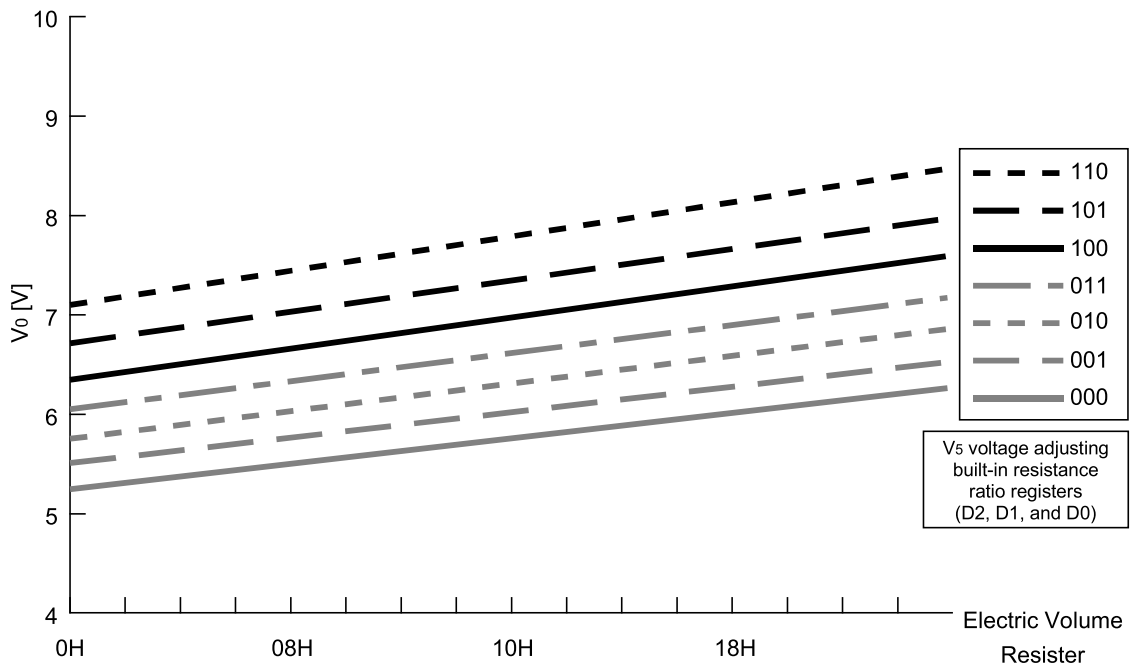


Fig. 10 S1D15711\*\*\*

V<sub>0</sub> voltage based on the values of V<sub>0</sub> voltage adjusting internal resistance ratio register and electronic volume register

<Setting example: When setting V<sub>0</sub> = 6.0V at Ta=25°C>  
 From Fig. 8 and Expression A-1.

Table 12

Description	Register				
	D4	D3	D2	D1	D0
V <sub>0</sub> voltage adjusting	–	–	0	0	1
electronic control	1	0	0	0	0

In this case, Table 13 lists the V<sub>0</sub> voltage variable range and pitch width using the electronic volume function.

Table 13

V <sub>0</sub>	Min.		Typ.		Max.	Unit
Variable range	5.5	to	6.0	to	6.5	[V]
Pitch width	about 31					[mV]



(B) When using the external resistor (not using the V<sub>0</sub> voltage adjusting internal resistor) ①  
 The liquid crystal power supply voltage V<sub>0</sub> can also be set by adding the resistors (R<sub>a</sub>' and R<sub>b</sub>') between V<sub>SS</sub> and V<sub>R</sub> and between V<sub>R</sub> and V<sub>0</sub> without the V<sub>0</sub> voltage adjusting built-in resistor (Internal resistance ratio set command for adjusting the V<sub>0</sub> voltage [27H]). Also in this case, the liquid crystal power supply voltage V<sub>0</sub> can be controlled using the command and the light and shade of liquid crystal display can be adjusted by using the

electronic volume function.  
 The V<sub>0</sub> voltage can be obtained from Expression B-1 by setting the external resistors R<sub>a</sub>' and R<sub>b</sub>' within the range of |V<sub>0</sub>| < |V<sub>OUT</sub>|.

$$V_0 = \left(1 + \frac{R_{b'}}{R_{a'}}\right) \cdot V_{EV} \quad (\text{Expression B-1})$$

$$= \left(1 + \frac{R_{b'}}{R_{a'}}\right) \cdot \left(1 - \frac{\alpha}{200}\right) \cdot V_{REG}$$

$$\left[ \because V_{EV} = \left(1 - \frac{\alpha}{200}\right) \cdot V_{REG} \right]$$

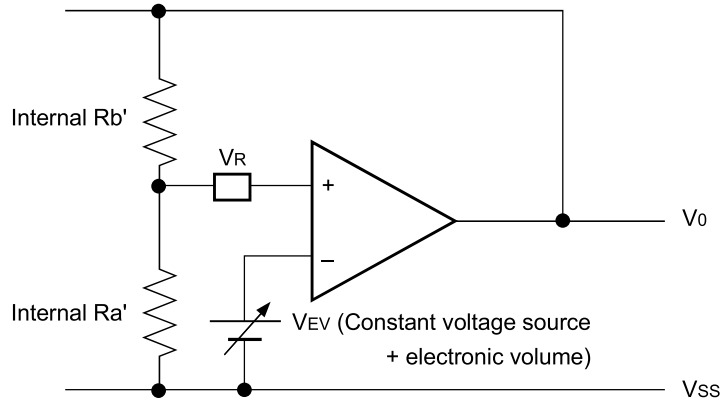


Fig. 11

<Setting example: When setting V<sub>0</sub>=6.0V at T<sub>a</sub>=25°C>

Set the value of the electronic volume register as the intermediate value (D4, D3, D2, D1, D0) = (1,0,0,0,0).  
 From the foregoing we can establish the expression:

$$\alpha = 15$$

$$V_{REG} = 1.2V$$

From Expression B-1, it follows that

$$V_0 = \left(1 + \frac{R_{b'}}{R_{a'}}\right) \cdot \left(1 - \frac{\alpha}{200}\right) \cdot V_{REG} \quad (\text{Expression B-2})$$

$$6.0V = \left(1 + \frac{R_{b'}}{R_{a'}}\right) \cdot \left(1 - \frac{15}{200}\right) \cdot 1.2$$

Also, suppose the current applied to R<sub>a</sub>' and R<sub>b</sub>' is 5μA.  
 $R_{a'} + R_{b'} = 1.2M\Omega$  (Expression B-2)

It follows that  
 Therefore from Expressions B-2 and B-3, we have

$$\frac{R_{b'}}{R_{a'}} = 4.4$$

$$R_{a'} = 272k\Omega$$

$$R_{b'} = 928k\Omega$$

In this case, Table 14 lists the V<sub>0</sub> voltage variable range and pitch width using the electronic volume function.

Table 14

V5	Min.	Typ.	Max.	Unit
Variable range	5.5	to 6.0	to 6.5	[V]
Pitch width		about 31		[mV]

(C) When using the external resistor (not using the V<sub>0</sub> voltage adjusting internal resistor) ②  
 In the use of the above-mentioned external resistor, the liquid crystal power supply voltage V<sub>0</sub> can also be set by adding the resistors to finely adjust R<sub>a</sub>' and R<sub>b</sub>'. Also in this case, the liquid crystal power supply voltage V<sub>0</sub> can be controlled using the command and the light and shade of liquid crystal display can be adjusted by using the electronic volume function.

The V<sub>0</sub> voltage can be obtained from the following expression C-1 by setting the external resistors R<sub>1</sub>, R<sub>2</sub> (variable resistors), and R<sub>3</sub> within the range of |V<sub>0</sub>| < |V<sub>OUT</sub>| and finely adjusting R<sub>2</sub> (ΔR<sub>2</sub>).

$$V_0 = \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot \left(1 - \frac{\alpha}{200}\right) \cdot V_{REG}$$

$$\left[ \because V_{EV} = \left(1 - \frac{\alpha}{200}\right) \cdot V_{REG} \right] \quad (\text{Expression C-1})$$

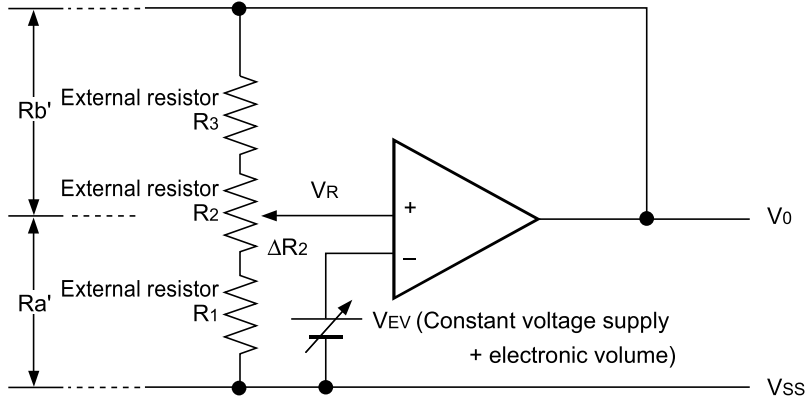


Fig. 12

<Setting example: When setting  $V_0 = 5.0$  to  $8.0V$  at  $T_a = 25^\circ C$ >

Set the value of the electronic volume register as the intermediate value (D4, D3, D2, D1, D0) = (1,0,0,0,0). From the foregoing we can establish the expression:

$$\alpha = 15$$

$$V_{REG} = 1.2V$$

When  $\Delta R_2 = 0\Omega$ , to obtain  $V_0 =$  (TBD) V from Expression C-1, it follows that

$$8.0V = \left(1 + \frac{R_3 + R_2}{R_1}\right) \cdot \left(1 - \frac{15}{200}\right) \cdot 1.2$$

(Expression C-2)

When  $\Delta R_2 = R_2$ , to obtain  $V_0 =$  (TBD) V, it follows that

$$5.0V = \left(1 + \frac{R_3}{R_1 + R_2}\right) \cdot \left(1 - \frac{15}{200}\right) \cdot 1.2$$

(Expression C-3)

Also, suppose the current applied between  $V_{SS}$  and  $V_0$  is  $5\mu A$ .

$$R_1 + R_2 + R_3 = 1.3M\Omega$$

(Expression C-4)

It follows that

Therefore from Expressions C-2, C-3, and C-4, we have

$$R_1 = 180k\Omega$$

$$R_2 = 109k\Omega$$

$$R_3 = 1011k\Omega$$

At this time, the  $V_0$  voltage variable range and notch width based on electronic volume function are given in the following Table when  $V_0 = 6.5V$  by  $R_2$  is assumed:

Table 15

$V_0$	Min.		Typ.		Max.	Unit
Variable range	5.9	to	6.5	to	7.0	[V]
Pitch width	about 35					[mV]

- When using the  $V_0$  voltage adjusting internal resistor or electronic volume function, the state where at least the  $V_0$  voltage adjusting circuit and voltage follower circuit are operated together needs to be set using the power control set command. Also when the boosting circuit is OFF, the voltage needs to be applied from  $V_{OUT}$ .
- The  $V_R$  pin is valid only when the  $V_0$  voltage adjusting internal resistor. Set the  $V_R$  pin to OPEN when using the  $V_0$  voltage adjusting internal resistor.
- Since the  $V_R$  pin has high input impedance, noise must be taken into consideration such as for short and shielded lines.

**Liquid crystal voltage generator circuit**

The  $V_0$  voltage is resistor-split within an IC and generates the  $V_1, V_2, V_3,$  and  $V_4$  potentials required for the liquid crystal drive.

Further, the  $V_1, V_2, V_3,$  and  $V_4$  potentials are impedance-

converted by the voltage follower and supplied to the liquid crystal drive circuit.

Using the bias set command allows you to select a desired bias ratio from 1/5 or 1/6.

**Command sequence when the built-in power supply is turned off**

To turn off the built-in power supply, set it in the power save state and then turn off the power supply according to the command sequence shown in Fig. 13 (procedure).

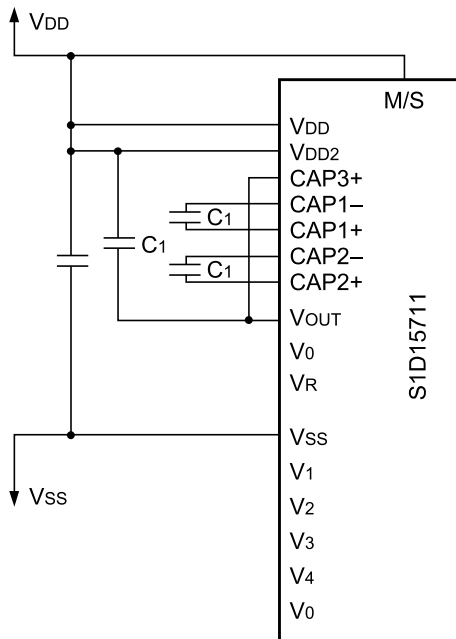
Procedure	Description (Command, state)	Command address								
		D7	D6	D5	D4	D3	D2	D1	D0	
Step1	Power save	1	0	1	0	1	1	1	0	} Power save command (Composite command of display OFF and display full lighting ON)
Step2	Turning off the built-in power supply	1	0	1	0	0	1	0	1	

Fig. 13

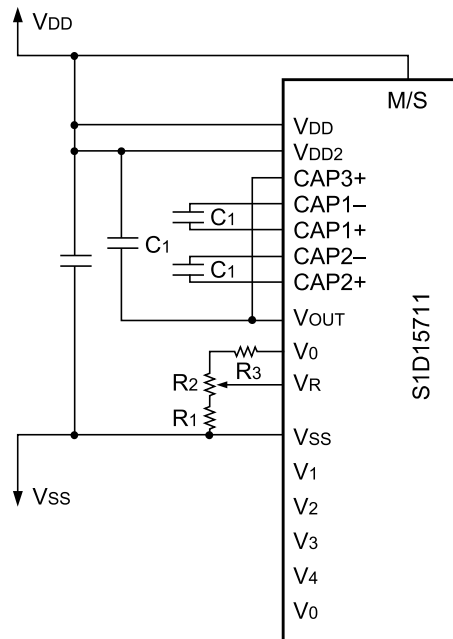
**Reference circuit examples**

① All the built-in power supply used

(1) When using the V<sub>0</sub> voltage adjusting built-in resistor  
(Example of V<sub>DD2</sub>=V<sub>DD</sub>, quadruple boosting)

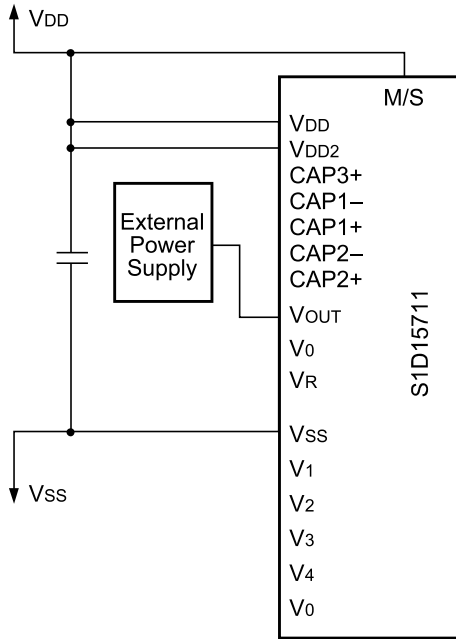


(2) When not using the V<sub>0</sub> voltage adjusting built-in resistor  
(Example of V<sub>DD2</sub>=V<sub>DD</sub>, quadruple boosting)

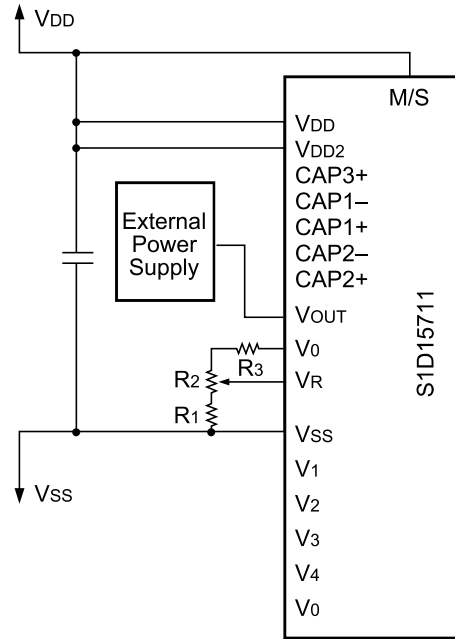


② Only the voltage adjusting circuit and V/F circuit used

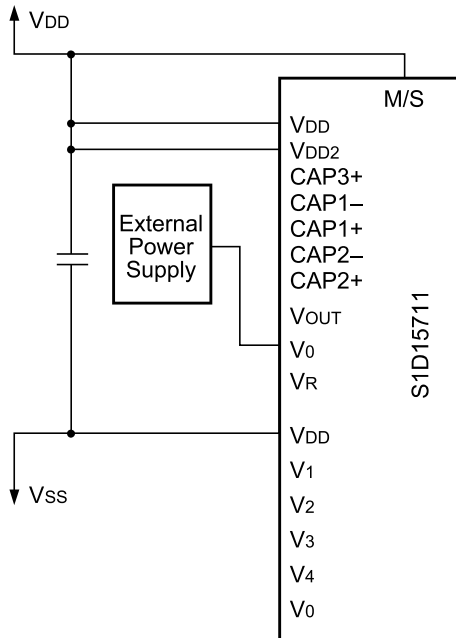
(1) When using the V<sub>0</sub> voltage adjusting built-in resistor



(2) When not using the V<sub>0</sub> voltage adjusting built-in resistor

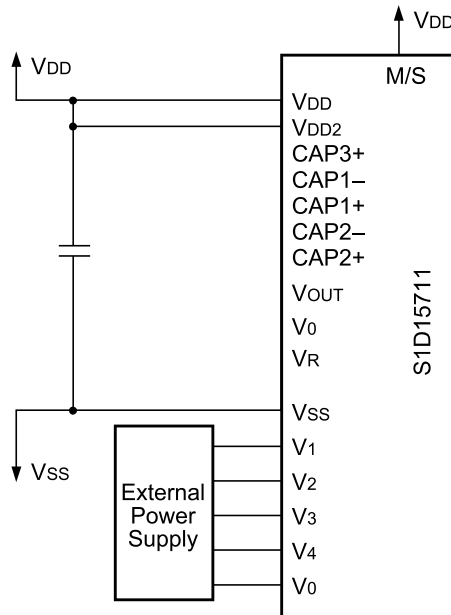


③ Only the V/F circuit used



④ Only the external power supply used

Depending on all external power supplies



Common reference setting example  
At V<sub>0</sub> ≒ 4.5 to 8.0V variable

Item	Setting value	Unit
C1	1.0 to 4.7	μF

Fig. 14

- \*1 Since the VR terminal input impedance is high, use short leads and shielded lines. When the VR terminal is not used, means should be taken to prevent capacitance of the line or others from being applied.
- \*2 C1 is determined according to the size of the LCD panel. Set a value so that the liquid crystal drive voltage can be stable.  
[Setting example] • Turn on the V0 adjusting circuit and the V/F circuit and apply external voltage.  
• Then turn on all built-in power supplies and determine C1.
- \*3 Capacity is connected in order to stabilize voltage between VDD and VSS power supplies.
- \*4 In case a large load panel is being driven by a built-in power supply and when the voltage level of V0 to V4 are not stable, it is possible to connect a capacitor between the V0 to V4 and the VSS for the purpose of stabilizing the voltage. Regarding the capacity, determine the capacity after confirming the indication quality targeting to a similar level of the capacity of C1.
- \*5 Do not use the built-in power supply circuit if the display panel's load is large or if its possible that sufficient display quality will not be achieved by using only the built-in power supply circuit. Alternatively, use the external liquid crystal drive voltage.

**Precautions when installing COG**

When installing the COG, consider that there is a resistance on the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). This resistance may cause the indications on the LCD not to conform or it may cause IC malfunctions. Therefore, when installing the COG, design the module paying sufficient attention to the following three points and make sufficient evaluations under actual conditions.

1. As much as possible, suppress the resistance that is occurring between the driver chip pin and the externally connected parts.  
The boosting capacitors (the capacitors connecting to respective CAP pins and capacitor being inserted between VOUT and VDD2) of this IC are being switched over by the transistor with an ON-resistance of about 10Ω. However, when installing the COG, the resistance of the ITO wiring is being inserted in unison with the switching transistor, thus dominating the boosting ability. Take considerable care when wiring each boosting capacitor, and take measures such as using thicker ITO wiring.  
As much as possible, suppress the resistance in the driver chip's power supply pin.

The power supply voltage may drop immediately due to an instantaneous current in areas like the switching part of the display clock. If the power supply pin's ITO wiring resistance is too high, then the voltage drop on the driver IC may increase significantly, causing malfunctions. Take considerable care when wiring the power supply line so that continuous power is supplied to the driver IC.

The IC also employs the power supply pin VDD2 for the power supply circuit, which is separate from the logic system's power supply pin VDD. If the noise from the power supply circuit affects the logic circuit, then supply separate power to the VDD and the VDD2 or use external liquid crystal drive voltage instead of the built-in power supply.

2. Create the COG module sample with different sheet resistance.  
Evaluate sufficiently and, as much as possible, use ones with an operational margin sheet resistance.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

**Reset Circuit**

When the RES input is set to the LOW level or the reset command is input, LSI enters initial setting states. The initial setting states are listed below.

- 1 Serial Interface Register Data Clear
- 2 Power Save Mode ON  
(Built-in oscillator circuit OFF, built-in power supply circuit OFF, display full lighting ON)
- 3 Display Normal rotation
- 4 Page Address Set to page 0.
- 5 Column Address Set to address 0.
- 6 Display Start Line Set to first line.
- 7 Segment Driver Direction Normal rotation
- 8 Common Driver Direction Normal direction
- 9 Remote Modify Line OFF
- 10 Power Control Register: (D2, D1, D0) = (0, 0, 0)
- 11 V0 Voltage Adjusting Built-in Resistance Ratio Register: (D2, D1, D0) = (0, 0, 0)
- 12 Electronic Control Register: (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0)

- 13 LCD Power Supply Bias Ratio Set to 1/5 bias.
- 14 Test Mode Reset

When the power is turned on, the initialization using the RES pin is required. After the initialization using the RES pin, each input pin needs to be controlled normally. Besides, when the MPU control signal has high impedance, overcurrent may be applied to an IC. After turning on the power, take action so that the input pin cannot have high impedance.

The S1D15711 Series discharge electric charges of V0 to VSS and VOUT to VDD2 at RES pin is set to the LOW level. If external power supplies for driving LCD are used, do not input external power while the RES pin is set to the LOW level to prevent short-circuiting between the external power supplies, VSS and VDD2.

## 7. COMMAND DESCRIPTION

The S1D15711 Series identifies data bus signals according to the combinations of A0,  $\overline{RD}(E)$ , and  $\overline{WR}(R/\overline{W})$ . Since the interpretation and execution of commands are performed only by the internal timing independently of external clocks. The 80 series MPU interface starts commands by inputting low pulses to the  $\overline{RD}$  pin at read and to the  $\overline{WR}$  pin at write operation. The 68 series MPU interface enters the read state when HIGH is input to the R/ $\overline{W}$  pin. It enters the write state when LOW is input to the same pin. It starts commands by inputting high pulses to the E pin (for the timing, see the Timing Characteristics of Chapter 10). Therefore the 68 series MPU interface differs from the 80 series MPU interface in that  $\overline{RD}(E)$  is set to “1 (H)” at display data read in the Command Description and Command Table. The command description is given below by taking the 80 series MPU interface as an example.

When selecting the serial interface, enter sequential data from D7.

### Command description

#### (1) Display ON/OFF

This command specifies display ON/OFF.

A0	E R/ $\overline{W}$		D7	D6	D5	D4	D3	D2	D1	D0	Setting
	$\overline{RD}$	$\overline{WR}$									
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

For display OFF, the segment and common drivers output the Vss level.

Further, for display OFF, when the display full lighting ON command is executed (otherwise, for display full lighting ON, when the display OFF command is executed, processing enters the power save mode).

#### (2) Display Start Line Set

This command specifies the display start line address of the display data RAM shown in Fig. 4. The display area is displayed for 9 lines from the specified line address to the line address increment direction. When this command is used to dynamically change the line address, the vertical smooth scroll and page change are enabled. For details, see the Line address circuit of “Function Description”.

A0	E R/ $\overline{W}$		D7	D6	D5	D4	D3	D2	D1	D0	Line address
	$\overline{RD}$	$\overline{WR}$									
0	1	0	0	1	0	0	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
							↓				↓
							0	1	0	0	6
							0	1	1	1	7

**(3) Page Address Set**

This command specifies the page address that corresponds to the low address when accessing the display data RAM shown in Fig. 4 from the MPU side. The display data RAM can access desired bits when the page address and column address are specified. Even when the page address is changed, the display state will not be changed. For details, see the Page address circuit of “Function Description”.

<b>E R/W</b>			<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>Page address</b>
<b>A0</b>	<b>RD</b>	<b>WR</b>									
0	1	0	1	0	1	1	0	0	0	0	0
										1	1

**(4) Column Address Set**

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (higher 4-bits and lower 4-bits) when it is set (set continuously in principle). Each time the display data RAM is accessed, the column address automatically increments (+), making it possible for the MPU to continuously read and write the display data. The page address is not changed continuously. For details, see “Column Address Circuit” in Function Description.

<b>E R/W</b>			<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	
<b>A0</b>	<b>RD</b>	<b>WR</b>									
High-order bit →	0	1	0	0	0	0	1	A7	A6	A5	A4
Low-order bit →							0	A3	A2	A1	A0

<b>A7</b>	<b>A6</b>	<b>A5</b>	<b>A4</b>	<b>A3</b>	<b>A2</b>	<b>A1</b>	<b>A0</b>	<b>Column address</b>
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	0
				↓				↓
1	1	0	0	0	1	1	0	198
1	1	0	0	0	1	1	1	199

**(5) Display Data Write**

This command writes 8-bit data to the specified address of the display data RAM. Since the column address is automatically incremented by 1 after the data is written, the MPU can successively write the display data.

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
1	1	0	Write data							

**(6) Display Data Read**

This command reads the 8-bit data in the specified address of the display data RAM. Since the column address is automatically incremented by 1 after the data is written, the MPU can successively read the data consisting of multiple words.

Besides, immediately after the column address is set, dummy read is required one time. For details, see the description of the Display data RAM and internal register access of "Function Description".

When using the serial interface, the display cannot be read.

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
1	0	1	Read data							

**(7) ADC Select (Segment Driver Direction Select)**

This command can reverse the correspondence relationship between the column address of the display RAM data shown in Fig. 4 and the segment driver output. Therefore the order of the segment driver output pin can be reversed using the command. After the display data is written and read, the column address is incremented by 1 according to the column address of Fig. 4. For details, see the Column address circuit of "Function Description".

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0	Setting
	RD	WR									
0	1	0	1	0	1	0	0	0	0	0	Clockwise (normal rotation)
										1	Counterclockwise (reversal)

**(8) Display Normal Rotation/Reversal**

This command can reversal display lighting and non-lighting without overwriting the contents of display data RAM. In this case, the contents of display data RAM are held.

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0	Setting
	RD	WR									
0	1	0	1	0	1	0	0	1	1	0	LCD on potential (normal rotation) RAM data HIGH
										1	LCD on potential (reversal) RAM data LOW



**(9) Display All Points ON/OFF**

This command can forcedly make all display set in the lighting state irrespective of the contents of display data RAM. In this case, the contents of display data RAM are held.

This command has priority over the display normal rotation/reversal command.

Also, when the display is OFF, execute the Display All Points ON Command (or when the display is ON, execute the Display OFF Command), and the power save mode will be selected.

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0	Setting
	RD	WR									
0	1	0	1	0	1	0	0	1	0	0	Normal display state
										1	Display all lighting

**(10) LCD Bias Set**

This command selects the bias ratio of the voltage required for liquid crystal drive. The command is valid when the V/F circuit of the power supply circuit is operated.

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0	Selected state
	RD	WR									
0	1	0	1	0	1	0	0	0	1	1	1/5 bias
										0	1/6 bias

**(11) Read Modify Write**

This command is used together with the end command. Once this command is entered, the column address can be incremented by 1 only using the display data write command instead of being changed using the display read command. This state is held until the end command is entered. When the end command is entered, the column address returns to the address when the read modify write command is entered. This function can reduce the load of the MPU when repeatedly changing data for a specific display area such as a blinking cursor.

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
0	1	0	1	1	1	0	0	0	0	0

\* The commands other than Display Data Read/Write can be used even in Read Modify Write mode. However, the column address set command cannot be used.

- Sequence for cursor display

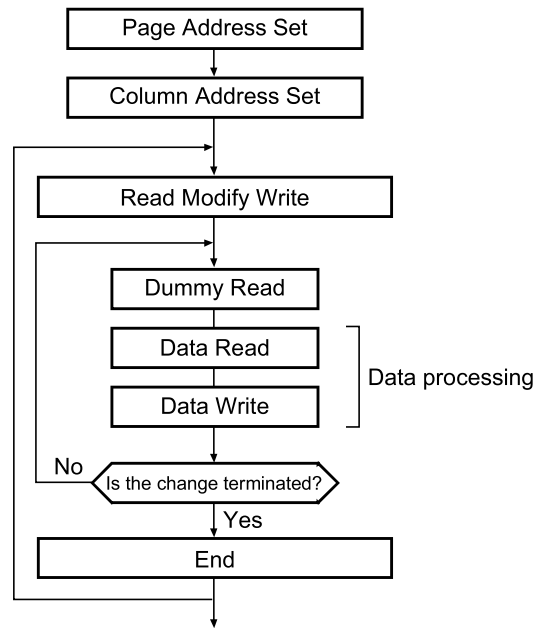


Fig. 15

**(12) End**

This command resets the Read Modify Write mode and returns the column address to the mode initial address.

E R/W		D7	D6	D5	D4	D3	D2	D1	D0
A0	RD WR								
0	1 0	1	1	1	0	1	1	1	0

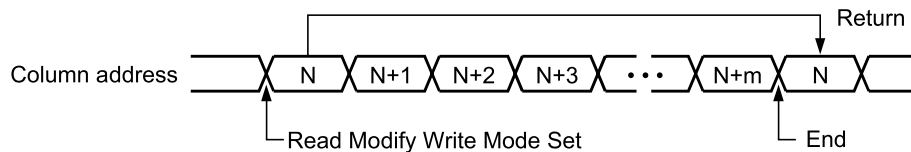


Fig. 16

**(13) Reset**

When this command is entered, this LSI is initialized. The execution of the reset command will not have any effect on the display data RAM. Further, the reset command cannot be used to perform strapping (discharging of an electric charge) between  $V_{OUT} - V_{DD2}$  and between  $V_0 - V_{SS}$ . For details, see the Reset of "Function Description".

Reset operation is performed after the reset command is entered.

For the detail, see "Reset" of Function Description. The reset operation is performed in the reset command input line.

E R/W		D7	D6	D5	D4	D3	D2	D1	D0
A0	RD WR								
0	1 0	1	1	1	0	0	0	1	0

The initialization when the power is applied is performed using the reset signal to the  $\overline{RES}$  pin. The reset command cannot be substituted for the signal.

**(14) Common Output State Selection**

This command can select the scanning direction of the COM output pin. For details, see the Common Output State Selection Circuit of “Function Description”.

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0	Selected state	
	RD	WR										
0	1	0	1	1	0	0	0	*	*	*	Normal rotation	COM0 → COM7
											Reversal	COM7 → COM0

\*: Invalid bit

**(15) Power Control Set**

This command sets the function of the power supply circuit. For details, see the Power Supply Circuit of “Function Description”.

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0	Selected state
	RD	WR									
0	1	0	0	0	1	0	1	0			Boosting circuit: OFF
											Boosting circuit: ON
								0			V adjusting circuit: OFF
											1
									0		V/F circuit: OFF
											1

(V/F circuit: Voltage follower circuit, V adjusting circuit: voltage adjusting circuit)

**(16) V0 Voltage Adjusting Internal Resistance Ratio Set**

This command sets the V0 voltage adjusting internal resistance ratio. For details, see the Power Supply Circuit of “Function Description”.

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0	Rb to Ra ratio
	RD	WR									
0	1	0	0	0	1	0	0	0	0	0	Small
											0
								0	1	0	↓
								1	1	0	Large
											1

**(17) Electronic Volume Set**

This command controls the liquid crystal drive voltage  $V_0$  output from the voltage adjusting circuit of the built-in liquid crystal power supply and can adjust the light and shade of liquid crystal display.

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0	V5
	RD	WR									
0	1	0	1	0	0	0	0	0	0	0	Small
0	1	0				0	0	0	0	1	
0	1	0				0	0	0	1	0	↓
							↓				
0	1	0				1	1	1	1	0	
0	1	0				1	1	1	1	1	Large

\*: Invalid bit

When not using the electronic volume function, set (1,0,0,0,0).

- Sequence of the electronic volume register set

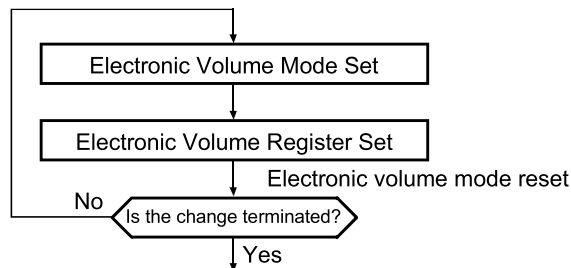


Fig. 17

**(18) Power save**

When display full lighting ON is set in the display OFF state, the power save state occurs and power consumption can greatly be reduced.

In the power save state, the operating state before the display data and power save activation is held, and the display data RAM can also be accessed from the MPU.

The power save state is reset using the procedure shown in Fig. 18.

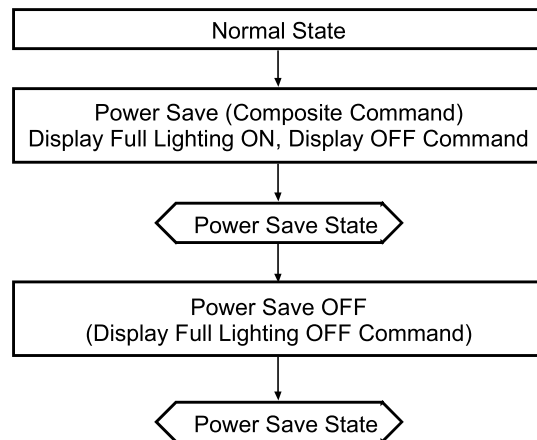


Fig. 18

## S1D15711 Series

In the power save mode, all the operations of LCD display systems are stopped, and the power consumption approximate to the static current when they are not accessed from the MPU can be reduced. The internal state in this state is as follows:

- (1) The oscillator circuit and the LCD power supply circuit are stopped.
- (2) All liquid crystal drive circuits are stopped and the segment and common drivers output the VSS level.

\* When using an external power supply, it is recommended that the function of the external power supply circuit should be stopped at power save activation. For example, when assigning each level of the crystal liquid drive voltage via an external (standalone) resistance splitting circuit, it is recommended that a circuit which cuts off the current flowing into the resistance splitting circuit should be added at power save activation. The S1D15711 Series is provided with a liquid crystal display blanking control pin  $\overline{\text{DOF}}$ , and the pin is set to **LOW** at power save activation. The function of the external power supply circuit can be stopped using the  $\overline{\text{DOF}}$  output.

### (19) NOP

Non-Operation

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
0	1	0	1	1	1	0	0	0	1	1

### (20) Test

IC chip test command. Do not use this command. If the test command is used incorrectly, it can be reset by setting the RES input to LOW or by using the reset command or display ON/OFF.

A0	E R/W		D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
0	1	0	1	1	*	1	*	*	*	*

\*: Invalid bit

(Note) Although the S1D15711 Series maintains the operation status as per the command, in case excessive external noise enters or when abrupt power voltage variation in excess of the specified value as per the “9. DC Characteristic Items” occurs, there is a possibility of changing the internal status or causing a malfunctioning. Such action that suppresses the generation of noise and prevents the effect of noise needs to be taken on installation and systems. Besides, to prevent sudden noise, it is recommended that the operating state should periodically be refreshed.

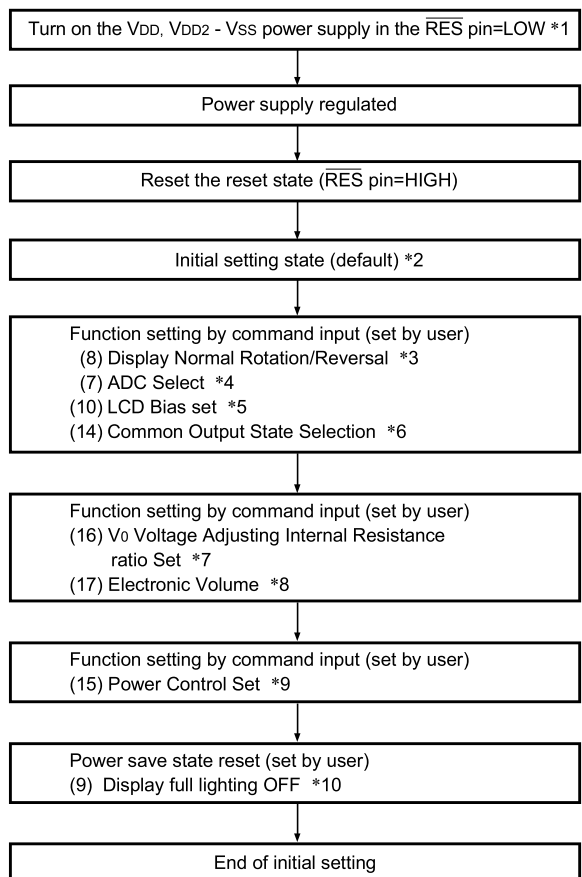
Table 16 S1D15711 Series Commands

Command	Command code										Function	
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1		D0
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	LCD display ON/OFF 0: OFF, 1: ON
(2) Display Start Line Set	0	1	0	0	1	Display start address					1	Sets the display start line address of the display RAM.
(3) Page Address Set	0	1	0	1	0	1	1	1	1	1	0	Display RAM: 0 : 0 page 1 : 1 page
(4) Column Address Set High-Order Bit	0	1	0	0	0	0	1	High order Column address			1	Sets the high-order four bits of the column address of the display RAM.
Column Address Set Low-Order Bit	0	1	0	0	0	0	0	Low order Column address			1	Sets the low-order four bits of the column address of the display RAM.
(5) Display Data Read	1	1	0	Write data								Writes data on the display RAM.
(6) Display Data Write	1	0	1	Read data								Reads data from the display RAM.
(7) ADC Select	0	1	0	1	0	1	0	0	0	0	0	Supports the SEG output of the display RAM address. 0: normal rotation, 1: Reversal
(8) Display Normal Rotation/Reversal	0	1	0	1	0	1	0	0	1	1	0	LCD display normal rotation/reversal 0: normal rotation, 1: Reversal
(9) Display All Points ON/OFF	0	1	0	1	0	1	0	0	1	0	0	Display all lighting 0: normal display, 1: All ON
(10) LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0	Sets the LCD drive voltage bias ratio. 0: 1/6, 1: 1/5
(11) Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address. At write operation: By 1, at read: 0
(12) End	0	1	0	1	1	1	0	1	1	1	0	Resets Read Modify Write.
(13) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal resetting
(14) Common Output State Selection	0	1	0	1	1	0	0	0	*	*	*	Selects the scanning direction of the COM output. 0: Normal rotation, 1: Reversal
(15) Power Control Set	0	1	0	0	0	1	0	1	Operating state		1	Selects the state of the built-in power supply
(16) V <sub>0</sub> Voltage Adjusting Internal Resistance Ratio Set	0	1	0	0	0	1	0	0	Resistance ratio setting		1	Selects the state of the internal resistance ratio (Rb/Ra).
(17) Electronic Volume Set	0	1	0	1	0	0	Electronic control value				1	Sets the V <sub>0</sub> output voltage in the electronic register.
(18) Power Save	-	-	-	-	-	-	-	-	-	-	-	Moves to the power save state. Display OFF and display all points ON compound command
(19) NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation command
(20) Test	0	1	0	1	1	*	1	*	*	*	*	Do not use the IC chip test command.

\*: Invalid bit

**Instruction Setup: Reference**

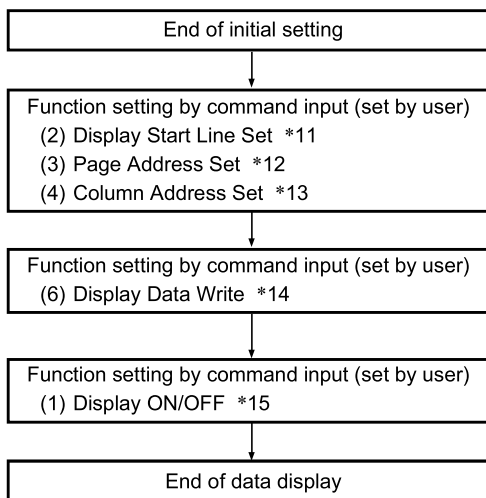
**(1) Initial Setting**



Notes: Reference items

- \*1: If external power supplies for driving LCD are used, do not supply voltage on VOUT or V0 pin during the period when RES = LOW. Instead, input voltage after releasing the reset state.  
6. Function Description “Reset Circuit”
- \*2: The contents of DDRAM are not defined even in the initial setting state after resetting.  
6. Function Description Section “Reset Circuit”
- \*3: 7. Command Description Item (8) Display Normal Rotation/Reversal
- \*4: 7. Command Description Item (7) ADC Select
- \*5: 7. Command Description Item (10) LCD Bias Set
- \*6: 7. Command Description Item (14) Common output state selection
- \*7: 6. Function Description Section “Power Supply Circuit” and 7. Command Description Item (16) V0 Voltage Adjusting Internal Resistance ratio Set
- \*8: 6. Function Description Section “Power Supply Circuit” and 7. Command Description Item (17) Electronic Volume
- \*9: 6. Function Description Section “Power Supply Circuit” and 7. Command Description Item (15) Power Control Set
- \*10 7. Command Description Item (9) Display All points ON/OFF and (18) Power Save

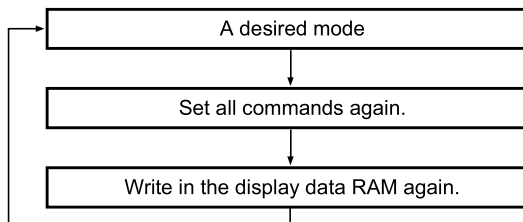
**(2) Data Display**



Notes: Reference items

- \*11: 7. Command Description Item (2) Display Start Line Set
- \*12: 7. Command Description Item (3) Page Address Set
- \*13: 7. Command Description Item (4) Column Address Set
- \*14: The contents of DDRAM is not defined after completing initial setting. Enter data in each DDRAM to be used for display.  
7. Command Description Item (5) Display Data Write
- \*15: Avoid activating the display function with entering space characters as the data if possible.  
7. Command Description Item (1) Display ON/OFF

**(3) Refresh \*16**

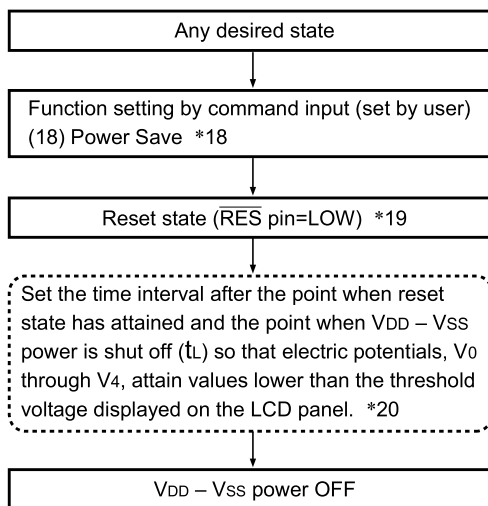


Notes: Reference items

- \*16: It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.



(4) Power \*17



Notes: Reference items

- \*17: This IC is a VDD - Vss power system circuit controlling the LCD driving circuit for the V0 - Vss power system. Shutting of power with voltage remaining in the V0 - Vss power system may cause uncontrolling voltage to be output from the SEG and COM pins. Follow the Power OFF sequence.
- \*18: 7. Command Description Item (18) Power Saving
- \*19: When external power supplies for driving LCD are used, turn all external power supplies off before entering reset state.  
6. Function Description Item Reset Circuit
- \*20: The threshold voltage of the LCD panel is about 1 [V].  
Set up tL so that the relationship, tL > tH, is maintained. A state of tL < tH may cause faulty display.

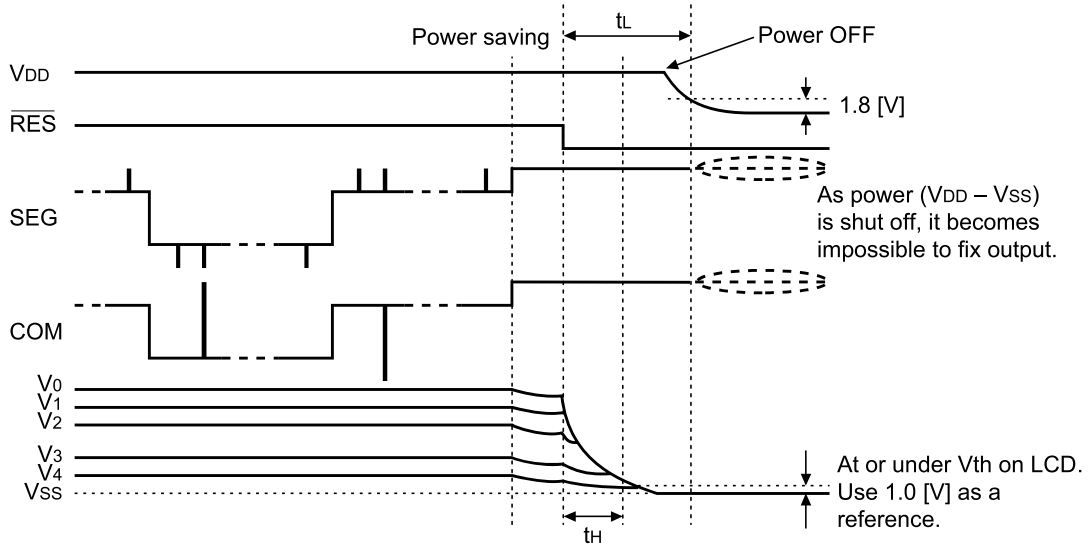
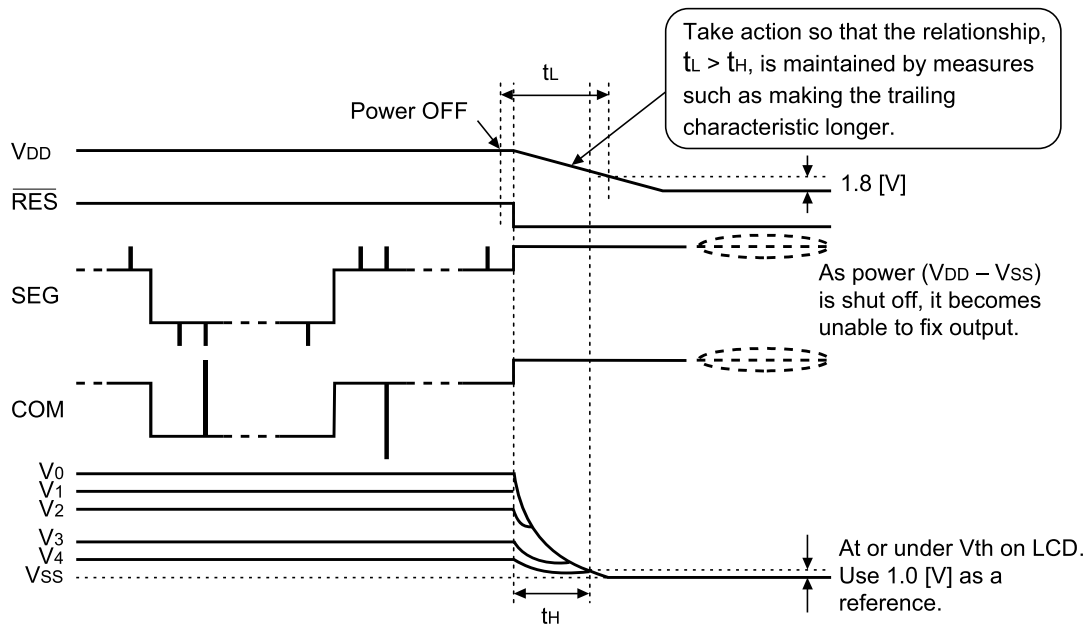


Fig. 19



If command control is disabled when power is OFF, take action so that the relationship,  $t_L > t_H$ , is maintained by measures such as making the trailing characteristic of power ( $V_{DD} - V_{SS}$ ) longer.

Fig. 20

8. ABSOLUTE MAXIMUM RATINGS

Table 17

VSS=0 V unless specified otherwise

Item		Symbol	Specification value	Unit
Power supply voltage		VDD	-0.3 to 6.0	V
Power supply voltage (2) (Based on VDD)	At triple boosting	VDD2	-0.3 to 5.0	
			-0.3 to 3.3	
	At quadruple boosting	-0.3 to 2.5		
Power supply voltage (3) (Based on VDD)		V0, VOUT	-0.3 to 10.0	
Power supply voltage (4) (Based on VDD)		V1, V2, V3, V4	-0.3 to V0	
Input voltage		VIN	-0.3 to VDD+0.3	
Output voltage		VO	-0.3 to VDD+0.3	
Operating temperature		TOPR	-40 to 85	°C
Storage temperature	TCP	TSTR	-55 to 100	
	Bare chip		-55 to 125	

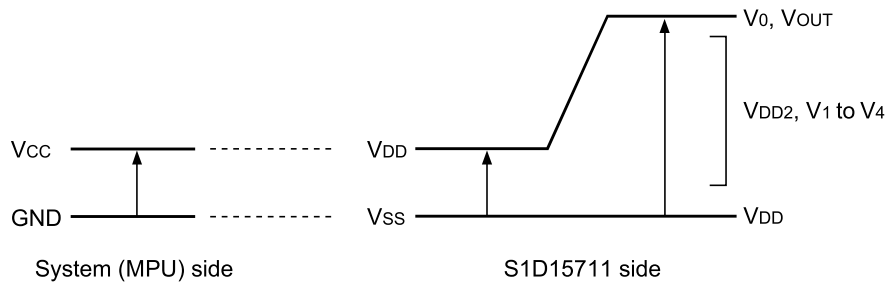


Fig. 21

- (Notes)
1. The values of the VDD2, V0 to V4, and VOUT voltages are based on VSS=0 V.
  2. The V1, V2, V3, and V4 voltages must always satisfy the condition of  $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ .
  3. Insure that voltage levels VDD2 and VOUT are always such that the relationship of  $V_{OUT} \geq V_{DD2} \geq V_{DD} \geq V_{SS}$  is maintained.
  4. When LSI is used exceeding the absolute maximum ratings, the LSI may be damaged permanently. Besides, it is desirable that the LSI should be used in the electrical characteristics condition for normal operation. If this condition is exceeded, the LSI may malfunction and have an adverse effect on the reliability of the LSI.

## 9. DC CHARACTERISTICS

Table 18

V<sub>SS</sub>=0 V, V<sub>DD</sub>=3.0 V ± 10%, and T<sub>a</sub>=-40 to +85°C

Item	Symbol	Condition	Specification value			Unit	Applicable pin	
			Min.	Typ.	Max.			
Operating voltage (1)	V <sub>DD</sub>	(Based on V <sub>SS</sub> )	1.8	—	5.5	V	V <sub>DD</sub> *1	
Operating voltage (2)	V <sub>SS2</sub>	(Based on V <sub>SS</sub> )	1.8	—	5.0		V <sub>SS2</sub>	
Operating voltage (3)	V <sub>0</sub>	(Based on V <sub>SS</sub> )	4.5	—	9.0		V <sub>0</sub> *2	
	V <sub>1</sub> , V <sub>2</sub>	(Based on V <sub>SS</sub> )	0.6×V <sub>0</sub>	—	V <sub>0</sub>		V <sub>1</sub> , V <sub>2</sub>	
	V <sub>3</sub> , V <sub>4</sub>	(Based on V <sub>SS</sub> )	V <sub>0</sub>	—	0.4×V <sub>0</sub>	V <sub>3</sub> , V <sub>4</sub>		
High level input voltage	V <sub>IHC</sub>		0.8×V <sub>DD</sub>	—	V <sub>DD</sub>	*3		
Low level input voltage	V <sub>ILC</sub>		V <sub>SS</sub>	—	0.2×V <sub>DD</sub>			
High level output voltage	V <sub>OHC</sub>	I <sub>OH</sub> =-0.5mA	0.8×V <sub>DD</sub>	—	V <sub>DD</sub>	*4		
Low level output voltage	V <sub>OLC</sub>	I <sub>OL</sub> =0.5mA	V <sub>SS</sub>	—	0.2×V <sub>DD</sub>			
Input leak current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>DD</sub> or V <sub>SS</sub>	-1.0	—	+1.0	μA	*5	
Output leak current	I <sub>LO</sub>		-3.0	—	+3.0		*6	
Liquid crystal driver On resistance	R <sub>ON</sub>	T <sub>a</sub> =25°C, V <sub>0</sub> =5V V <sub>0</sub> =7V	—	4.2	8.0	kΩ	SE <sub>Gn</sub> COM <sub>n</sub> *7	
			—	3.0	5.0			
Static current consumption	I <sub>SSQ</sub>	T <sub>a</sub> =25°C	—	0.01	5.0	μA	V <sub>SS</sub> , V <sub>SS2</sub> V <sub>0</sub>	
Output leak current	I <sub>OQ</sub>	V <sub>0</sub> =9V (Based on V <sub>DD</sub> )	—	0.01	15.0			
Input pin capacity	C <sub>IN</sub>	T <sub>a</sub> =25°C, f=1MHz	—	25	40	pF		
Oscillating frequency	Built-in oscillation	f <sub>OSC</sub>	T <sub>a</sub> =25°C	42.47	46.08	50.69	kHz	*8
	External input	f <sub>CL</sub>		4.8	5.8	6.8		CL *8

Table 19

Item	Symbol	Condition	Specification value			Unit	Applicable pin	
			Min.	Typ.	Max.			
Built-in power supply circuit	Input voltage	V <sub>SS2</sub>	At double boosting (Based on V <sub>SS</sub> )	1.8	—	5.0	V	V <sub>SS2</sub>
		V <sub>SS2</sub>	At triple boosting (Based on V <sub>SS</sub> )	1.8	—	3.3		V <sub>DD2</sub>
		V <sub>SS2</sub>	At quadruple boosting (Based on V <sub>SS</sub> )	1.8	—	2.5		V <sub>DD2</sub>
	Boosting output voltage	V <sub>OUT</sub>	(Based on V <sub>SS</sub> )	—	—	10.0	V <sub>OUT</sub>	
	Voltage adjusting circuit operating voltage	V <sub>OUT</sub>	(Based on V <sub>SS</sub> )	5.0	—	10.0	V <sub>OUT</sub>	
	V/F circuit operating voltage	V <sub>0</sub>	(Based on V <sub>SS</sub> )	4.5	—	9.0	V <sub>0</sub> *9	
Reference voltage	V <sub>REG0</sub>	T <sub>a</sub> =25°C, -0.1%/°C	1.16	1.2	1.24	*10		

[\*: see page 45.]

## S1D15711 Series

### Dynamic current consumption value (1) During display operation and built-in power supply OFF

Current values dissipated by the whole IC when the external power supply is used

Table 20 Display All White

Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15711D00B000	IDD (1)	VDD=VDD2=3.0V, V0=7.2V	—	15	30	μA	*11
		VDD=VDD2=3.0V, V0=9.0V	—	15	30		

Table 21 Display Checker Pattern

Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15711D00B000	IDD (1)	VDD=VDD2=3.0V, V0=7.2V	—	17	34	μA	*11
		VDD=VDD2=3.0V, V0=9.0V	—	18	36		

### Dynamic current consumption value (2) During display operation and built-in power supply ON

Current values dissipated by the whole IC containing the built-in power supply circuit

Table 22 Display All White

Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15711D00B000	IDD (2)	VDD=VDD2=3.3V Triple boosting, V0=7.0V	—	59	118	μA	*12

Table 23 Display Checker Pattern

Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15711D00B000	IDD (2)	VDD=VDD2=3.3V Triple boosting, V0=7.0V	—	63	126	μA	*12

### Current consumption at power save VSS=0 V and VDD=3.0 V ±10%

Table 24

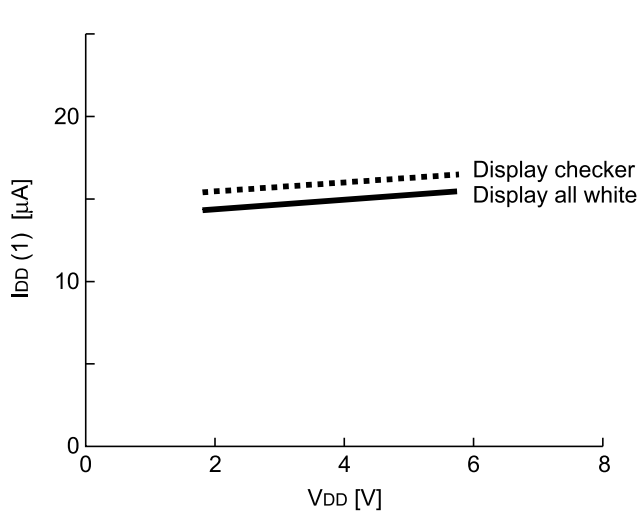
Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15711D00B000	IDDS		—	0.01	1.0	μA	

[\*: see page 45.]

[Reference data 1]

- Dynamic current consumption (1) External power supply used and LCD being displayed



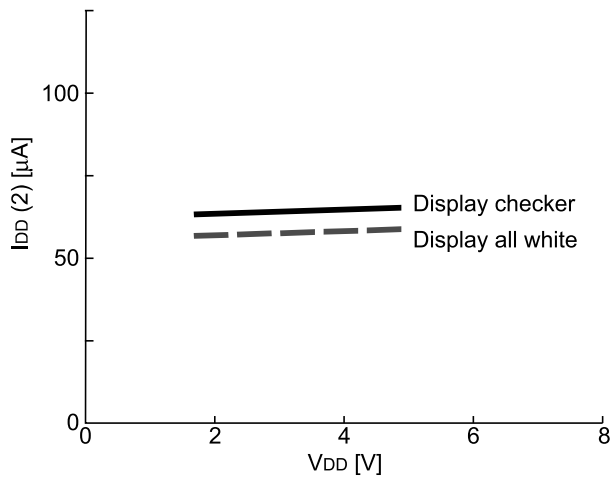
Condition: Built-in power supply OFF  
 External power supply used  
 V<sub>0</sub> = 7.2 V  
 Display pattern: All white/  
 checker  
 T<sub>a</sub> = 25°C

Remarks: \*11

Fig. 22

[Reference data 2]

- Dynamic current consumption (2) Built-in power supply used and LCD being displayed



Condition: Built-in power supply ON  
 Quadruple boosting  
 V<sub>DD2</sub> = 3.3 V  
 V<sub>0</sub> = 7.0 V  
 Display pattern: All white/  
 checker  
 T<sub>a</sub> = 25°C

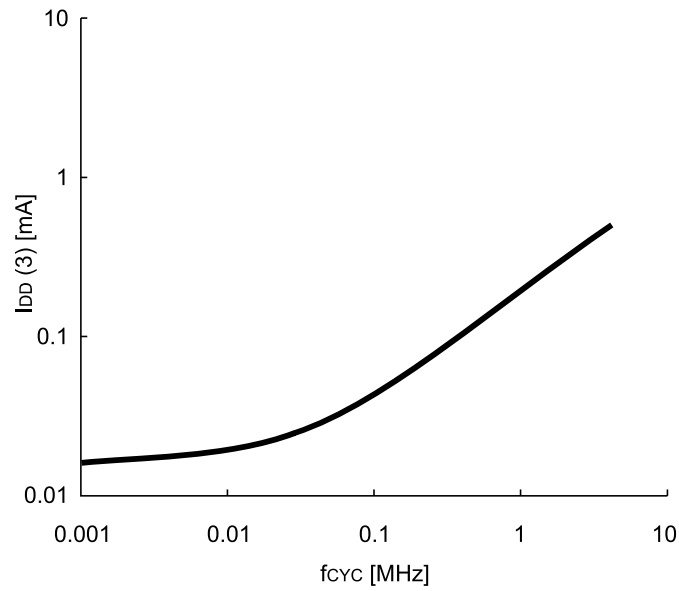
Remarks: \*12

[\*: see page 45.]

Fig. 23

[Reference data 3]

- Dynamic current consumption (3) During access



Indicates the current consumption when the checker pattern is always written at f<sub>CYC</sub>.

Only I<sub>DD</sub>(1) when not accessed

Condition: Built-in power supply OFF and external power supply used

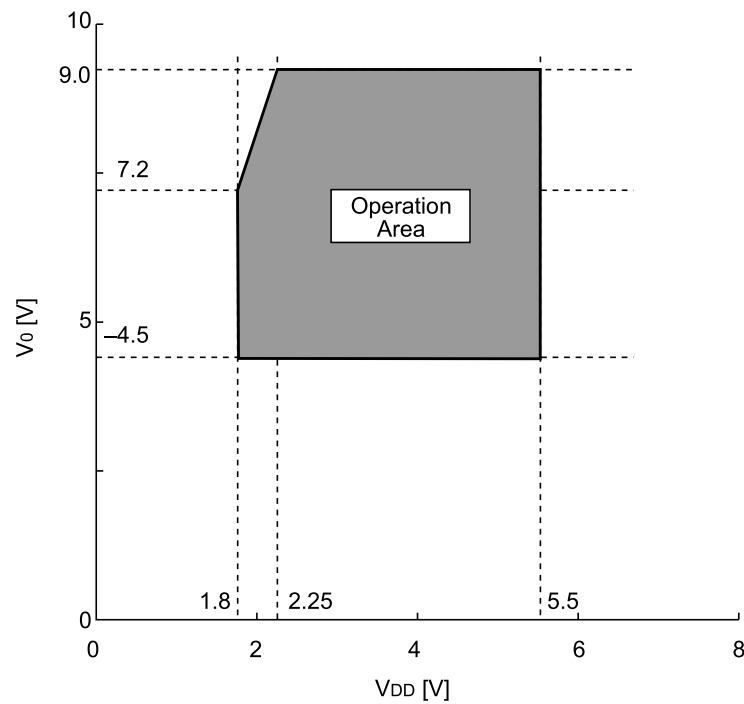
V<sub>DD</sub> = 3.0 V,

V<sub>0</sub> = 6.0 V

T<sub>a</sub> = 25°C

Fig. 24

[Reference data 4]



V<sub>DD</sub> and V<sub>0</sub> system operating voltage ranges

Remarks: \*2

[\*: see page 45.]

Fig. 25

### Relationships between the oscillating frequency $f_{OSC}$ , display clock frequency $f_{CL}$ , and liquid crystal frame frequency $f_{FR}$

Table 25

Item	$f_{CL}$	$f_{FR}$
When built-in oscillator circuit used	$\frac{f_{OSC}}{64}$	$\frac{f_{OSC}}{64 \times 9}$
When built-in oscillator circuit not used	External input ( $f_{CL}$ )	$\frac{f_{CL}}{16 \times 9}$

( $f_{FR}$  indicates the alternating current cycle of the liquid crystal and does not indicate that of the FR signal.)

[Reference items marked by \*]

- \*1 The wide operating voltage range is not warranted. However, when there is a sudden voltage change it cannot be warranted.
- \*2 For the  $V_{DD}$  and  $V_0$  operating voltage ranges, see Fig. 27. These ranges are applied when using the external power supply.
- \*3 A0, D0 to D5, D6 (SCL), D7 (SI),  $\overline{RD}$  (E),  $\overline{WR}$  (R/ $\overline{W}$ ),  $\overline{CS}$ , CL, FR, M/S, C86, P/S,  $\overline{DOF}$ , and  $\overline{RES}$  pins
- \*4 D0 to D7, FR, FRS,  $\overline{DOF}$  and CL pins
- \*5 A0,  $\overline{RD}$  (E),  $\overline{WR}$  (R/ $\overline{W}$ ),  $\overline{CS}$ , M/S, C86, P/S and  $\overline{RES}$  pins
- \*6 Applied when D0 to D5, D6 (SCL), D7 (SI), CL, FR, and  $\overline{DOF}$  pins are in the high impedance state
- \*7 Resistance value when the 0.1 V voltage is applied between the output pin SEGn or COMn and power supply pins (V1, V2, V3, and V4). Specified within the range of operating voltage (3)  
 $R_{ON} = 0.1 \text{ V} / \Delta I$  ( $\Delta I$  indicates the current applied when 0.1 V is applied between the power ON.)
- \*8 For the relationship between the oscillating frequency and frame frequency. The specification value of the external input item is a recommended value.
- \*9 The  $V_0$  voltage adjusting circuit is adjusted within the voltage follower operating voltage range.
- \*10 This is the internal voltage reference supply for the  $V_0$  voltage regulator circuit. The thermal slope  $V_{REG}$  of the S1D15711 Series is about  $-0.1\%/^{\circ}\text{C}$ .
- \*11 and \*12 Indicate the current dissipated by a single IC at built-in oscillator circuit used, 1/5 bias, and display ON.  
 Does not include the current due to the LCD panel capacity and wiring capacity.  
 Applicable only when there is no access from the MPU.
- \*12 When the  $V_0$  voltage adjusting built-in resistor is used



10. TIMING CHARACTERISTICS

(1) System bus read/write characteristics 1 (80 series MPU)

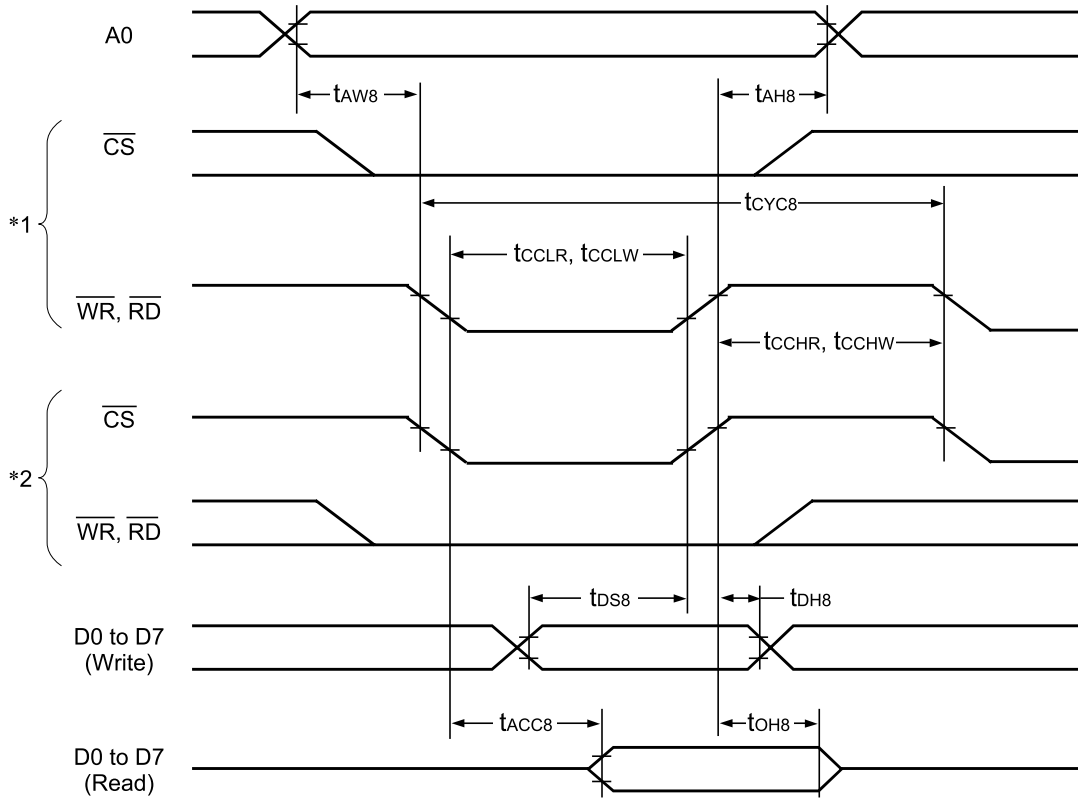


Fig. 26

Table 26

[VDD=4.5V to 5.5V, Ta=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time	A0	tAW8		0	—	
System cycle time	A0	tCYC8		300	—	
Control LOW pulse width (Write)	$\overline{WR}$	tCCLW		50	—	
Control LOW pulse width (Read)	$\overline{RD}$	tCCLR		100	—	
Control HIGH pulse width (Write)	$\overline{WR}$	tCCHW		50	—	
Control HIGH pulse width (Read)	$\overline{RD}$	tCCHR		50	—	
Data setup time	D0 to D7	tDS8		40	—	
Data hold time		tDH8		0	—	
$\overline{RD}$ access time		tACC8	CL=100pF	—	90	
Output disable time		tOH8		5	70	

Table 27

[V<sub>DD</sub>=2.7V to 4.5V, T<sub>a</sub>=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t <sub>AH8</sub>		0	—	ns
Address setup time		t <sub>AW8</sub>		0	—	
System cycle time	A0	t <sub>CYC8</sub>		500	—	
Control LOW pulse width (Write)	$\overline{WR}$	t <sub>CCLW</sub>		100	—	
Control LOW pulse width (Read)	$\overline{RD}$	t <sub>CCLR</sub>		200	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t <sub>CCHW</sub>		100	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t <sub>CCHR</sub>		100	—	
Data setup time	D0 to D7	t <sub>DS8</sub>		70	—	
Data hold time		t <sub>DH8</sub>		0	—	
$\overline{RD}$ access time		t <sub>ACC8</sub>	CL=100pF	—	180	
Output disable time		t <sub>OH8</sub>		5	100	

Table 28

[V<sub>DD</sub>=1.8V to 2.7V, T<sub>a</sub>=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t <sub>AH8</sub>		0	—	ns
Address setup time		t <sub>AW8</sub>		0	—	
System cycle time	A0	t <sub>CYC8</sub>		1000	—	
Control LOW pulse width (Write)	$\overline{WR}$	t <sub>CCLW</sub>		150	—	
Control LOW pulse width (Read)	$\overline{RD}$	t <sub>CCLR</sub>		300	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t <sub>CCHW</sub>		150	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t <sub>CCHR</sub>		150	—	
Data setup time	D0 to D7	t <sub>DS8</sub>		120	—	
Data hold time		t <sub>DH8</sub>		0	—	
$\overline{RD}$ access time		t <sub>ACC8</sub>	CL=100pF	—	260	
Output disable time		t <sub>OH8</sub>		10	200	

- \*1. This is the case of accessing by  $\overline{WR}$  and  $\overline{RD}$  when  $\overline{CS} = \text{LOW}$ .
- \*2. This is the case of accessing by  $\overline{CS}$  when  $\overline{WR}$  and  $\overline{RD} = \text{LOW}$ .
- \*3. The rise and fall times (t<sub>r</sub> and t<sub>f</sub>) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (t<sub>r</sub>+t<sub>f</sub>) ≤ (t<sub>CYC8</sub>-t<sub>CCLW</sub>-t<sub>CCHW</sub>) or (t<sub>r</sub>+t<sub>f</sub>) ≤ (t<sub>CYC8</sub>-t<sub>CCLR</sub>-t<sub>CCHR</sub>).
- \*4. All timings are specified based on the 20 and 80% of V<sub>DD</sub>.
- \*5. t<sub>CCLW</sub> and t<sub>CCLR</sub> are specified for the overlap period when  $\overline{CS}$  is at LOW level and  $\overline{WR}$ ,  $\overline{RD}$  are at the LOW level.

(2) System bus read/write characteristics 2 (68 series MPU)

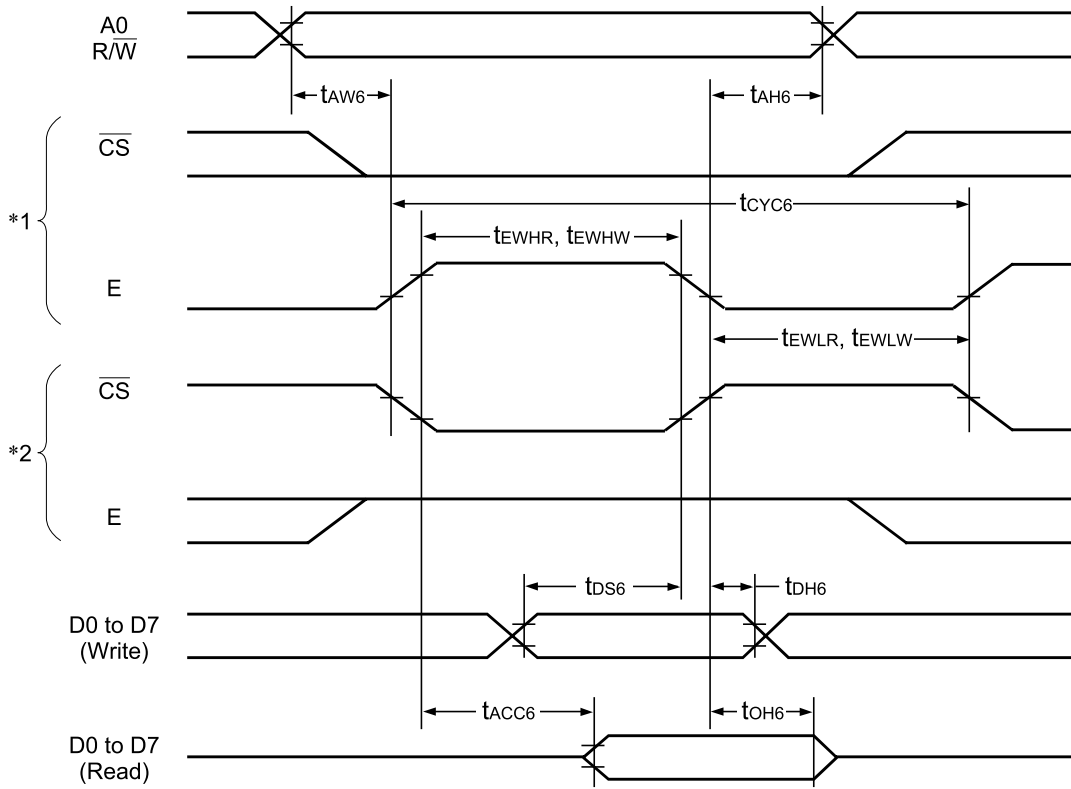


Fig. 27

Table 29

[VDD=4.5V to 5.5V, Ta=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAW6		10	—	
System cycle time		tCYC6		300	—	
Data setup time	D0 to D7	tDS6		40	—	
Data hold time		tDH6		0	—	
Access time		tACC6	CL=100pF	—	90	
Output disable time		tOH6		5	70	
Enable HIGH pulse width	Read	E	tEWHR	100	—	
	Write		tEWHW	50	—	
Enable LOW pulse width	Read	E	tEWLR	50	—	
	Write		tEWLW	50	—	

Table 30

[V<sub>DD</sub>=2.7V to 4.5V, T<sub>a</sub>=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t <sub>AH6</sub>		15	—	ns
Address setup time		t <sub>AW6</sub>		15	—	
System cycle time		t <sub>CYC6</sub>		500	—	
Data setup time	D0 to D7	t <sub>DS6</sub>		70	—	
Data hold time		t <sub>DH6</sub>		0	—	
Access time		t <sub>ACC6</sub>	CL=100pF	—	180	
Output disable time		t <sub>OH6</sub>		5	100	
Enable HIGH pulse width	Read	E	t <sub>EWHR</sub>	200	—	
	Write		t <sub>EWHW</sub>	100	—	
Enable LOW pulse width	Read	E	t <sub>EWLR</sub>	100	—	
	Write		t <sub>EWLW</sub>	100	—	

Table 31

[V<sub>DD</sub>=1.8V to 2.7V, T<sub>a</sub>=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t <sub>AH6</sub>		20	—	ns
Address setup time		t <sub>AW6</sub>		20	—	
System cycle time		t <sub>CYC6</sub>		1000	—	
Data setup time	D0 to D7	t <sub>DS6</sub>		120	—	
Data hold time		t <sub>DH6</sub>		0	—	
Access time		t <sub>ACC6</sub>	CL=100pF	—	260	
Output disable time		t <sub>OH6</sub>		10	200	
Enable HIGH pulse width	Read	E	t <sub>EWHR</sub>	300	—	
	Write		t <sub>EWHW</sub>	150	—	
Enable LOW pulse width	Read	E	t <sub>EWLR</sub>	150	—	
	Write		t <sub>EWLW</sub>	150	—	

- \*1 This is the case of accessing by E when  $\overline{CS} = \text{LOW}$ .
- \*2 This is the case of accessing by  $\overline{CS}$  when E = HIGH.
- \*3 The rise and fall times (t<sub>r</sub> and t<sub>f</sub>) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (t<sub>r</sub>+t<sub>f</sub>) ≤ (t<sub>CYC6</sub>-t<sub>EWLW</sub>-t<sub>EWHW</sub>) or (t<sub>r</sub>+t<sub>f</sub>) ≤ (t<sub>CYC6</sub>-t<sub>EWLR</sub>-t<sub>EWHR</sub>).
- \*4 All timings are specified based on the 20 and 80% of V<sub>DD</sub>.
- \*5 t<sub>EWLW</sub> and t<sub>EWLR</sub> are specified for the overlap period when  $\overline{CS}$  is at LOW level and E is at the HIGH level.

(3) Serial interface

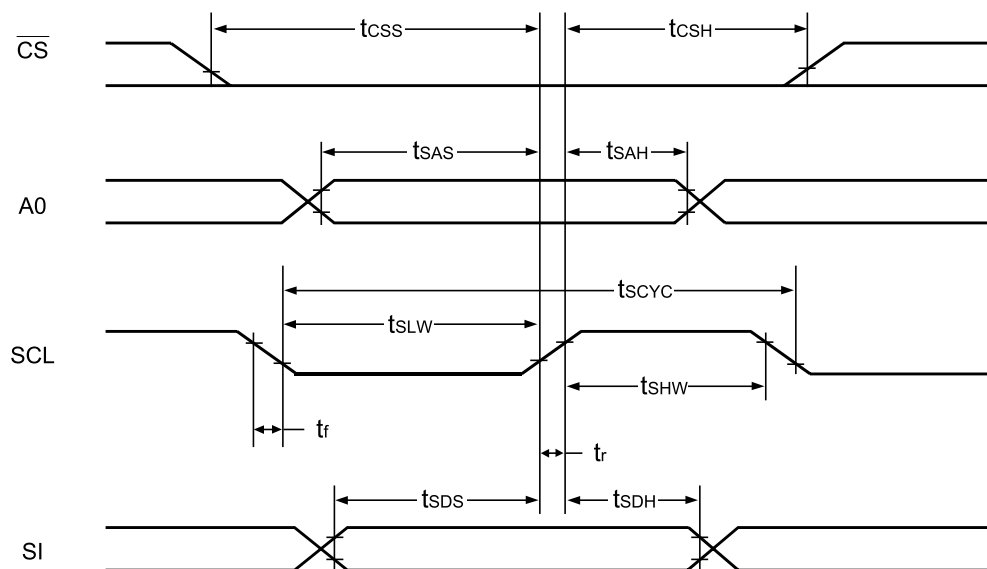


Fig. 28

Table 32

[V<sub>DD</sub>=4.5V to 5.5V, T<sub>a</sub>=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	tSCYC		120	—	ns
SCL HIGH pulse width		tSHW		40	—	
SCL LOW pulse width		tsLW		40	—	
Address setup time	A0	tsAS		50	—	
Address hold time		tsAH		50	—	
Data setup time	SI	tsDS		25	—	
Data hold time		tsDH		25	—	
CS-SCL time	CS	tcSS		50	—	
		tcSH		50	—	

Table 33

[V<sub>DD</sub>=2.7V to 4.5V, T<sub>a</sub>=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	tSCYC		150	—	ns
SCL HIGH pulse width		tSHW		50	—	
SCL LOW pulse width		tsLW		50	—	
Address setup time	A0	tsAS		75	—	
Address hold time		tsAH		75	—	
Data setup time	SI	tsDS		50	—	
Data hold time		tsDH		50	—	
CS-SCL time	CS	tcSS		75	—	
		tcSH		75	—	

Table 34

[V<sub>DD</sub>=1.8V to 2.7V, T<sub>a</sub>=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	tSCYC		200	—	ns
SCL HIGH pulse width		tSHW		75	—	
SCL LOW pulse width		tSLW		75	—	
Address setup time	A0	tsAS		75	—	
Address hold time		tsAH		75	—	
Data setup time	SI	tsDS		50	—	
Data hold time		tsDH		50	—	
CS-SCL time	CS	tcSS		100	—	
		tcSH		100	—	

\*1 The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns.

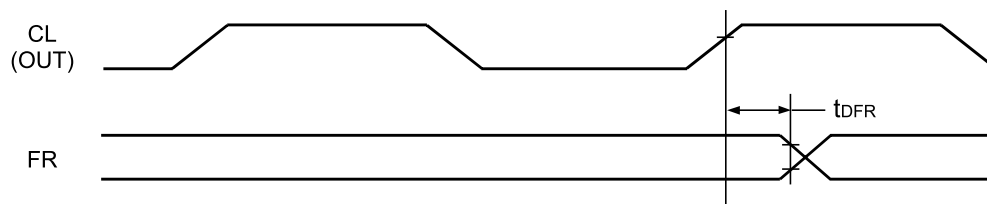
\*2 All timings are specified based on the 20 and 80% of V<sub>DD</sub>.**(4) Display control output timing**

Fig. 29

Table 35

[V<sub>DD</sub>=4.5V to 5.5V, T<sub>a</sub>=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	tDFR	CL=50pF	—	10	40	ns

Table 36

[V<sub>DD</sub>=2.7V to 4.5V, T<sub>a</sub>=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	tDFR	CL=50pF	—	20	80	ns

Table 37

[V<sub>DD</sub>=1.8V to 2.7V, T<sub>a</sub>=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	tDFR	CL=50pF	—	50	200	ns

\*1 Valid only when the master mode is selected.

\*2 All timings are specified based on the 20 and 80% of V<sub>DD</sub>.

\*3 Pay attention not to cause delays of the timing signals CL and FR to the slave side by wiring resistance, etc., while master/slave operations are in progress. If these delays occur, indication failures such as flickering may occur.

(5) Reset input timing

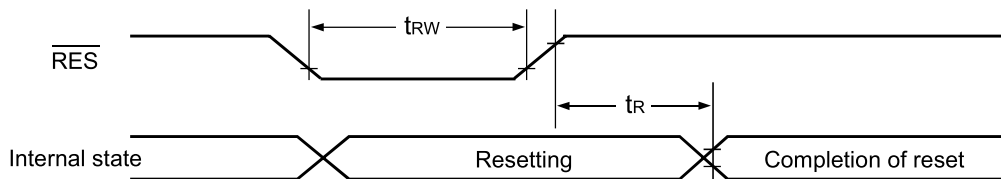


Fig. 30

Table 38

[VDD=4.5V to 5.5V, Ta=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		tR		—	—	500	μs
Reset LOW pulse width	RES	tRW		500	—	—	

Table 39

[VDD=2.7V to 4.5V, Ta=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		tR		—	—	1000	μs
Reset LOW pulse width	RES	tRW		1000	—	—	

Table 40

[VDD=1.8V to 2.7V, Ta=-40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		tR		—	—	1500	μs
Reset LOW pulse width	RES	tRW		1500	—	—	

\*1 All timings are specified based on the 20 and 80% of VDD.

## 11. MICROPROCESSOR (MPU) INTERFACE: REFERENCE

The S1D15711 Series can directly be connected to the 80 system MPU and 68 series MUP. It can also be operated with a fewer signal lines by using the serial interface.

The S1D15711 Series is used for the multiple chip configuration to expand the display area. In this case, it can select the ICs that are accessed individually using the Chip Select signal.

After the initialization using the RES pin, the respective input pins of the S1D15711 Series need to be controlled normally.

### (1) 80 series MPU

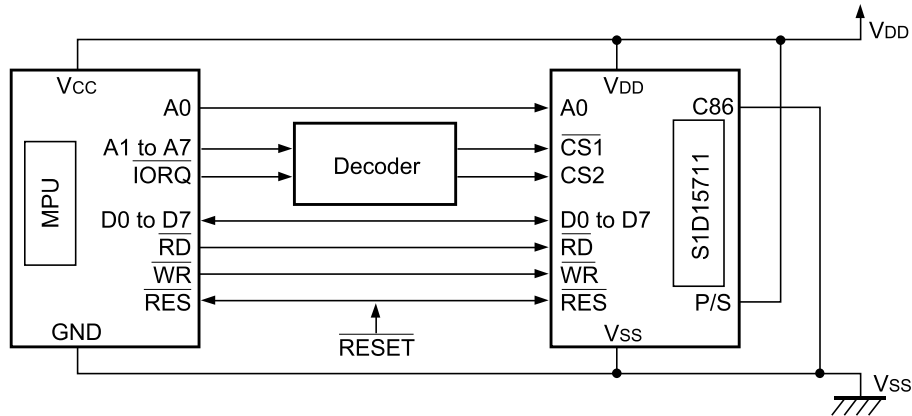


Fig. 31-1

### (2) 68 series MPU

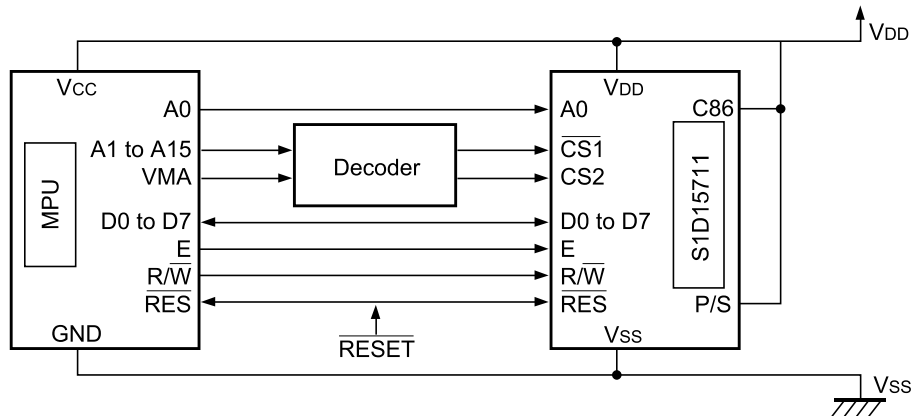


Fig. 31-2

### (3) Serial interface

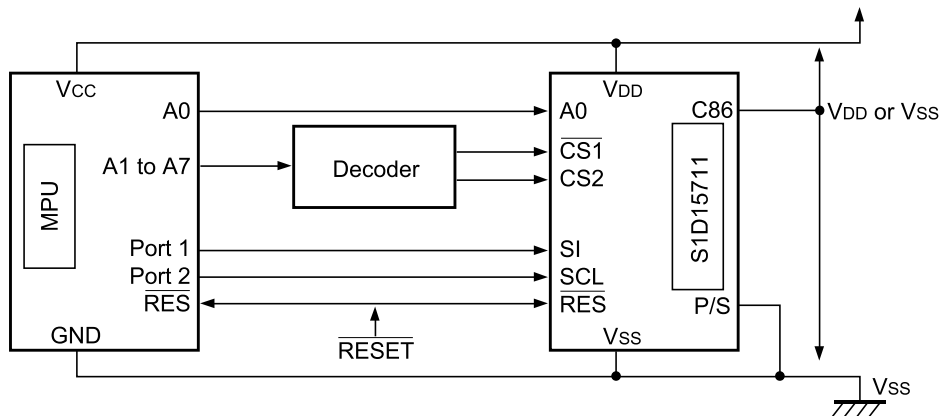


Fig. 31-3



12. CONNECTION BETWEEN LCD DRIVERS: REFERENCE

The S1D15711 Series is used for the multiple chip configuration to easily expand the liquid crystal display area. Use the same device (S1D15711\*\*\*\*/S1D15711\*\*\*\*) for the master/slave.

S1D15711(master) ↔ S1D15711(slave)

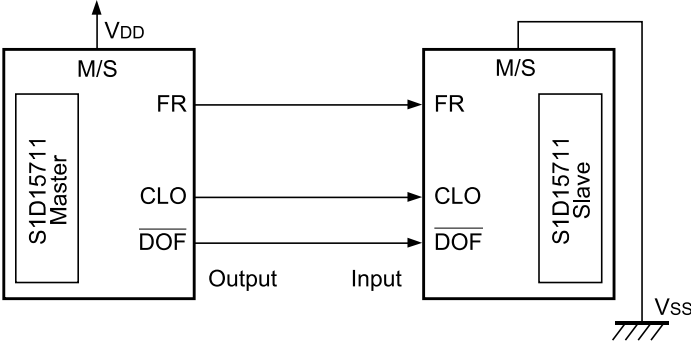


Fig. 32

### 13. LCD PANEL WIRING: REFERENCE

The S1D15711 Series is used for the multiple chip configuration to easily expand the liquid crystal display area. Use the same device (S1D15711\*\*\*\*/S1D15711\*\*\*\*) for the multiple chip configuration.

#### (1) 1-chip configuration

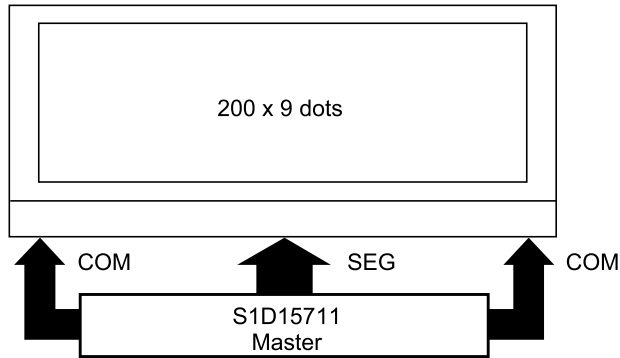


Fig. 33-1

#### (2) 2-chip configuration

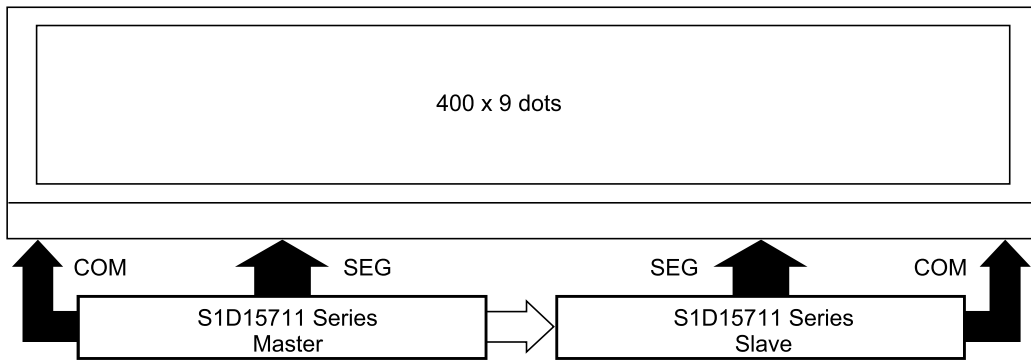


Fig. 33-2

## **14. CAUTIONS**

Cautions must be exercised on the following points when using this Development Specification:

1. This Development Specification is subject to change for engineering improvement.
2. This Development Specification does not guarantee execution of the industrial proprietary rights or other rights, or grant a license. Examples of applications described in This Development Specification are intended for your understanding of the Product. We are not responsible for any circuit problem or the like arising from the use of them.
3. Reproduction or copy of any part or whole of this Development Specification without permission of our company, or use thereof for other business purposes is strictly prohibited.

For the use of the semi-conductor,cautions must be exercised on the following points:

[Cautions against Light]

The semiconductor will be subject to changes in characteristics when light is applied. If this IC is exposed to light, operation error may occur. To protect the IC against light, the following points should be noted regarding the substrate or product where this IC is mounted:

- (1) Designing and mounting must be provided to get a structure which ensures a sufficient resistance of the IC to light in practical use.
- (2) In the inspection process, environmental configuration must be provided to ensure a sufficient resistance of the IC to light.
- (3) Means must be taken to ensure resistance to light on all the surfaces, backs and sides of the IC