EVALUATION KIT AVAILABLE

MAX14606/MAX14607

Overvoltage Protectors with Reverse Bias Blocking

General Description

The MAX14606/MAX14607 overvoltage protection devices feature low 54mΩ (typ) on-resistance (R_{ON}) internal FETs and protect low-voltage systems against voltage faults up to +36V. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components.

The devices automatically choose the accurate internal trip thresholds. The internal OVLO are preset to typical 5.87V (MAX14606) or 6.8V (MAX14607).

The MAX14606/MAX14607 feature reverse bias blocking capability. Unlike other overvoltage protectors, when the MAX14606/MAX14607 are disabled, the voltage applied to OUT does not feed back into IN. These devices also feature thermal shutdown to protect against overcurrent events.

The MAX14606/MAX14607 are specified over the extended -40°C to +85°C temperature range, and are available in 9-bump WLP packages.

Applications

Tablets

Smart Phones

Portable Media Players

***Ordering Information/Selector Guide* appears at end of data sheet.**

***Typical Operating Circuit* appears at end of data sheet.**

Visit www.maximintegrated.com/products/patents for product patent marking information.

Benefits and Features

- **Protect High-Power Portable Devices**
  - **Wide Operating Input Voltage Protection from +2.3V to +36V**
  - **3A Continuous Current Capability**
  - **Integrated 54mΩ (typ) nMOSFET Switch**
- **Flexible Overvoltage Protection Design**
  - **Easy Paralleling**
  - **$\overline{\text{ACOK}}$ Indicates Input Is in Range**
  - **Preset Accurate Internal OVLO Thresholds**
    5.87V ±3% (MAX14606)
    6.8V ±3% (MAX14607)
- **Additional Protection Features Increase System Reliability**
  - **Reverse Bias Blocking Capability**
  - **Soft-Start to Minimize Inrush Current**
  - **Internal 15ms Startup Debounce**
  - **Thermal Shutdown Protection**
- **Save Space**
  - **9-Bump, 1.3mm x 1.3mm, WLP Package**

For related parts and recommended products to use with this part, refer to: **www.maximintegrated.com/MAX14606.related**.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-6147; Rev 0; 12/11

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
IN ..... -0.3V to +40V
OUT ..... -0.3V to +40V
IN - OUT ..... -6V to +40V
$\overline{EN}$, $\overline{ACOK}$ ..... -0.3V to +6V
OVLO ..... -0.3V to +10V

Continuous Current into IN, OUT ..... ±3A
Continuous Power Dissipation (T_A = +70°C)
WLP (derate 11.9mW/°C above +70°C) 952mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... +84°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +2.3V to +36V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	V_{IN} goes from low to high, $\overline{ACOK}$ goes from high to low		2.3		36	V
Input Supply Current	I_{IN}	$\overline{EN}$ low, V_{IN} = 5V, I_{OUT} = 0mA			70	120	µA
Input Disable Current	I_{IN_DIS}	$\overline{EN}$ low, V_{IN} = 5V, V_{OVLO} < V_{OVLO_TH}			60	120	µA
Input Shutdown Current	I_{IN_Q}	$\overline{EN}$ high, V_{IN} = 5V, V_{OUT} = 0V			6	12	µA
Output Disable Current	I_{OUT_DIS}	$\overline{EN}$ low, V_{OUT} = 5V, V_{IN} = 5V, V_{OVLO} < V_{OVLO_TH} or $\overline{EN}$ low, V_{OUT} = 5V, V_{IN} > V_{IN_OVLO}				3	µA
Output Shutdown Current	I_{OUT_SD}	$\overline{EN}$ high, V_{OUT} = 5V, V_{IN} = 5V				5.5	µA
OVP (IN TO OUT)							
On-Resistance (IN to OUT)	R_{ON}	V_{IN} = 5V, I_{OUT} = 100mA			54	100	mΩ
Internal Overvoltage Lockout Threshold	V_{IN_OVLO}	IN rising	MAX14606	5.75	5.87	6.00	V
			MAX14607	6.6	6.8	7.0	
		IN falling	MAX14606	5.5			
			MAX14607	6.4			
OUT Load Capacitance	C_{OUT}					1000	µF
OVLO							
OVLO Clamp Current		V_{OVLO} = 5.5V, V_{IN} = 5V			9.7	25	µA
OVLO Open Voltage	V_{OVLO_OP}	$V_{\overline{EN}}$ = 0V			2.95	3.6	V
OVLO Pullup Resistance	R_{OVLO_PU}				500		kΩ
OVLO Force Off Voltage	V_{OVLO_TH}			0.6	1.221	1.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +2.3V to +36V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL SIGNALS ($\overline{EN}$, $\overline{ACOK}$)						
$\overline{EN}$ Input High Voltage	V_{IH}		1.4			V
$\overline{EN}$ Input Low Voltage	V_{IL}				0.4	V
$\overline{EN}$ Input Leakage Current	I_{EN_LEAK}	V_{IN_OVLO} or 5.5V	-1		+1	µA
$\overline{ACOK}$ Output Low Voltage	V_{OL}	V_{IO} = 3.3V, I_{SINK} = 1mA (see the *Typical Operating Circuit*)			0.4	V
$\overline{ACOK}$ Leakage Current	V_{ACOK_LEAK}	V_{IO} = 3.3V, $\overline{ACOK}$ deasserted (see the *Typical Operating Circuit*)	-1		+1	µA
TIMING CHARACTERISTICS						
IN Debounce Time	t_{DEB}	2.3V < V_{IN} < V_{OVLO} to charge-pump on, Figure 1	10	15	35	ms
IN/OUT OVP Soft-Start Time	t_{SS}	2.3V < V_{IN} < V_{OVLO} to 90% of V_{OUT}		30		ms
OVP Turn-On Time During Soft-Start	t_{ON}	V_{IN} = 5V, R_L = 50Ω, C_L = 10µF, V_{OUT} = 20% of V_{IN} to 80% of V_{IN}, Figure 1		2		ms
Turn-Off Time	t_{OFF}	V_{IN} > V_{OVLO} 2V/µs to V_{OUT} = 80% of V_{IN}, R_L = 50Ω, Figure 1		1.5		µs
		$\overline{EN}$ low to high to V_{OUT} = 80% of V_{IN}, R_L = 50Ω, Figure 1		84		
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			+150		°C
Thermal Hysteresis	T_{HYST}			20		°C

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

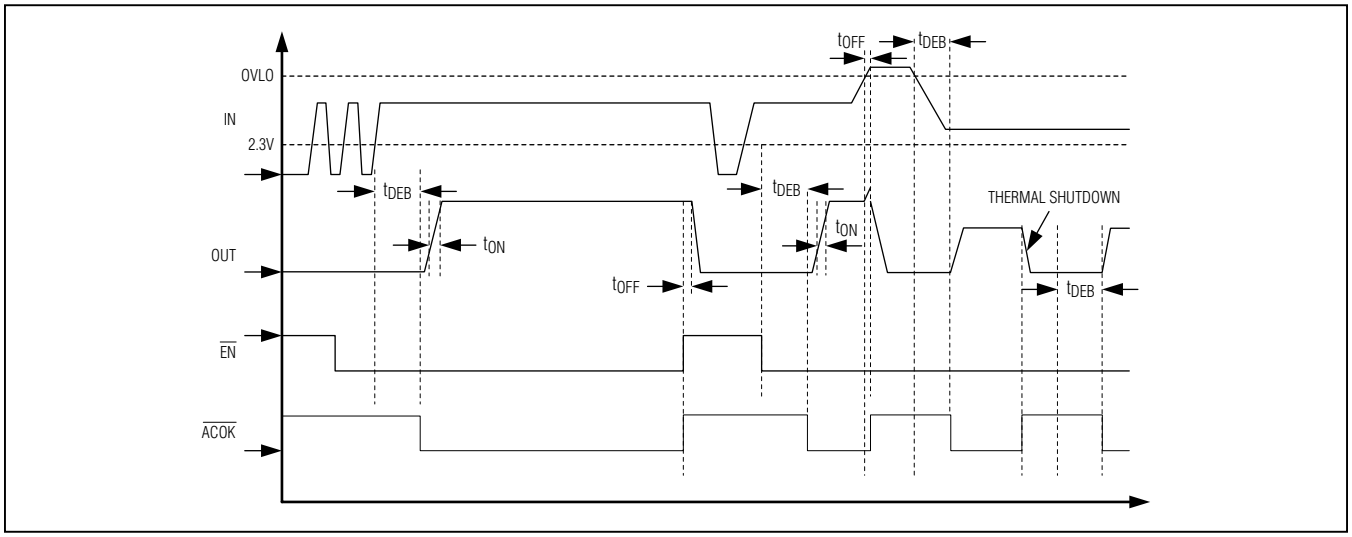
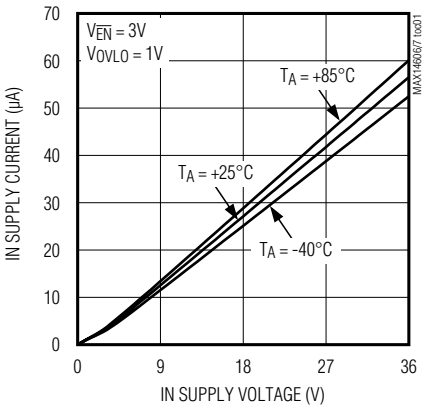


Figure 1. Timing Diagram

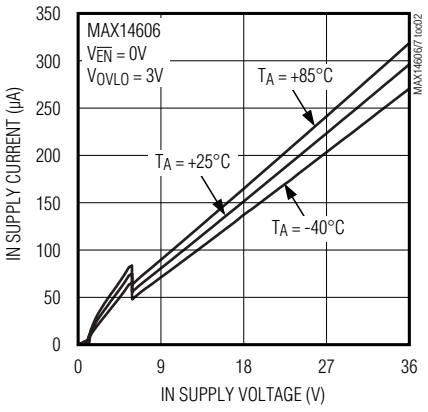
Typical Operating Characteristics

(V_{IN} = +5V, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

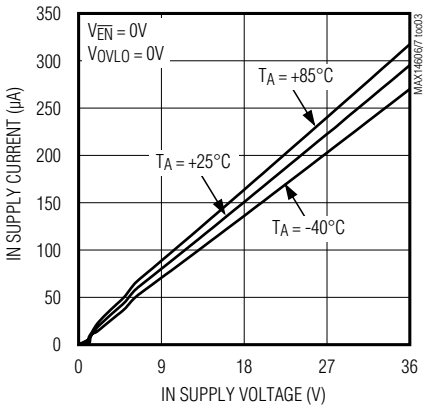
SUPPLY CURRENT vs. SUPPLY VOLTAGE



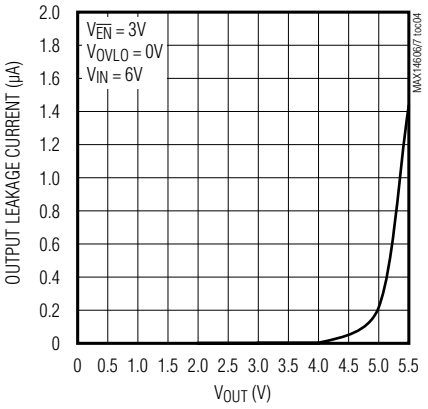
SUPPLY CURRENT vs. SUPPLY VOLTAGE



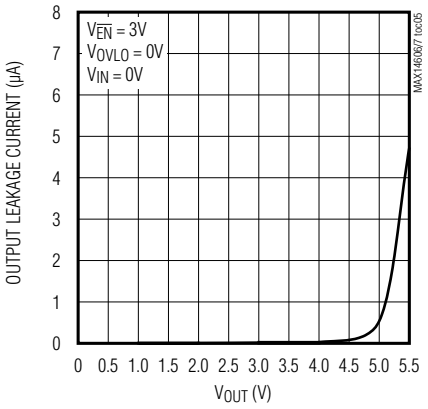
SUPPLY CURRENT vs. SUPPLY VOLTAGE



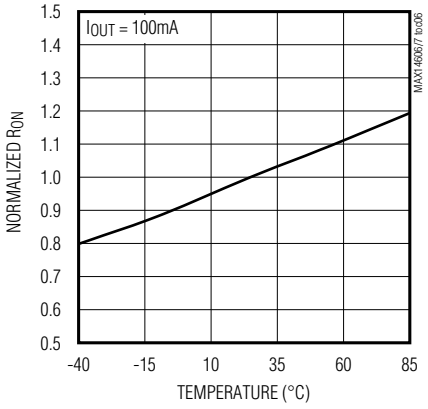
OUTPUT LEAKAGE CURRENT vs. OUTPUT VOLTAGE



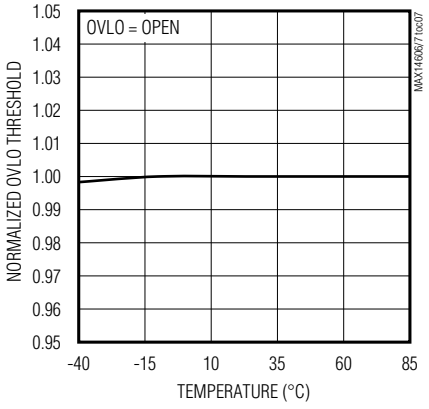
OUTPUT LEAKAGE CURRENT vs. OUTPUT VOLTAGE



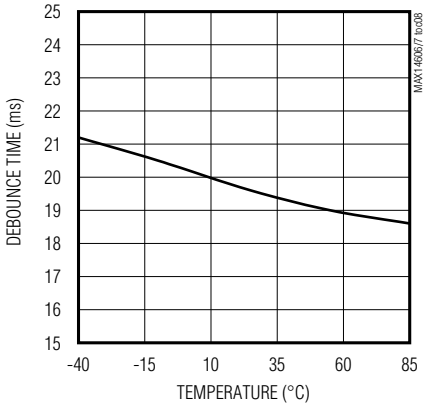
NORMALIZED R_{ON} vs. TEMPERATURE



NORMALIZED OVLO THRESHOLD vs. TEMPERATURE



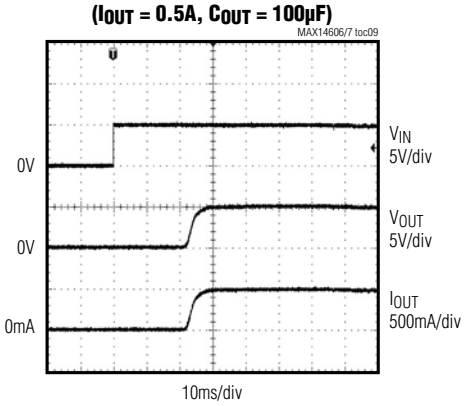
DEBOUNCE TIME vs. TEMPERATURE



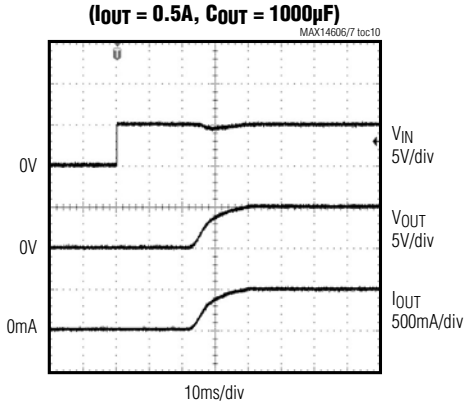
Typical Operating Characteristics (continued)

(V_{IN} = +5V, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

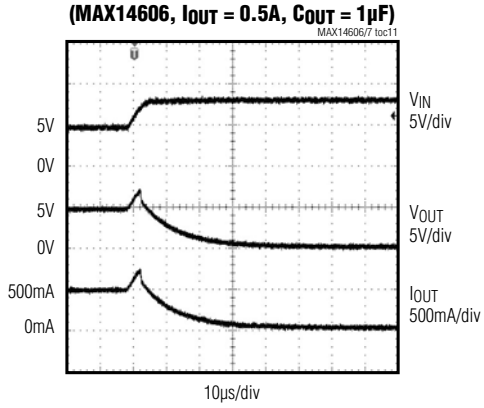
POWER-UP RESPONSE (I_{OUT} = 0.5A, C_{OUT} = 100µF)



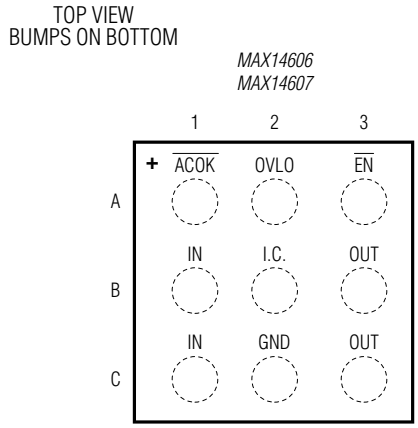
POWER-UP RESPONSE (I_{OUT} = 0.5A, C_{OUT} = 1000µF)



OVERVOLTAGE FAULT RESPONSE (MAX14606, I_{OUT} = 0.5A, C_{OUT} = 1µF)



Bump Configuration

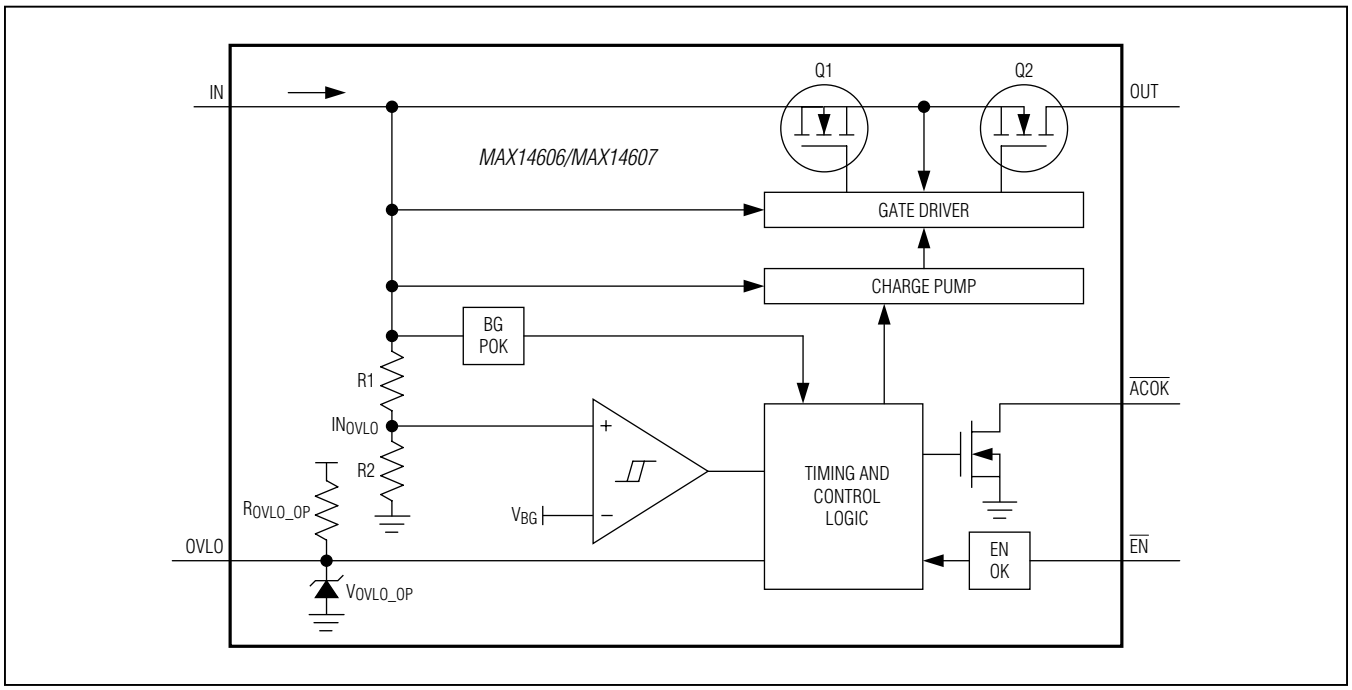


WLP

Bump Description

PIN	NAME	FUNCTION
A1	$\overline{ACOK}$	Open-Drain Flag Output. $\overline{ACOK}$ is driven low after input voltage is stable between minimum V_{IN} and V_{OVLO} after debounce. Connect a pullup resistor from $\overline{ACOK}$ to the logic I/O voltage of the host system. $\overline{ACOK}$ is high impedence after thermal shutdown.
A2	OVLO	Overvoltage Lockout Input. When forced low, it forces the pass element to be switched off. When left unconnected, the part operates normally using its internal OVLO threshold.
A3	$\overline{EN}$	Active-Low Enable Input. Drive $\overline{EN}$ low to turn on the device. Drive $\overline{EN}$ high to turn off the device.
B1, C1	IN	Overvoltage Protection Input. Bypass IN with a 1µF ceramic capacitor for high ±15kV HBM ESD protection. No capacitor is required for ±2kV HBM ESD protection. Externally connect both IN together.
B2	I.C.	Internally Connected. I.C. is internally connected to ground. Leave I.C. unconnected or connect to GND.
B3, C3	OUT	Overvoltage Protection Output. Bypass OUT with a 1µF ceramic capacitor. Externally connect both OUT together.
C2	GND	Ground

Functional Diagram



Detailed Description

The MAX14606/MAX14607 overvoltage protection (OVP) devices feature low on-resistance (R_{ON}) internal FETs (Q1+Q2) and protect low-voltage systems against voltage faults up to +36V. If the input voltage exceeds the overvoltage threshold, the output is disconnected from the input to prevent damage to the protected components. The 15ms debounce time prevents false turn-on of the internal FETs during startup.

Soft-Start

To minimize inrush current, the MAX14606/MAX14607 feature a soft-start capability to slowly turn on Q1 and Q2. Soft-start begins when $\overline{ACOK}$ is asserted and ends after 15ms (typ).

Overvoltage Lockout (OVLO)

The MAX14606/MAX14607 use the internal OVLO comparator with the internally set OVLO value. When IN goes above the overvoltage lockout threshold (V_{IN_OVLO}), OUT is disconnected from IN and $\overline{ACOK}$ is deasserted. When IN drops below V_{IN_OVLO}, the debounce time starts counting. After the debounce time, OUT follows IN again and $\overline{ACOK}$ is asserted.

There are a few options of $\overline{ACOK}$ and shutdown conditions to choose from with different OVLO and $\overline{EN}$ input combinations (Table 1). For applications that need $\overline{ACOK}$ present and OVP open, drive $\overline{EN}$ low and use OVLO as a digital input to enable and disable the OVP switch.

Table 1. Logic Input Table

OVLO \ $\overline{EN}$	LOW	HIGH
Low	OVP Disabled (Reverse Blocking Present) $\overline{ACOK}$ Present; I_{IN} = 70µA (typ)	OVP Shutdown (Reverse Blocking Present) $\overline{ACOK}$ Not Present; I_{IN} = 5µA (typ)
High	OVP Enabled $\overline{ACOK}$ Present; I_{IN} = 70µA (typ)	OVP Shutdown (Reverse Blocking Present) $\overline{ACOK}$ Not Present; I_{IN} = 5µA (typ)

Reverse Bias Blocking

When the MAX14606/MAX14607 are in overvoltage condition, $\overline{EN}$ is high, OVLO is low, or thermal shutdown is on, then the switch between IN and OUT is open and the two back-to-back diodes of the two series switches block reverse bias. Therefore, when the voltage is applied at the output, current does not travel back to the input.

Thermal Shutdown Protection

The MAX14606/MAX14607 feature thermal shutdown protection to protect the device from overheating. The device enters thermal shutdown when the junction temperature exceeds +150°C (typ), and the device is back to normal operation again after the temperature drops by approximately 20°C (typ). In thermal shutdown, the overvoltage protector is disabled and $\overline{ACOK}$ is high.

Applications Information

IN Bypass Capacitor

For most applications, it is recommended to bypass IN to GND with a 1µF, 30V ceramic capacitor as close to the device as possible to enable ±15kV HBM ESD protection on IN. In addition, observe good layout practices such as placing the bypass capacitor next to the connector. IC power and ground must also be routed from the connector to the bypass capacitor and then to the MAX14606/MAX14607. In this way, the capacitor will absorb the ESD energy and thereby protect the device from a high-voltage ESD event.

OUT Output Capacitor

The slow turn-on time provides a soft-start function that allows the devices to charge an output capacitor up to 1000µF without turning off due to an overcurrent condition.

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test methodology and results.

Human Body Model ESD Protection

Figure 2 shows the HBM, and Figure 3 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

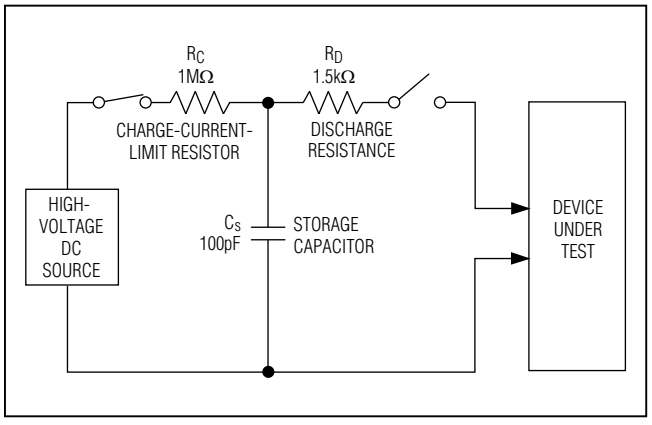


Figure 2. Human Body ESD Test Model

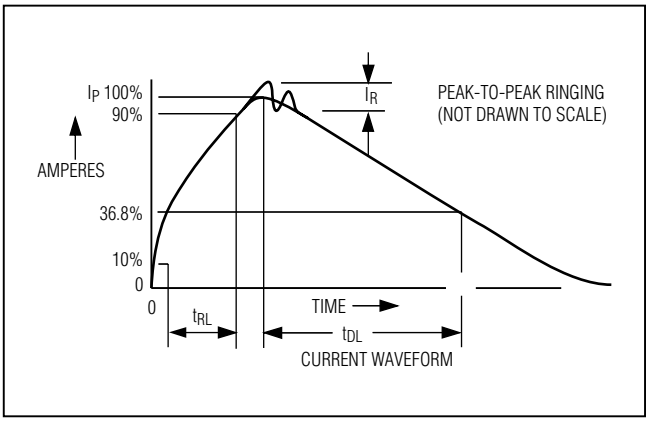
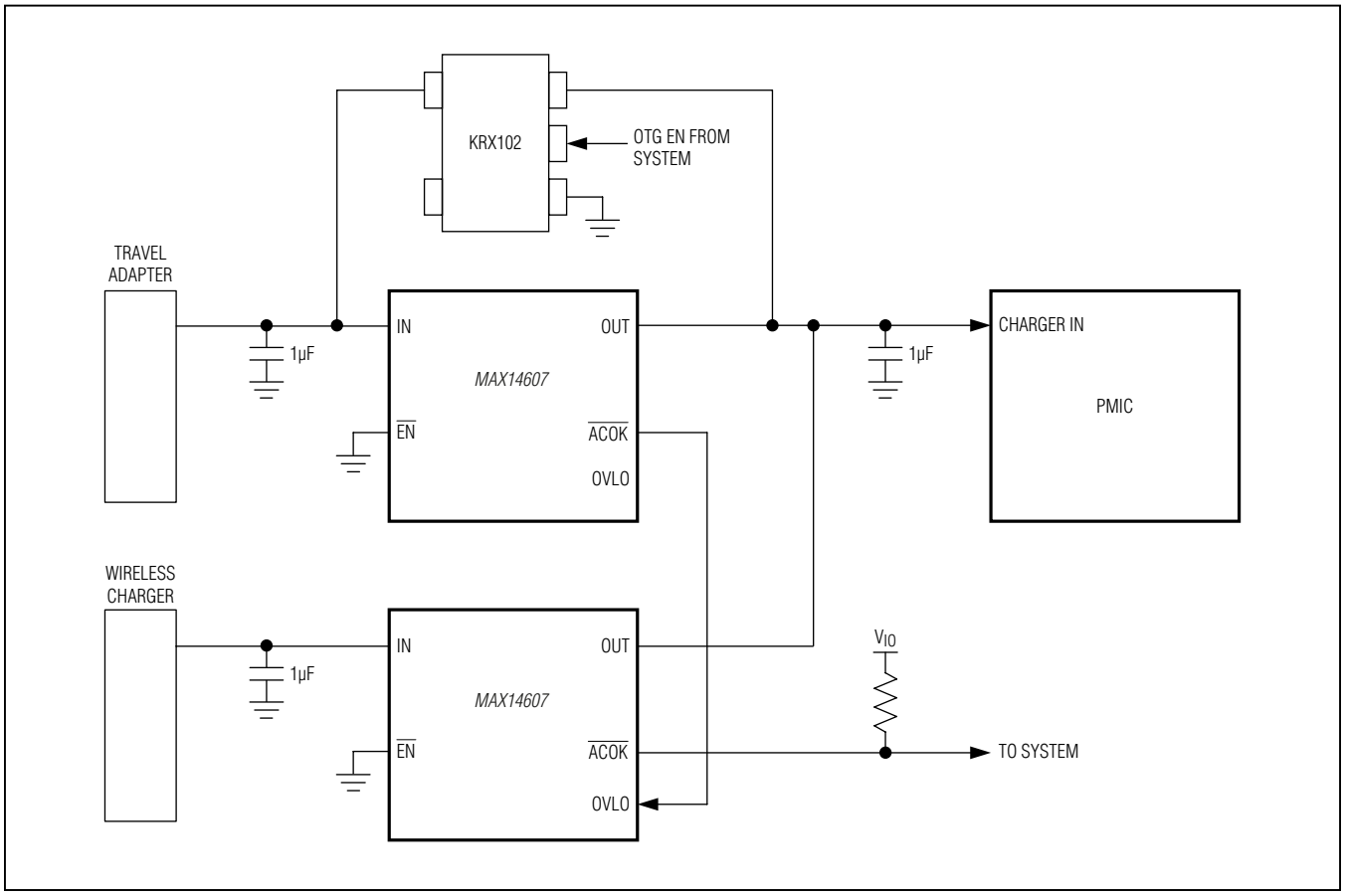


Figure 3. Human Body Current Waveform

Typical Operating Circuit



Ordering Information/Selector Guide

PART	OVLO (V)	TOP MARK	PIN-PACKAGE
MAX14606EWL+T	5.87	AJR	9 WLP
MAX14607EWL+T	6.80	AJS	9 WLP

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*
+Denotes a lead(Pb)-free package/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 WLP	W91B1+6	**21-0430**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/11	Initial release	—