19-3312; Rev 0; 7/04

EVALUATION KIT AVAILABLE

Power IC with Integrated MOSFETs for Isolated IEEE 802.3af PD and Telecom Power-Supply Applications

General Description

The MAX5074 isolated PWM power IC features integrated switching power MOSFETs connected in a voltage-clamped, two-transistor, power-circuit configuration. This device can be used in both forward and flyback configurations with a wide input voltage range from 11V to 76V and up to 15W of output power.

The voltage-clamped power topology enables full recovery of stored magnetizing and leakage inductive energy for enhanced efficiency and reliability. A look-ahead signal for driving secondary-side synchronous rectifiers can be used to increase efficiency.

A wide array of protection features includes UVLO, overtemperature shutdown, and short-circuit protection with hiccup current limit for enhanced performance and reliability. Operation up to 500kHz allows smaller external magnetics and capacitors.

The MAX5074 is rated for operation over the -40°C to +125°C temperature range and is available in a 20-pin TSSOP package.

Warning: The MAX5074 is designed to work with high voltages. Exercise caution.

Applications

IEEE 802.3af PD Power Supplies

Isolated IP Phone Power Supplies

High-Efficiency Telecom/Datacom Power Supplies

48V Input, Isolated Power-Supply Modules

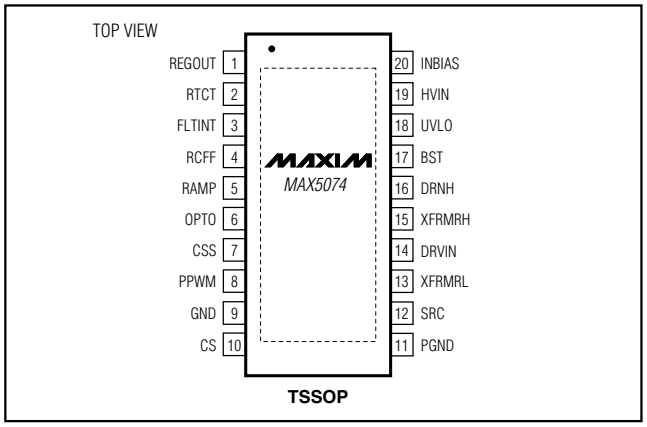
WLAN Access-Point Power Supplies

ADSL Line Cards

ADSL Line-Driver Power Supplies

Distributed Power Systems with 48V Bus

Pin Configuration



Features

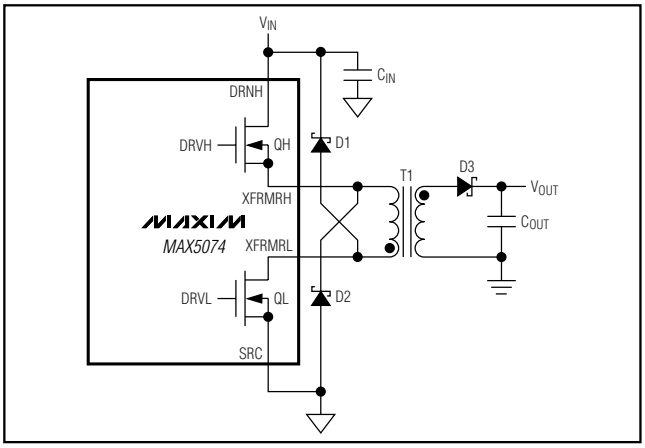
- ♦ **Clamped, Two-Switch Power IC for High Efficiency**
- ♦ **No Reset Winding Required**
- ♦ **Up to 15W Output Power**
- ♦ **Bias Voltage Regulator with Automatic High-Voltage Supply Turn-Off**
- ♦ **11V to 76V Wide Input Voltage Range**
- ♦ **Integrated High-Voltage 0.4Ω Power MOSFETs**
- ♦ **Feed-Forward Voltage-Mode Control For Fast Input Transient Rejection**
- ♦ **Programmable Brownout Undervoltage Lockout**
- ♦ **Internal Overtemperature Shutdown**
- ♦ **Indefinite Short-Circuit Protection With Programmable Fault Integration**
- ♦ **Integrated Look-Ahead Signal for Secondary-Side Synchronous Rectification**
- ♦ **>90% Efficiency with Synchronous Rectification**
- ♦ **Up to 500kHz Switching Frequency**
- ♦ **High-Power (1.74W), Small-Footprint 20-Pin Thermally Enhanced TSSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5074AUP	-40°C to +125°C	20-TSSOP-EP*

**EP = Exposed pad.*

Simplified Application Circuit



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ABSOLUTE MAXIMUM RATINGS

HVIN, INBIAS, DRNH, XFRMRH, XFRMRL to GND ..... -0.3V to +80V
BST to GND ..... -0.3V to +95V
BST to XFRMRH ..... -0.3V to +12V
PGND to GND ..... -0.3V to +0.3V
UVLO, RAMP, CSS, OPTO, FLTINT, RCFF, RTCT to GND ..... -0.3V to +12V
SRC, CS to GND ..... -0.3V to +6V
REGOUT, DRVIN to GND ..... -0.3V to +12V
REGOUT to HVIN ..... -80V to +0.3V
REGOUT to INBIAS ..... -80V to +0.3V
REGOUT Current 50mA
PPWM to GND ..... -0.3V to (REGOUT + 0.3V)
PPWM Current ..... ±20mA
DRNH, XFRMRH, XRFMRL, SRC Continuous Current (Average)
T_J = +125°C 0.9A
T_J = +150°C 0.6A
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP-EP (derate 21.7mW/°C above +70°C) 1.739W
20-Pin TSSOP-EP (θ_{JA}) ..... 46°C/W
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{HVIN} = 12V, C_{INBIAS} = 1µF, C_{REGOUT} = 2.2µF, R_{RTCT} = 25kΩ, C_{RTCT} = 100pF, C_{BST} = 0.22µF, V_{CSS} = V_{CS} = 0V, V_{RAMP} = V_{UVLO} = 3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range	V_{HVIN}		11		76	V
OSCILLATOR (RTCT)						
PWM Frequency	f_S	R_{RTCT} = 25kΩ, C_{RTCT} = 100pF		256		kHz
Maximum PWM Duty Cycle	D_{MAX}	R_{RTCT} = 25kΩ, C_{RTCT} = 100pF		47		%
Maximum RTCT Frequency	$f_{RTCTMAX}$	(Note 2)		1		MHz
RTCT Peak Trip Level	V_{TH}			0.51 x V_{REGOUT}		V
RTCT Valley Trip Level				0.04 x V_{REGOUT}		V
RTCT Input Bias Current				±1		µA
RTCT Discharge MOSFET $R_{DS(ON)}$		Sinking 20mA		30	60	Ω
RTCT Discharge Pulse Width				50		ns
LOOK-AHEAD LOGIC (PPWM)						
PPWM to XFRMRL Output Propagation Delay	t_{PPWM}	PPWM rising to XFRMRL falling		110		ns
PPWM Output High	V_{OH}	Sourcing 2mA	7.0		11.0	V
PPWM Output Low	V_{OL}	Sinking 2mA			0.4	V
PWM COMPARATOR (OPTO, RAMP, RCFF)						
Common-Mode Range	V_{CM-PWM}		0		5.5	V
Input Offset Voltage				10		mV
Input Bias Current			-2		+2	µA
RAMP to XFRMRL Propagation Delay		From RAMP (50mV overdrive) rising to XFRMRL rising		100		ns
Minimum OPTO Voltage		V_{CSS} = 0V, OPTO sinking 2mA		1.47		V
Minimum RCFF Voltage		RCFF sinking 2mA		2.18		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{HVIN} = 12V, C_{INBIAS} = 1µF, C_{REGOUT} = 2.2µF, R_{RTCT} = 25kΩ, C_{RTCT} = 100pF, C_{BST} = 0.22µF, V_{CSS} = V_{CS} = 0V, V_{RAMP} = V_{UVLO} = 3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REGOUT LDO (REGOUT)						
REGOUT Voltage Set Point	V_{REGOUT}	INBIAS floating, V_{HVIN} = 11V to 76V	8.3		9.2	V
		V_{INBIAS} = V_{HVIN} = 11V to 76V	9.5		11.0	
REGOUT Load Regulation		INBIAS floating, V_{HVIN} = 15V, I_{REGOUT} = 0 to 30mA			0.25	V
		V_{INBIAS} = V_{HVIN} = 15V, I_{REGOUT} = 0 to 30mA			0.25	
REGOUT Dropout Voltage		INBIAS floating, I_{REGOUT} = 30mA			1.25	V
		V_{INBIAS} = V_{HVIN}, I_{REGOUT} = 30mA			1.25	
REGOUT Undervoltage Lockout Threshold		REGOUT rising	6.6		7.4	V
REGOUT Undervoltage Lockout Threshold Hysteresis		REGOUT falling		0.7		V
SOFT-START (CSS)						
Soft-Start Current	I_{CSS}			33		µA
INTEGRATING FAULT PROTECTION (FLTINT)						
FLTINT Source Current	I_{FLTINT}			80		µA
FLTINT Trip Point		FLTINT rising		2.7		V
FLTINT Hysteresis				0.8		V
INTERNAL POWER MOSFETs (See Figure 1, QH and QL)						
On-Resistance	$R_{DS(ON)}$	V_{DRVIN} = V_{BST} = 9V, V_{XFRMRH} = V_{SRC} = 0V, I_{DS} = 50mA		0.4	0.8	Ω
Off-State Leakage Current			-5		+5	µA
Total Gate Charge Per FET				15		nC
HIGH-SIDE DRIVER						
Low-to-High Delay		Driver delay until FET V_{GS} reaches 0.9 x (V_{BST} - V_{XFRMRH}) and is fully on		80		ns
High-to-Low Delay		Driver delay until FET V_{GS} reaches 0.1 x (V_{BST} - V_{XFRMRH}) and is fully off		40		ns
Driver Output Voltage		BST to XFRMRH with high side on		8		V
LOW-SIDE DRIVER						
Low-to-High Delay		Driver delay until FET V_{GS} reaches 0.9 x V_{DRVIN} and is fully on		80		ns
High-to-Low Delay		Driver delay until FET V_{GS} reaches 0.1 x V_{DRVIN} and is fully off		40		ns
CURRENT-LIMIT COMPARATOR (CS)						
Current-Limit Threshold Voltage	V_{ILIM}		140	156	172	mV
Current-Limit Input Bias Current	I_{BILIM}	0 < V_{CS} < 0.3V	-2		+2	µA

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ELECTRICAL CHARACTERISTICS (continued)

(V_{HVIN} = 12V, C_{INBIAS} = 1µF, C_{REGOUT} = 2.2µF, R_{RTCT} = 25kΩ, C_{RTCT} = 100pF, C_{BST} = 0.22µF, V_{CSS} = V_{CS} = 0V, V_{RAMP} = V_{UVLO} = 3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

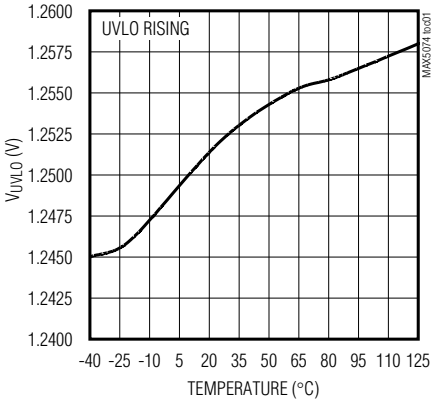
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to XFRMRL	t_{dILIM}	From CS rising (10mV overdrive) to XFRMRL rising		160		ns
BOOST VOLTAGE CIRCUIT (See Figure 1, QB)						
Driver Output Delay	t_{PPWMD}			200		ns
One-Shot Pulse Width	t_{PWQB}			300		ns
QB $R_{DS(ON)}$		Sinking 20mA		30	60	Ω
THERMAL SHUTDOWN						
Shutdown Temperature	T_{SH}	Temperature rising		+160		°C
Thermal Hysteresis	T_{HYST}			15		°C
UNDERVOLTAGE LOCKOUT (UVLO)						
UVLO Threshold	V_{UVLO}	V_{UVLO} rising	1.14		1.38	V
UVLO Hysteresis	V_{HYST}			140		mV
UVLO Input Bias Current	I_{BUVLO}	V_{UVLO} = 3V	-100		+100	nA
SUPPLY CURRENT						
Supply Current		From V_{HVIN} = 11V to 76V, V_{CSS} = 0V, V_{INBIAS} = 11V		0.7	2	mA
		From V_{INBIAS} = 11V to 76V, V_{CSS} = 0V, V_{HVIN} = 76V		4.4	6.0	
		From V_{HVIN} = 76V		7		
Standby Supply Current		V_{UVLO} = 0V			1	mA

Note 1: All limits at -40°C are guaranteed by design and not production tested.
Note 2: Output switching frequency is half of oscillator frequency.

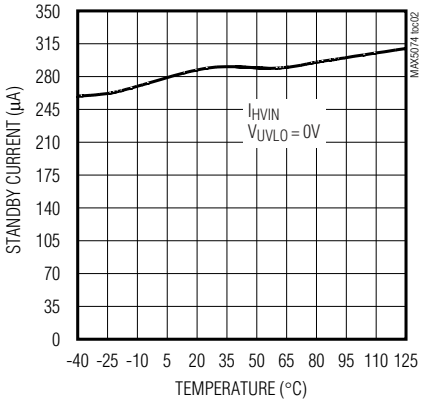
Typical Operating Characteristics

(V_{HVIN} = 48V, V_{INBIAS} = 15V, C_{INBIAS} = 1µF, C_{REGOUT} = 2.2µF, R_{RTCT} = 25kΩ, C_{RTCT} = 100pF, C_{BST} = 0.22µF, V_{CSS} = V_{CS} = 0V, V_{RAMP} = V_{UVLO} = 3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

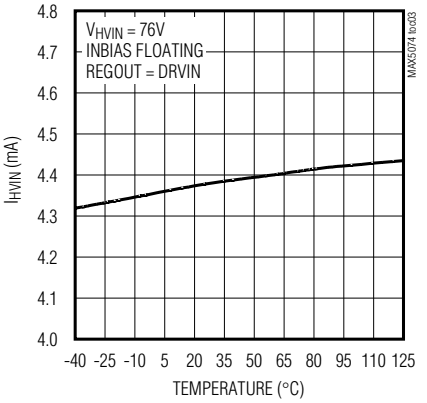
UNDERVOLTAGE LOCKOUT THRESHOLD vs. TEMPERATURE



STANDBY CURRENT vs. TEMPERATURE



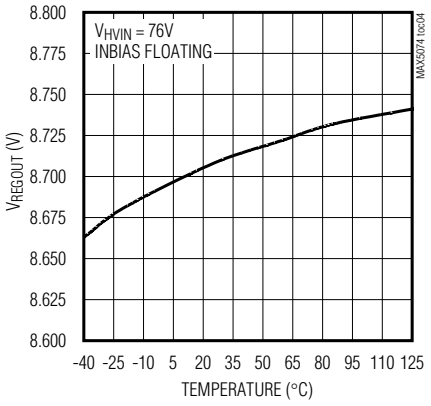
HVIN INPUT CURRENT vs. TEMPERATURE



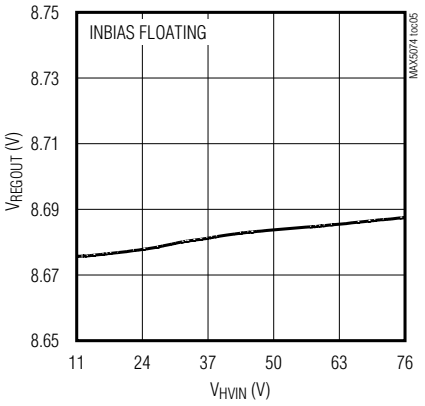
Typical Operating Characteristics (continued)

(V_{HVIN} = 48V, V_{INBIAS} = 15V, C_{INBIAS} = 1µF, C_{REGOUT} = 2.2µF, R_{RTCT} = 25kΩ, C_{RTCT} = 100pF, C_{BST} = 0.22µF, V_{CSS} = V_{CS} = 0V, V_{RAMP} = V_{UVLO} = 3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

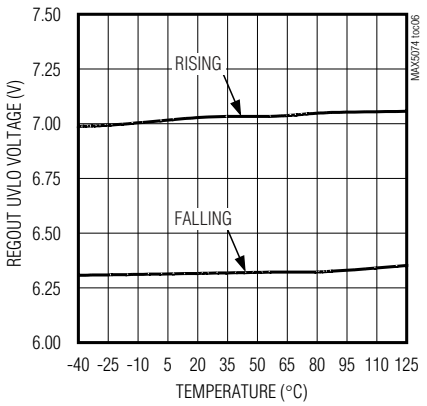
REGOUT VOLTAGE vs. TEMPERATURE



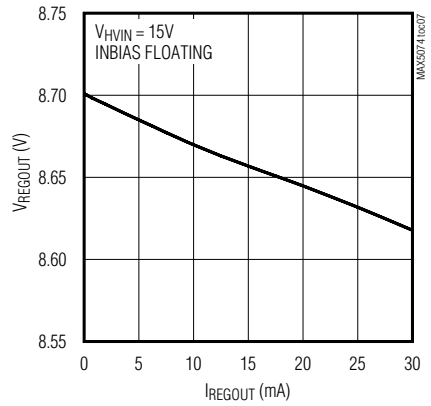
REGOUT VOLTAGE vs. INPUT VOLTAGE



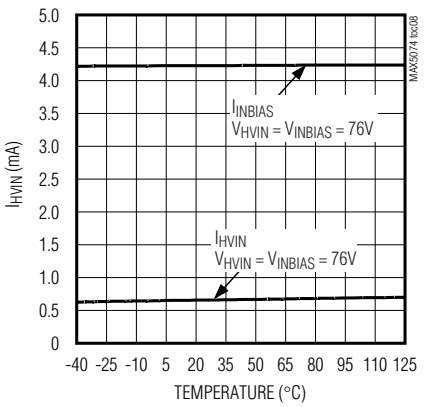
REGOUT UVLO VOLTAGE vs. TEMPERATURE



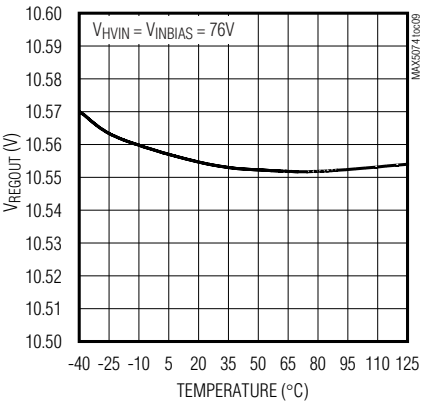
REGOUT VOLTAGE vs. LOAD CURRENT



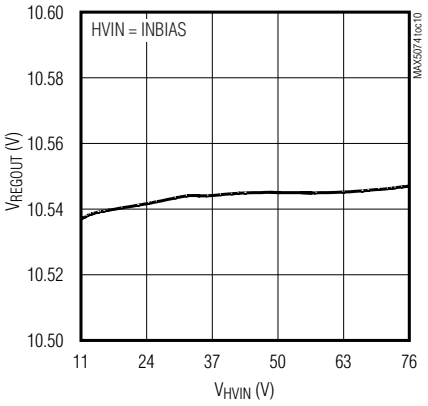
HVIN AND INBIAS INPUT CURRENT vs. TEMPERATURE



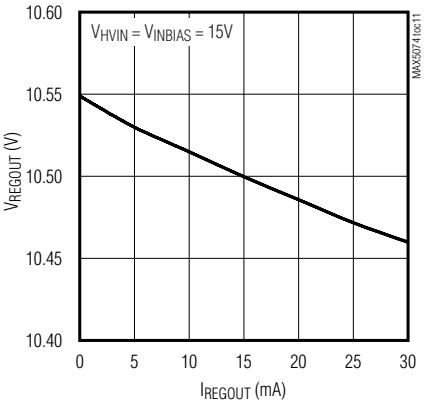
REGOUT VOLTAGE vs. TEMPERATURE



REGOUT VOLTAGE vs. INPUT VOLTAGE



REGOUT VOLTAGE vs. LOAD CURRENT



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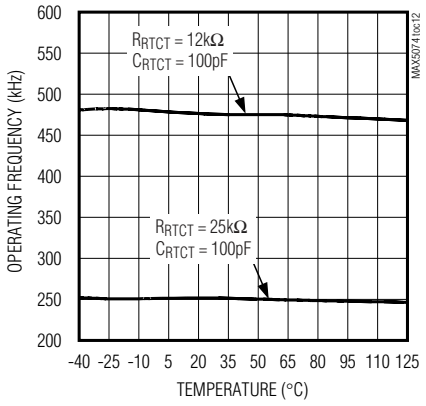
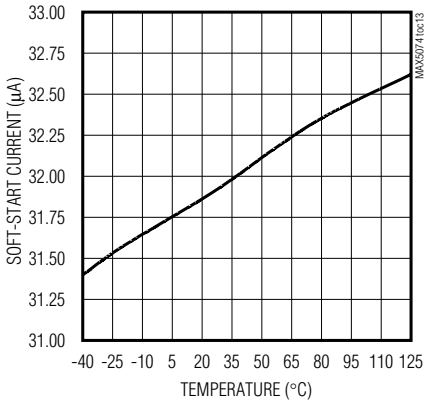
Typical Operating Characteristics (continued)

(V_{HVIN} = 48V, V_{INBIAS} = 15V, C_{INBIAS} = 1µF, C_{REGOUT} = 2.2µF, R_{RTCT} = 25kΩ, C_{RTCT} = 100pF, C_{BST} = 0.22µF, V_{CSS} = V_{CS} = 0V, V_{RAMP} = V_{UVLO} = 3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

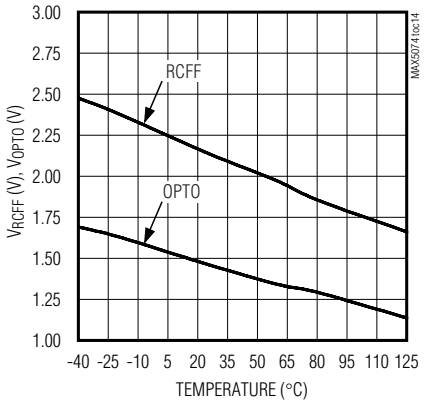
OPERATING FREQUENCY vs. TEMPERATURE



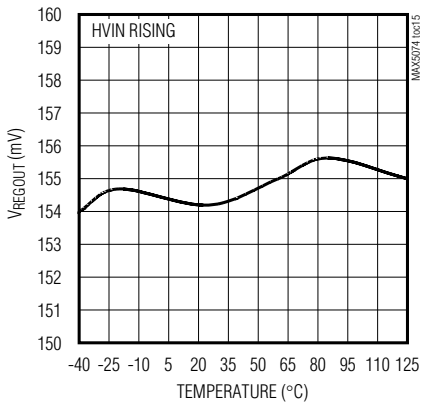
SOFT-START CURRENT vs. TEMPERATURE



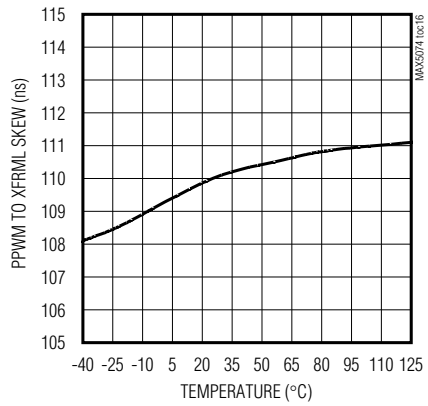
MINIMUM RCFF AND OPTO LEVELS vs. TEMPERATURE



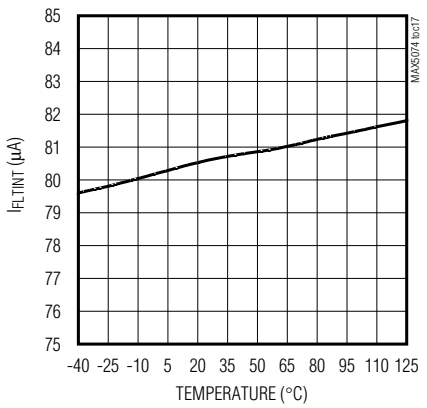
CURRENT-LIMIT COMPARATOR THRESHOLD vs. TEMPERATURE



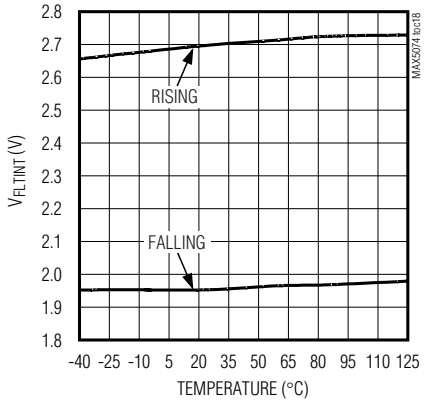
PPWM TO XFRMRL SKEW vs. TEMPERATURE



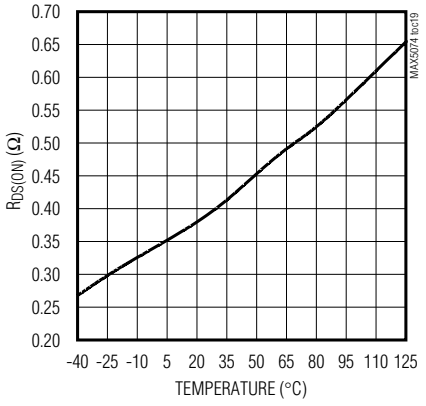
FLTINT CURRENT vs. TEMPERATURE



FLTINT SHUTDOWN VOLTAGE vs. TEMPERATURE



POWER MOSFETS $R_{DS(ON)}$ vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	REGOUT	Regulator Output. Always present as long as HVIN is powered with a voltage above UVLO threshold. Bypass REGOUT to GND with a minimum 2.2µF ceramic capacitor.
2	RTCT	Oscillator Frequency Set Input. Connect a resistor from RTCT to REGOUT and a capacitor from RTCT to GND to set the oscillator frequency.
3	FLTINT	Fault Integration Input. During persistent current-limit faults, a capacitor connected to FLTINT is charged with an internal 80µA current source. Switching is terminated when V_{FLTINT} reaches 2.7V. An external resistor connected in parallel discharges the capacitor. Switching resumes when V_{FLTINT} drops to 1.9V.
4	RCFF	Feed-Forward Input. To generate the PWM ramp, connect a resistor from RCFF to HVIN and a capacitor from RCFF to GND.
5	RAMP	PWM Ramp Sense Input. Connect RAMP to RCFF.
6	OPTO	PWM Comparator Inverting Input. Connect the collector of the optotransistor to OPTO and a pullup resistor to REGOUT.
7	CSS	Soft-Start and Reference. Connect a 10nF or greater capacitor from CSS to GND.
8	PPWM	PWM Pulse Output. PPWM leads the internal power MOSFET pulse by approximately 100ns.
9	GND	Signal Ground. Connect GND to PGND.
10	CS	Current-Sense Input. The current-limit threshold is internally set to 156mV relative to PGND. The device has an internal noise filter. If necessary, connect an external RC filter for additional filtering.
11	PGND	Power Ground. Connect PGND to GND.
12	SRC	Internal Low-Side Power MOSFET Source. Connect SRC to PGND with a low-value resistor for current limiting.
13	XFRMRL	Low-Side Connection for the Isolation Transformer
14	DRVIN	MOSFET Gate-Driver Supply Input. Bypass DRVIN with at least 0.1µF to PGND. Connect DRVIN to REGOUT.
15	XFRMRH	High-Side Connection for the Isolation Transformer
16	DRNH	Drain Connection of the Internal High-Side PWM Power MOSFET. Connect DRNH to the most positive rail of the input supply. Bypass DRNH appropriately to handle the heavy switching current through the transformer.
17	BST	Boost Input. BST is the boost connection point for the high-side MOSFET driver. Connect a minimum 0.1µF capacitor from BST to XFRMRH with short and wide PC board traces.
18	UVLO	Undervoltage Lockout Input. Connect a resistive divider from HVIN to UVLO and from UVLO to GND to set the UVLO threshold.
19	HVIN	High-Voltage Input. Connect HVIN to the most positive input supply rail.
20	INBIAS	Input from the Rectified Bias Winding. INBIAS is an input to the internal linear voltage regulator (REGOUT).
—	EP	Exposed Paddle. EP is internally connected to GND. Connect the exposed paddle to a copper pad to improve power dissipation.

Power IC with Integrated MOSFETs for Isolated IEEE 802.3af PD and Telecom Power-Supply Applications

Detailed Description

The MAX5074 PWM power IC is the primary-side controller for voltage-mode, isolated forward or flyback power converters. This device provides a high degree of integration aimed at reducing the cost and printed circuit board area of isolated output power supplies. Use the MAX5074 primarily in 48V power bus applications.

The MAX5074 is a complete power IC capable of delivering up to 15W of output power. This device contains PWM circuitry and integrated power MOSFETs. Figure 1 shows the MAX5074's block diagram. The MAX5074 includes undervoltage lockout, overtemperature shutdown, and short-circuit protection for enhanced performance and reliability. Operation up to 500kHz allows the use of small external magnetics and capacitors.

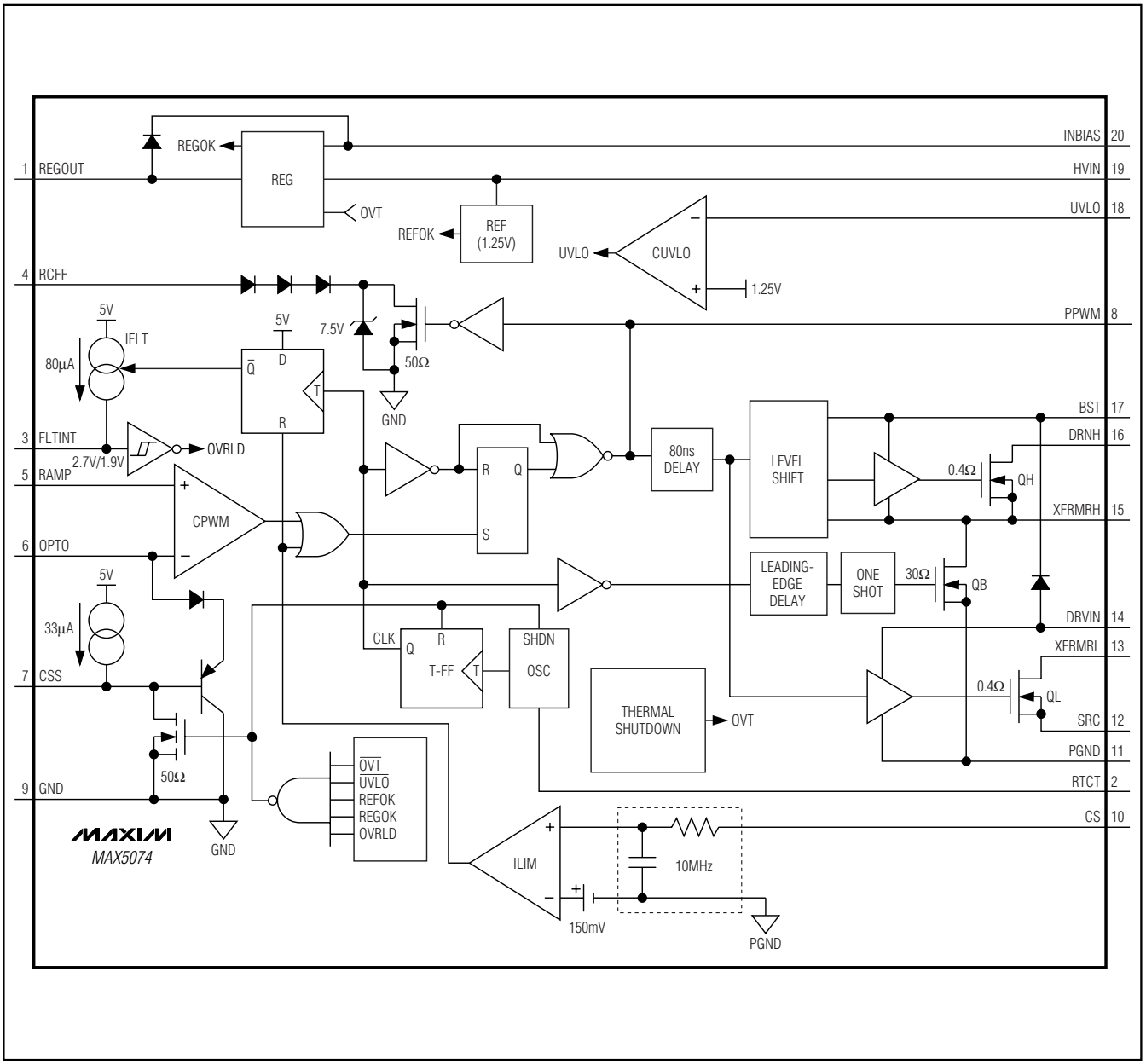


Figure 1. Block Diagram

Power IC with Integrated MOSFETs for Isolated IEEE 802.3af PD and Telecom Power-Supply Applications

Power Topology

The two-switch forward converter topology offers outstanding robustness against faults and transformer saturation while affording efficient use of the integrated 0.4Ω power MOSFETs. Voltage-mode control with feed-forward compensation allows the rejection of input supply disturbances within a single cycle similar to that of current-mode controlled topologies.

The two-switch power topology recovers energy stored in both the magnetizing and the parasitic leakage inductances of the transformer. The *Typical Application Circuit*, forward converter (Figure 3) shows the schematic diagram of a 48V input and 5V, 3A output isolated power supply. Figure 4 shows the schematic diagram of a flyback converter using the MAX5074.

Undervoltage Lockout (UVLO)

The UVLO block monitors the input voltage HVIN through an external resistive divider (R24 and R25) connected to UVLO (see Figure 3). Use the following equation to calculate R24 and R25:

$$V_{UVLOIN} = V_{UVLO} \times \left(1 + \frac{R24}{R25}\right)$$

where V_{UVLOIN} is the desired input voltage lockout level and V_{UVLO} is the undervoltage lockout threshold (1.25V, typ).

Internal Regulators

As soon as power is provided to HVIN, internal power supplies power the UVLO detection circuitry. REGOUT is used to drive the internal power MOSFETs. Bypass REGOUT with a minimum 2.2µF ceramic capacitor. The HVIN LDO steps down V_{HVIN} to a nominal output voltage (REGOUT) of 8.75V. A second parallel LDO powers REGOUT from INBIAS. A tertiary winding connected through a diode to INBIAS powers up REGOUT once switching commences. This will bring REGOUT to 10.5V (typ) and shut off the current flowing from HVIN to REGOUT. This results in a lower on-chip power dissipation and higher efficiency.

Soft-Start

Program the MAX5074 soft-start with an external capacitor between CSS and GND. When the device turns on, the soft-start capacitor (C_{CSS}) charges with a constant current of 33µA, ramping up to 7.3V. During this time, the feedback pin (OPTO) is clamped to V_{CSS} + 0.6V. This initially holds the duty cycle lower than the value the regulator tries to impose, thus preventing voltage overshoot at the output. When the MAX5074 turns off, the soft-start capacitor internally discharges to GND.

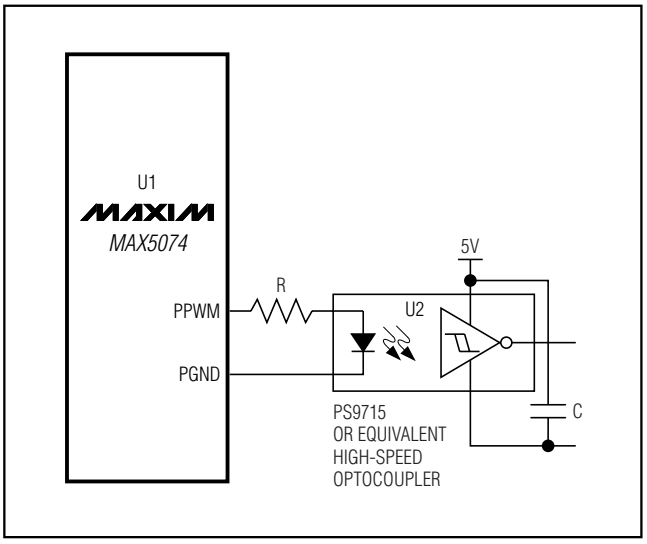


Figure 2. Secondary-Side Synchronous Rectifier Driver Using a High-Speed Optocoupler

Secondary-Side Synchronization

The MAX5074 provides convenient synchronization for optional secondary-side synchronous rectifiers. Figure 2 shows the connection diagram with a high-speed optocoupler. Choose an optocoupler with a propagation delay of less than 80ns. The synchronizing pulse is generated approximately 110ns ahead of the main pulse that drives the two power MOSFETs.

Voltage-Mode Control and the PWM Ramp

For voltage-mode control, the feed-forward PWM ramp is generated at RCFF. From RCFF, connect a capacitor to GND and a resistor to HVIN. The ramp generated is applied to the noninverting input of the PWM comparator at RAMP and has a minimum voltage of approximately 2V. The slope of the ramp is determined by the voltage at HVIN and affects the overall loop gain. The ramp peak must remain below the dynamic range of RCFF of 5.5V. Assuming the maximum duty cycle approaches 50% at a minimum input voltage (PWM UVLO turn-on threshold), use the following formula to calculate the minimum value of either the ramp capacitor or resistor:

$$R_{RCFF}C_{RCFF} \geq \frac{V_{UVLOIN}}{2f_S V_{R(P-P)}}$$

where f_S is the switching frequency, $V_{R(P-P)}$ is the peak-to-peak ramp voltage (2V, typ).

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Maximize the signal-to-noise ratio by setting the ramp peak as high as possible. Calculate the low-frequency, small-signal gain of the power stage (the gain from the inverting input of the PWM comparator to the output) using the following formula:

$$G_{PS} = N_{SP} \times R_{RCFF} \times C_{RCFF} \times f_S$$

where N_{SP} is the secondary to primary power transformer turns ratio.

Oscillator

The MAX5074 oscillator is externally programmable through a resistor connected from RTCT to REGOUT and a capacitor connected from RTCT to GND. The PWM frequency will be 1/2 the frequency at RTCT with a 50% duty cycle. Use the following formula to calculate the oscillator components:

$$R_{RTCT} \cong \frac{1}{2f_S(C_{RTCT} + C_{PCB})\ln\left(\frac{V_{REGOUT}}{V_{REGOUT} - V_{TH}}\right)}$$

where C_{PCB} is the stray capacitance on the PC board (14pF, typ), V_{TH} is the RTCT peak trip level, and f_S is the switching frequency.

Integrating Fault Protection

The integrating fault protection feature allows the MAX5074 to ignore transient overcurrent conditions for a programmable amount of time, giving the power supply time to behave like a current source to the load. This can happen, for example, under load-current transients when the control loop requests maximum current to keep the output voltage from going out of regulation. Program the ignore time externally by connecting a capacitor to FLTINT. Under sustained overcurrent faults, the voltage across this capacitor ramps up toward the FLTINT shutdown threshold (typically 2.7V). When FLTINT reaches the threshold, the power supply shuts down. A high-value bleed resistor connected in parallel with the FLTINT capacitor allows the capacitor to discharge toward the restart threshold (typically 1.9V). Crossing the restart threshold soft-starts the supply again.

The ILIM comparator provides cycle-by-cycle current limiting with a typical threshold of 156mV. The fault integration circuit works by forcing an 80µA current into FLTINT for one clock every time the current-limit comparator ILIM (Figure 1) trips. Use the following formula to calculate the approximate capacitor needed for the desired shutdown time:

$$C_{FLTINT} \cong \frac{I_{FLTINT} t_{SH}}{1.4}$$

where I_{FLTINT} is typically 80µA, and t_{SH} is the desired ignore time during which current-limit events from the current-limit comparator are ignored.

This is an approximate formula; some testing may be required to fine tune the actual value of the capacitor.

Calculate the approximate bleed resistor needed for the desired recovery time using the following formula:

$$R_{FLTINT} \cong \frac{t_{RT}}{C_{FLTINT}\ln\left(\frac{2.7}{1.9}\right)}$$

where t_{RT} is the desired recovery time.

Choose at least $t_{RT} = 10 \times t_{SH}$. Typical values for t_{SH} range from a few hundred microseconds to a few milliseconds.

Shutdown

Shut down the MAX5074 by driving UVLO to GND using an open-collector or open-drain transistor connected to GND. The IC will be internally shut down if REGOUT is below its UVLO level. The MAX5074 also features internal thermal shutdown using a temperature sensor that monitors the high-power area. A thermal fault arises from excessive dissipation in the power MOSFETs or in the regulator. When the temperature limit is reached (+160°C), the temperature sensor terminates switching and shuts down the regulator. The integration of thermal shutdown and the power MOSFETs results in a very robust power circuit.

Applications Information

Isolated Telecom Power Supply

Figure 3 shows a typical application circuit of an isolated power supply with a 30V to 60V input. This power supply is fully protected and can sustain a continuous short circuit at its output terminals.

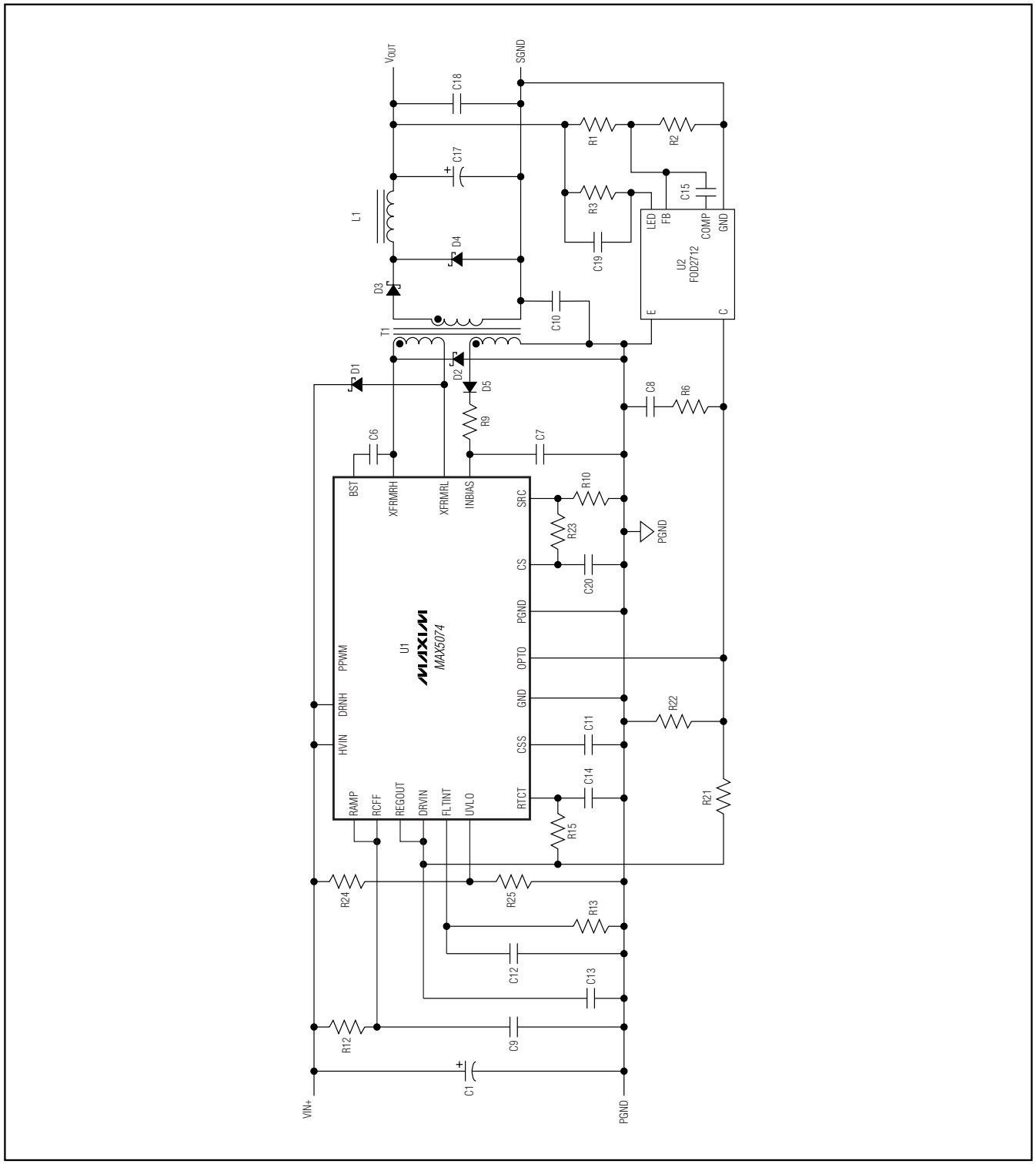

Figure 3. Typical Application Circuit (48V Power Supply, Evaluation Kit Available)

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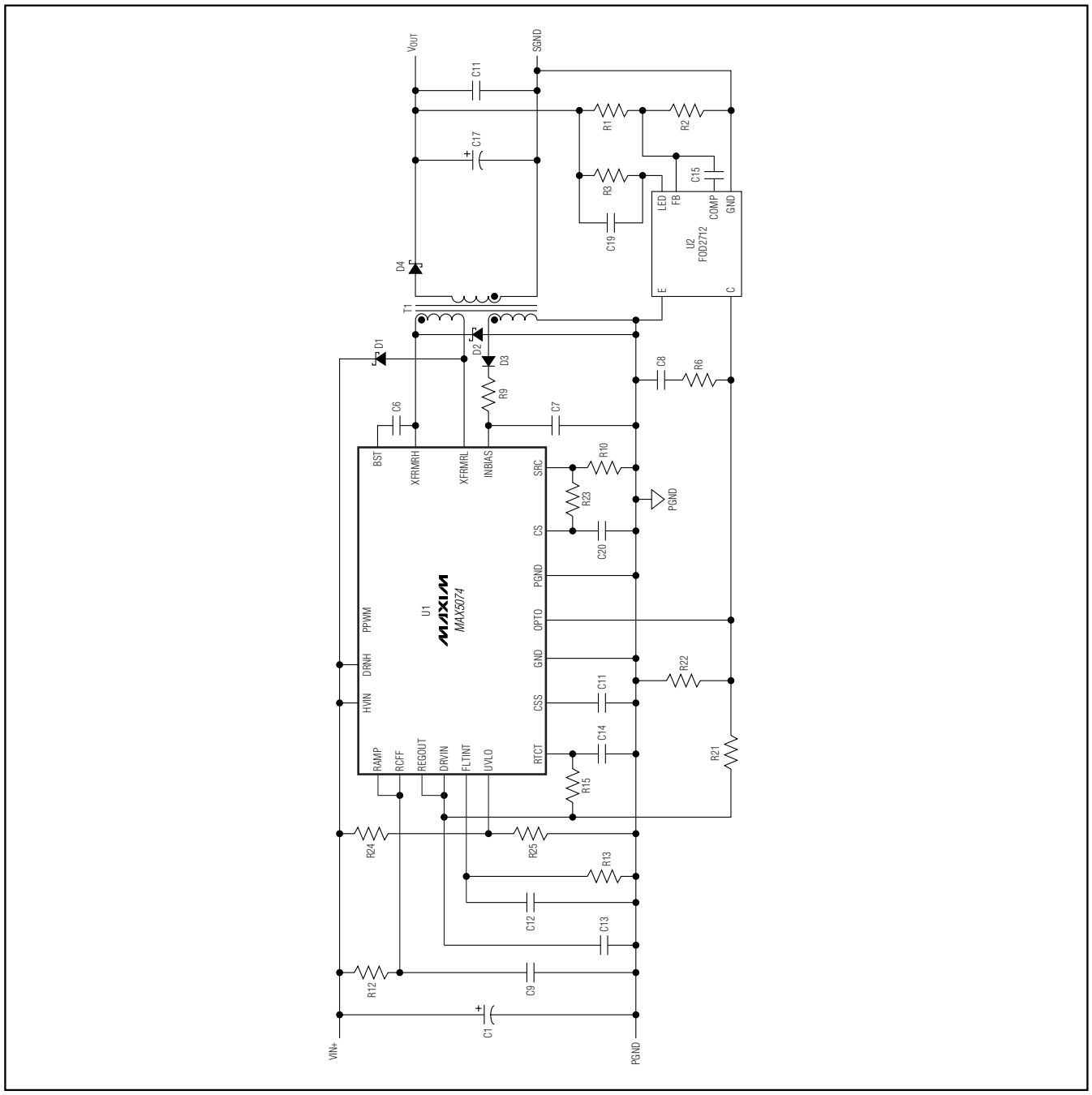


Figure 4. For lower power applications, the MAX5074 can be used in a flyback converter configuration. This eliminates the need for an output inductor and simplifies the design of multiple output power supplies.

Chip Information

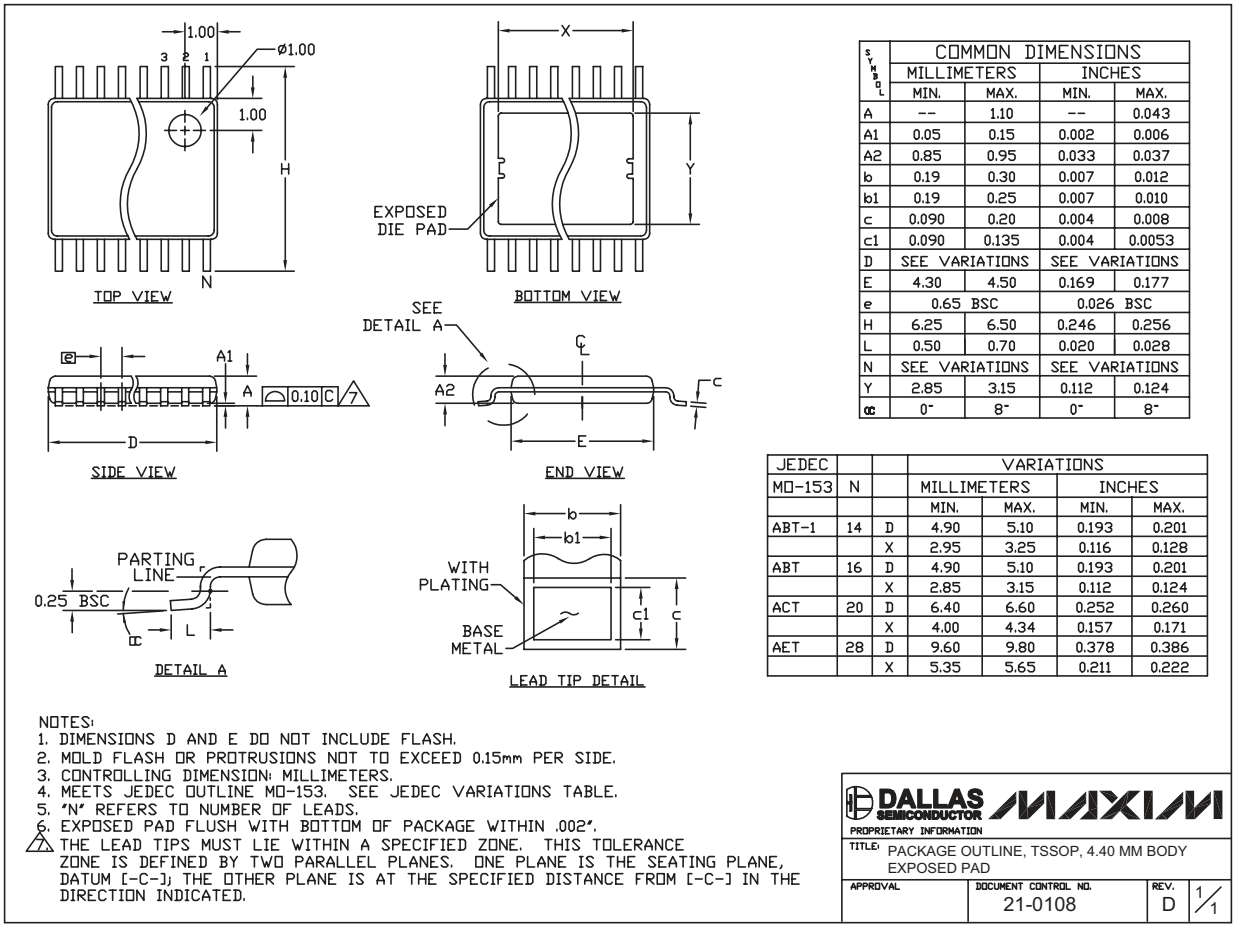
TRANSISTOR COUNT: 7043

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP 4.4mm BODY.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	--	1.10	--	0.043
A1	0.05	0.15	0.002	0.006
A2	0.85	0.95	0.033	0.037
b	0.19	0.30	0.007	0.012
b1	0.19	0.25	0.007	0.010
c	0.090	0.20	0.004	0.008
c1	0.090	0.135	0.004	0.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	0.112	0.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT-1	14	D	4.90	5.10	0.193	0.201
		X	2.95	3.25	0.116	0.128
ABT	16	D	4.90	5.10	0.193	0.201
		X	2.85	3.15	0.112	0.124
ACT	20	D	6.40	6.60	0.252	0.260
		X	4.00	4.34	0.157	0.171
AET	28	D	9.60	9.80	0.378	0.386
		X	5.35	5.65	0.211	0.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0108	D	1/1