MOSFET – N-Channel, QFET®

1000 V, 1.6 A, 9 Ω

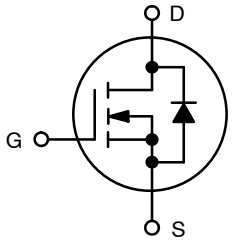
FQU2N100, FQD2N100

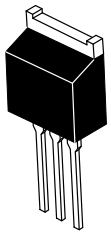
This N−Channel enhancement mode power MOSFET is produced using **onsemi**'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on−state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

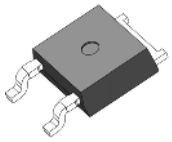
- 1.6 A, 1000 V, $R_{DS(on)}$ = 9 Ω (Max.) @ V_{GS} = 10 V, I_D = 0.8 A
- Low Gate Charge (Typ. 12 nC)
- Low Crss (Typ. 5 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free, Halid Free and are RoHS Compliant

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
1000 V	9 Ω @ 10 V	1.6 A





DPAK3 (IPAK)
CASE 369AR



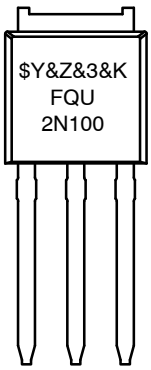
DPAK3 (TO−252 3 LD)
CASE 369AS

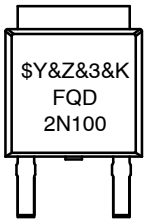
MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	1000	V
Drain Current − Continuous (T_C = 25°C) − Continuous (T_C = 100°C)	I_D	1.6 1.0	A
Drain Current − Pulsed (Note 1)	I_{DM}	6.4	A
Gate−Source Voltage	V_{GSS}	±30	V
Single Pulsed Avalanche Energy (Note 2)	E_{AS}	160	mJ
Avalanche Current (Note 1)	I_{AR}	1.6	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	5.0	mJ
Peak Diode Recovery dv/dt (Note 3)	dv/dt	5.5	V/ns
Power Dissipation (T_A = 25°C) *	P_D	2.5	W
Power Dissipation (T_C = 25°C) − Derate above 25°C		50 0.4	W W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	−55 to +150	°C
Maximum Lead Temperature for Soldering Purposes, 1/8" (from case for 5 seconds)	T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAMS





FQU2N100,
FQD2N100 = Device Code
$Y = **onsemi** Logo
&Z = Assembly Location
&3 = 3−Digit Date Code
&K = 2−Digits Lot Run Traceability Code

ORDERING INFORMATION

Device	Package	Shipping†
FQU2N100TU	DPAK3 (IPAK) (Pb−Free)	70 Units / Tube
FQD2N100TM	DPAK3 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case, Max.	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (minimum pad of 2 oz copper) , Max.	110	°C/W
	Thermal Resistance, Junction−to−Ambient (* 1 in2 pad of 2 oz copper), Max.	50	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	1000	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.976	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 1000 V, V_{GS} = 0 V	–	–	10	μA
		V_{DS} = 800 V, T_C = 125°C	–	–	100	
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = −30 V, V_{DS} = 0 V	–	–	−100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain−Source On Resistance	V_{GS} = 10 V, I_D = 0.8 A	–	7.1	9	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 0.8 A	–	1.9	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	400	520	pF
C_{oss}	Output Capacitance		–	40	52	
C_{rss}	Reverse Transfer Capacitance		–	5	6.5	
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 500 V, I_D = 2.0 A, R_G = 25 Ω (Note 4)	–	13	35	ns
t_r	Turn−On Rise Time		–	30	70	
$t_{d(off)}$	Turn−Off Delay Time		–	25	60	
t_f	Turn−Off Fall Time		–	35	80	
Q_g	Total Gate Charge	V_{DS} = 800 V, I_D = 2.0 A, V_{GS} = 10 V (Note 4)	–	12	15.5	nC
Q_{gs}	Gate−Source Charge		–	2.5	–	
Q_{gd}	Gate−Drain Charge		–	6.5	–	
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	1.5	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	6.0	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.6 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 2.0 A, dI_F/dt = 100 A/μs	–	520	–	ns
Q_{rr}	Reverse Recovery Charge		–	2.3	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. L = 120 mH, I_{AS} = 1.6 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25°C.
3. I_{SD} ≤ 2.0 A, di/dt ≤ 300A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C.
4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

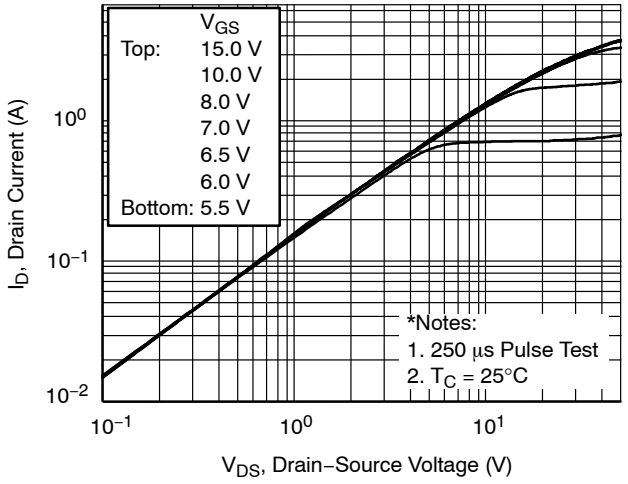


Figure 1. On−Region Characteristics

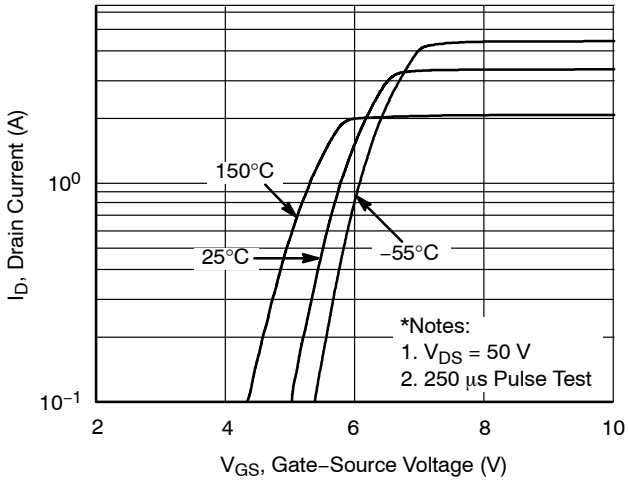


Figure 2. Transfer Characteristics

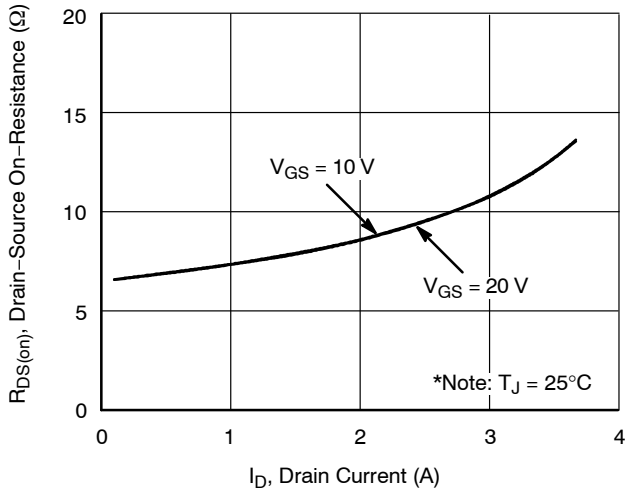


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

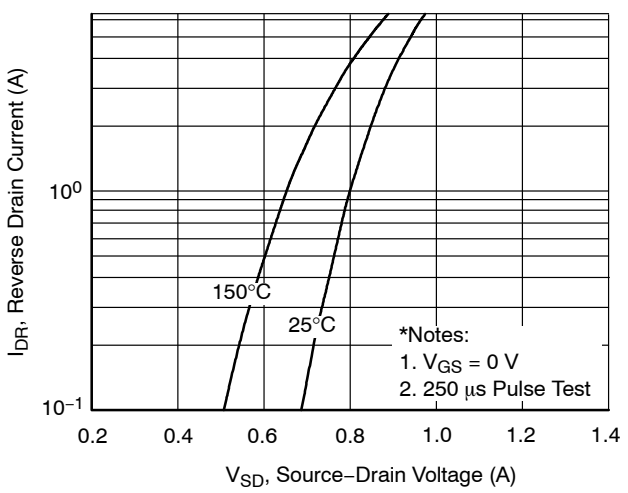


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

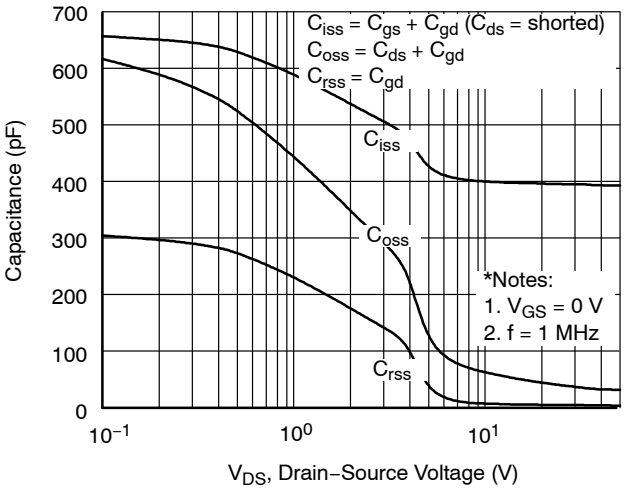


Figure 5. Capacitance Characteristics

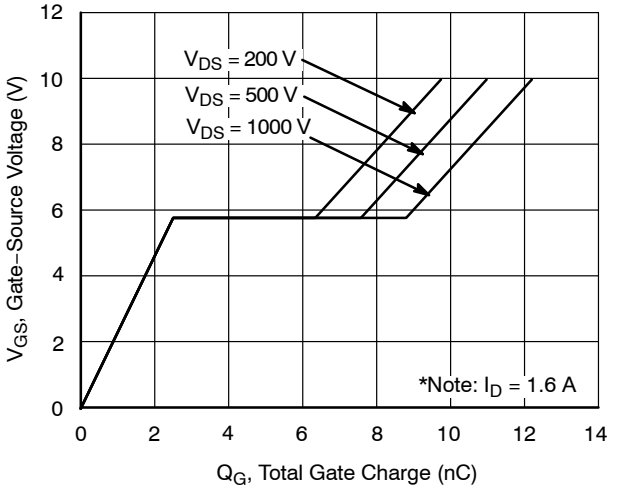


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

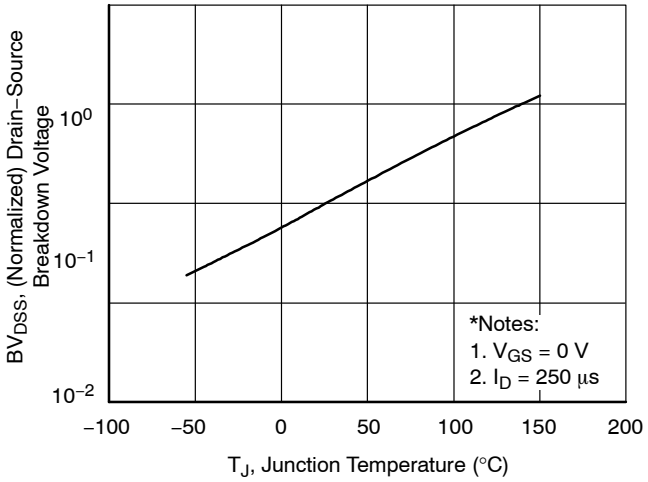


Figure 7. Breakdown Voltage Variation vs. Temperature

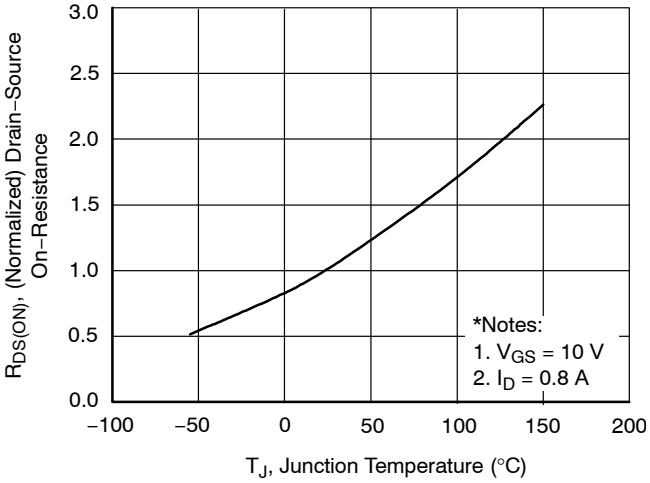


Figure 8. On−Resistance Variation vs. Temperature

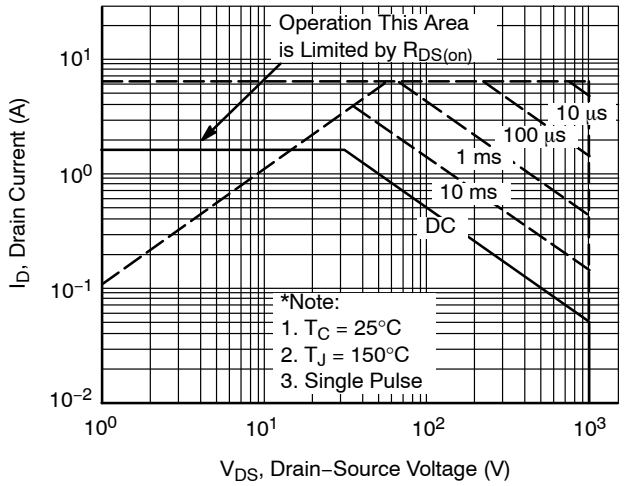


Figure 9. Maximum Safe Operating Area

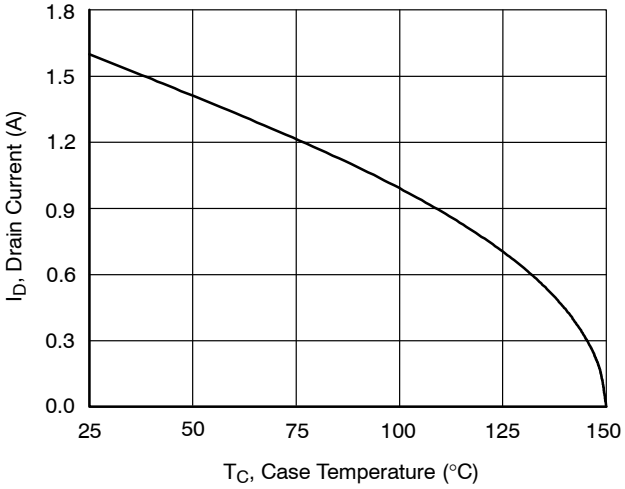


Figure 10. Maximum Drain Current vs. Case Temperature

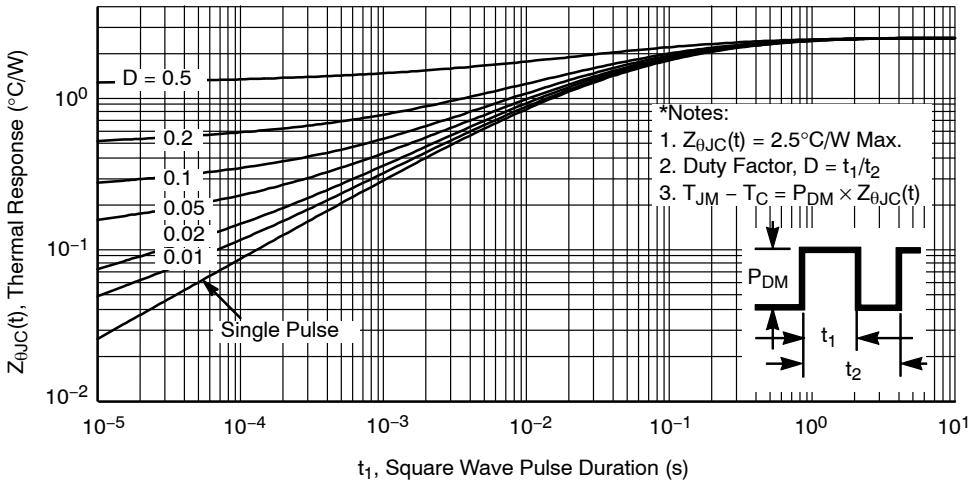


Figure 11. Transient Thermal Response Curve

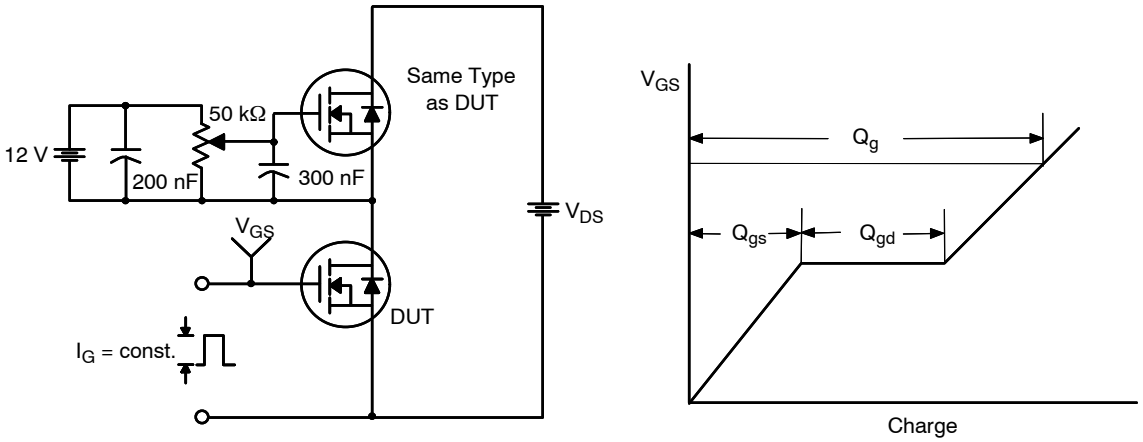


Figure 12. Gate Charge Test Circuit & Waveform

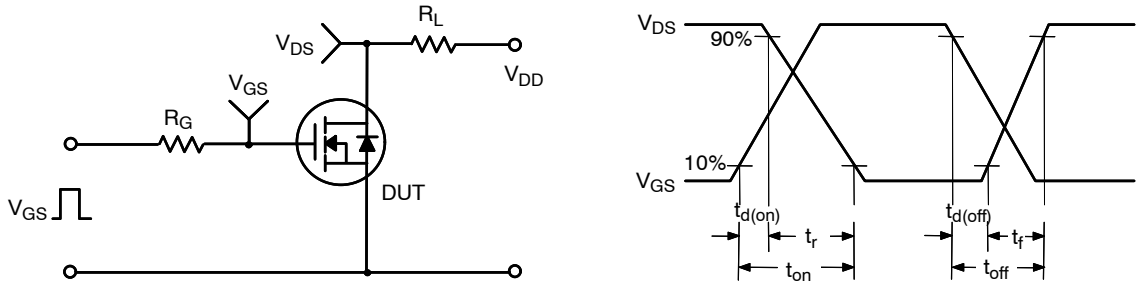


Figure 13. Resistive Switching Test Circuit & Waveforms

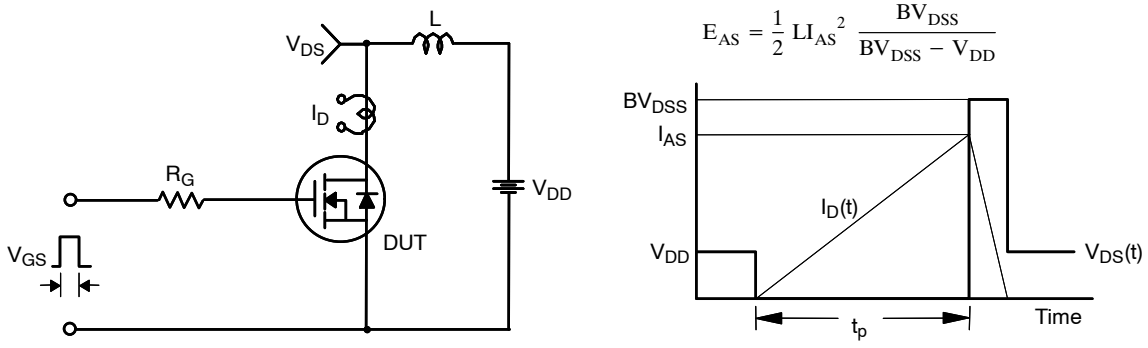


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

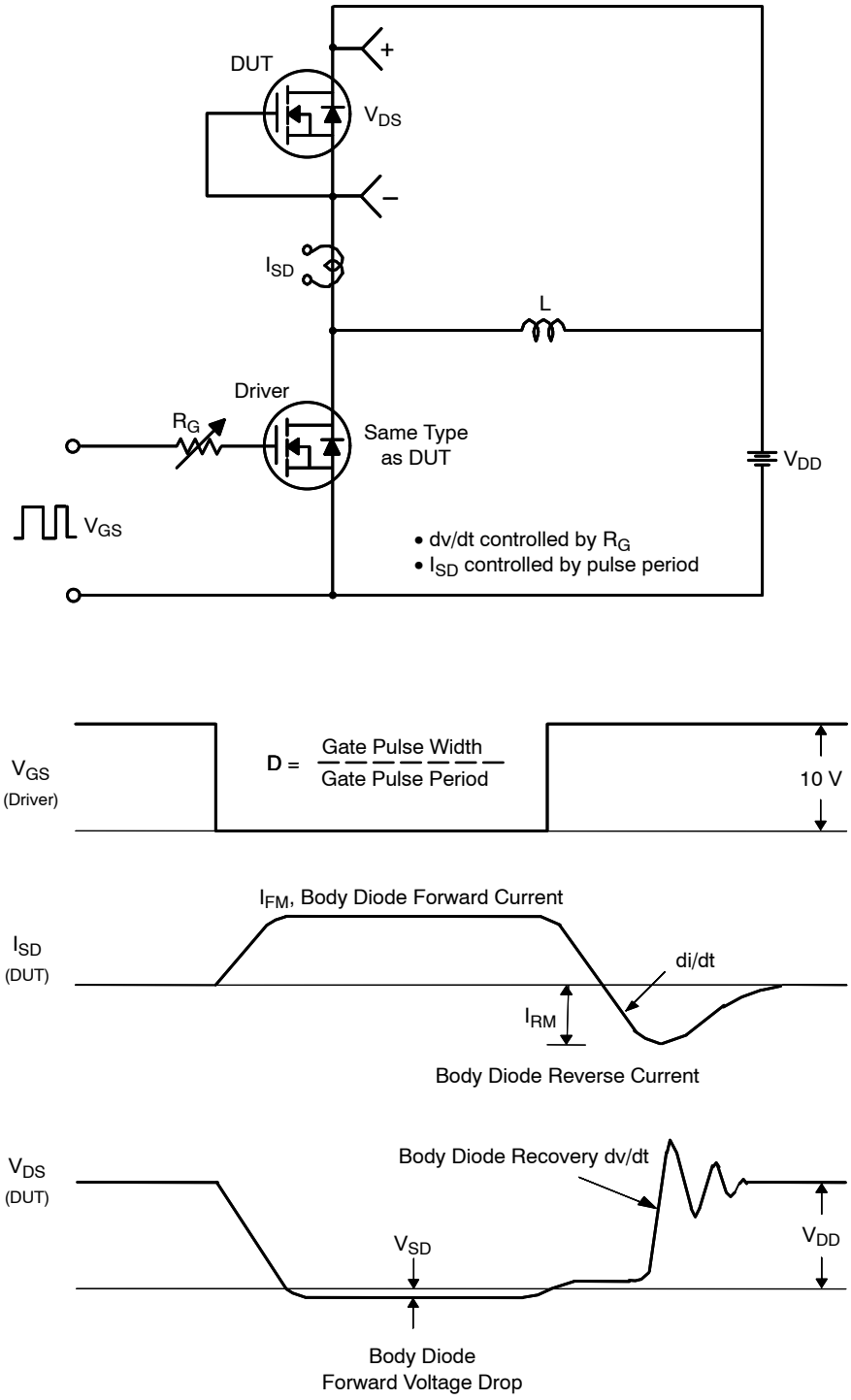
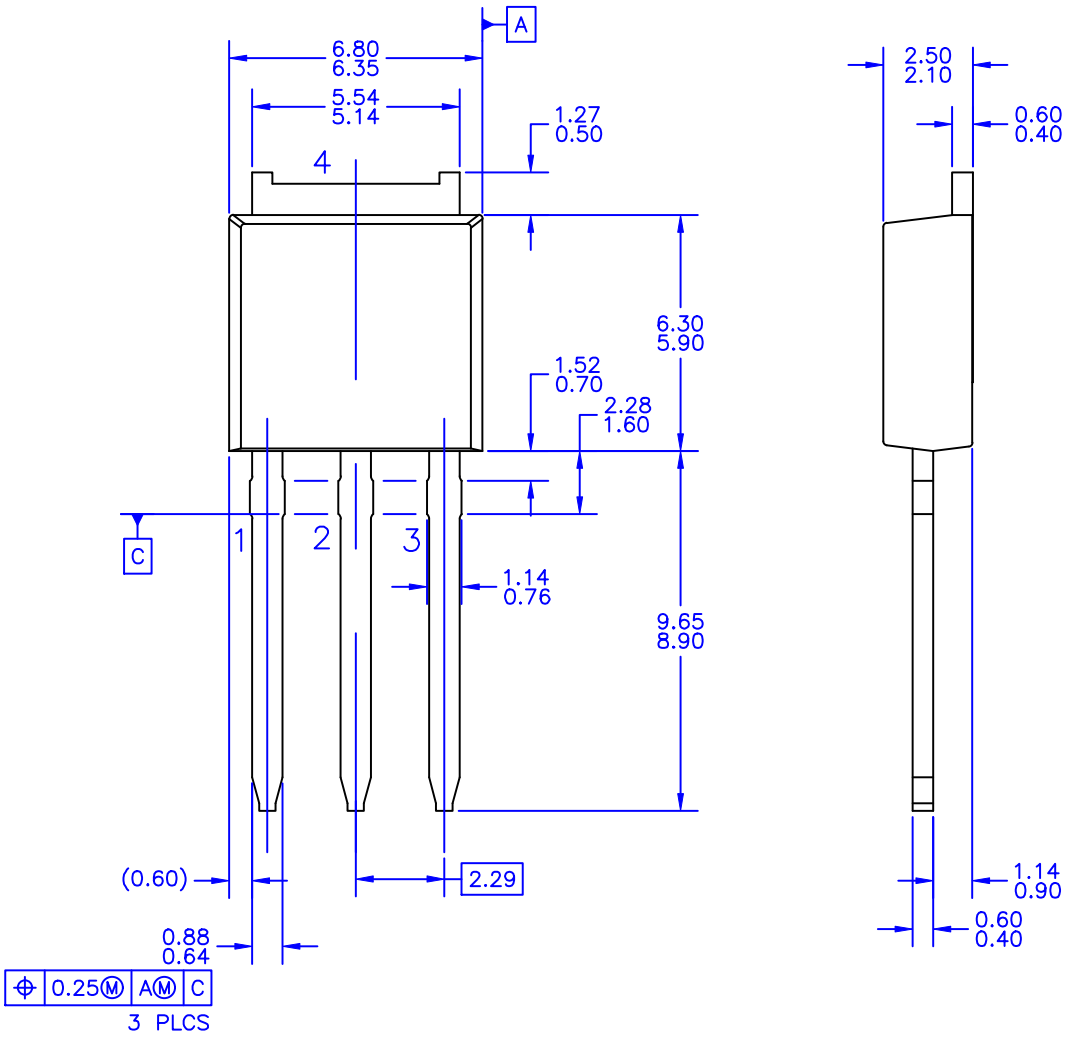
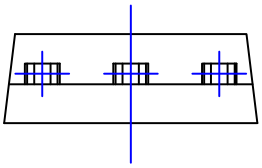


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

DPAK3 (IPAK)
CASE 369AR
ISSUE O

DATE 30 SEP 2016





NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) THIS PACKAGE CONFORMS TO JEDEC, TO−251, ISSUE C, VARIATION AA, DATED SEP 1988.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

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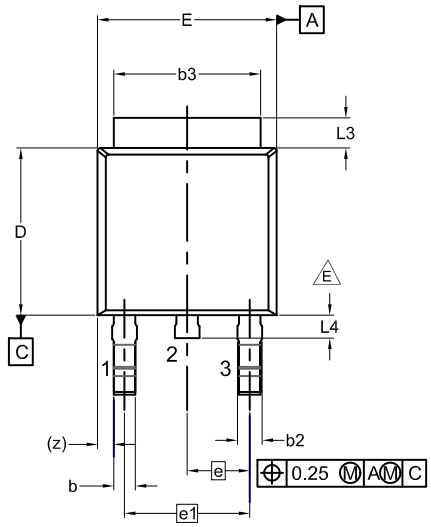
DESCRIPTION:	**DPAK3 (IPAK)**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

DPAK3 (TO−252 3 LD)
CASE 369AS
ISSUE A

DATE 28 SEP 2022



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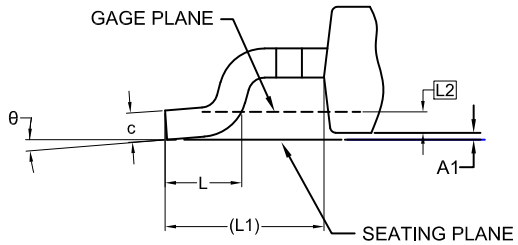
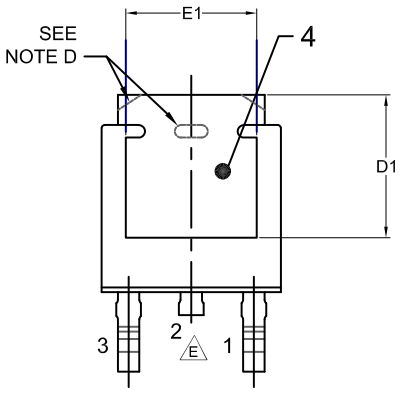
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



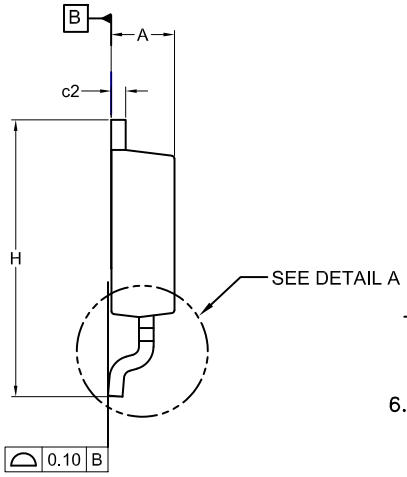
DETAIL A
(ROTATED -90°)
SCALE: 12X

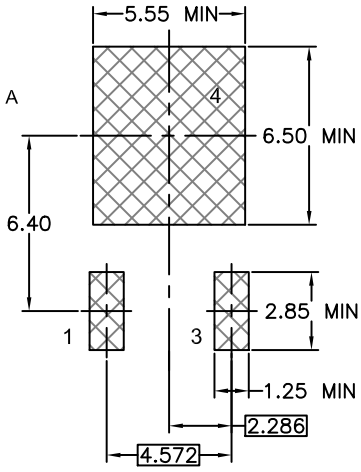
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	—	—
E	6.35	6.54	6.73
E1	4.32	—	—
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	—	—	1.02
θ	0°	---	10°

NON-DIODE PRODUCTS VERSION



NON-DIODE PRODUCTS VERSION





LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK3 (TO−252 3 LD)	PAGE 1 OF 1

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