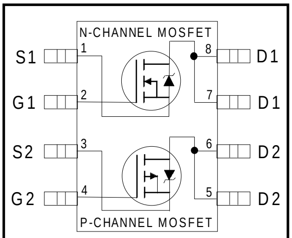
International
IOR Rectifier

PD - 91269I

IRF7507

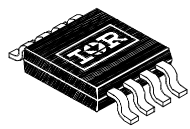
HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Very Small SOIC Package
- Low Profile (<1.1mm)
- Available in Tape & Reel
- Fast Switching



Top View

	N-Ch	P-Ch
V_{DSS}	20V	-20V
$R_{DS(on)}$	0.135Ω	0.27Ω


Micro8

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The new Micro8 package, with half the footprint area of the standard SO-8, provides the smallest footprint available in an SOIC outline. This makes the Micro8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.1mm) of the Micro8 will allow it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.

Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	20	-20	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS}	2.4	-1.7	
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS}	1.9	-1.4	A
I_{DM}	Pulsed Drain Current①	19	-14	
P_D @T_A = 25°C	Maximum Power Dissipation④	1.25		W
P_D @T_A = 70°C	Maximum Power Dissipation④	0.8		W
	Linear Derating Factor	10		mW/°C
V_{GS}	Gate-to-Source Voltage	± 12		V
V_{GSM}	Gate-to-Source Voltage Single Pulse tp<10µS	16		V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	-5.0	V/ns
T_J , T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C
	Soldering Temperature, for 10 seconds	240 (1.6mm from case)		

Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	100	°C/W

12/1/98

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	20	—	—	V	V_{GS} = 0V, I_D = 250μA
		P-Ch	-20	—	—		V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.041	—	V/°C	Reference to 25°C, I_D = 1mA
		P-Ch	—	-0.012	—		Reference to 25°C, I_D = -1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	0.085	0.14	Ω	V_{GS} = 4.5V, I_D = 1.7A ③
			—	0.120	0.20		V_{GS} = 2.7V, I_D = 0.85A ③
		P-Ch	—	0.17	0.27		V_{GS} = -4.5V, I_D =-1.2A③
			—	0.28	0.40		V_{GS} = -2.7V, I_D =-0.6A ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	0.7	—	—	V	V_{DS} = V_{GS}, I_D = 250μA
		P-Ch	-0.7	—	—		V_{DS} = V_{GS}, I_D = -250μA
g_{fs}	Forward Transconductance	N-Ch	2.6	—	—	S	V_{DS} = 10V, I_D = 0.85A ③
		P-Ch	1.3	—	—		V_{DS} = -10V, I_D = -0.6A③
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	V_{DS} = 16 V, V_{GS} = 0V
		P-Ch	—	—	-1.0		V_{DS} = -16V, V_{GS} = 0V
		N-Ch	—	—	25		V_{DS} = 16 V, V_{GS} = 0V, T_J = 125°C
		P-Ch	—	—	-25		V_{DS} = -16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	±100		V_{GS} = ± 12V
Q_g	Total Gate Charge	N-Ch	—	5.3	8.0	nC	N-Channel I_D = 1.7A, V_{DS} = 16V, V_{GS} = 4.5V ④ P-Channel I_D = -1.2A, V_{DS} = -16V, V_{GS} = -4.5V
		P-Ch	—	5.4	8.2		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	0.84	1.3		
		P-Ch	—	0.96	1.4		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	2.2	3.3		
		P-Ch	—	2.4	3.6		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	5.7	—	ns	N-Channel V_{DD} = 10V, I_D = 1.7A, R_G = 6.0Ω, R_D = 5.7Ω ④ P-Channel V_{DD} = -10V, I_D = -1.2A, R_G = 6.0Ω, R_D = 8.3Ω
		P-Ch	—	9.1	—		
t_r	Rise Time	N-Ch	—	24	—		
		P-Ch	—	35	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	15	—		
		P-Ch	—	38	—		
t_f	Fall Time	N-Ch	—	16	—		
		P-Ch	—	43	—		
C_{iss}	Input Capacitance	N-Ch	—	260	—	pF	N-Channel V_{GS} = 0V, V_{DS} = 15V, ƒ = 1.0MHz ③ P-Channel V_{GS} = 0V, V_{DS} = -15V, ƒ = 1.0MHz
		P-Ch	—	240	—		
C_{oss}	Output Capacitance	N-Ch	—	130	—		
		P-Ch	—	130	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	61	—		
		P-Ch	—	64	—		

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	1.25	A	
		P-Ch	—	—	-1.25		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	19		
		P-Ch	—	—	-14		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.2	V	T_J = 25°C, I_S = 1.7A, V_{GS} = 0V ③
		P-Ch	—	—	-1.2		T_J = 25°C, I_S = -1.2A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	N-Ch	—	39	59	ns	N-Channel T_J = 25°C, I_F = 1.7A, di/dt = 100A/μs P-Channel ③ T_J = 25°C, I_F = -1.2A, di/dt = -100A/μs
		P-Ch	—	52	78		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	37	56	nC	
		P-Ch	—	63	95		

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 21)

② N-Channel I_{SD} ≤ 1.7A, di/dt ≤ 66A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C
P-Channel I_{SD} ≤ -1.2A, di/dt ≤ 100A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C

③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

④ Surface mounted on FR-4 board, t ≤ 10sec.

N - Channel

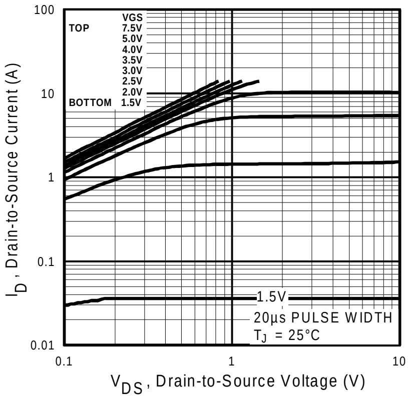


Fig 1. Typical Output Characteristics

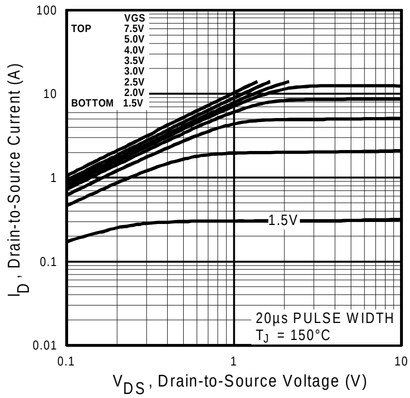


Fig 2. Typical Output Characteristics

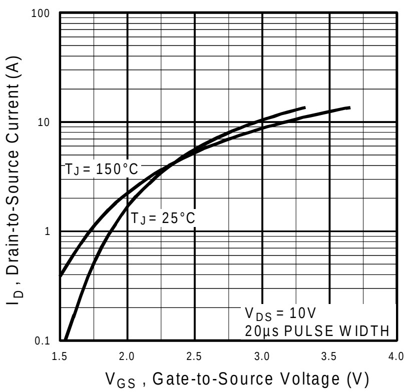


Fig 3. Typical Transfer Characteristics

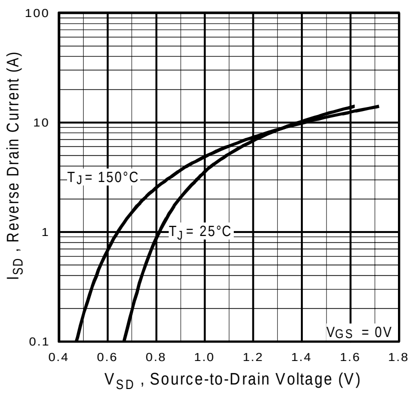


Fig 4. Typical Source-Drain Diode Forward Voltage

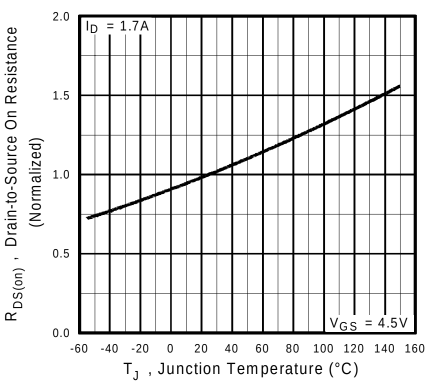


Fig 5. Normalized On-Resistance Vs. Temperature

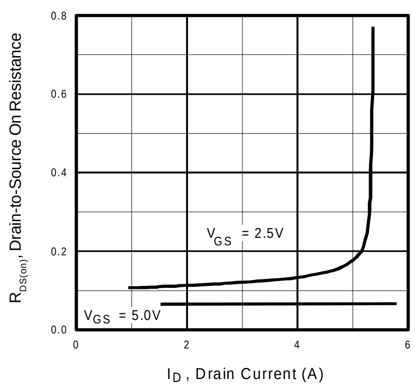


Fig 6. Typical On-Resistance Vs. Drain Current

N - Channel

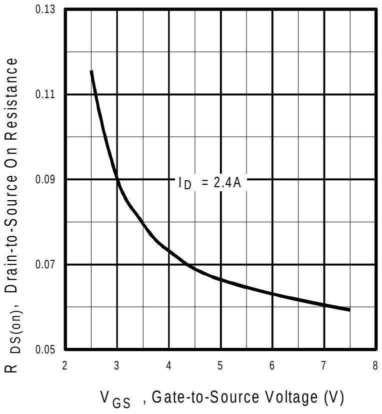


Fig 7. Typical On-Resistance Vs. Gate Voltage

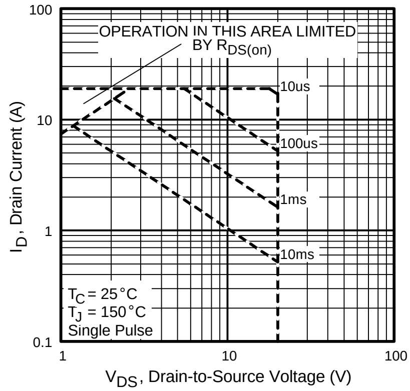


Fig 8. Maximum Safe Operating Area

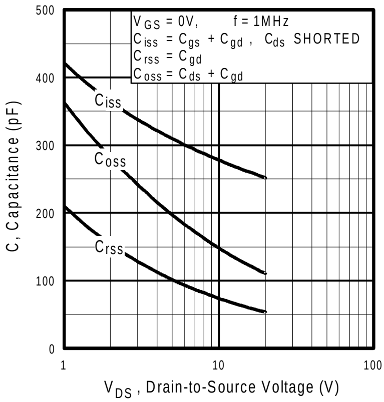


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

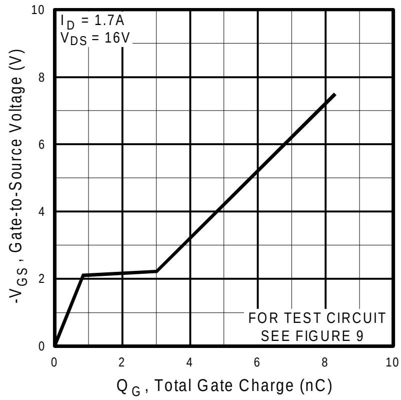


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

P - Channel

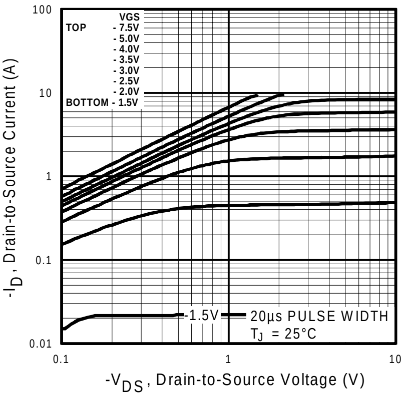


Fig 11. Typical Output Characteristics

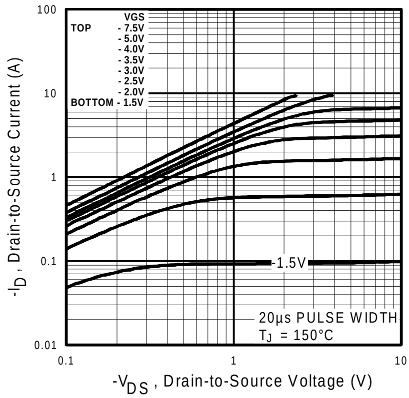


Fig 12. Typical Output Characteristics

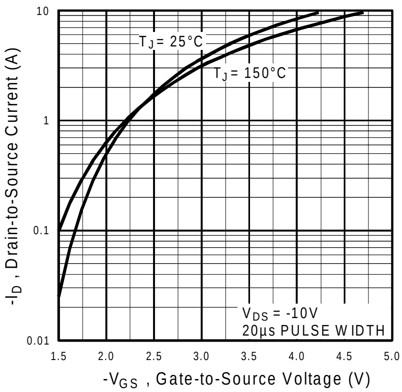


Fig 13. Typical Transfer Characteristics

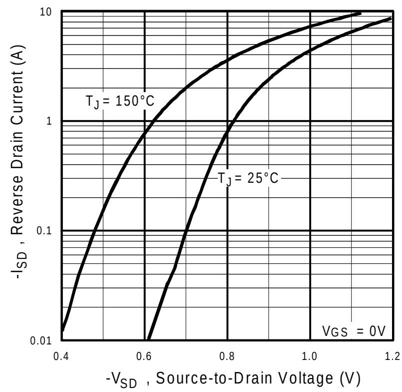


Fig 14. Typical Source-Drain Diode Forward Voltage

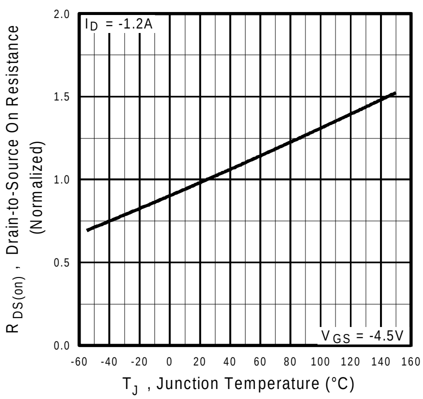


Fig 15. Normalized On-Resistance Vs. Temperature

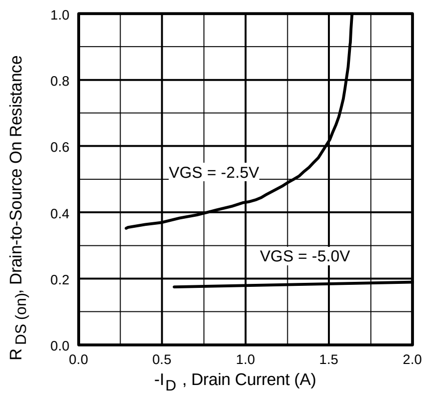


Fig 16. Typical On-Resistance Vs. Drain Current

P - Channel

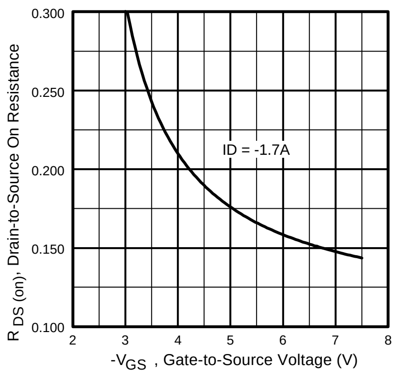


Fig 17. Typical On-Resistance Vs. Gate Voltage

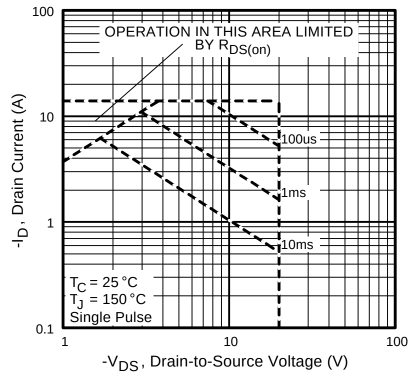


Fig 18. Maximum Safe Operating Area

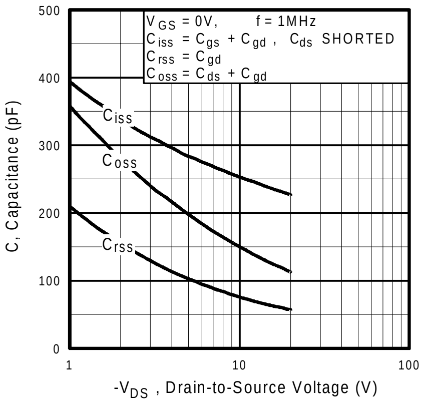


Fig 19. Typical Capacitance Vs. Drain-to-Source Voltage

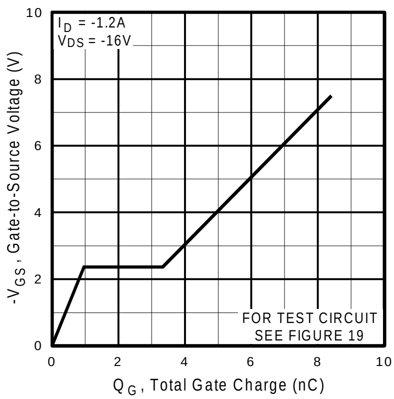


Fig 20. Typical Gate Charge Vs. Gate-to-Source Voltage

N-P - Channel

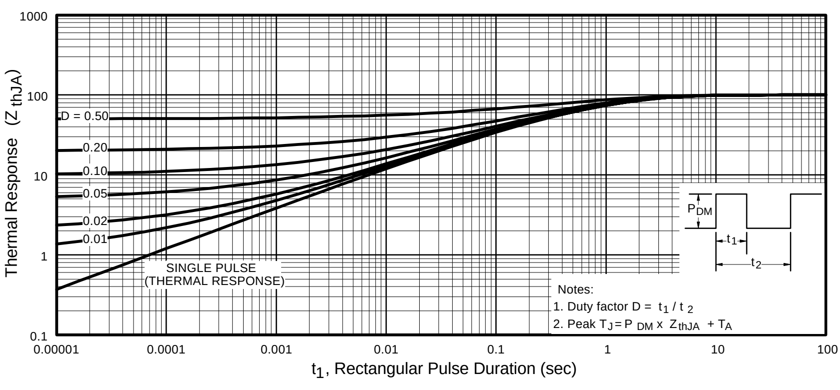
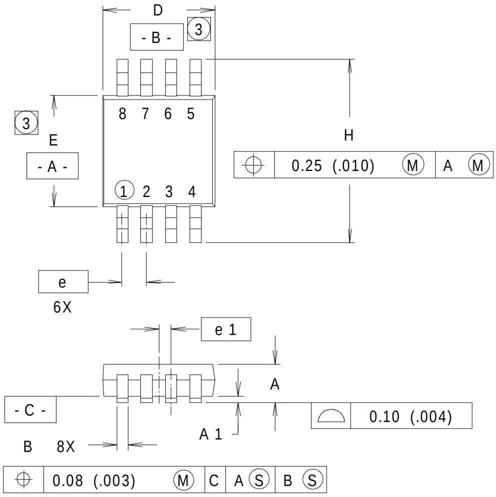


Fig 21. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

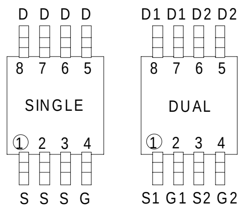
Package Outline

Micro8 Outline

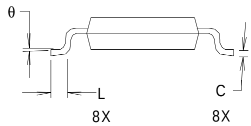
Dimensions are shown in millimeters (inches)



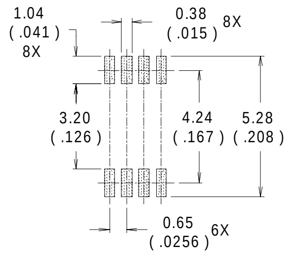
LEAD ASSIGNMENTS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.036	.044	0.91	1.11
A1	.004	.008	0.10	0.20
B	.010	.014	0.25	0.36
C	.005	.007	0.13	0.18
D	.116	.120	2.95	3.05
e	.0256 BASIC		0.65 BASIC	
e1	.0128 BASIC		0.33 BASIC	
E	.116	.120	2.95	3.05
H	.188	.198	4.78	5.03
L	.016	.026	0.41	0.66
θ	0°	6°	0°	6°



RECOMMENDED FOOTPRINT



NOTES:

1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.

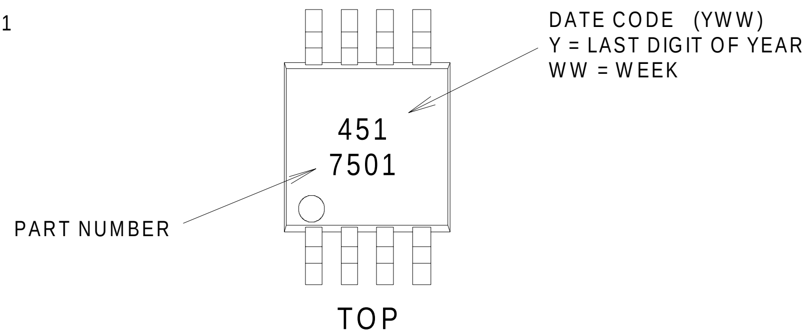
2 CONTROLLING DIMENSION : INCH.

3 DIMENSIONS DO NOT INCLUDE MOLD FLASH.

Part Marking Information

Micro8

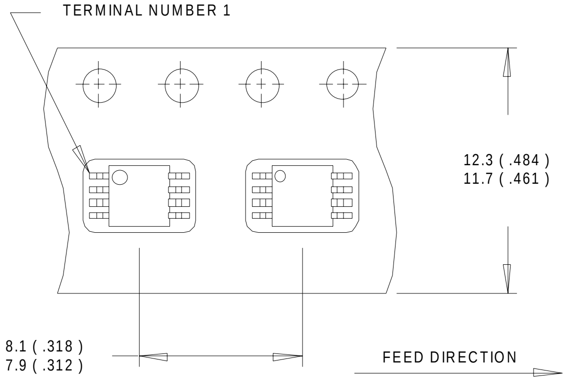
EXAMPLE : THIS IS AN IRF7501



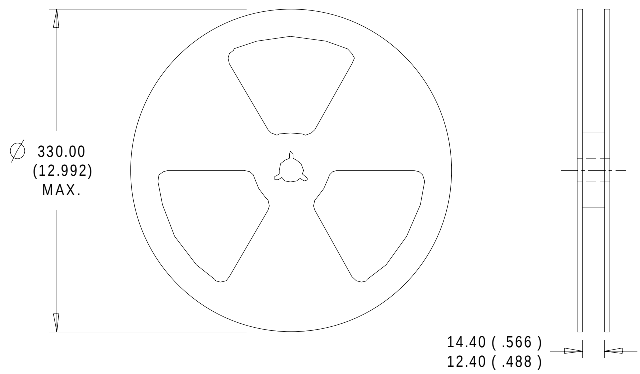
Tape & Reel Information

Micro8

Dimensions are shown in millimeters (inches)



NOTES:
1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. CONTROLLING DIMENSION : MILLIMETER.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

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