TPS2358 Dual-Slot ATCA™ AdvancedMC™ Controller Evaluation Module

1 Introduction

The Dual-Slot AdvancedMC™ Controller Evaluation Module (EVM) is a PCB platform for users to learn about the features and operation of the TPS2358 integrated circuit from Texas Instruments (TI). The TPS2358 Dual-Slot ATCA™ AdvancedMC™ Controller manages two 12-V and two 3.3-V power rails, and features inrush and fault current limiting, FET OR'ing, input UVLO protection and logic-level enable inputs. Current control on the 12-V rails has a high degree of programmability, including independent current limit and fast trip thresholds. Overcurrent fault timing is managed with user-programmable shut-down delays, and each of the four power channels has dedicated fault and power good reporting outputs. In addition, current sense and pass and block FET's for the 3.3-V channels are fully integrated into the device.

Power management applications based on the TPS2358 are easily configured to meet the requirements for 12-V and 3.3-V control of Advanced Mezzanine Card (AdvancedMC™) modules. Each device incorporated onto a Carrier Card provides full control for two AdvancedMC™ slots according to the requirements of the Advanced Telecommunications Computing Architecture (ATCA™) specification, PICMG 3.0. In addition, the input supply FET OR'ing control for the 12-V rails facilitates efficient redundant supply implementations in Micro Telecommunications Computing Architecture (MicroTCA™) systems.

2 Description

2.1 Module Overview

The TPS2358EVM is a single-board evaluation platform consisting of two main sections. When oriented with the board nomenclature and switch labels in a normal, upright reading position towards the user, the top portion contains the TPS2358 device and typically required components. The bottom section contains more ancillary circuitry intended to facilitate exercising the device through various application scenarios. Power connectors are organized with inputs along the left edge of the board, outputs along the right.

The main (upper) section of the board is comprised of the four power channels, including the featured device, support passives, input and output banana jacks, control FET's (for 12-V rails), and power planes. The board contains various capacitors for simulation of input bulk capacitance as may be present on driven AdvancedMC™ modules; alternatively, the user's test loads can be connected at the output banana jacks. Various timing capacitor options, for each power rail, are available and user-selectable via DIP switch S7. Numerous jumpers are provided throughout the circuit for maximum configuration flexibility. Test points are available for voltage and waveform monitoring.

The bottom section contains two expansion port connectors and the status LED's. Slide switches for actuation of the chip enable inputs are organized in a row along the bottom edge of the PCB.

2.2 Typical Applications

The TPS2358EVM was designed with independent input and output banana jacks for up to two each 12-V input and 3.3-V input power supplies, and up to two each 12-V and 3.3-V output power rails. This provides the greatest flexibility for configuring the EVM for either ATCA™ or MicroTCA™ applications.

By connecting the two 12-V inputs and two 3.3-V inputs together, the TPS2358EVM can manage the application of a single 12-V supply and single 3.3-V supply to two AdvancedMC-like loads. This configuration allows users to learn about the device operation in non-redundant applications. Driving the supply inputs independently while ganging together the common potential output nodes demonstrates operation in redundant systems, albeit through a common controller IC. In either case, switch-selectable timing capacitors complete device configuration for the target application.

As supplied from the factory, the EVM comes with current limits programmed for the requirements of Management Power and Payload Power control for AdvancedMC™ modules. However, limit thresholds on the 12-V channels are programmable by the user; instructions for modifying current limits are included below. This flexibility with the TPS2358 enables use in other, proprietary systems requiring 12-V and 3.3-V supply control.

Lastly, the EVM features two expansion ports and related jumpers needed to parallel multiple devices together to create a true redundant system. Additional EVM modules for this purpose can be ordered directly from the TI website at http://www.productfolderURL, or contact your local TI representative.

2.3 Features

The TPS2358EVM includes the following features:

- One TPS2358 Dual-Slot ATCA™ AdvancedMC™ Controller
- Programming and sense resistors (12-V)
- Low R_{DS}(ON) pass and block FET's (12-V)
- Input and output power jacks for external supply and optional load connection
- Up to 880 μF (4 × 220 μF) jumpered load capacitors (each channel) for simulated Payload Power output bulk capacitance
- 150 μF jumpered load capacitor for each Management Power channel
- Multiple, switch-selectable fault timer settings, each channel
- Slide switch actuation of enable inputs
- Expansion port headers

The use of these features is described in greater detail later in this document.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the TPS2358EVM are given below in Table 1.

Table 1. Absolute Maximum Ratings[1][2]

PARAMETER	RATING
Input voltage range, +12-V supply	–0.3 V to 13.8 V
Input voltage range, +3.3-V supply	–0.3 V to 4 V
Applied voltage, pins of J21, J22 $\overline{EN12x}$, $\overline{ORENx}$	–0.3 V to (V_{IN}(12VINx) + 0.5 V)
Applied voltage, pins of J21, J22 SUMx, $\overline{EN3x}$	–0.3 V to (V_{IN}(3V3INx) + 0.5 V)
Output current, 12-V outputs	TBD
Output current, 3.3-V outputs	Internally limited by device
Output current, SUMx	-5 mA
Storage temperature range	–55°C to 150°C

(1) All voltages are with respect to the EVM GND node.
(2) Currents are positive into and negative out of the specified terminal.

3.2 Recommended Operating Conditions

The recommended operating conditions for the TPS2358EVM are given in Table 2.

Table 2. Recommended Operating Conditions, TPS2358EVM[1][2]

PARAMETER	MIN	TYP	MAX	UNITS
Input supply voltage, +12-V	8.8	12	13.2	V
Input supply voltage, +12-V (for specified V_{OUT})	11.3	12	13.2	V
Input supply voltage, +3.3-V	2.85	3.3	3.5	V
Input supply voltage, +3.3-V (for specified V_{OUT})	3.235	3.3	3.465	V
Load current, Payload Power Out (either channel)			–7.4	A
Load current, Mgmt Power Out (either channel)			–165	mA

(1) All voltages are with respect to the EVM GND node.
(2) Currents are positive into and negative out of the specified terminal.

3.3 Electrical Characteristics

The electrical characteristics of the TPS2358EVM are as listed in Table 3.

Table 3. Electrical Characteristics, TPS2358EVM(1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
UNLESS OTHERWISE NOTED: V_{IN}(12VINx) and V_{IN}(3V3INx) per Table 2 under *(for specified V_{OUT})*. T_A = 25°C					
Output Voltage, Payload Power Out (either channel)	$\overline{EN12x}$ = HI, $\overline{ORENx}$ = HI, $I_{LPWR} < I_{LPWR\_MAX}$	10.8		13.2	V
Output Voltage, Mgmt Power Out (either channel)	$\overline{EN3x}$ = HI, $I_{LMP} < I_{LMP\_MAX}$	3.135		3.465	V
Current limit threshold, Payload Power (either channel)		7.4	8.36	9.1	A
Current limit threshold, Mgmt Power (either channel)		170	195	225	mA
Fast trip threshold, Payload Power (either channel)				24.5	A
Fast trip threshold, Mgmt Power (either channel)				400	mA
Output capacitance, Payload Power (C_{L_PWR}) (each channel)	All 4 load caps connected	704	880	1056	µF
Output capacitance, Mgmt Power (C_{L_MP}) (each channel)	Load cap connected	120	150	180	µF
Output ramp time, Payload Power	V_{IN} = 12V–13.2V, V_O = 0V to 98% × V_{IN}, R_{LOAD} = 1K, C_{LOAD} = C_{L_PWR}		1.31	2.01	mS
Output ramp time, Mgmt Power	V_{IN} = 3.3V–3.465V, V_O = 0 V to 98% V_{IN}, R_{LOAD} = 270, C_{LOAD} = CL_MP		2.57	3.74	mS

(1) All voltages are with respect to the EVM GND node.

4 Schematic Diagram

The schematic diagram for the TPS2358EVM is shown in Figure 1 and Figure 2.

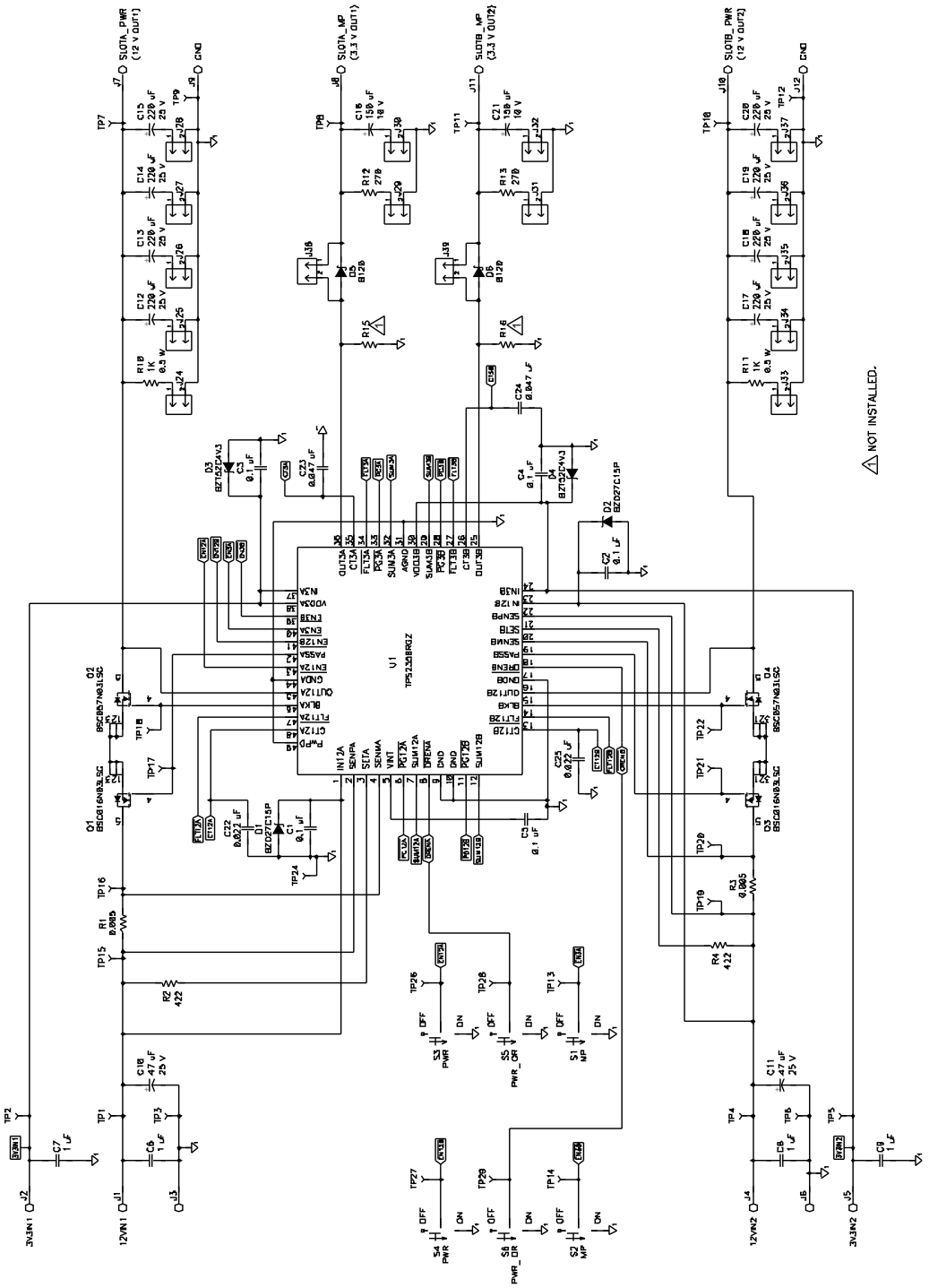


Figure 1. TPS2358 Evaluation Module Schematic Diagram, Sheet 1

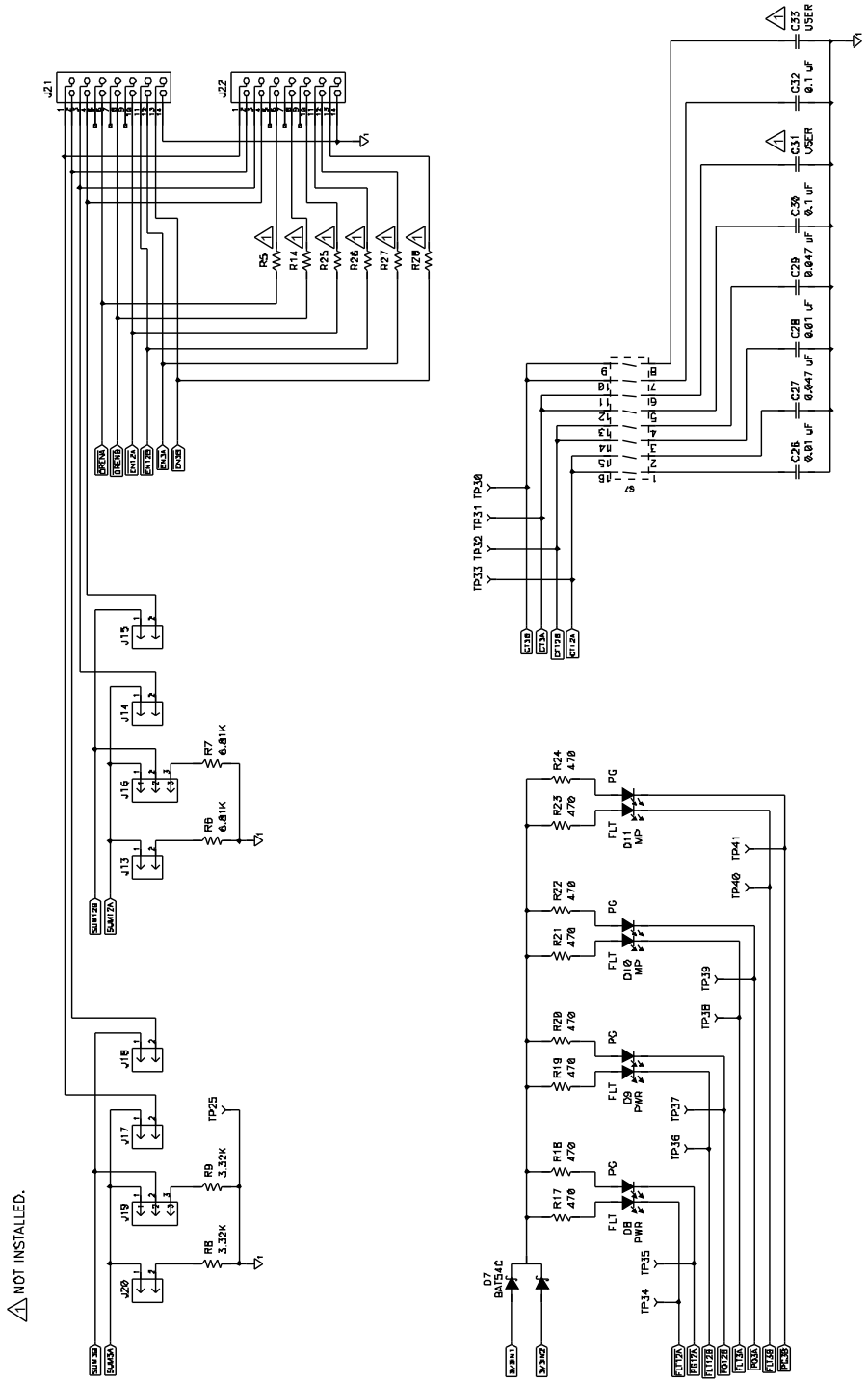


Figure 2. TPS2358 Evaluation Module Schematic Diagram, Sheet 2

5 Test Set-Up

5.1 Equipment Requirements

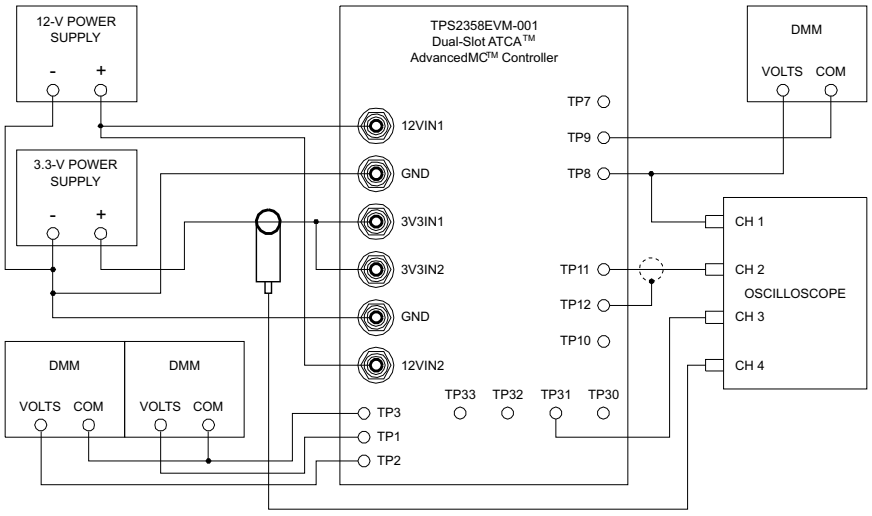
The following test and interface equipment (not supplied) is required to verify EVM module operation, and begin using the EVM.

- Power supply, 3.3 VDC, 500 mA minimum
- Power supply, 15 VDC, 10 A minimum
- Digital multimeters
- Oscilloscope, 4 channel, with current probe

Connect the TPS2358EVM and test equipment as shown in Figure 3 for functional check-out of the board and a good starting point for user evaluation of device operation. Screen print labeling on the board employs a naming convention in keeping with the nomenclature of the target ATCA™ and MicroTCA™ applications. Input 3.3-V supplies are connected to the 3V3INx jacks, and 12-V supplies are connected to the 12VINx jacks. A cross-reference of power rail labeling to standards naming is shown in Table 4.

Table 4. TPS2358EVM Output Net and Jack Naming

REF.DES.	CONNECTOR	LABEL DESCRIPTION
J8	SLOT A MP	AdvancedMC™ Slot A Management Power
J7	SLOT A PWR	AdvancedMC™ Slot A Payload Power
J9	GND	Common load return node for Slot A
J11	SLOT B MP	AdvancedMC™ Slot B Management Power
J10	SLOT B PWR	AdvancedMC™ Slot B Payload Power
J12	GND	Common load return node for Slot B



(1) The 3V3INx jacks can be jumpered together with a short test lead at the board, fed from a single lead from the power supply.

(2) Run separate leads from the GND jacks back to a common return point made near the power supply output terminals.

Figure 3. TPS2358EVM Set-up — Non-Redundant System Connection

6 Test Procedure

The following procedure can be used to verify functional operation of the EVM assembly upon receipt.

6.1 Jumper Installation

The TPS2358EVM makes use of various jumpers for quick change of functional configurations. Verify the module was supplied with shunt jumpers installed across the headers listed in Table 5. For 3-poin headers, note the pin pairs to be connected.. Reconfigure jumper connections if necessary.

Table 5. Initial Jumper Settings

Signal and Control Jumpers
J13, J20
J16-2 to J16-3, J19-2 to J19-3
J24 – J28
J29, J30
J31, J32
J33 - J37
J38, J39

On the EVM board, place the ENABLE slide switches, located along the bottom edge of the PCB, in the initial positions shown in Table 6.

Table 6. ENABLE Switch Initial Positions

Section	Switch Name	Initial Position
SLOT A	MP	HI
	PWR	HI
	PWR_OR	LO
SLOT B	MP	HI
	PWR	HI
	PWR_OR	LO

Set all 8 DIP positions of switch S7 to the CLOSED position.

6.2 Check-Out Steps

Turn the voltage adjust knobs of both power supplies fully CCW. Adjust the current limit control of the 15-V supply for 10 amps minimum output.

If not already done, connect the EVM and test equipment as shown in Figure 3.

Turn on the 3.3-V power supply, and adjust the output for 3.3 V 5% at test point TP2. Turn on the second supply, and adjust the output for 12 V 5% at TP1. Verify all STATUS LED's (located just above the slide switches) are OFF.

On the oscilloscope, set the Channel 1 and 2 amplifiers to the 2 V/div scale, and position the traces appropriately in the top half of the display for viewing 3.3-V magnitude waveforms. Set the Channel 3 amplifier scale to 100 or 200 mV/div, and position that trace about one division below center of the screen. Set the current pulse amplifier scale to 100 mA/div, and position that trace towards the bottom of the scope screen. Set the scope to trigger on the rising edge of Channel 1, at a threshold of about 1.5 V. Set the time base to 1 mS/div, and set the trigger mode to NORMAL.

On the EVM board, place the SLOT A MP ENABLE switch in the LO position. The SLOT A MP green STATUS LED should illuminate. On the oscilloscope, verify a waveform capture was obtained similar to the one shown in Figure 4. The total voltage ramp time of the Channel 1 waveform, from 0 volts to about 3.2 volts should be 2.6 0.6 mS. The Channel 3 waveform should attain a peak amplitude (prior to pulling low again) of about 180 mV, for a nominal 2.6 ms output ramp time. The actual amplitude obtained varies linearly with the ramp time, and has some inherent tolerance of its own. The peak amplitude of the current pulse on Channel 4 should be 195 25 mA. A DVM can be used to verify the voltage at TP8 (with respect to ground at TP9) is within 10 mV of the 3.3-V input supply voltage at 3V3IN1 (TP2).

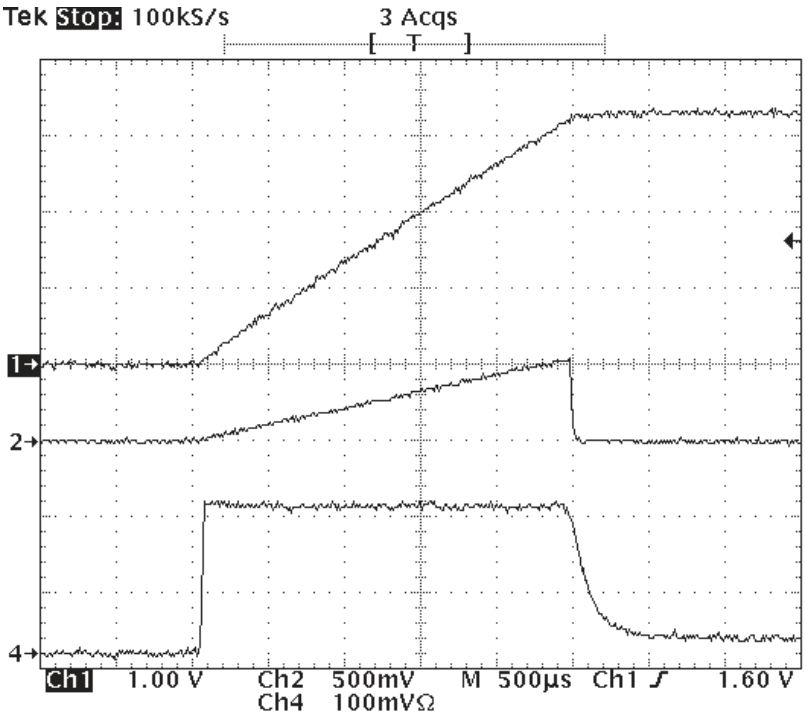


Figure 4. Output Ramp-Up Waveforms – 3.3-A Rail

Move the Channel 3 scope probe to test point TP30. Set the scope to trigger on Channel 2. Place the EVM SLOT B MP ENABLE switch in the LO position. The SLOT B MP green STATUS LED should illuminate. On the scope screen, verify a waveform capture was obtained similar to that shown in Figure 5. The Channel 2, 3 and 4 waveform parameters should be similar to those indicated above for Figure 4. A DVM can be used to verify the output voltage at TP11 (with respect to ground at TP12) is within 10 mV of the 3.3-V input supply setting.

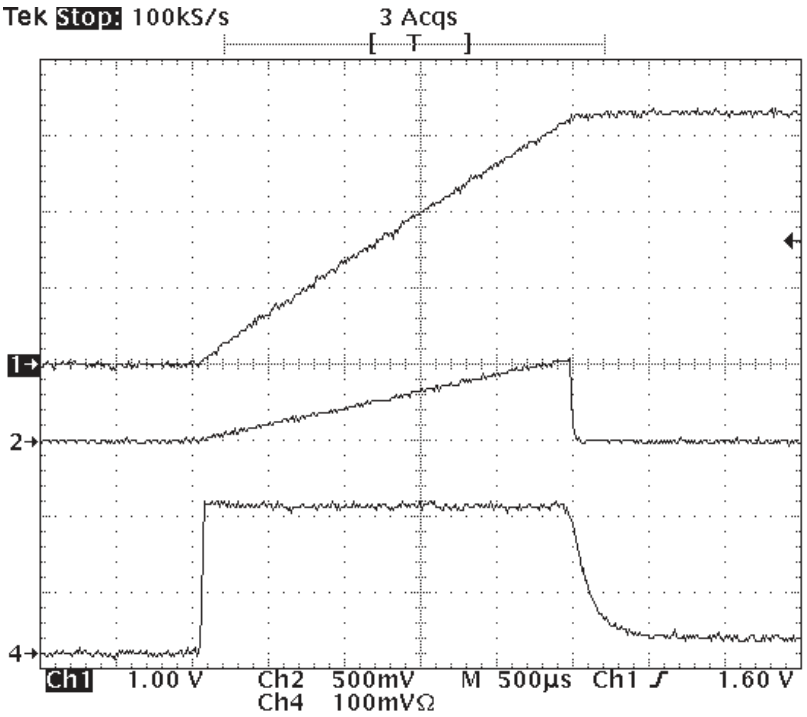


Figure 5. Output Ramp-up Waveforms – 3.3B Rail

Change the oscilloscope probe connections and amplifier settings as shown below. It may be beneficial to move the Channel 1 and 2 trace positions for viewing a couple of 12-V waveforms in the top half of the screen.

- Chan. 1 -- TP7: 5 V/div
- Chan. 2 -- TP10: 5 V/div
- Chan. 3 -- TP32: 100 or 200 mV/div

Remove the current probe from the 3.3 V supply lead, and clamp it across the 12VIN2 supply lead. Change the Channel 4 amplifier setting to 5 A/div. Set the time base to 500 S/div, and adjust the scope trigger threshold to about 3 volts.

On the EVM board, place the SLOT B PWR ENABLE switch to the LO position. The SLOT B PWR green LED should illuminate. On the scope, verify a waveform capture was obtained similar to that shown in Figure 6. The total voltage ramp time of the Channel 2 trace, from 0 volts to about 11.8 V should be 1.3 0.3 mS. Note that the extent of variance of the 12-V supply setting from a nominal 12.0 V affects this timing result. A linearly ramping waveform should be visible on the Channel 3 trace, terminating some time after the output (Channel 2) charges to input potential. The average amplitude of the current pulse (i.e., across the flattest part of the peak) on Channel 4 should be 7.9 0.8 A. A DVM can be used to verify the voltage at TP10 (with respect to ground at TP12) is essentially the same as the input supply potential at 12VIN2.

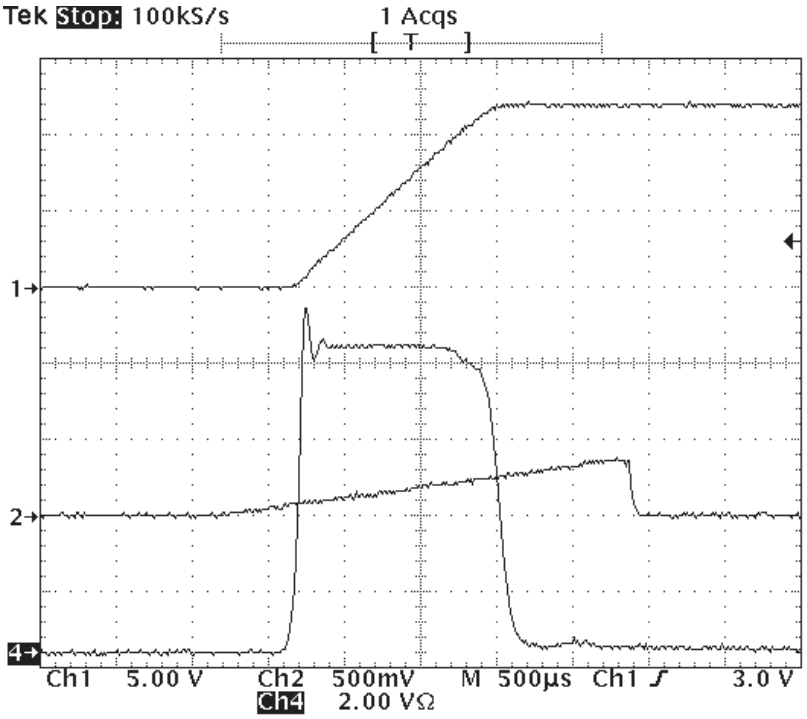


Figure 6. Output Ramp-up Waveforms – 12B Rail

Reconnect the Channel 3 scope probe to test point TP33. Set the scope to trigger on Channel 1. Disconnect the current probe and reconnect it across the 12VIN1 supply lead. Move the probe ground lead to test point TP9. Set the SLOT A PWR ENABLE switch to the LO position. The SLOT A PWR green STATUS LED should illuminate. On the scope, verify a waveform capture was obtained similar to that shown in Figure 7. The Channel 1, 3 and 4 waveform parameters should be similar to those indicated above for Figure 6. Again, the extent of variance of the 12-V supply setting from a nominal 12.0 V affects the ramp-up timing result. A DVM can be used to verify the voltage at TP7 (with respect to ground at TP9) is essentially the same as the input supply potential at 12VIN1.

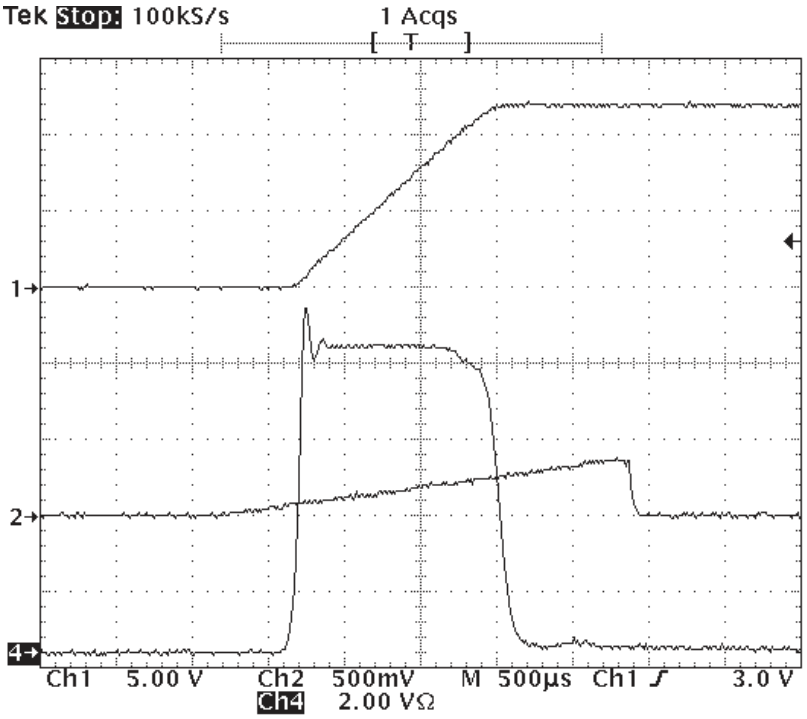


Figure 7. Output Ramp-up Waveforms – 12A Rail

The 12-V channel input OR'ing operation can be confirmed as follows: connect voltmeters across the 12-V output test points (SLOT A at TP7, SLOT B at TP10) and a convenient ground point. Setting the SLOT A PWR_OR switch to LO should cause the Slot A output voltage to drop by about 600 mV (i.e., a diode drop). Setting the SLOT B PWR_OR switch to LO should cause the Slot B output to drop by about 600 mV.

When any of the output channels are disabled (ENABLE switch returned to HI position), the corresponding output should decay towards 0 volts.

Module operation as indicated in the above steps is a good indication of a fully functional board and correct set-up. This is also a good starting point for further test and user evaluation of the device.

7 EVM Feature Details

7.1 Test Points

The TPS2358EVM contains numerous test points throughout the circuit for user monitoring of waveforms and voltage measurement. Table 7 lists the module test points and the signal available at each one. The EVM PCB layout connects all ground nodes and supply returns to a common GND node, via several power plane areas. However, due to potentially high loading conditions on the two Payload Power outputs, multiple ground test points are provided to mitigate the measurement impact of return current drops. Therefore, where appropriate, certain test points are paired in the table with the pertinent reference point for meter return connections.

Table 7. Module Test Points

TEST POINT NAME	REF. POINT	SIGNAL NAME	DESCRIPTION
TP1	TP3	12VIN1	Input 12 V supply for AdvancedMC™ Slot A
TP2		3V3IN1	Input 3.3 V supply for AdvancedMC™ Slot A
TP4	TP6	12VIN2	Input 12 V supply for AdvancedMC™ Slot B
TP5		3V3IN2	Input 3.3 V supply for AdvancedMC™ Slot B
TP7	TP9	SLOTA_PWR	AdvancedMC™ Slot A Payload Power, 12 V output
TP8		SLOTA_MP	AdvancedMC™ Slot A Management Power, 3.3 V output
TP10	TP12	SLOTB_PWR	AdvancedMC™ Slot B Payload Power, 12 V output
TP11		SLOTB_MP	AdvancedMC™ Slot B Management Power, 3.3 V output
TP13	TP24, TP25	$\overline{\text{EN3A}}$	Active-low enable input to TPS2358 for the channel A 3.3 V rail
TP14		$\overline{\text{EN3B}}$	Active-low enable input to TPS2358 for the channel B 3.3 V rail
TP15	TP16		Slot A 12-V load current sense voltage
TP17	TP24	PASSA	TPS2358 channel A pass FET gate drive output
TP18		BLKA	TPS2358 channel A block/OR'ing FET gate drive output
TP19	TP20		Slot B 12-V load current sense voltage
TP21	TP25	PASSB	TPS2358 channel B pass FET gate drive output
TP22		BLKB	TPS2358 channel B block/OR'ing FET gate drive output
TP26	TP24, TP25	$\overline{\text{EN12A}}$	Active-low enable input to the TPS2358 for the channel A 12-V rail
TP27		$\overline{\text{EN12B}}$	Active-low enable input to the TPS2358 for the channel B 12-V rail
TP28		$\overline{\text{ORENA}}$	Channel A OR'ing FET/function enable signal to the TPS2358
TP29		$\overline{\text{ORENB}}$	Channel B OR'ing FET/function enable signal to the TPS2358
TP30	TP24, TP25	CT3B	Timing cap waveform for the Slot B 3.3-V rail (SLOTB_MP)
TP31		CT3A	Timing cap waveform for the Slot A 3.3-V rail (SLOTA_MP)
TP32		CT12B	Timing cap waveform for the Slot B 12-V rail (SLOTB_PWR)
TP33		CT12A	Timing cap waveform for the Slot A 12-V rail (SLOTA_PWR)
TP34	Var.	$\overline{\text{FLT12A}}$	Slot A 12-V open-drain, active-low FAULT output indication
TP35		$\overline{\text{PG12A}}$	Slot A 12-V open-drain, active-low POWERGOOD output indication
TP36		$\overline{\text{FLT12B}}$	Slot B 12-V open-drain, active-low FAULT output indication
TP37		$\overline{\text{PG12B}}$	Slot B 12-V open-drain, active-low POWERGOOD output indication
TP38		$\overline{\text{FLT3A}}$	Slot A 3.3-V open-drain, active-low FAULT output indication
TP39		$\overline{\text{PG3A}}$	Slot A 3.3-V open-drain, active-low POWERGOOD output indication
TP40		$\overline{\text{FLT3B}}$	Slot B 3.3-V open-drain, active-low FAULT output indication
TP41		$\overline{\text{PG3B}}$	Slot B 3.3-V open-drain, active-low POWERGOOD output indication

On the TPS2358EVM, the device fault ($\overline{\text{FLTx}}$) and power good ($\overline{\text{PGx}}$) outputs are all used to drive the STATUS LED's. Power for LED drive is derived from a diode-OR of the two 3.3-V input supplies.

7.2 Connecting Loads to the TPS2358EVM

Each of the four power rails of the TPS2358EVM is supplied with some amount of load capacitance in the form of discrete electrolytics. The capacitors can be connected to or disconnected from their associated output nodes using 100-mil, 2-pin shunt jumpers across the on-board PCB headers. These capacitors are intended to simulate input bulk capacitance which may be encountered at the front ends of AdvancedMC™ modules plugged into the card slots of the target application. The AdvancedMC™ standard specifies the maximum allowable input capacitance on both Management and Payload Power rails. The TPS2358EVM provides up to 150 µF capacitance on each of the two Management Power outputs, according to the AdvancedMC™ maximum limit. The EVM also provides up to 880 µF of capacitance, implemented in increments of 220 µF devices, on each of the Payload Power rails, to approximate the 800 µF limit of the standard. In addition, low-level (mA) load resistors can be jumpered in across each output and return. These limited load resistors are intended primarily as reset devices between output ramp events, particularly when loaded with significant capacitance.

Table 8 lists the EVM module's output voltage nodes, and for each one indicates the associated jumper reference designators, and the resultant load value with jumper installed.

Table 8. EVM On-board Loads

OUTPUT RAIL	JUMPER	DEVICE	VALUE
SLOTA_MP	J30	C16	150 µF
	J29	R12	270 Ω
SLTB_MP	J32	C21	150 µF
	J31	R13	270 Ω
SLOTA_PWR	J25	C12	220 µF
	J26	C13	220 µF
	J27	C14	220 µF
	J28	C15	220 µF
	J24	R10	1 kΩ
SLOTB_PWR	J34	C17	220 µF
	J35	C18	220 µF
	J36	C19	220 µF
	J37	C20	220 µF
	J33	R11	1 kΩ

Banana jacks are provided along the right-hand edge of the board for connection of the user's optional test loads. The output banana jack reference designators are listed in Table 4 along with the voltage rail available at each one. Also, the net names are screen printed on the PCB, adjacent to their respective jacks.

8 Assembly Drawing and PCB Layout

The top assembly drawing and individual PCB layers for the TPS2358EVM are shown in the following figures.

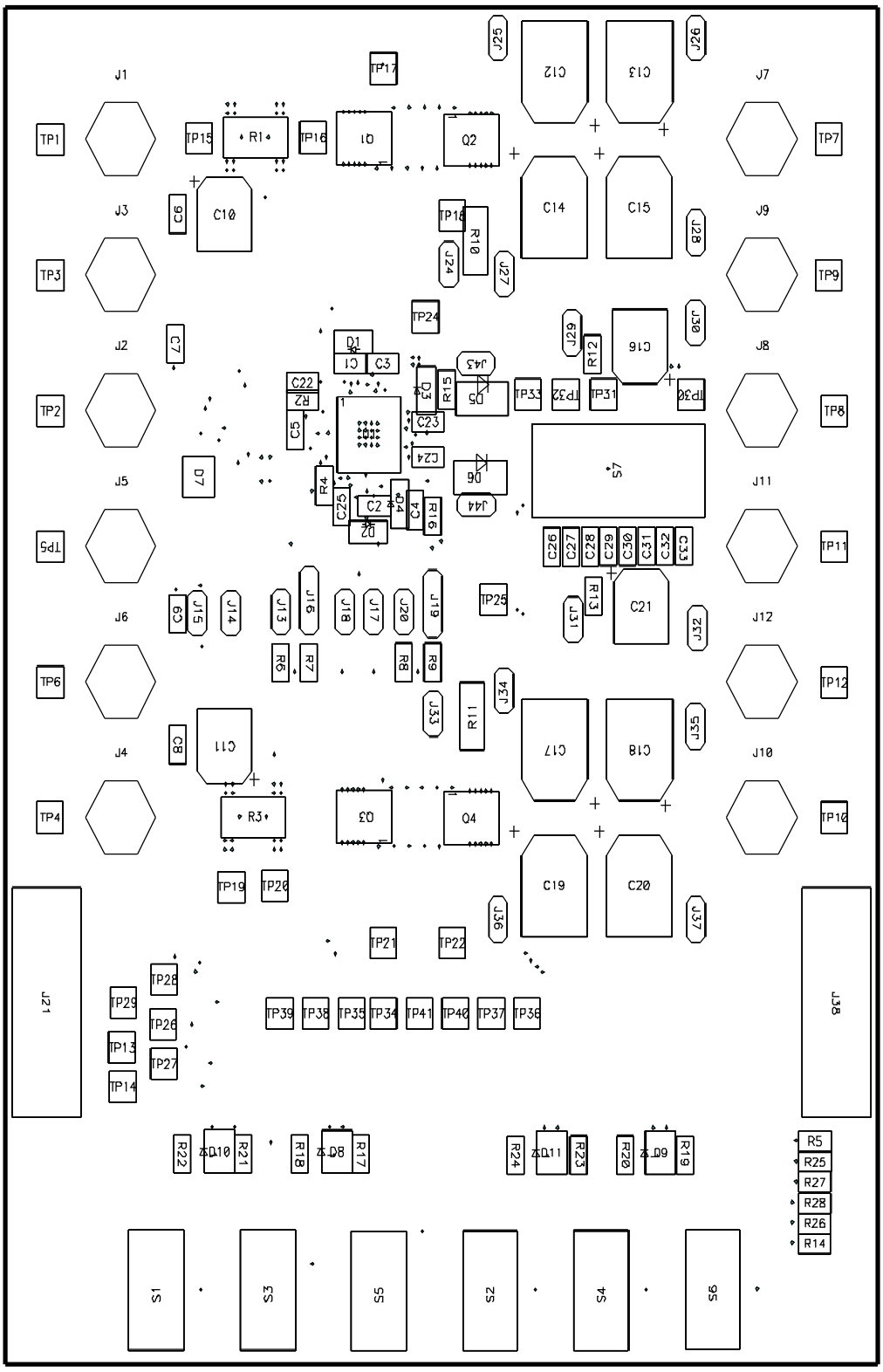


Figure 8.

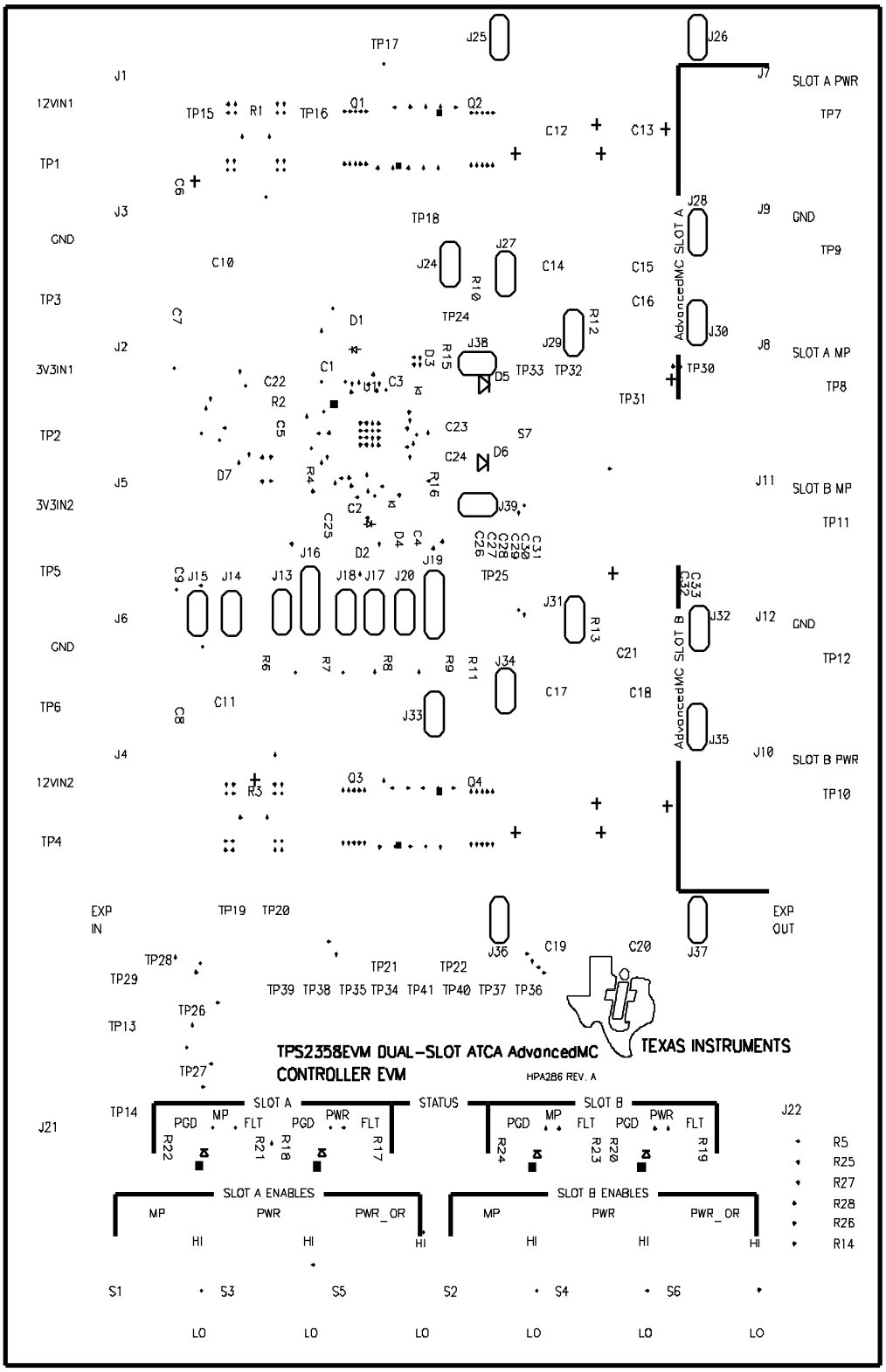

TPS2358EVM DUAL-SLOT ATCA AdvancedMC
CONTROLLER EVM
HPA286 REV. A
TEXAS INSTRUMENTS
SLOT A
STATUS
SLOT B
SLOT A ENABLES
SLOT B ENABLES
AdvancedMC SLOT A
AdvancedMC SLOT B
SLOT A PWR
SLOT A MP
SLOT B MP
SLOT B PWR
12VIN1
12VIN2
3V3IN1
3V3IN2
EXP IN
EXP OUT
GND

Figure 9.

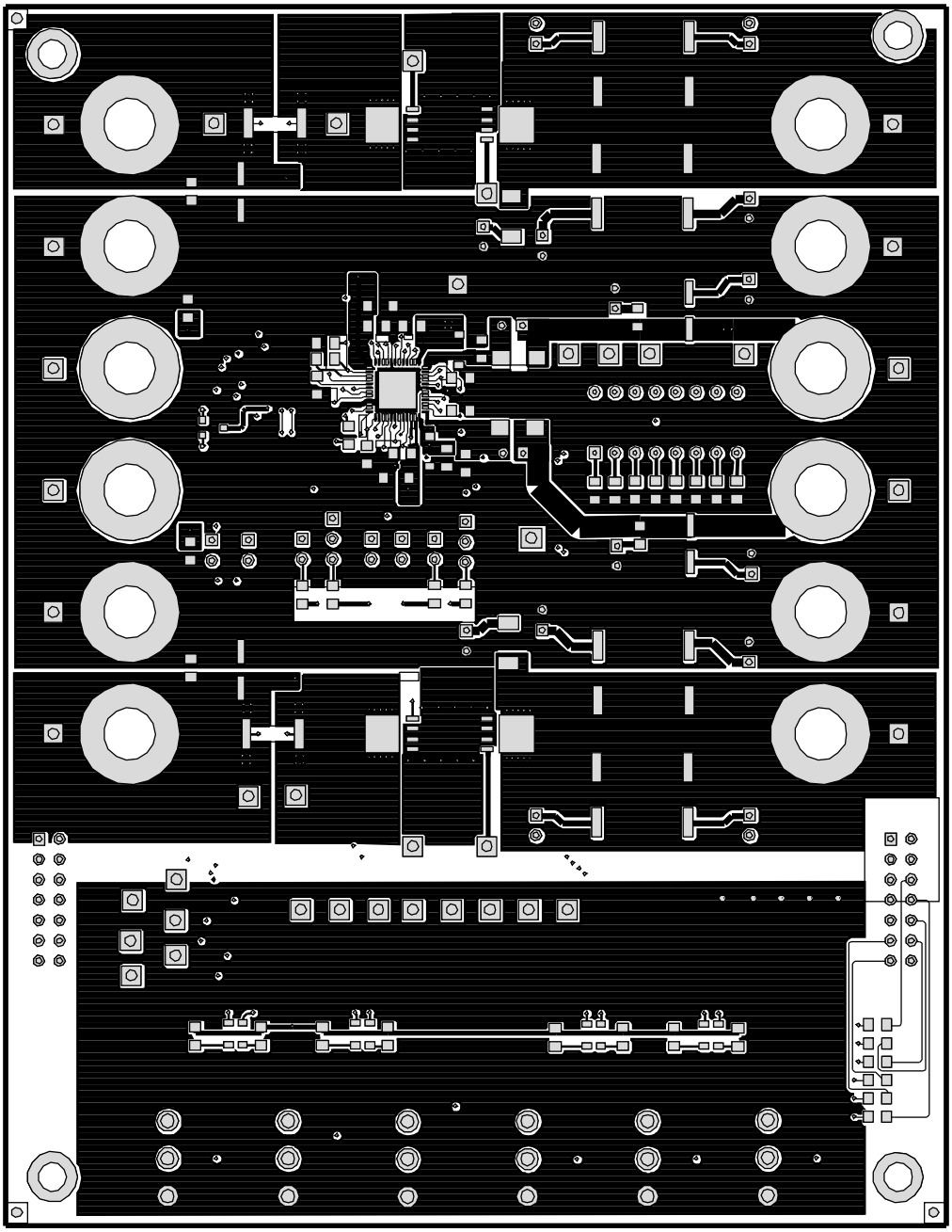


Figure 10.

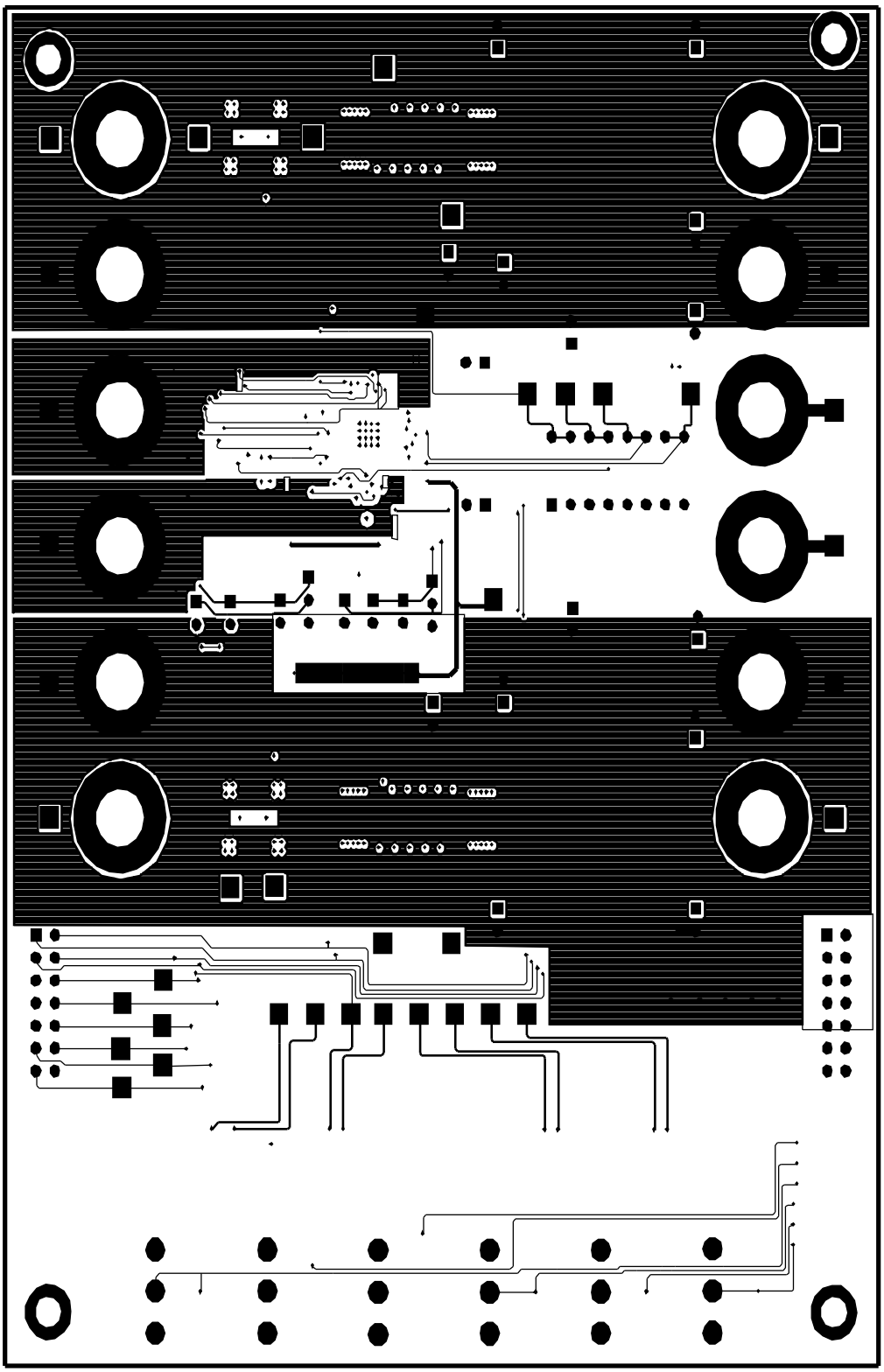


Figure 11.

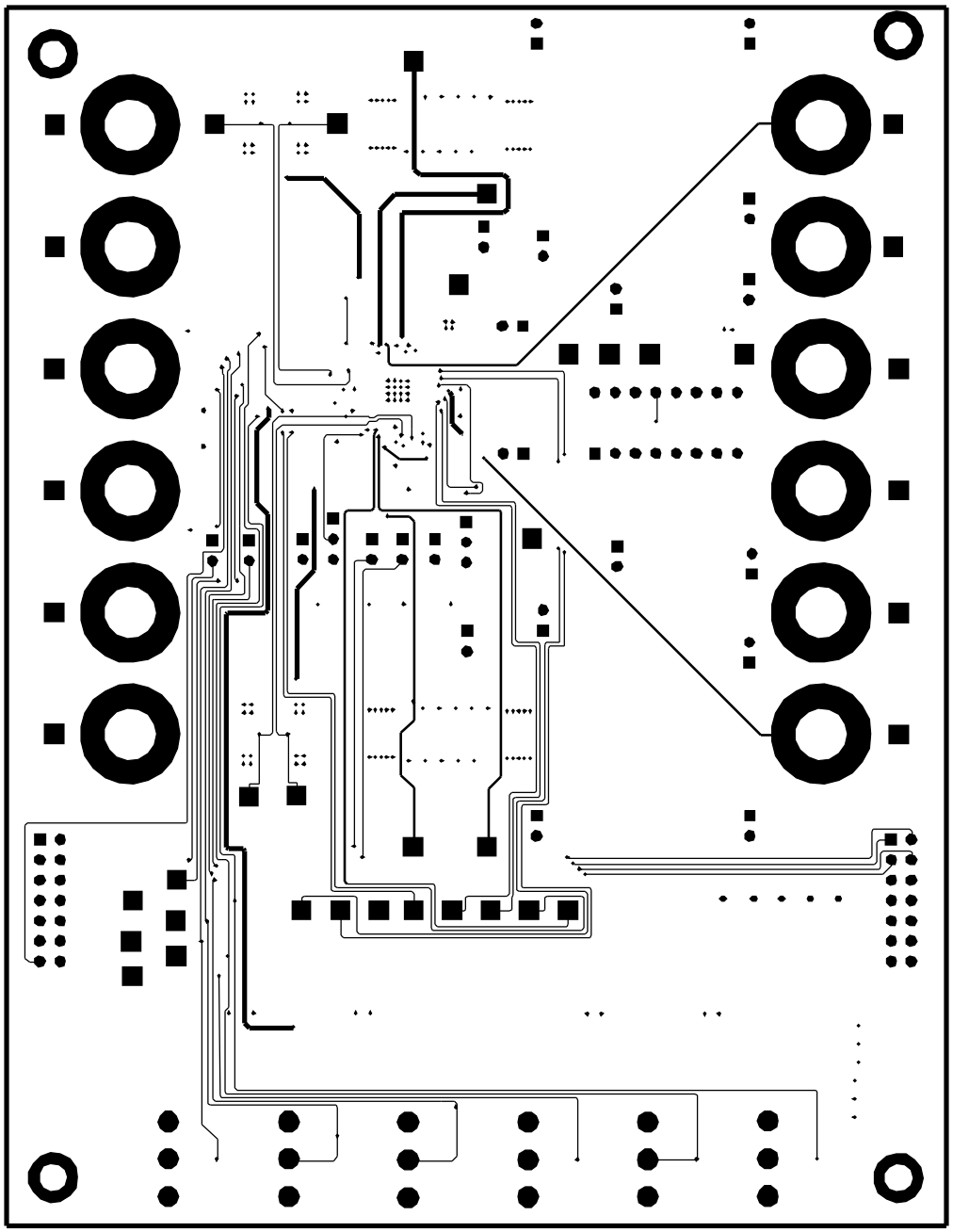


Figure 12.

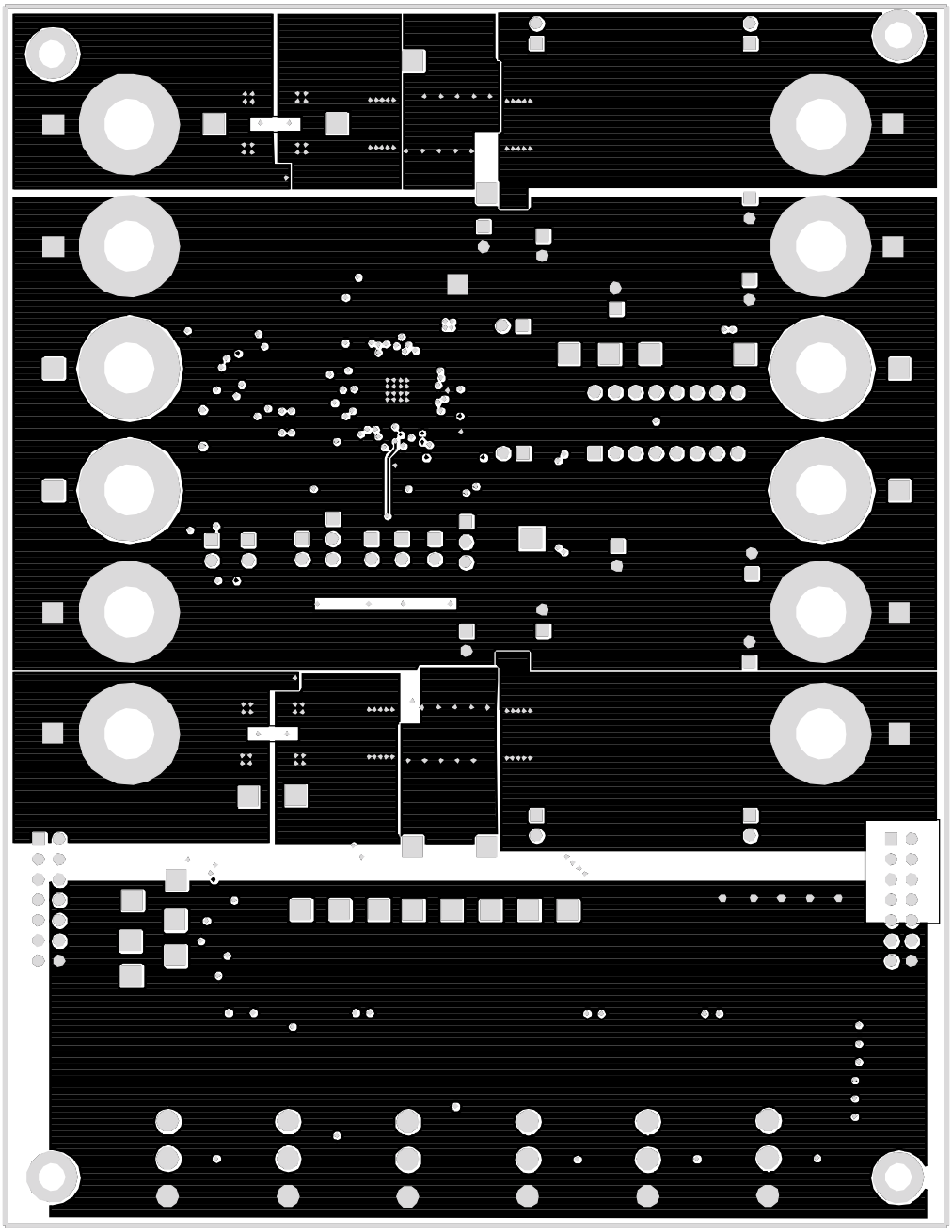


Figure 13.

9 List of Materials

Table 9. List of Materials[1]

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
5	C1, C2, C3, C4, C5	Capacitor, ceramic, 25 V, X7R, 20%, 0.1 µF, 0805	Std.	Std.
2	C10, C11	Capacitor, aluminum, SM, 25 V, 20%, 47 µF, case D	EEV-FK1E470P	Panasonic
8	C12, C13, C14, C15, C17, C18, C19, C20	Capacitor, aluminum, SM, 25 V, 20%, 220 µF, case F	EEV-FK1E221P	Panasonic
2	C16, C21	Capacitor, aluminum, SM, 10 V, 20%, 150 µF, case D	EEV-FK1A151P	Panasonic
2	C22, C25	Capacitor, ceramic, 10 V, X7R, 10%, 0.022 µF, 0805	Std.	Std.
4	C23, C24, C27, C29	Capacitor, ceramic, 10 V, X7R, 10%, 0.047 µF, 0805	Std.	Std.
2	C26, C28	Capacitor, ceramic, 10 V, X7R, 10%, 0.01 µF, 0805	Std.	Std.
2	C30, C32	Capacitor, ceramic, 10 V, X7R, 10%, 0.1 µF, 0805	Std.	Std.
0	C31, C33	Capacitor, ceramic, 10 V, X7R, 10%, USER, 0805	Std.	Std.
4	C6, C7, C8, C9	Capacitor, ceramic, 25 V, X7R, 20%, 1 µF, 0805	Std.	Std.
2	D1, D2	Diode, zener, 15 V at 50 mA, 800 mW max., Pzsm = 300 W, D0-219AB	BZD27C15P	Vishay
2	D3, D4	Diode, zener, 4.3 V, 500 mW max., SOD-123	BZT52C4V3	Diodes
2	D5, D6	Diode, Schottky, 1 A, 20 V, SMA	B120	Diodes
1	D7	Diode, dual Schottky, com, cathode, 30 V, 200 mA, SOT-23	BAT54C	Diodes
4	D8, D9, D10, D11	Diode, LED, red/green, 1210, 45/35 mcd @ 20 mA, 0.126 x 0.106in.	LTST-C155KGJRKT	Lite-On
12	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12	Jack, banana, non-ins., PC mount, TH	3267	Pomona
22	J13, J14, J15, J17, J18, J20, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39	Header, 2 pin, 100-mil spacing, 0.100 in. x 2	PEC36SAAN	Sullins
2	J16, J19	Header, 3 pin, 100-mil spacing, 0.100 in. x 3	PEC36SAAN	Sullins
2	J21, J22	Header, PCB mnt., vert., 2 x 7, 100-mil spacing, 0.100 in. x 2 x 7	2514-6002UB	3M
2	Q1, Q3	Transistor, NFET, 30 V, 100 A, $R_{DS(on)}$ < 5 mΩ, TDSON-8	"BSC016N03LSG ## or BSC022N03SG"	Infineon
2	Q2, Q4	Transistor, NFET, 30 V, $R_{DS(on)}$ < 20 mΩ, TDSON-8	"BSC057N03LSG ## or BSC050N03LSG or BSC042N03LSG or BSC022N03SG or BSC016NO3LSG"	Infineon
2	R1, R3	Resistor, metal strip, 1 W, 1%, 0.005, 2512	WSL2512-5L000FEA	Vishay-Dale
2	R10, R11	Resistor, chip, 1/2 W, 5%, 1 kΩ, 2010	Std.	Std.

(1) Part number information is for reference only to further illustrate component characteristics; substitution of other mfgrs' part of equal or better specification is permissible. Substitution NOT allowed on part numbers marked with double asterisk (**).

Table 9. List of Materials (continued)

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
2	R12, R13	Resistor, chip, 1/10 W, 5%, 270 Ω, 0805	Std.	Std.
8	R17, R18, R19, R20, R21, R22, R23, R24	Resistor, chip, 1/10 W, 5%, 470 Ω, 0805	Std.	Std.
2	R2, R4	Resistor, chip, 1/10 W, 1%, 422 Ω, 0805	Std.	Std.
0	R5, R14, R15, R16, R25, R26, R27, R28	Resistor, chip, 1/10 W, 5%, 0805,	Std.	Std.
2	R6, R7	Resistor, chip, 1/10 W, 1%, 6.81 kΩ, 0805	Std.	Std.
2	R8, R9	Resistor, chip, 1/10 W, 1%, 3.32 kΩ, 0805	Std.	Std.
6	S1, S2, S3, S4, S5, S6	Switch, slide, SPDT, vert. act., PC mount, 0.500 x 0.260 in.	"1101M2S3CBE2 or 1101M2S3CKE2 or 1101M2S3CQE2"	C&K Switch
1	S7	Switch, DIP, SPST, raised rocker, 8 pos., 0.380 x 0.880 inch	"76SB08S(T) or BD08"	"Grayhill or C&K Switch"
34	TP1, TP2, TP4, TP5, TP7, TP8, TP10, TP11, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40, TP41	Test point, white, 0.062 in. hole, TH	5012	Keystone
6	TP3, TP6, TP9, TP12, TP24, TP25	Test point, black, 0.062 in. hole, TH	5011	Keystone
1	U1	Dual-Slot ATCA AdvancedMC Controller, QFN-48	TPS2358RGZ	Texas Instruments
1	N/A	PCB, FR-4, 4-layer, SMOBC, 4.63" x 6.0" x .062"	HPA286**	Any
20	N/A	Shunt, open top	151-8000	Kobiconn
4	N/A	Spacer, nylon, hex, #6-32, 0.625"	14HTSP020	Eagle
4	N/A	Screw, nylon, rnd hd, #6-32, 0.25"	010632R025	Eagle

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