Low Capacitance, 16-Channel and 8-Channel iCMOS Multiplexers with 1.2 V and 1.8 V JEDEC Logic Compliance

FEATURES

- <1 pC charge injection over full signal range
- 1.5 pF off capacitance
- 120 Ω on resistance
- Fully specified at ±15 V/+12 V
- V_L supply for low logic-level compatibility
  - 1.8 V JEDEC standard compliant (JESD8-7A)
  - 1.2 V JEDEC standard compliant (JESD8-12A.01)
- Rail-to-rail operation
- Break-before-make switching action
- 32-lead, 5 mm × 5 mm LFCSP

APPLICATIONS

- Audio and video routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Communication systems
- FPGA and microcontroller systems

GENERAL DESCRIPTION

The ADG1206L/ADG1207L are monolithic *i*CMOS® analog multiplexers comprising sixteen single channels and eight differential channels, respectively. The ADG1206L switches one of sixteen inputs to a common output, as determined by the 4-bit binary address lines A0, A1, A2, and A3. The ADG1207L switches one of eight differential inputs to a common differential output, as determined by the 3-bit binary address lines A0, A1, and A2. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched off. When on, each channel conducts equally well in both directions and has an input signal range that extends to the supplies.

An external low voltage (V_L) supply provides flexibility for lower logic control. The ADG1206L/ADG1207L are both 1.2 V and 1.8 V JEDEC standard compliant.

FUNCTIONAL BLOCK DIAGRAMS

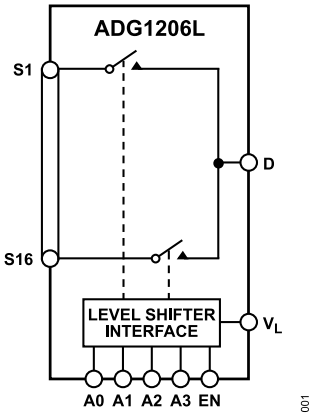


Figure 1. ADG1206L Functional Block Diagram

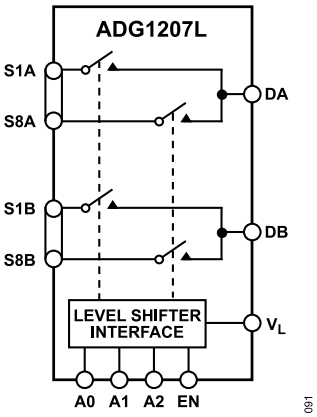


Figure 2. ADG1207L Functional Block Diagram

PRODUCT HIGHLIGHTS

1. Ultralow capacitance.
2. Guaranteed switch off when digital inputs are floating.

TABLE OF CONTENTS

REVISION HISTORY

1/2023—Revision 0: Initial Version

SPECIFICATIONS

OPERATING SUPPLY VOLTAGES

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/ Comments
SUPPLY VOLTAGE					
Dual	±5		±16.5	V	Positive supply voltage (V_{DD}) to negative supply voltage (V_{SS})
Single	5		16.5	V	V_{DD} to GND, V_{SS} = GND = 0 V
DIGITAL VOLTAGE					
Single	1.1		1.3	V	Logic power supply voltage (V_L) to GND, logic control input voltage (V_{Ax}) = 1.2 V logic
	1.65		1.95	V	V_L to GND, V_{Ax} = 1.8 V logic

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V, V_L = 1.1 V to 1.95 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +13.5 V, V_{SS} = −13.5 V
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	120			Ω typ	V_S = ±10 V, I_S = −1 mA, see Figure 27
	200	240	270	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	3.5			Ω typ	V_S = ±10 V, I_S = −1 mA
	6	10	12	Ω max	
On-Resistance Flatness (R_{FLAT}) (On)	20			Ω typ	V_S = ±5 V, I_S = −1 mA
	64	76	83	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage (I_S) (Off)	±0.03			nA typ	V_D = ±10 V, V_S = ∓10 V, see Figure 28
	±0.2	±0.6	±1	nA max	
Drain Off Leakage (I_D) (Off)	±0.05			nA typ	V_D = ±10 V, V_S = ∓10 V, see Figure 28
	±0.2	±0.6	±2	nA max	
Channel On Leakage (I_D, I_S) (On)	±0.08			nA typ	V_S = V_D = ±10 V, see Figure 29
	±0.2	±0.6	±2	nA max	
DIGITAL INPUTS					
Input High Voltage (V_{INH})			0.65 × V_L	V min	
Input Low Voltage (V_{INL})			0.35 × V_L	V max	
Input High Current (I_{INH})	55			µA typ	V_{Ax} = V_L = 1.8 V, see the Theory of Operations section
			90	µA max	
	40			µA typ	V_{Ax} = V_L = 1.2 V, see the Theory of Operations section
			65	µA max	
Input Low Current (I_{INL})	2.5			µA typ	V_{Ax} = 0 V
			8	µA max	
Digital Input Capacitance (C_{IN})	5			pF typ	
DYNAMIC CHARACTERISTICS					

SPECIFICATIONS

Table 2. (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Transition Time ($t_{TRANSITION}$)	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	154	182	204	ns max	V_S = 10 V, see Figure 30
Enable Delay On Time (t_{ON}) (EN)	96			ns typ	R_L = 300 Ω, C_L = 35 pF
	120	133	147	ns max	V_S = 10 V, see Figure 32
Enable Delay Off Time (t_{OFF}) (EN)	130			ns typ	R_L = 300 Ω, C_L = 35 pF
	156	180	196	ns max	V_S = 10 V, see Figure 32
Break-Before-Make Time Delay (t_{BBM})	25			ns typ	R_L = 300 Ω, C_L = 35 pF
			22	ns min	V_{S1} = V_{S2} = 10 V, see Figure 31
Charge Injection	0.6			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 33
Off Isolation	−79			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34
Channel-to-Channel Crosstalk	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 36
Total Harmonic Distortion (THD)	−57			dB typ	R_L = 10 kΩ, 5 V_{RMS}, f = 20 Hz to 20 kHz
Total Harmonic Distortion Plus Noise (THD+N)	0.15			% typ	R_L = 10 kΩ, 5 V_{RMS}, f = 20 Hz to 20 kHz, see Figure 37
−3 dB Bandwidth, ADG1206L	280			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 35
−3 dB Bandwidth, ADG1207L	490			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 35
Insertion Loss	−6.5			dB typ	R_L = 50 Ω, C_L = 5 pF, see Figure 35
Source Off Capacitance (C_S) (Off)	1.5			pF typ	V_S = 0 V, f = 1 MHz
	2			pF max	V_S = 0 V, f = 1 MHz
Drain Off Capacitance (C_D) (Off), ADG1206L	11			pF typ	V_S = 0 V, f = 1 MHz
	12			pF max	V_S = 0 V, f = 1 MHz
Drain Off Capacitance (C_D) (Off), ADG1207L	7			pF typ	V_S = 0 V, f = 1 MHz
	9			pF max	V_S = 0 V, f = 1 MHz
Drain On Capacitance (C_D) (On), Source On Capacitance (C_S) (On), ADG1206L	13			pF typ	V_S = 0 V, f = 1 MHz
	15			pF max	V_S = 0 V, f = 1 MHz
Drain On Capacitance (C_D) (On), Source On Capacitance (C_S) (On), ADG1207L	8			pF typ	V_S = 0 V, f = 1 MHz
	10			pF max	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Positive Supply Current (I_{DD})	55			μA typ	V_{Ax} = 0 V or V_L
			95	μA max	
Negative Supply Current (I_{SS})	0.001			μA typ	V_{Ax} = 0 V or V_L
			1	μA max	
Digital Supply Current (I_{VL})	45			μA typ	V_{Ax} = V_L = 1.8 V
			70	μA max	
	30			μA typ	V_{Ax} = V_L = 1.2 V
			55	μA max	

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, V_L = 1.1 V to 1.95 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 10.8 V, V_{SS} = 0 V
Analog Signal Range			0 to V_{DD}	V	
On Resistance (R_{ON})	300			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA, see Figure 27
	475	567	625	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	5			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA

SPECIFICATIONS

Table 3. (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
	16	26	27	Ω max	
On-Resistance Flatness (R_{FLAT}) (On)	60			Ω typ	V_S = 3 V to 9 V, I_S = −1 mA
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage (I_S) (Off)	±0.02			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V, see Figure 28
	±0.2	±0.6	±1	nA max	
Drain Off Leakage (I_D) (Off)	±0.05			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V, see Figure 28
	±0.2	±0.6	±2	nA max	
Channel On Leakage (I_D, I_S) (On)	±0.08			nA typ	V_S = V_D = 1 V to 10 V, see Figure 29
	±0.2	±0.6	±2	nA max	
DIGITAL INPUTS					
Input High Voltage (V_{INH})			0.65×V_L	V min	
Input Low Voltage (V_{INL})			0.35×V_L	V max	
Input High Current (I_{INH})	55			µA typ	V_{Ax} = V_L = 1.8 V, see the Theory of Operations section
			90		
	40			µA typ	V_{Ax} = V_L = 1.2 V, see the Theory of Operations section
			65	µA max	
Input Low Current (I_{INL})	2.5			µA typ	V_{Ax} = 0 V
			8		
Digital Input Capacitance (C_{IN})	5			pF typ	
DYNAMIC CHARACTERISTICS					
Transition Time ($t_{TRANSITION}$)	140			ns typ	R_L = 300 Ω, C_L = 35 pF
	201	242	275	ns max	V_S = 8 V, see Figure 30
Enable Delay On Time (t_{ON}) (EN)	128			ns typ	R_L = 300 Ω, C_L = 35 pF
	161	190	207	ns max	V_S = 8 V, see Figure 32
Enable Delay Off Time (t_{OFF}) (EN)	150			ns typ	R_L = 300 Ω, C_L = 35 pF
	184	211	230	ns max	V_S = 8 V, see Figure 32
Break-Before-Make Time Delay (t_{BBM})	40			ns typ	R_L = 300 Ω, C_L = 35 pF
			33	ns min	V_{S1} = V_{S2} = 8 V, see Figure 31
Charge Injection	0.3			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 33
Off Isolation	−79			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34
Channel-to-Channel Crosstalk	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 36
Total Harmonic Distortion (THD)	−41			dB typ	R_L = 10 kΩ, 5 V_{RMS}, f = 20 Hz to 20 kHz, see Figure 36
Total Harmonic Distortion Plus Noise (THD + N)	0.81			% typ	R_L = 10 kΩ, 5 V_{RMS}, f = 20 Hz to 20 kHz, see Figure 36
−3 dB Bandwidth, ADG1206L	185			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 35
−3 dB Bandwidth, ADG1207L	300			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 35
Insertion Loss	−12.1			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 35
Source Off Capacitance (C_S) (Off)	1.5			pF typ	Source voltage (V_S) = 6 V, f = 1 MHz
	2			pF max	V_S = 6 V, f = 1 MHz
Drain Off Capacitance (C_D) (Off), ADG1206L	13			pF typ	V_S = 6 V, f = 1 MHz
	15			pF max	V_S = 6 V, f = 1 MHz
Drain Off Capacitance (C_D) (Off), ADG1207L	9			pF typ	V_S = 6 V, f = 1 MHz
	11			pF max	V_S = 6 V, f = 1 MHz
Drain On Capacitance (C_D) (On), Source On Capacitance (C_S) (On), ADG1206L	15			pF typ	V_S = 6 V, f = 1 MHz
	17			pF max	V_S = 6 V, f = 1 MHz

SPECIFICATIONS

Table 3. (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Drain On Capacitance (C_D) (On), Source On Capacitance (C_S) (On), ADG1207L	10			pF typ	V_S = 6 V, f = 1 MHz
	12			pF max	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Positive Supply Current (I_{DD})	55			µA typ	V_{Ax} = 0 V or V_L
			95	µA max	
Digital Supply Current (I_{VL})	45			µA typ	V_{Ax} = V_L = 1.8 V
			70	µA max	
	30			µA typ	V_{Ax} = V_L = 1.2 V
			55	µA max	

CONTINUOUS CURRENT PER CHANNEL, SXA, SXB, OR DX

Table 4. ADG1206L, One Channel On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx or Dx (θ_{JA} = 63.8°C/W)[1]				
V_{DD} = +15 V, V_{SS} = −15 V	36	9.8	2.5	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V	32	9.5	2.5	mA maximum

[1] Sx refers to the S1 to S16 pins. Dx refers to D1.

Table 5. ADG1207L, Two Channels On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx or Dx (θ_{JA} = 63.8°C/W)[1]				
V_{DD} = +15 V, V_{SS} = −15 V	27.5	9	2.5	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V	24.6	8.6	2.5	mA maximum

[1] Sx refers to the S1A to S8A and S1B to S8B pins. Dx refers to DA and DB pins.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
V_L to GND	−0.3 V to +2.25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[2]	GND − 0.3 V to 2.25 V, or 30 mA, whichever occurs first
Peak Current, Sx or Dx[3]	78 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx[3]	Data[4] + 15%
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb-Free	As per JEDEC J-STD-020

1 Overvoltages at A, EN, S, or D are clamped by internal diodes. Current must be limited to the maximum ratings given.

2 Overvoltages at the Ax and EN digital input pins are clamped by internal diodes.

3 Sx refers to the S1 to S16. Dx refers to DA and DB.

4 See Table 3 and Table 4.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JC} is the function to the bottom of the case value.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-32-7[1]	63.8	32.8	°C/W

1 Thermal impedance simulated values are based on the JEDEC 2S2P thermal test board without thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADG1206L/ADG1207L

Table 8. ADG1206L/ADG1207L, 32-Lead LFCSP

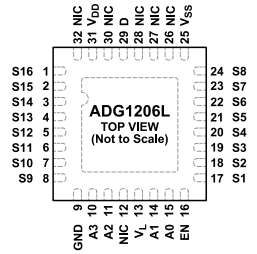
ESD Model	Withstand Threshold (kV)	Class
HBM[1]	±2	1C
FICDM	±1.25	C3

1 This is the HBM for the input/output port to supplies, the input/output port to input/output port, and for all other inputs.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NO INTERNAL CONNECTION.
2. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE EXPOSED PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

002

Figure 3. ADG1206L Pin Configuration

Table 9. ADG1206L Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S16	Source Terminal 16. Can be an input or an output.
2	S15	Source Terminal 15. Can be an input or an output.
3	S14	Source Terminal 14. Can be an input or an output.
4	S13	Source Terminal 13. Can be an input or an output.
5	S12	Source Terminal 12. Can be an input or an output.
6	S11	Source Terminal 11. Can be an input or an output.
7	S10	Source Terminal 10. Can be an input or an output.
8	S9	Source Terminal 9. Can be an input or an output.
9	GND	Ground (0 V) Reference.
10	A3	Logic Control Input.
11	A2	Logic Control Input.
12, 26, 27, 28, 30, 32	NIC	No Internal Connection.
13	V_L	Logic Power Supply Potential.
14	A1	Logic Control Input.
15	A0	Logic Control Input.
16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
17	S1	Source Terminal 1. Can be an input or an output.
18	S2	Source Terminal 2. Can be an input or an output.
19	S3	Source Terminal 3. Can be an input or an output.
20	S4	Source Terminal 4. Can be an input or an output.
21	S5	Source Terminal 5. Can be an input or an output.
22	S6	Source Terminal 6. Can be an input or an output.
23	S7	Source Terminal 7. Can be an input or an output.
24	S8	Source Terminal 8. Can be an input or an output.
25	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
29	D	Drain Terminal. Can be an input or an output.
31	V_{DD}	Most Positive Power Supply Potential.
	EPAD	Exposed Pad. The exposed pad must be tied to the substrate, V_{SS}.

Table 10. ADG1206L Truth Table

A3	A2	A1	A0	EN	On Switch
X[1]	X[1]	X[1]	X[1]	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 10. ADG1206L Truth Table (Continued)

A3	A2	A1	A0	EN	On Switch
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

[1] X = don't care.

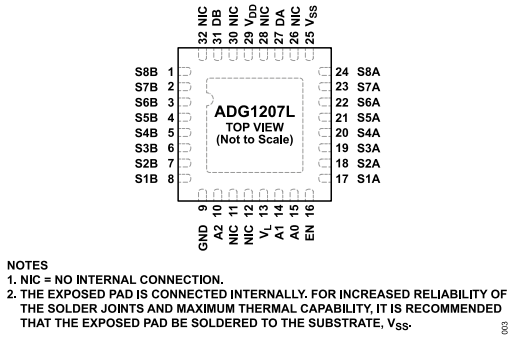


Figure 4. ADG1207L Pin Configuration

Table 11. ADG1207L Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S8B	Source Terminal 8B. Can be an input or an output.
2	S7B	Source Terminal 7B. Can be an input or an output.
3	S6B	Source Terminal 6B. Can be an input or an output.
4	S5B	Source Terminal 5B. Can be an input or an output.
5	S4B	Source Terminal 4B. Can be an input or an output.
6	S3B	Source Terminal 3B. Can be an input or an output.
7	S2B	Source Terminal 2B. Can be an input or an output.
8	S1B	Source Terminal 1B. Can be an input or an output.
9	GND	Ground (0 V) Reference.
10	A2	Logic Control Input.
11, 12, 26, 28, 30, 32	NIC	No Internal Connection.
13	V_L	Logic Power Supply Potential
14	A1	Logic Control Input.
15	A0	Logic Control Input.
16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
17	S1A	Source Terminal 1A. Can be an input or an output.
18	S2A	Source Terminal 2A. Can be an input or an output.
19	S3A	Source Terminal 3A. Can be an input or an output.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 11. ADG1207L Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
20	S4A	Source Terminal 4A. Can be an input or an output.
21	S5A	Source Terminal 5A. Can be an input or an output.
22	S6A	Source Terminal 6A. Can be an input or an output.
23	S7A	Source Terminal 7A. Can be an input or an output.
24	S8A	Source Terminal 8A. Can be an input or an output.
25	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
27	DA	Drain Terminal A. Can be an input or an output.
29	V_{DD}	Most Positive Power Supply Potential.
31	DB	Drain Terminal B. Can be an input or an output.
	EPAD	Exposed Pad. The exposed pad must be tied to the substrate, V_{SS}.

Table 12. ADG1207L Truth Table

A2	A1	A0	EN	On Switch Pair
X[1]	X[1]	X[1]	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

[1] X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

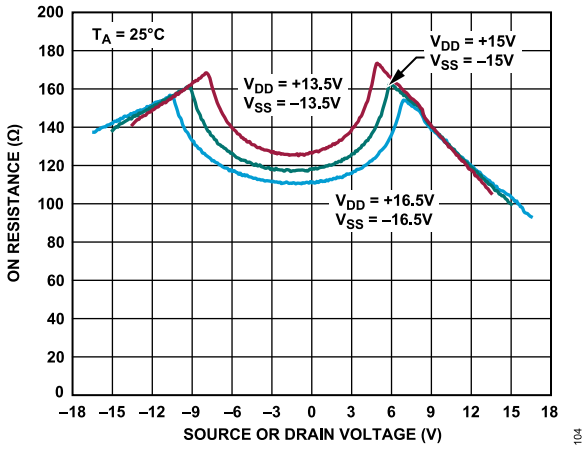


Figure 5. On Resistance as a Function of V_D (V_S) for 15 V ± 10% Dual Supply

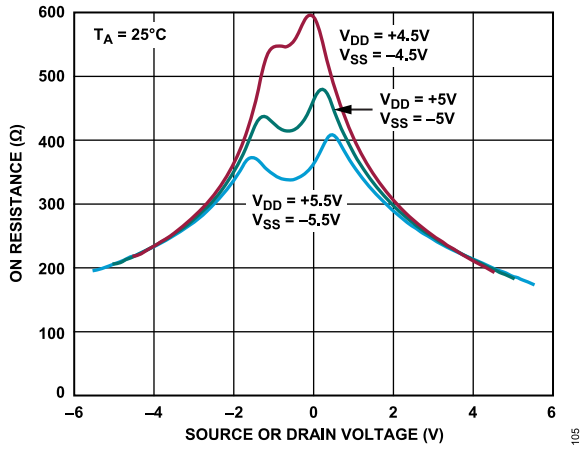


Figure 6. On Resistance as a Function of V_D (V_S) for 5 V ± 10% Dual Supply

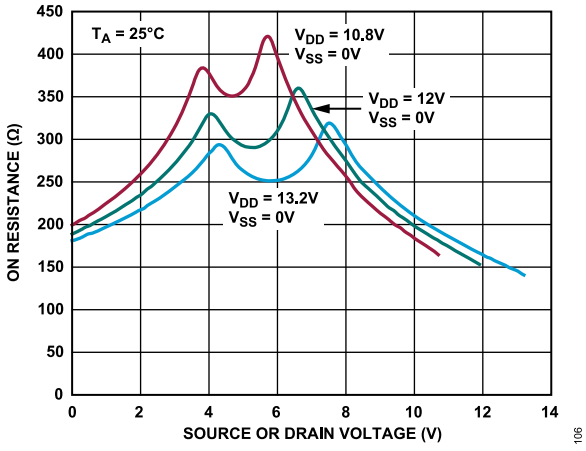


Figure 7. On Resistance as a Function of V_D (V_S) for 12 V ± 10% Single Supply

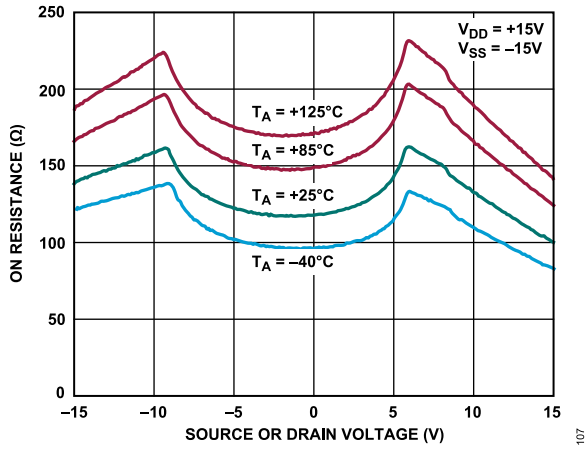


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

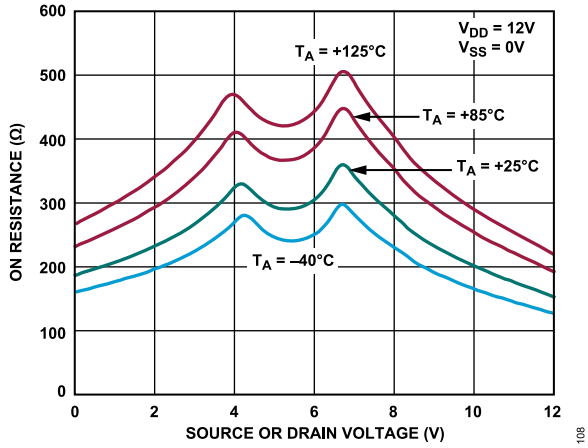


Figure 9. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

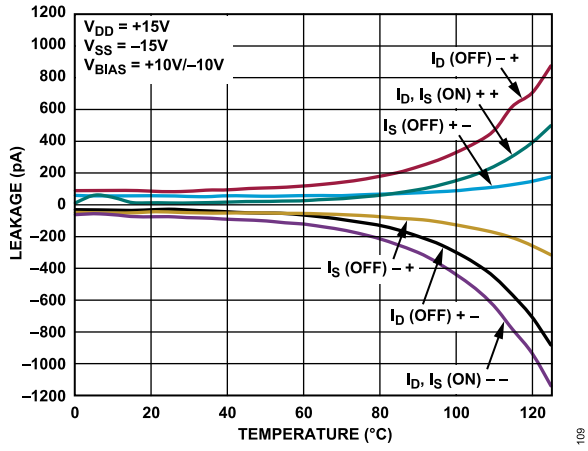


Figure 10. ADG1206L Leakage Currents as a Function of Temperature, Dual Supply

TYPICAL PERFORMANCE CHARACTERISTICS

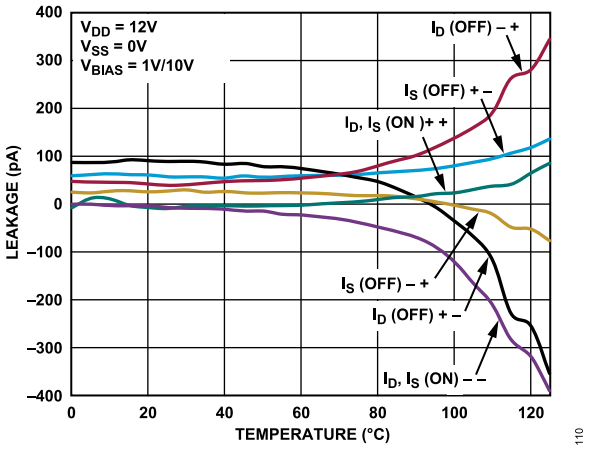


Figure 11. ADG1206L Leakage Currents as a Function of Temperature, Single Supply

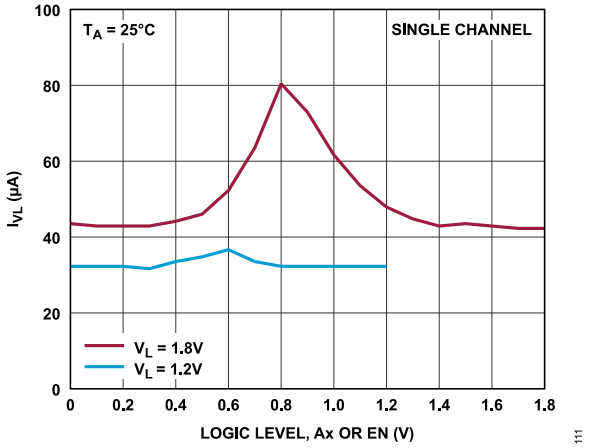


Figure 12. I_{VL} vs. Logic Level

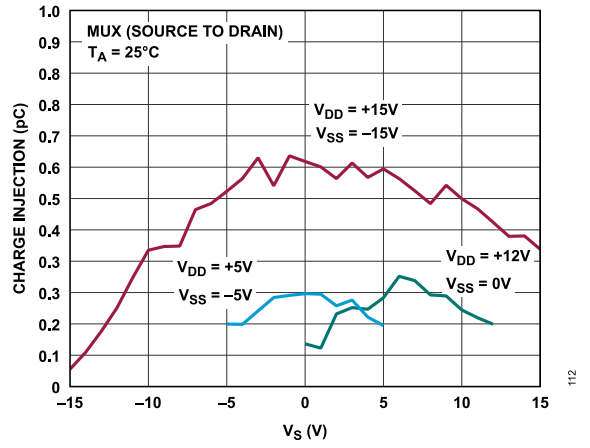


Figure 13. Charge Injection vs. V_S, Source-to-Drain

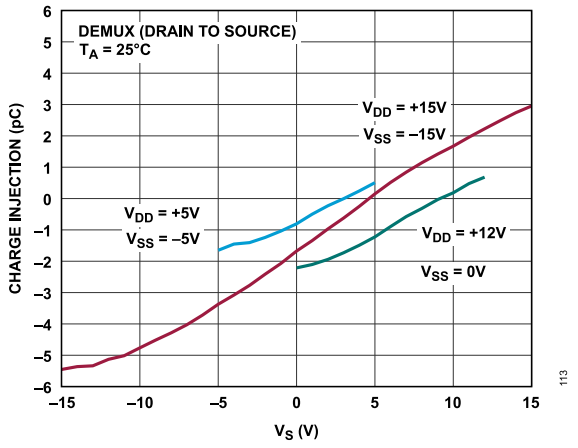


Figure 14. Charge Injection vs. V_S, Drain-to-Source

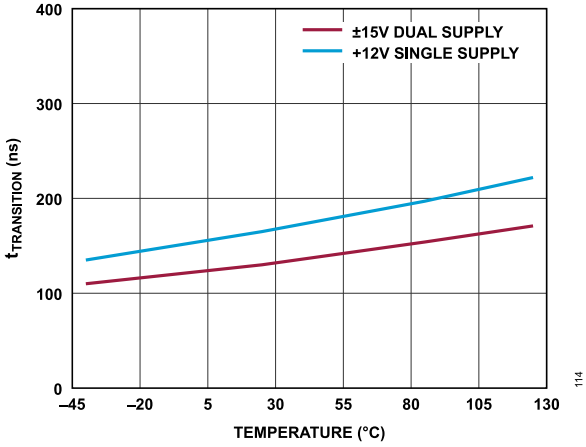


Figure 15. Transition Time ($t_{TRANSITION}$) vs. Temperature

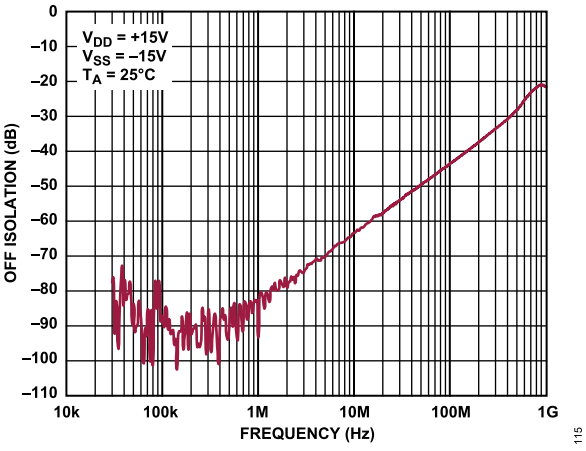


Figure 16. Off Isolation vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

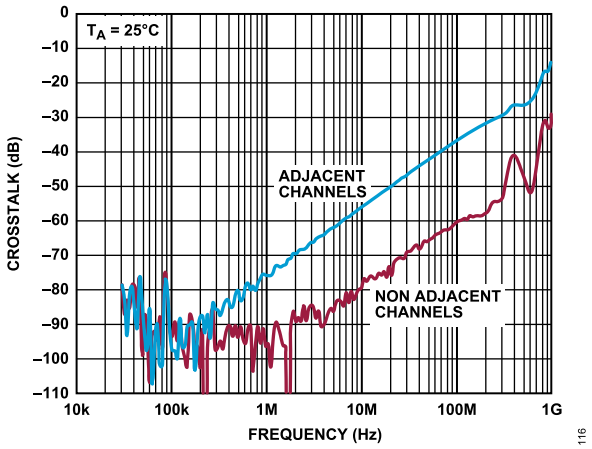


Figure 17. Crosstalk vs. Frequency, ADG1206L

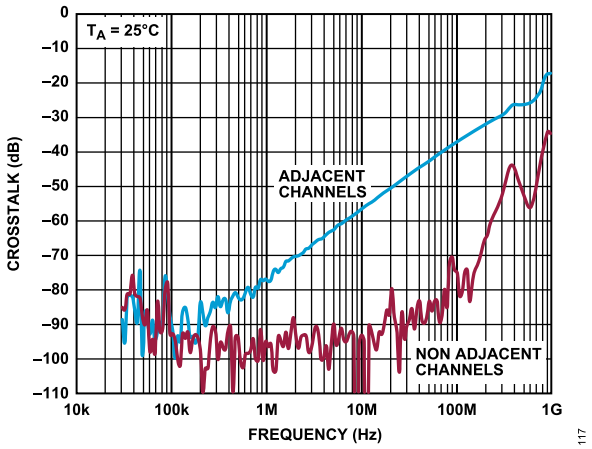


Figure 18. Crosstalk vs. Frequency, ADG1207L

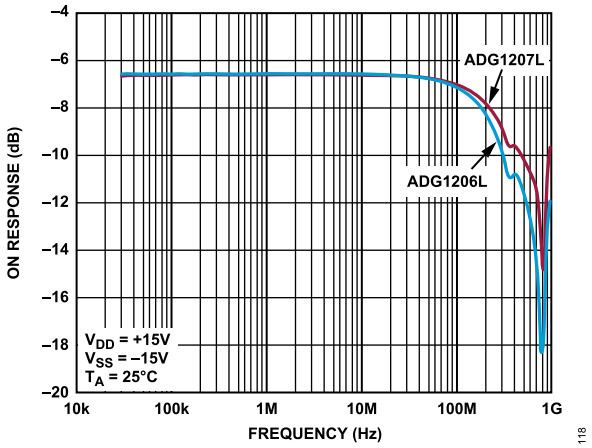


Figure 19. On Response vs. Frequency

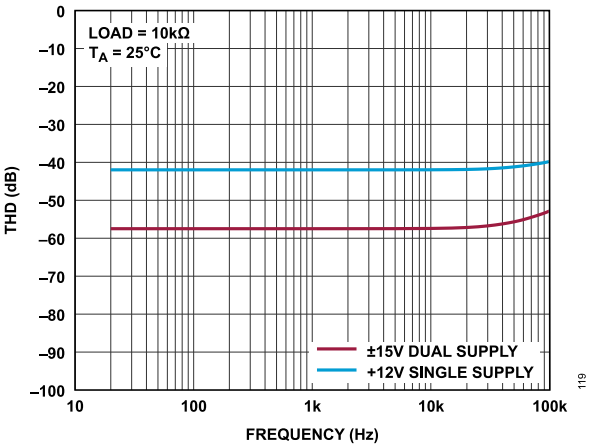


Figure 20. THD vs. Frequency

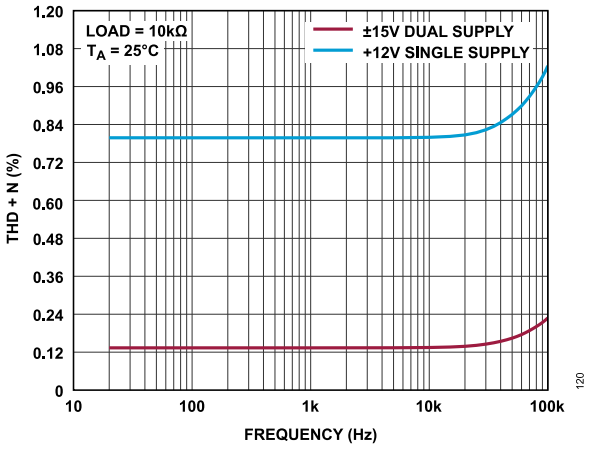


Figure 21. THD + N vs. Frequency

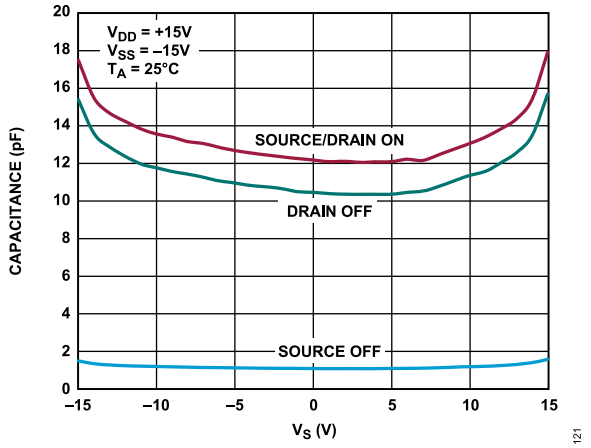


Figure 22. Capacitance vs. V_S, ±15 V Dual Supply, ADG1206L

TYPICAL PERFORMANCE CHARACTERISTICS

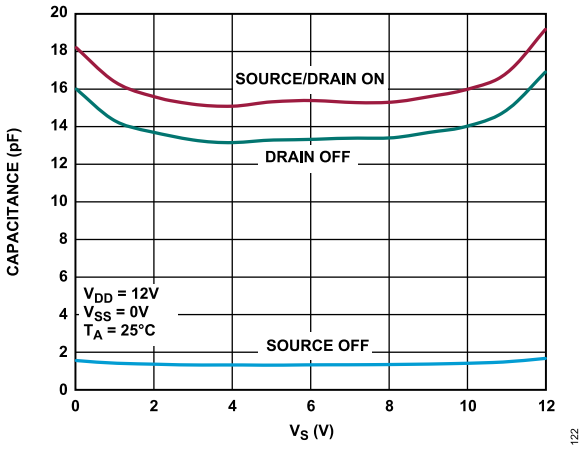


Figure 23. Capacitance vs. V_S, 12 V Single Supply, ADG1206L

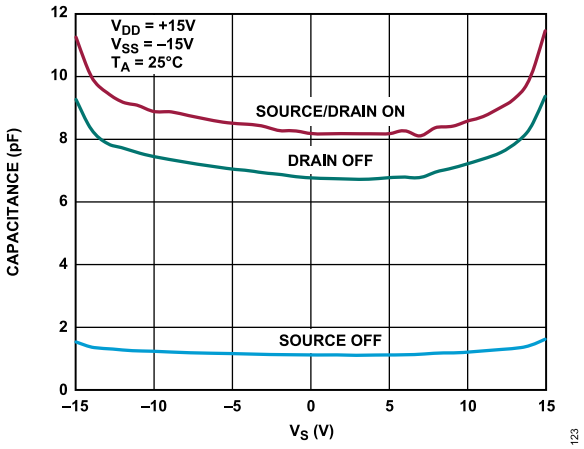


Figure 24. Capacitance vs. V_S, ±15 V Dual Supply, ADG1207L

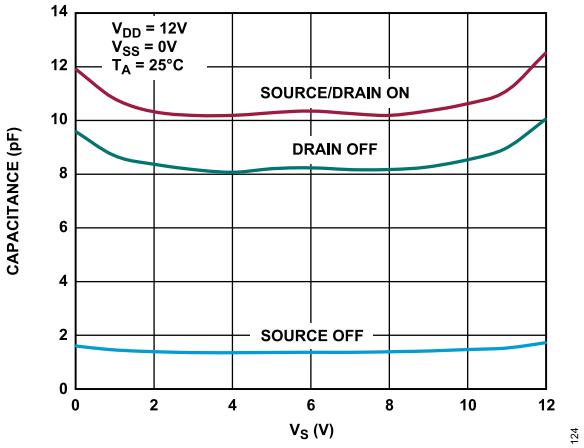


Figure 25. Capacitance vs. V_S, 12 V Single Supply, ADG1207L

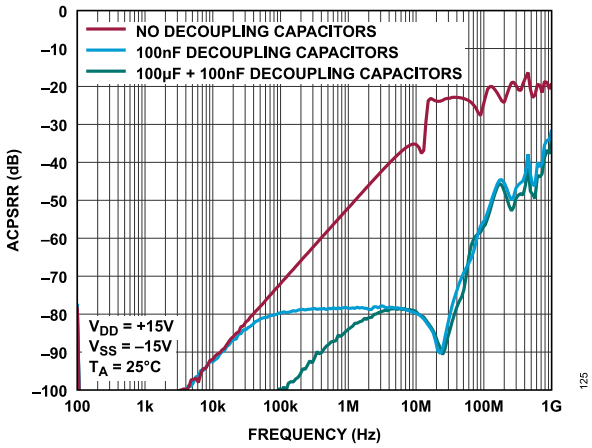


Figure 26. ACPSRR vs. Frequency

TEST CIRCUITS

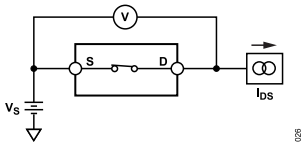


Figure 27. On Resistance (I_{DS} is the Drain to Source Current)

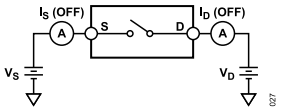


Figure 28. Off Leakage

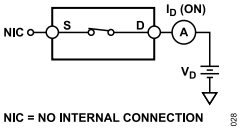


Figure 29. On Leakage

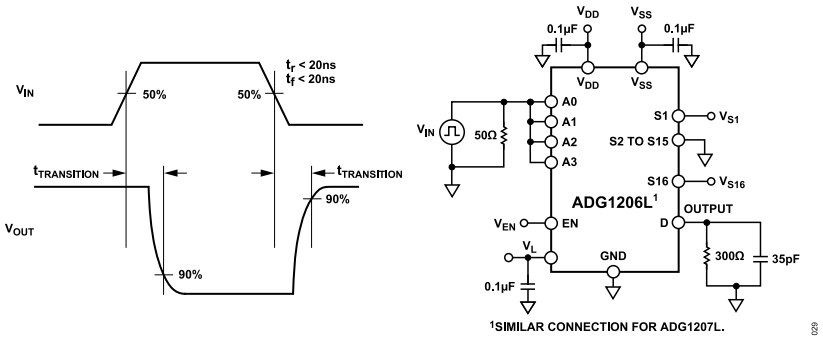


Figure 30. Address to Output Switching Times, $t_{TRANSITION}$ (V_{OUT} is the Output Voltage)

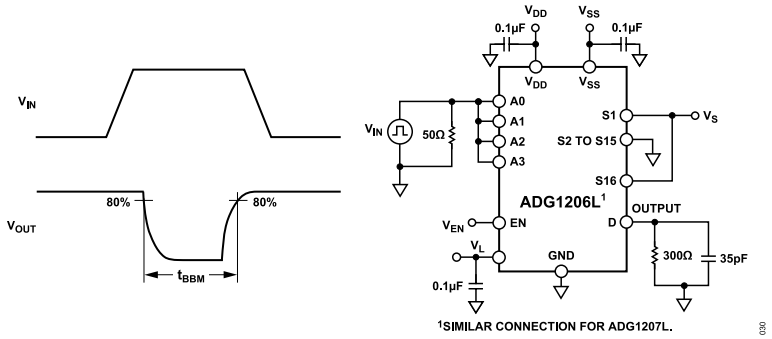


Figure 31. Break-Before-Make Delay, t_{BBM}

TEST CIRCUITS

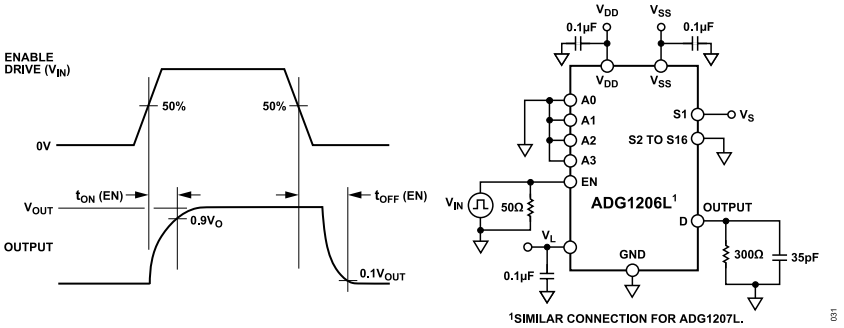


Figure 32. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

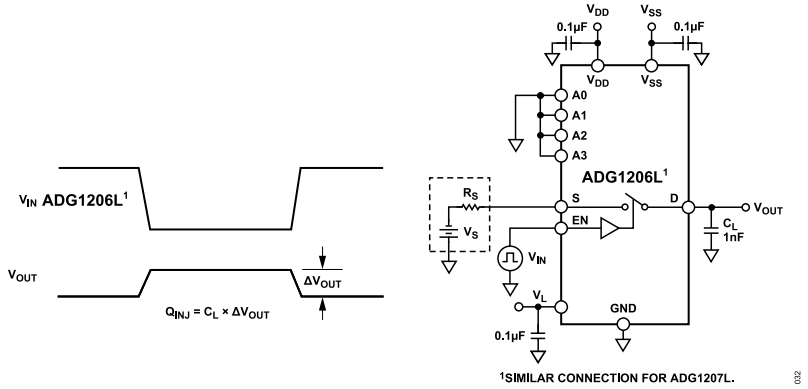


Figure 33. Charge Injection

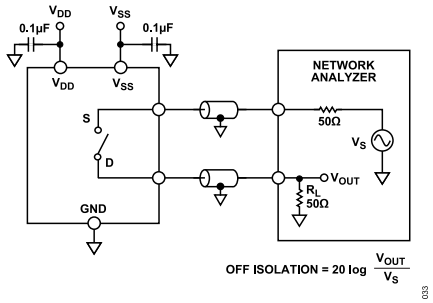


Figure 34. Off Isolation

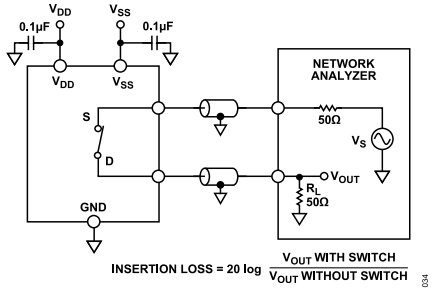


Figure 35. Bandwidth

TEST CIRCUITS

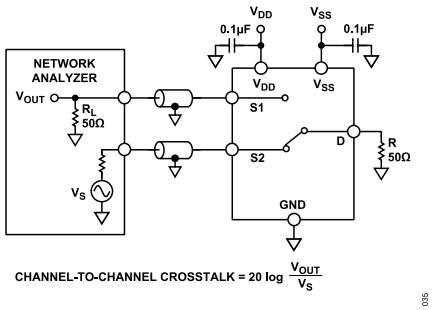


Figure 36. Channel-to-Channel Crosstalk

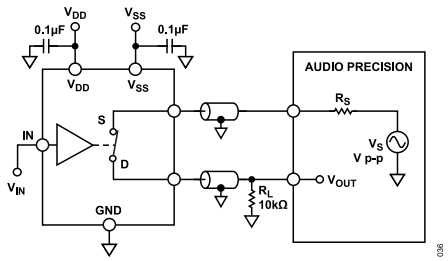


Figure 37. THD + Noise

TERMINOLOGY

R_{ON}

R_{ON} is the ohmic resistance between D and S.

ΔR_{ON}

ΔR_{ON} is the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

$R_{FLAT(ON)}$ is defined as the difference between the maximum and minimum value of on resistance as measured.

I_S (Off)

I_S (off) is the source leakage current when the switch is off.

I_D (Off)

I_D (off) is the drain leakage current when the switch is off.

I_D, I_S (On)

I_D and I_S (on) is the channel leakage current when the switch is on.

V_D (V_S)

V_D (V_S) is the analog voltage on Terminals D and S.

C_S (Off)

C_S (off) is the channel input capacitance for the off condition.

C_D (Off)

C_D (off) is the channel output capacitance for the off condition.

C_D, C_S (On)

C_D and C_S (on) is the on switch capacitance.

C_{IN}

C_{IN} is the digital input capacitance.

t_{ON} (EN)

t_{ON} (EN) is the delay time between the 50% and 90% points of the digital input and the switch on condition.

t_{OFF} (EN)

t_{OFF} (EN) is the delay time between the 50% and 90% points of the digital input and the switch off condition.

$t_{TRANSITION}$

$t_{TRANSITION}$ is the delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{BBM}

t_{BBM} is the off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} is the input current of the digital input.

I_{DD}

I_{DD} is the positive supply current.

I_{SS}

I_{SS} is the negative supply current.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off channel.

Chanel-to-Channel Crosstalk

Channel-to-channel crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

−3 dB Bandwidth

The −3 dB bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response

On response is the frequency response of the on switch.

Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion (THD)

THD is the sum of the powers of all harmonic components to the power of the fundamental frequency.

Total Harmonic Distortion Plus Noise (THD + N)

THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR measures the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by

TERMINOLOGY

a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

THEORY OF OPERATIONS

SWITCH ARCHITECTURE

The ADG1206L/ADG1207L are multiplexers that are compatible with 1.2 V or 1.8 V logic depending on the V_L input.

V_L FLEXIBILITY

An external V_L supply provides logic control flexibility for lower logic levels.

The following V_L conditions must be satisfied for the switch to operate in either 1.2 V or 1.8 V logic operation:

- 1.2 V logic: V_L = 1.1 V to 1.3 V
- 1.8 V logic: V_L = 1.65 V to 1.95 V

1.2 V AND 1.8 V JEDEC COMPLIANCE

The ADG1206L/ADG1207L are both 1.2 V and 1.8 V JEDEC standard compliant (normal range) to the digital input threshold. This compliance with the digital-input threshold ensures low voltage CMOS logic compatibility when operating with a valid logic power-supply range.

The following are the switch digital input requirements for both 1.2 V and 1.8 V logic:

- $V_{INH} = 0.65 \times V_L$
- $V_{INL} = 0.35 \times V_L$

INITIALIZATION TIME

The digital section of the ADG1206L/ADG1207L go through an initialization phase during V_{DD}, V_{SS}, and V_L power up. After V_{DD}, V_{SS}, and V_L power-up, ensure that there is a minimum of 50 µs from the time of power-up before any digital input is issued.

Ensure that V_{DD}, V_{SS}, and V_L do not drop out during the 50 µs initialization phase because it may result in an incorrect timing performance of the ADG1206L/ADG1207L.

SWITCHES IN A KNOWN STATE

The ADG1206L/ADG1207L switches are off when the digital inputs are floating, which prevents unwanted signals passing through the switches. This built-in feature of the ADG1206L/ADG1207L eliminates the need for an external pull-down resistor to be installed. The ADG1206L/ADG1207L can pull-down floating digital inputs against leakage currents up to half of I_{INH}.

APPLICATIONS INFORMATION

FIELD PROGRAMMABLE GATE ARRAY (FPGA) LOW LOGIC COMPLIANCE

Figure 38 shows a typical application where the ADG1206L/ADG1207L is used together with an FPGA or microcontroller. The flexible V_L pin can be tied to the digital supply voltage (V_{CCO}), and the INx input can be tied directly to the digital IOx ports for ease of use.

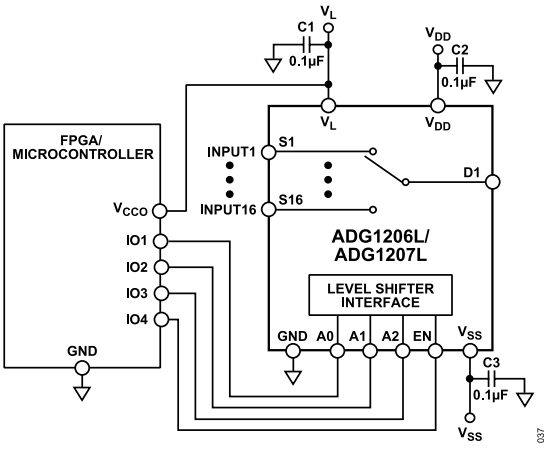


Figure 38. Typical Application

The ADG1206L/ADG1207L is 1.2 V and 1.8 V JEDEC standard compliant, which ensures that the logic input specifications, V_{INH} and V_{INL}, meet the digital output specifications, minimum V_{OH} and maximum V_{OL}, of the FPGA or microcontroller. Common implementations do not guarantee logic level compatibility, which can introduce implementation risks. The ADG1206L/ADG1207L eliminate these risks by complying with the widely accepted 1.2 V and 1.8 V logic level standard.

V_{OH} AND V_{OL}, AND V_{INH} AND V_{INL} RELATIONSHIP

It is recommended to confirm that the logic output high (V_{OH}) of the FPGA or microcontroller is higher than the input logic high (V_{INH}). In addition, the logic output low (V_{OL}) of the FPGA or microcontroller must be lower than the input low (V_{INL}). Figure 39 shows the 1.2 V logic compatibility relationship between V_{OH} and V_{OL} of the FPGA or the microcontroller with the INx inputs of the ADG1206L/ADG1207L, V_{INH} and V_{INL}.

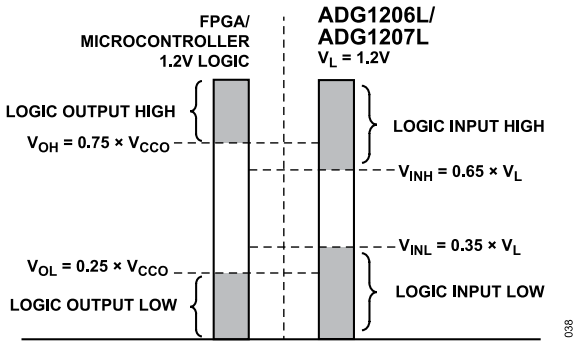


Figure 39. 1.2 V Logic Compatibility Between V_{OH} and V_{OL} and V_{INH} and V_{INL}

Figure 40 shows the 1.8 V logic compatibility relationship between V_{OH} and V_{OL} of the FPGA or the microcontroller with the INx inputs of the ADG1206L/ADG1207L, V_{INH} and V_{INL}.

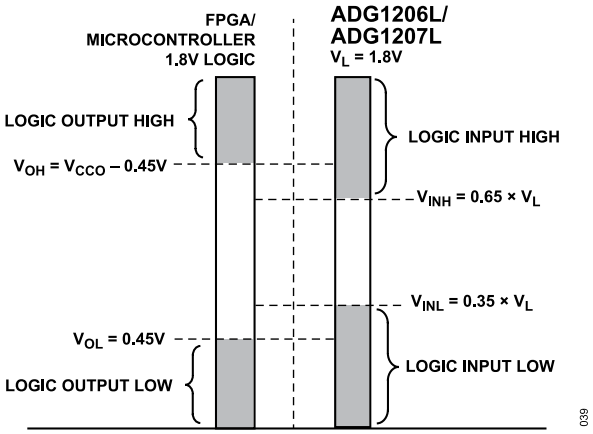


Figure 40. 1.8 V Logic Compatibility Between V_{OH} and V_{OL} and V_{INH} and V_{INL}

POWER SUPPLY RAILS

To guarantee correct operation of the ADG1206L/ADG1207L, a minimum of 0.1 µF and 10 µF decoupling capacitors are required on the V_{DD}, V_{SS}, and V_L supply pins.

The ADG1206L/ADG1207L can operate with V_{DD} and V_{SS} dual supplies between ±5 V to ±16.5 V. This device can also operate with a V_{DD} single supply between 5 V to 16.5 V and a V_L between 1.1 V to 1.95 V. However, the V_{DD} to V_{SS} range must not exceed 18 V, and the V_L range must not exceed 2.25 V, as stated in the Absolute Maximum Ratings section.

It is possible to operate the ADG1206L and ADG1207L with asymmetrical supplies or at other voltage supplies within the range shown in Table 1. However, the switch characteristics change. These changes include, but are not limited to, analog signal range, on resistance, leakage, V_{INH}, V_{INL}, and switching times. The typical performance characteristics can be used as a guide to switch performance vs. supply voltage.

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a symmetrical bipolar power solution is shown in Figure 41. The ADP5070 (dual switching regulator) generates a positive and negative supply rail for the ADG1206L/ADG1207L. Also shown in Figure 41 are two optional positive and negative, low dropout (LDO) regulators, the ADP7118 and ADP7182, respectively, that can reduce the output ripple of the ADP5070 in ultralow noise sensitive applications.

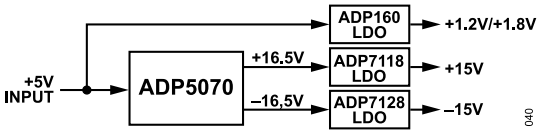


Figure 41. Bipolar Power Solution

POWER SUPPLY SEQUENCING

Take care to ensure correct power supply sequencing. Incorrect power supply sequencing can result in the device being subjected to stresses beyond the maximum ratings listed in Table 6. Ensure that the analog power supplies (V_{DD} and V_{SS}) and ground (GND) are present before applying V_L, the digital inputs, and the analog inputs. Failure to adhere to this sequence may result in damage to the device.

OUTLINE DIMENSIONS

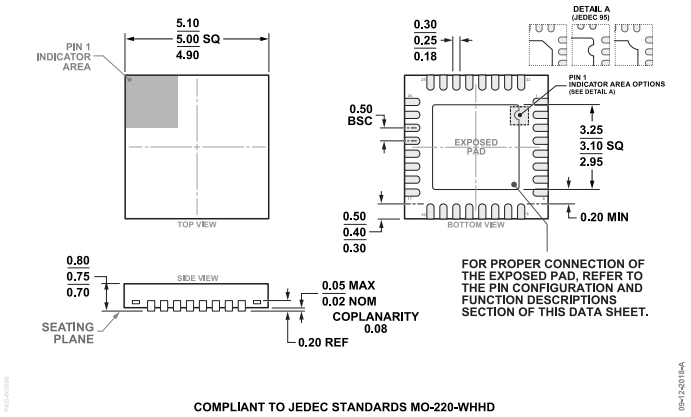


Figure 42. 32-Lead Lead Frame Chip Scale Package [LFCSP] 5 mm × 5 mm Body and 0.75 mm Package Height (CP-32-7) Dimensions shown in millimeters

Updated: January 11, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADG1206LYCPZ-REEL7	-40°C to +125°C	32-Lead LFCSP (5mm x 5mm w/ EP)	Reel, 1500	CP-32-7
ADG1207LYCPZ-REEL7	-40°C to +125°C	32-Lead LFCSP (5mm x 5mm w/ EP)	Reel, 1500	CP-32-7

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADG1206LEBZ	Evaluation Board
EVAL-ADG1207LEBZ	Evaluation Board

[1] Z = RoHS Compliant Part.