19-5142; Rev 1; 9/10

EVALUATION KIT AVAILABLE

Single-Port, 40W, IEEE 802.3af/at PSE Controller with Integrated MOSFET

General Description

The MAX5971A is a single-port, power-sourcing equipment (PSE) power controller designed for use in IEEE® 802.3af/at-compliant PSE. This device provides powered device (PD) discovery, classification, current limit, and DC and AC load-disconnect detections. The MAX5971A operates automatically without the need for any software programming and features an integrated power MOSFET and sense resistor. The device also supports new Class 5 and 2-event classification for detection and classification of high-power PDs. The MAX5971A provides up to 40W to a single port (Class 5 enabled) and still provides high-capacitance detection for legacy PDs.

The MAX5971A provides input undervoltage lockout (UVLO), input overvoltage lockout, overtemperature detection, output voltage slew-rate limit during startup, and LED status indication.

The MAX5971A is available in a space-saving, 28-pin TQFN (5mm x 5mm) power package, and is rated for the extended (-40°C to +85°C) temperature range.

Applications

Single-Port PSE End-Point Applications

Single-Port PSE Power Injectors (Midspan Applications)

Switches/Routers

Industrial Automation Equipment

Wireless LAN Access Point/WiMAX™ Base Station

Features

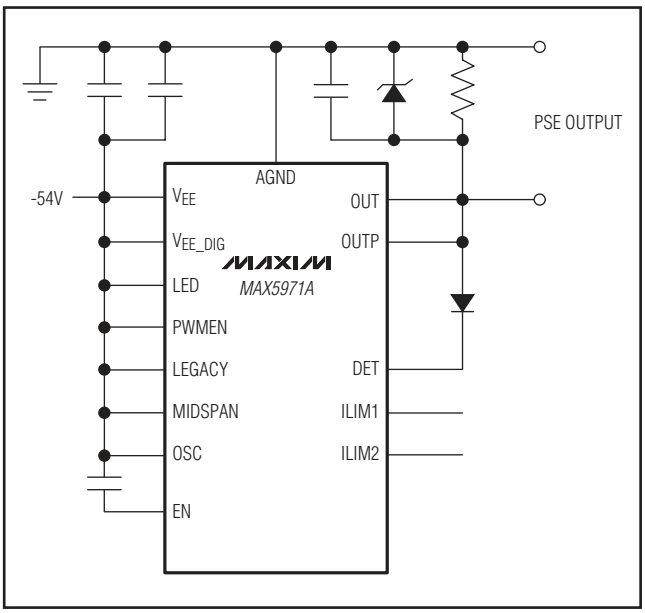
- **IEEE 802.3af/at Compliant**
- **Up to 40W for Single-Port PSE Applications**
- **Integrated 0.5Ω Power MOSFET and Sense Resistor**
- **PD Detection and Classification**
- **Programmable Current Limit for Class 5 PDs**
- **High-Capacitance Detection for Legacy Devices**
- **Supports Both DC and AC Load Removal Detections**
- **Current Foldback and Duty Cycle-Controlled Current Limit**
- **LED Indicator for Port Status**
- **Direct Fast-Shutdown Control Capability**
- **Space-Saving, 28-Pin TQFN (5mm x 5mm) Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5971AETI+	-40°C to +85°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Operating Circuit



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Single-Port, 40W, IEEE 802.3af/802.3at PSE Controller with Integrated MOSFET

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to V_{EE}, unless otherwise noted.)
AGND, DET, LED .....-0.3V to +80V
OUT .....-0.3V to (V_{AGND} + 0.3V)
OUTP .....-6V to (V_{AGND} + 0.3V)
VEE_DIG .....-0.3V to +0.3V
OSC .....-0.3V to +6V
EN, PWMEN, MIDSPAN, LEGACY, ILIM1, ILIM2 ....-0.3V to +4V
Maximum Current Into LED 40mA
Maximum Current Into OUT .....Internally regulated
Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 34.5mW/°C above +70°C) 2758mW

Package Thermal Resistance (Note 1)
θ_{JA} .....29°C/W
θ_{JC} .....2°C/W
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AGND} - V_{EE} = 32V to 60V, T_A = -40°C to +85°C, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} - V_{EE} = +54V, T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Operating Voltage Range	V_{AGND}	V_{AGND} - V_{EE}		32		60	V
Supply Current	I_{EE}	V_{OUT} = V_{EE}, all logic inputs unconnected, measured at AGND in power mode			2.5	4	mA
CURRENT LIMIT							
Current Limit	I_{LIM}	Maximum I_{LOAD} allowed during current-limit conditions, V_{OUT} = 0V (Note 3)	Class 0, 1, 2, 3	400	420	441	mA
			Class 4	684	720	756	
			Class 5 if ILIM1 = V_{EE}, ILIM2 = unconnected	807	850	893	
			Class 5 if ILIM1 = unconnected, ILIM2 = V_{EE}	855	900	945	
			Class 5 if ILIM1 = V_{EE}, ILIM2 = V_{EE}	902	950	998	
Foldback Initial OUT Voltage	V_{FLBK_ST}	V_{AGND} - V_{OUT} below which the current limit starts folding back			27		V
Foldback Final OUT Voltage	V_{FLBK_END}	V_{AGND} - V_{OUT} below which the current limit reaches I_{TH_FB}			10		V
Minimum Foldback Current Limit Threshold	I_{TH_FB}	V_{OUT} = V_{AGND}			166		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} - V_{EE} = 32V to 60V, T_A = -40°C to +85°C, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} - V_{EE} = +54V, T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OVERCURRENT							
Overcurrent Threshold	I_{CUT}	Overcurrent threshold allowed for $t \le t_{FAULT}$, V_{OUT} = 0V (Note 3)	Class 0, 1, 2, 3	351	370	389	mA
			Class 4	602	634	666	
			Class 5 if ILIM1 = V_{EE}, ILIM2 = unconnected	710	748	785	
			Class 5 if ILIM1 = unconnected, ILIM2 = V_{EE}	752	792	832	
			Class 5 if ILIM1 = V_{EE}, ILIM2 = V_{EE}	794	836	878	
INTERNAL POWER							
DMOS On-Resistance	$R_{DS(ON)}$	Measured from OUT to V_{EE}, I_{OUT} = 100mA	T_A = +25°C		0.5	0.9	Ω
			T_A = +85°C		0.6	1.3	
Power-Off OUT Leakage Current	I_{OUT_LEAK}	V_{EN} = V_{EE}, V_{OUT} = V_{AGND}				10	µA
SUPPLY MONITORS							
V_{EE} Undervoltage Lockout	V_{EE_UVLO}	V_{AGND} - V_{EE}, V_{AGND} increasing			28.5		V
V_{EE} Undervoltage Lockout Hysteresis	V_{EE_UVLOH}	Port is shutdown if: V_{AGND} - V_{EE} < V_{EE_UVLO} - V_{EE_UVLOH}			3		V
V_{EE} Overvoltage Lockout	V_{EE_OV}	V_{AGND} - V_{EE} > V_{EE_OV}, V_{AGND} increasing			62.5		V
V_{EE} Overvoltage Lockout Hysteresis	V_{EE_OVH}				1		V
Thermal Shutdown Threshold	T_{SHD}	Port is shutdown and device resets if the junction temperature exceeds this limit, temperature increasing			150		°C
Thermal Shutdown Hysteresis	T_{SHDH}	Temperature decreasing			20		°C
OUTPUT MONITOR							
OUT Input Current	I_{BOUT}	V_{OUT} = V_{AGND}, probing phases				6	µA
Idle Pullup Current at OUT	I_{DIS}	OUTP discharge current, detection and classification off, port shutdown, V_{OUTP} = V_{AGND} - 2.8V		200		265	µA
Short to V_{EE} Detection Threshold	DCN_{TH}	V_{OUT} - V_{EE}, V_{OUT} decreasing, enabled during detection		1.5	2.0	2.5	V
Short to V_{EE} Detection Threshold Hysteresis	DCN_{HY}				220		mV
LOAD DISCONNECT							
DC Load-Disconnect Threshold	I_{DCTH}	Minimum load current allowed before disconnect (DC disconnect active), V_{OUT} = 0V		5	7.5	10	mA
AC Load-Disconnect Threshold	I_{ACTH}	Current into DET, for I_{DET} < I_{ACTH} the port powers off (AC disconnect active)		115	130	145	µA

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ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} - V_{EE} = 32V to 60V, T_A = -40°C to +85°C, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} - V_{EE} = +54V, T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Triangular Wave Peak-to-Peak Voltage Amplitude	AMP_{TRW}	Measured at DET, referred to AGND		3.85	4	4.2	V
OSC Pullup/Pulldown Currents	I_{OSC}	Measured at OSC		26	32	39	µA
ACD_EN Threshold	V_{ACD_EN}	V_{OSC} - V_{EE} > V_{ACD_EN} to activate AC disconnect		270	330	380	mV
Load Disconnect Timer	t_{DISC}	Time from I_{RSENSE} < I_{DCTH} (DC disconnect active) or I_{DET} < I_{ACTH} (AC disconnect active) to gate shutdown		300		400	ms
DETECTION							
Detection Probe Voltage (First Phase)	V_{DPH1}	V_{AGND} - V_{DET} during the first detection phase		3.8	4	4.2	V
Detection Probe Voltage (Second Phase)	V_{DPH2}	V_{AGND} - V_{DET} during the second detection phase		9	9.3	9.6	V
Current-Limit Protection	I_{DLIM}	V_{DET} = V_{AGND} during detection, measure current through DET		1.50	1.75	2.00	mA
Short-Circuit Threshold	V_{DCP}	If V_{AGND} - V_{OUT} < V_{DCP} after the first detection phase a short circuit to AGND is detected.			1		V
Open-Circuit Threshold	I_{D_OPEN}	First point measurement current threshold for open condition			20		µA
Resistor Detection Window	R_{DOK}	(Note 4)		19		26.5	kΩ
Resistor Rejection Window	R_{DBAD}	Detection rejects lower values				15.5	kΩ
		Detection rejects higher values		32			
CLASSIFICATION							
Classification Probe Voltage	V_{CL}	V_{AGND} - V_{DET} during classification		16		20	V
Current-Limit Protection	I_{CILIM}	V_{DET} = V_{AGND}, during classification measure current through DET		65		80	mA
Classification Current Thresholds	I_{CL}	Classification current thresholds between classes	Class 0, Class 1	5.5	6.5	7.5	mA
			Class 1, Class 2	13.0	14.5	16.0	
			Class 2, Class 3	21	23	25	
			Class 3, Class 4	31	33	35	
			Class 4 upper limit (Note 5)	45	48	51	
Mark Event Voltage	V_{MARK}	V_{AGND} - V_{DET} during mark event		8		10	V
Mark Event Current Limit	I_{MARK_LIM}	V_{DET} = V_{AGND}, during mark event measure current through DET		55		80	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} - V_{EE} = 32V to 60V, T_A = -40°C to +85°C, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} - V_{EE} = +54V, T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS/OUTPUTS (Voltages referenced to V_{EE})						
Digital Input Low	V_{IL}				0.8	V
Digital Input High	V_{IH}		2.4			V
Internal Input Pullup Current	I_{PU}	Pullup current to internal digital supply to set default values	3	5	7	µA
LED Output Low Voltage	V_{LED_LOW}	I_{LED} = 10mA, PWM disabled, port power-on			0.8	V
LED Output Leakage	I_{LED_LEAK}	PWM disabled, shutdown mode, V_{LED} = 60V			10	µA
PWM Frequency				25		kHz
PWM Duty Cycle				6.25		%
TIMING						
Startup Time	t_{START}	Time during which a current limit set to 420mA is allowed, starts when power is turned on	50	60	70	ms
Fault Time	t_{FAULT}	Maximum allowed time for an overcurrent condition set by I_{CUT} after startup	50	60	70	ms
Detection Reset Time	t_{ME}	Time allowed for the port voltage to reset before detection starts		80	90	ms
Detection Time	t_{DET}	Maximum time allowed before detection is completed			330	ms
Midspan Mode Detection Delay	t_{DMID}		2	2.2	2.4	s
Classification Time	t_{CLASS}	Time allowed for classification		19	23	ms
Mark Event Time		Time allowed for mark event	7	9	11	ms
V_{EEUVLO} Turn-On Delay	t_{DLY}	Time V_{AGND} must be above the V_{EEUVLO} thresholds before the device operates		5.2		ms
Restart Timer	$t_{RESTART}$	Time the device waits before turning on after an overcurrent fault		16 x t_{FAULT}		ms

Note 2: This device is production tested at T_A = +25°C. Limits at T_A = -40°C and +85°C are guaranteed by design.

Note 3: If ILIM1 and ILIM2 are both unconnected, Class 5 detection is disabled. See the *Class 5 PD Classification* section and Table 3 for details and settings.

Note 4: R_{DOK} = (V_{OUT2} - V_{OUT1})/(I_{DET2} - I_{DET1}). V_{OUT1}, V_{OUT2}, I_{DET2}, and I_{DET1} represent the voltage at OUT and the current at DET during phase 1 and 2 of the detection, respectively.

Note 5: If Class 5 is enabled, this is the classification current thresholds from Class 4 to Class 5.

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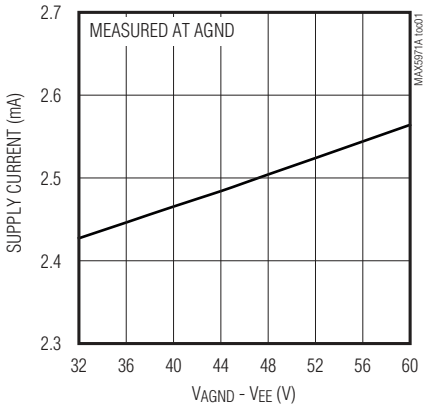
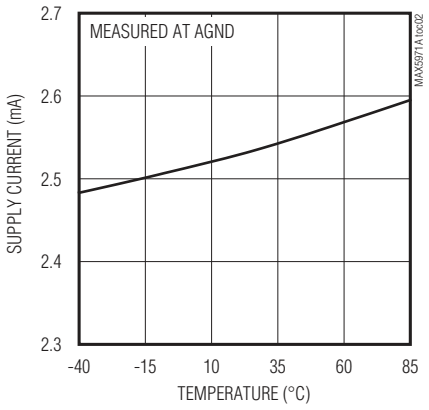
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

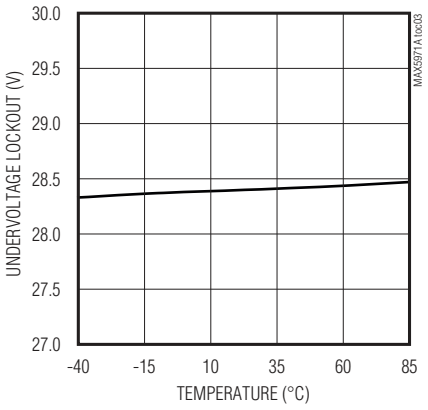
ANALOG SUPPLY CURRENT vs. INPUT VOLTAGE



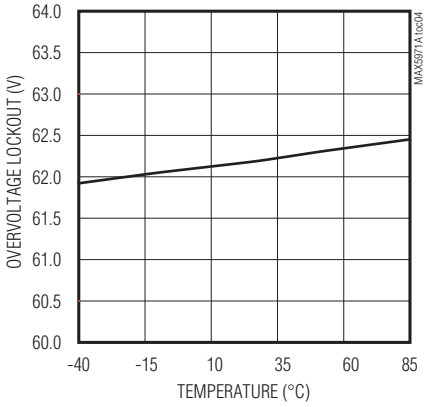
ANALOG SUPPLY CURRENT vs. TEMPERATURE



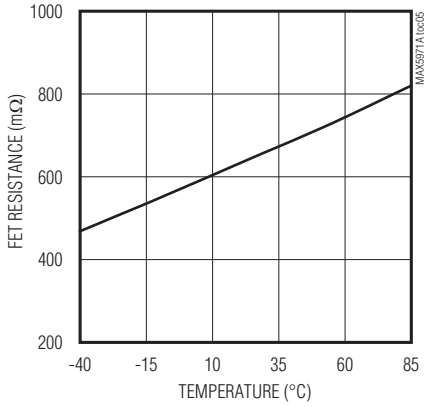
VEE UNDERVOLTAGE LOCKOUT vs. TEMPERATURE



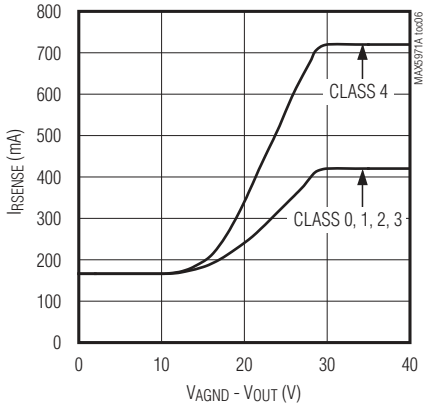
VEE OVERVOLTAGE LOCKOUT vs. TEMPERATURE



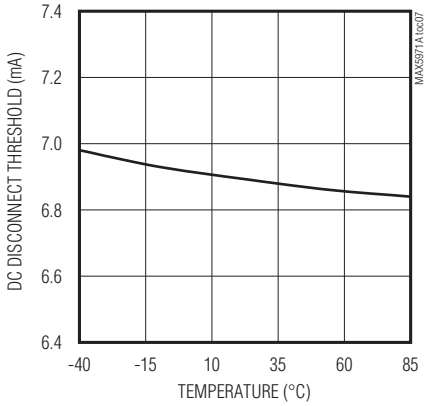
INTERNAL FET RESISTANCE vs. TEMPERATURE



FOLDBACK CURRENT-LIMIT THRESHOLD vs. OUTPUT VOLTAGE



DC DISCONNECT THRESHOLD vs. TEMPERATURE

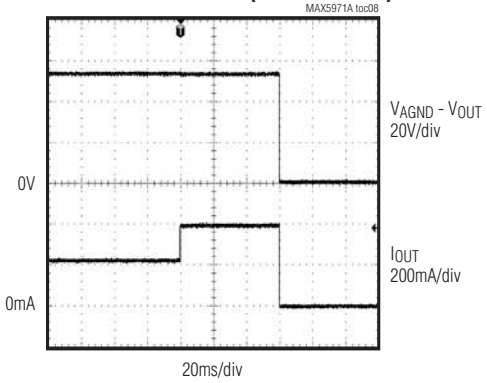


Single-Port, 40W, IEEE 802.3af/802.3at PSE Controller with Integrated MOSFET

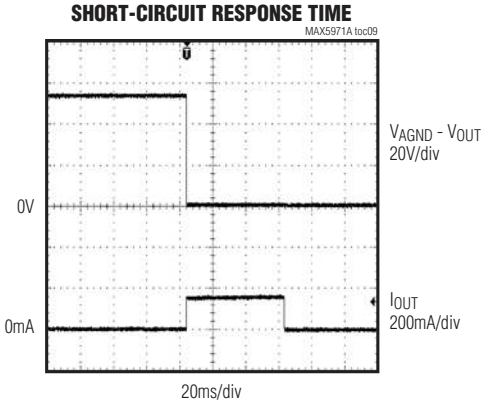
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

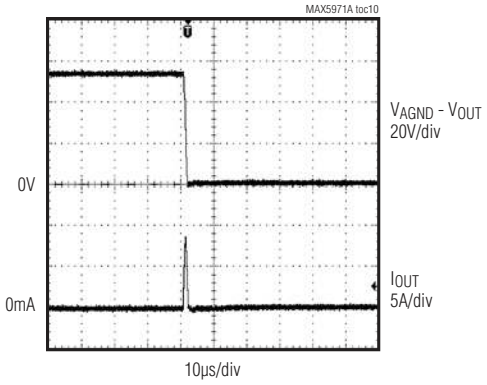
OVERCURRENT TIMEOUT (240Ω TO 138Ω)



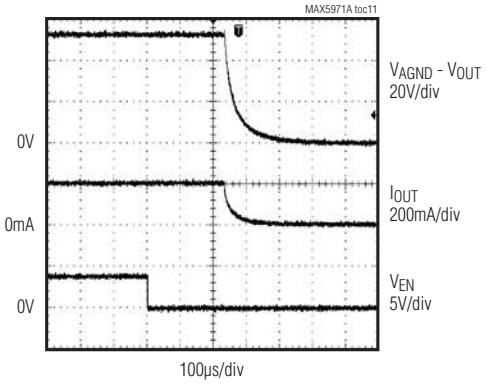
SHORT-CIRCUIT RESPONSE TIME



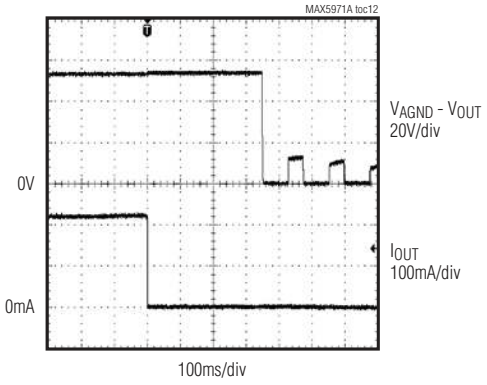
SHORT-CIRCUIT TRANSIENT RESPONSE



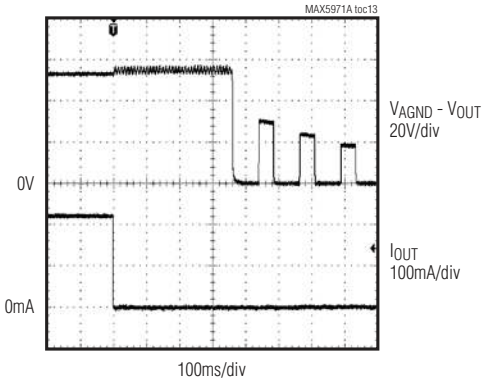
EN TO OUT TURN-OFF DELAY



ZERO-CURRENT DETECTION WAVEFORM WITH DC DISCONNECT ENABLED



ZERO-CURRENT DETECTION WAVEFORM WITH AC DISCONNECT ENABLED

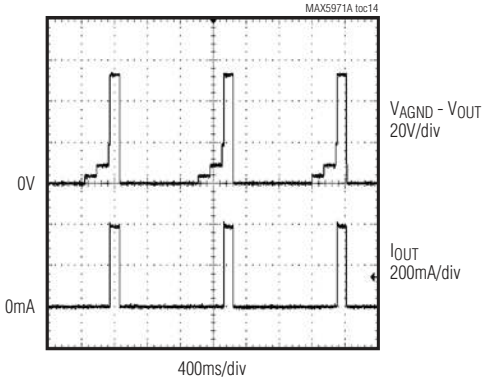


Single-Port, 40W, IEEE 802.3af/802.3at PSE Controller with Integrated MOSFET

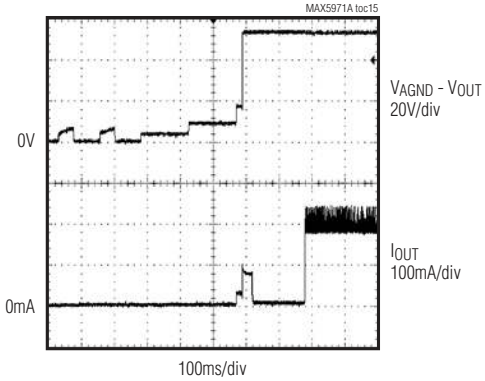
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

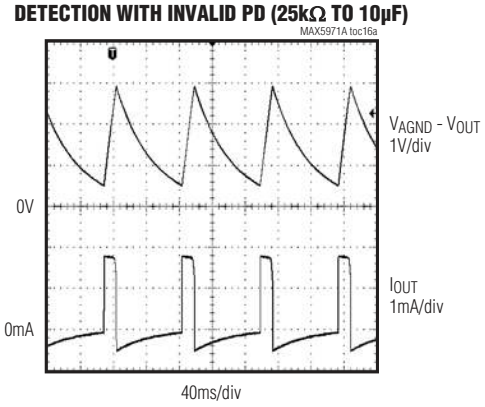
OVERCURRENT RESTART DELAY



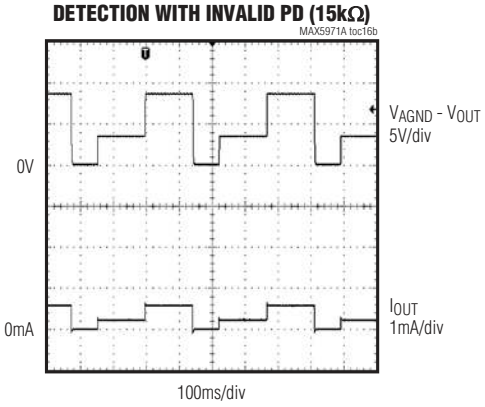
STARTUP WITH A VALID PD



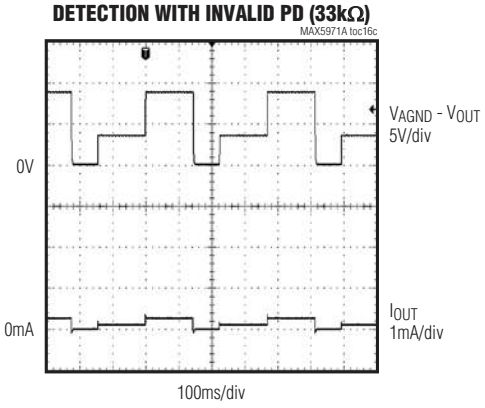
DETECTION WITH INVALID PD (25kΩ TO 10µF)



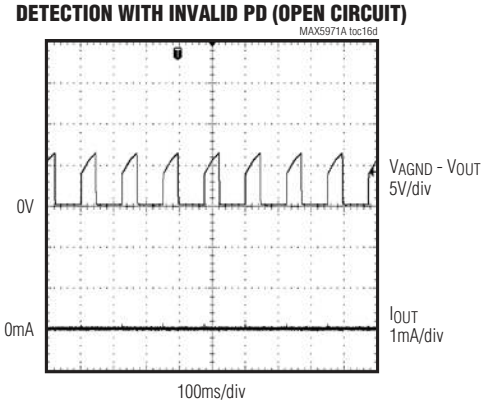
DETECTION WITH INVALID PD (15kΩ)



DETECTION WITH INVALID PD (33kΩ)



DETECTION WITH INVALID PD (OPEN CIRCUIT)

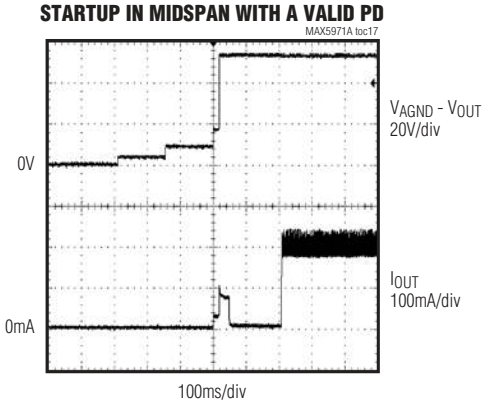


Single-Port, 40W, IEEE 802.3af/802.3at PSE Controller with Integrated MOSFET

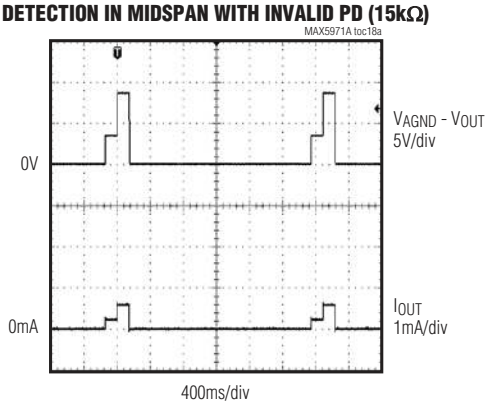
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

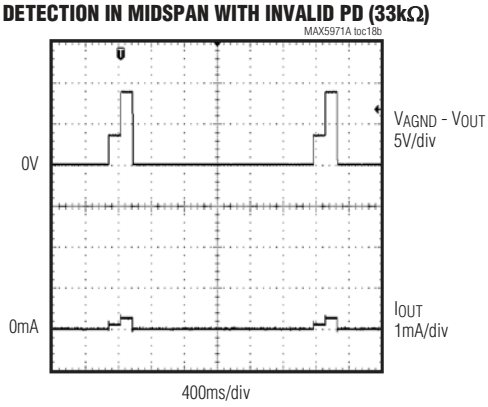
STARTUP IN MIDSPAN WITH A VALID PD



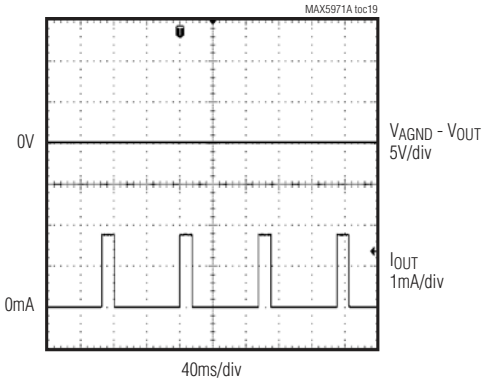
DETECTION IN MIDSPAN WITH INVALID PD (15kΩ)



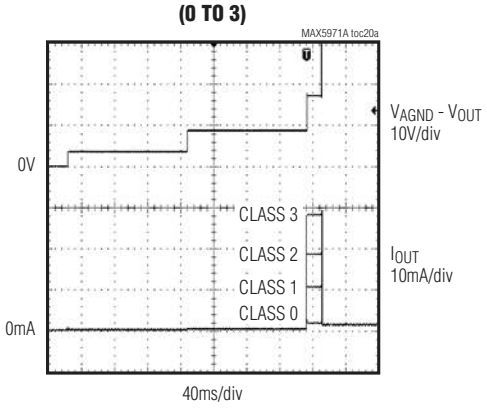
DETECTION IN MIDSPAN WITH INVALID PD (33kΩ)



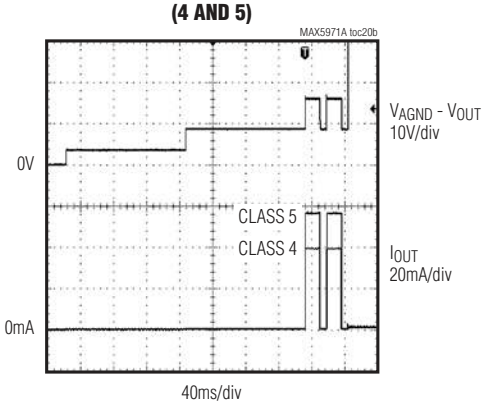
DETECTION IN OUTPUT SHORTED TO AGND



CLASSIFICATION WITH DIFFERENT PD CLASSES (0 TO 3)



CLASSIFICATION WITH DIFFERENT PD CLASSES (4 AND 5)

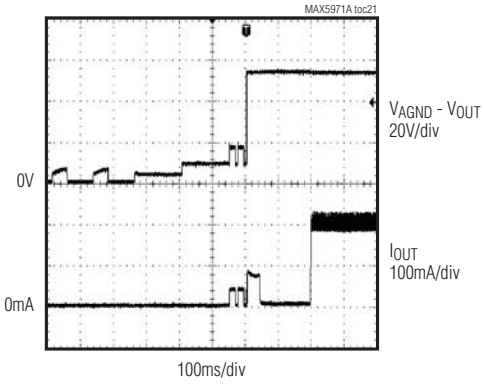


Single-Port, 40W, IEEE 802.3af/802.3at PSE Controller with Integrated MOSFET

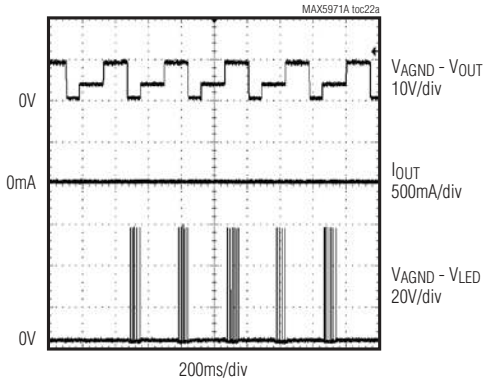
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

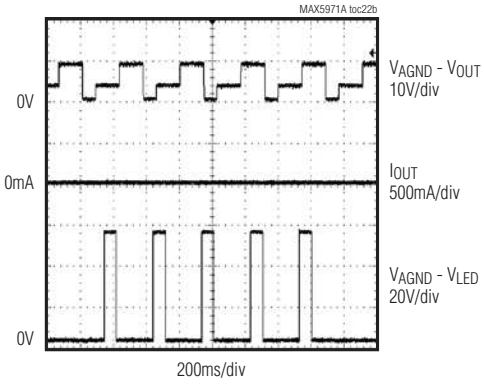
STARTUP USING 2-EVENT CLASSIFICATION WITH A VALID PD



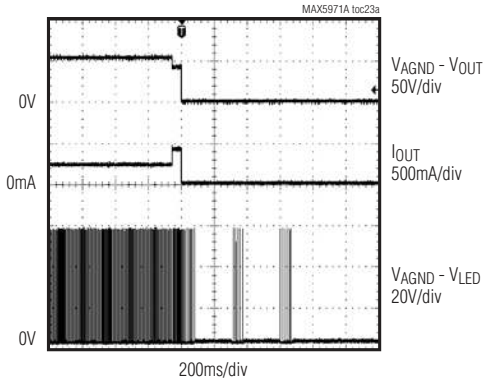
LED DETECTION FAULT WITH PWM ENABLED



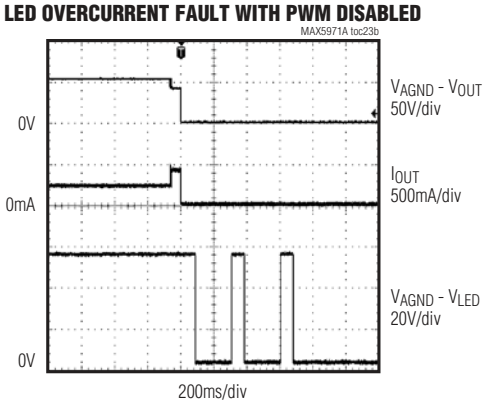
LED DETECTION FAULT WITH PWM DISABLED



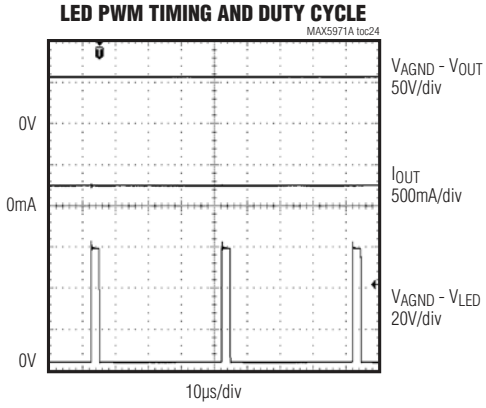
LED OVERCURRENT FAULT WITH PWM ENABLED



LED OVERCURRENT FAULT WITH PWM DISABLED

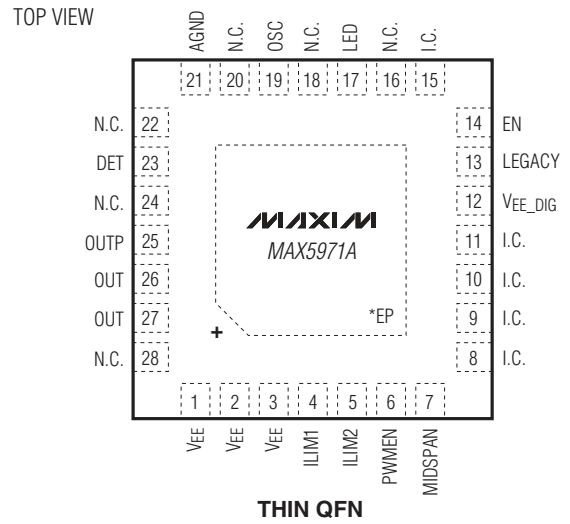


LED PWM TIMING AND DUTY CYCLE



Single-Port, 40W, IEEE 802.3af/802.3at PSE Controller with Integrated MOSFET

Pin Configuration



THIN QFN

*EXPOSED PAD, CONNECT TO AGND.

Pin Description

PIN	NAME	FUNCTION
1, 2, 3	V_{EE}	Analog Low-Side Supply Input. Bypass with an external 100V, 47µF capacitor in parallel with a 100V, 0.1µF ceramic capacitance between AGND and V_{EE}.
4	ILIM1	Class 5 Current-Limit Digital Adjust 1. Referenced to V_{EE}. ILIM1 is internally pulled up to the digital supply. Use ILIM1 with ILIM2 to enable Class 5 operation and to adjust the Class 5 current-limit value. See the *Electrical Characteristics* table and Table 3 in the *Class 5 PD Classification* section for details.
5	ILIM2	Class 5 Current-Limit Digital Adjust 2. Referenced to V_{EE}. ILIM2 is internally pulled up to the digital supply. Use ILIM2 with ILIM1 to enable Class 5 operation and to adjust the Class 5 current-limit value. See the *Electrical Characteristics* table and Table 3 in the *Class 5 PD Classification* section for details.
6	PWMEN	PWM Control Logic Input. Referenced to V_{EE}. PWMEN is internally pulled up to the digital supply. Leave unconnected to enable the internal PWM to drive the LED pin. Force low to disable the internal PWM.
7	MIDSPAN	Detection Collision Avoidance Logic Input. Referenced to V_{EE}. MIDSPAN is internally pulled up to the digital supply. Leave unconnected to activate the detection collision avoidance circuitry for midspan PSE systems. Force low to disable this function for an end-point PSE system. The MIDSPAN logic level latches after the device is powered up or after a reset condition.
8–11, 15	I.C.	Internally Connected. Connect I.C. to V_{EE}.
12	V_{EE_DIG}	Digital Low-Side Supply Input. Connect to V_{EE} externally.

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Pin Description (continued)

PIN	NAME	FUNCTION
13	LEGACY	Legacy Detection Logic Input. Referenced to V_{EE}. LEGACY is internally pulled up to the digital supply. Leave unconnected to activate the legacy PD detection. Force low to disable this function. The LEGACY logic level latches after the device is powered up or after a reset condition.
14	EN	Enable Input. Referenced to V_{EE}. EN is internally pulled up to the digital supply. Leave unconnected to enable the device. Force low for at least 40µs to reset the device. The MIDSPAN, OSC, and LEGACY states latch-in when the reset condition is removed (low-to-high transition).
16, 18, 20, 22, 24, 28	N.C.	No Connection. Not internally connected. Leave N.C. unconnected.
17	LED	LED Indicator Open-Drain Output. Referenced to V_{EE}. LED can sink 10mA and can drive an external LED directly. Blinking functionality is provided to signal different conditions (see the *PWM and LED Signals* section). Connect LED to AGND externally (see Figures 6 and 7) or to an external supply (if available) through a series resistance.
19	OSC	AC-Disconnect Triangular Wave Output. Bypass with a 100nF (±10% tolerance) external capacitor to V_{EE} to enable the AC disconnect function. Connect OSC to V_{EE} to disable the AC disconnect function and to activate the DC disconnect function. The OSC state latches after the device is powered up or after a reset condition.
21	AGND	High-Side Supply Input
23	DET	Detection/Classification Voltage Output. DET is used to set the detection mark event and classification probe voltages and for the AC current sensing when using the AC disconnect function. To use the AC disconnect function, place a 1kΩ and 0.47µF RC series in parallel with the external protection diode to OUTP (see Figure 7).
25	OUTP	Port Pullup Output. OUTP is used to pull up the port voltage to AGND when needed. If AC disconnect is used, connect OUTP to the anode of the AC-blocking diode. If AC disconnect is not used, connect OUTP to OUT (see Figures 6 and 8). Bypass OUTP to AGND with a 100V, 0.1µF ceramic capacitor.
26, 27	OUT	Integrated MOSFET Output. If DC disconnect is used, connect the port output to OUTP (see Figures 6 and 8). If the AC disconnect function is used, connect OUT to the cathode of the AC-blocking diode (see Figure 7).
—	EP	Exposed Pad. Connect EP to V_{EE} externally. See the *Layout Procedure* section for details.

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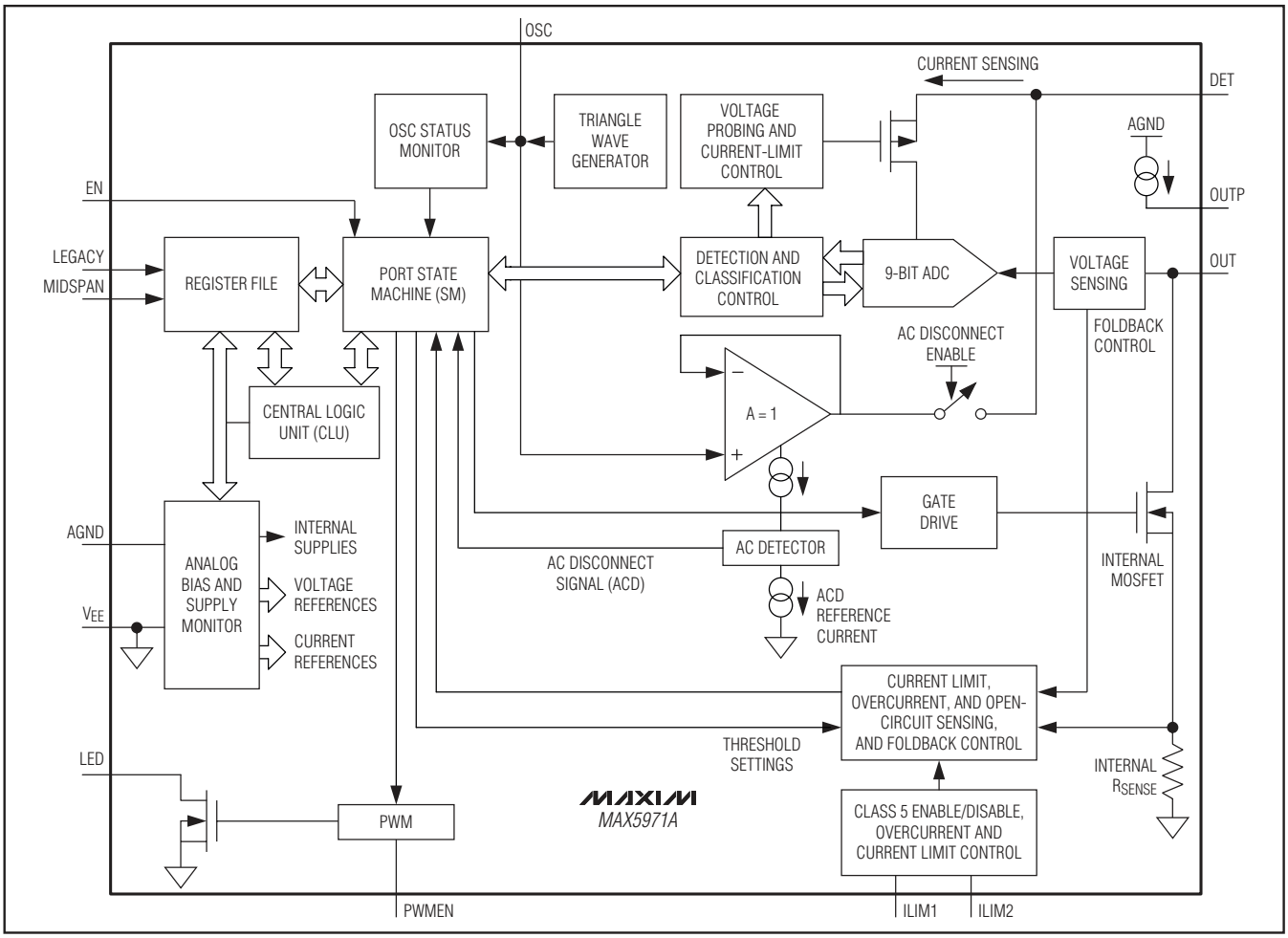
Simplified Diagram



Detailed Description

The MAX5971A is a single-port, PSE power controller designed for use in IEEE 802.3af/IEEE 802.3at-compliant PSE. This device provides PD discovery, classification, current limit, and DC and AC load-disconnect detections. The MAX5971A operates automatically without the need for any software programming and features an integrated power MOSFET and sense resistor. The device also supports new Class 5 and 2-event classification for detection and classification of high-power PDs. The MAX5971A provides up to 40W to a single port (Class 5 enabled) and still provides high-capacitance detection for legacy PDs.

The MAX5971A provides input UVLO, input overvoltage lockout, overtemperature detection, output voltage slew-rate limit during startup, and LED status indication.

Reset

The MAX5971A is reset by any of the following conditions:

1) Power-up. Reset condition is cleared once V_{EE} rises above the UVLO threshold.
2) Hardware reset. Reset occurs once the EN input is driven low (> 40µs typ.) any time after power-up. The device exits the reset condition once the EN input is driven high again.
3) Thermal shutdown. The device enters thermal shutdown at 150°C. The device exits thermal shutdown and is reset once the temperature drops below 130°C.

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During a reset, the MAX5971A latches in the state of MIDSPAN, LEGACY, and OSC. During normal operation, changes to these inputs are ignored.

Midspan Mode

In midspan mode, the device adopts cadence timing during the detection phase. When cadence timing is enabled and a failed detection occurs, the port waits between 2s and 2.4s before attempting to detect again. Midspan mode is activated by setting MIDSPAN high and then powering or resetting the device. By default, the MIDSPAN input is internally pulled high. Force MIDSPAN low to disable this function.

Automatic Operation

The MAX5971A operates automatically after the reset condition is cleared. The device performs detection and classification, and powers up the port automatically once a valid PD is detected at the port. If a valid PD is not connected at the port, the MAX5971A repeats the detection routine continuously until a valid PD is connected.

PD Detection

During normal operation, the MAX5971A probes the output for a valid PD. A valid PD has a 25kΩ discovery signature characteristic as specified in the IEEE 802.3af/802.3at standard. Table 1 shows the IEEE 802.3at specification for a PSE detecting a valid PD signature.

During detection, the MAX5971A keeps the internal MOSFET off and forces two probe voltages through DET. The current through DET is measured as well as the voltage at OUT. A two-point slope measurement is used, as specified by the IEEE 802.3af/802.3at standard, to verify the device connected to the port.

An external diode, in series with the DET input, restricts PD detection to the first quadrant as specified by the IEEE 802.3af/802.3at standard. To prevent damage to non-PD devices, and to protect itself from an output short circuit, the MAX5971A limits the current into DET to less than 2mA maximum during PD detection.

In midspan mode, the MAX5971A waits at least 2.0s before attempting another detection cycle after every failed detection. The first detection, however, happens immediately after exiting a reset condition.

High-Capacitance Detection

The status of the LEGACY input is latched during power-up or after reset condition is cleared. The LEGACY input is internally pulled high enabling high-capacitance detection. Unless high-capacitance detection is needed, connect LEGACY to V_{EE} to disable this function. If high-capacitance detection is enabled, PD signature capacitances up to 47µF (typ) are accepted.

Table 1. PSE PI Detection Modes Electrical Requirements (IEEE 802.3at)

PARAMETER	SYMBOL	MIN	MAX	UNITS	ADDITIONAL INFORMATION
Open-circuit voltage	V_{OC}		30	V	In detection mode only
Short-circuit current	I_{SC}		5	mA	In detection mode only
Valid test voltage	V_{VALID}	2.8	10	V	
Voltage difference between test points	ΔV_{TEST}	1		V	
Time between any two test points	t_{BP}	2		ms	This timing implies a 500Hz maximum probing frequency
Slew rate	V_{SLEW}		0.1	V/µs	
Accept signature resistance	R_{GOOD}	19	26.5	kΩ	
Reject signature resistance	R_{BAD}	< 15	> 33	kΩ	
Open-circuit resistance	R_{OPEN}	500		kΩ	
Accept signature capacitance	C_{GOOD}		150	nF	
Reject signature capacitance	C_{BAD}	10		µF	
Signature offset voltage tolerance	V_{OS}	0	2.0	V	
Signature offset current tolerance	I_{OS}	0	12	µA	

Powered Device Classification (PD Classification)

During the PD classification mode, the MAX5971A forces a probe voltage (-18V typ) at DET and measures the current into DET. The measured current determines the class of the PD. If the ILIM1 and ILIM2 pins are both left unconnected, the MAX5971A classifies the PD based on Table 33.9 of the IEEE 802.3at standard (see Table 2). If the measured current exceeds 51mA, the MAX5971A does not power the PD, but returns to the idle state before attempting a new detection cycle.

Class 5 PD Classification

The MAX5971A supports high power beyond the IEEE 802.3at standard by providing an additional classification (Class 5) if needed. To enable Class 5 detection and select the corresponding current-limit/overcurrent thresholds, ILIM1 and ILIM2 must be set based on the combinations detailed in Table 3. Once Class 5 is enabled, during classification, if the MAX5971A detects currents in excess of the Class 4 upper limit threshold, the PD is classified as a Class 5 powered device. The PD is guaranteed to be classified as a Class 5 device for any classification current from 51mA up to the classification current-limit threshold.

The Class 5 overcurrent threshold and current limit is set with ILIM1 and ILIM2. ILIM1 and ILIM2 are both referenced to V_{EE} and are internally pulled up to the digital supply. Leave ILIM1 and ILIM2 unconnected to disable Class 5 detection and to be fully compliant to IEEE 802.3at standard classification. Class 5 detection is enabled, and the corresponding overcurrent threshold and current limit is adjusted, by connecting one or both to V_{EE} (see Table 3).

2-Event PD Classification

If the result of the first classification event is Class 0 through Class 3, then only a single classification event occurs as shown in Figure 1. However, if the result is Class 4 or Class 5 (when enabled), the device performs a second classification event as shown in Figure 2. Between the classification cycles, the MAX5971A performs a first and second mark event as required by the IEEE 802.3at standard, forcing a -9.0V probing voltage at DET.

Powered State

When the MAX5971A enters a powered state, the t_{FAULT} and t_{DISC} timers are reset. When the startup timer has timed out, the device enters a normal powered condition, allowing power delivery to the PD.

Table 2. PSE Classification of a PD (Table 33.9 of the IEEE 802.3at Standard)

MEASURED I_{CLASS} (mA)	CLASSIFICATION
0 to 5	Class 0
> 5 and < 8	Can be Class 0 or 1
8 to 13	Class 1
> 13 and < 16	Either Class 1 or 2
16 to 21	Class 2
> 21 and < 25	Either Class 2 or 3
25 to 31	Class 3
> 31 and < 35	Either Class 3 or 4
35 to 45	Class 4
> 45 and < 51	Either Class 4 or Invalid

Table 3. Class 5 Overcurrent Threshold and Current-Limit Settings

ILIM1 CONFIGURATION	ILIM2 CONFIGURATION	OVERCURRENT THRESHOLD (mA)	CURRENT LIMIT (mA)
Unconnected	Unconnected	Class 5 disabled	Class 5 disabled
V_{EE}	Unconnected	748	850
Unconnected	V_{EE}	792	900
V_{EE}	V_{EE}	836	950

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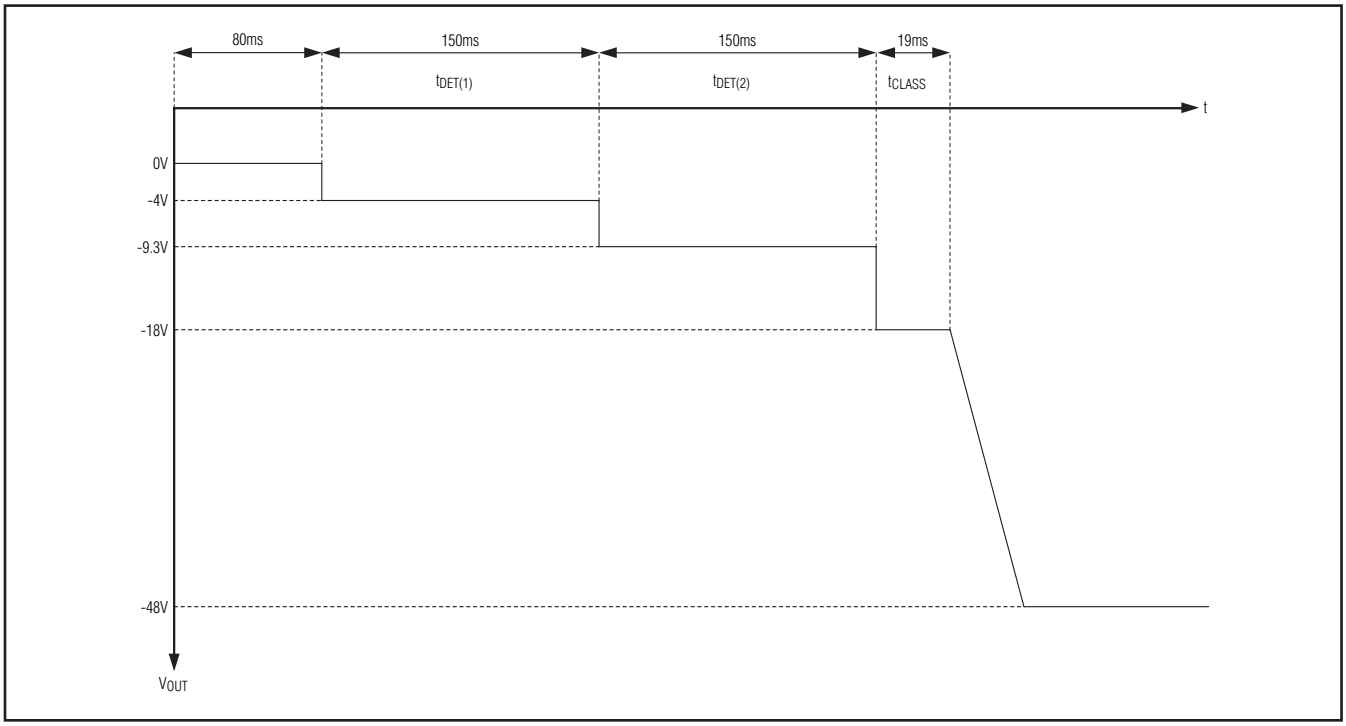

Figure 1. Detection, Classification, and Port Power-Up Sequence

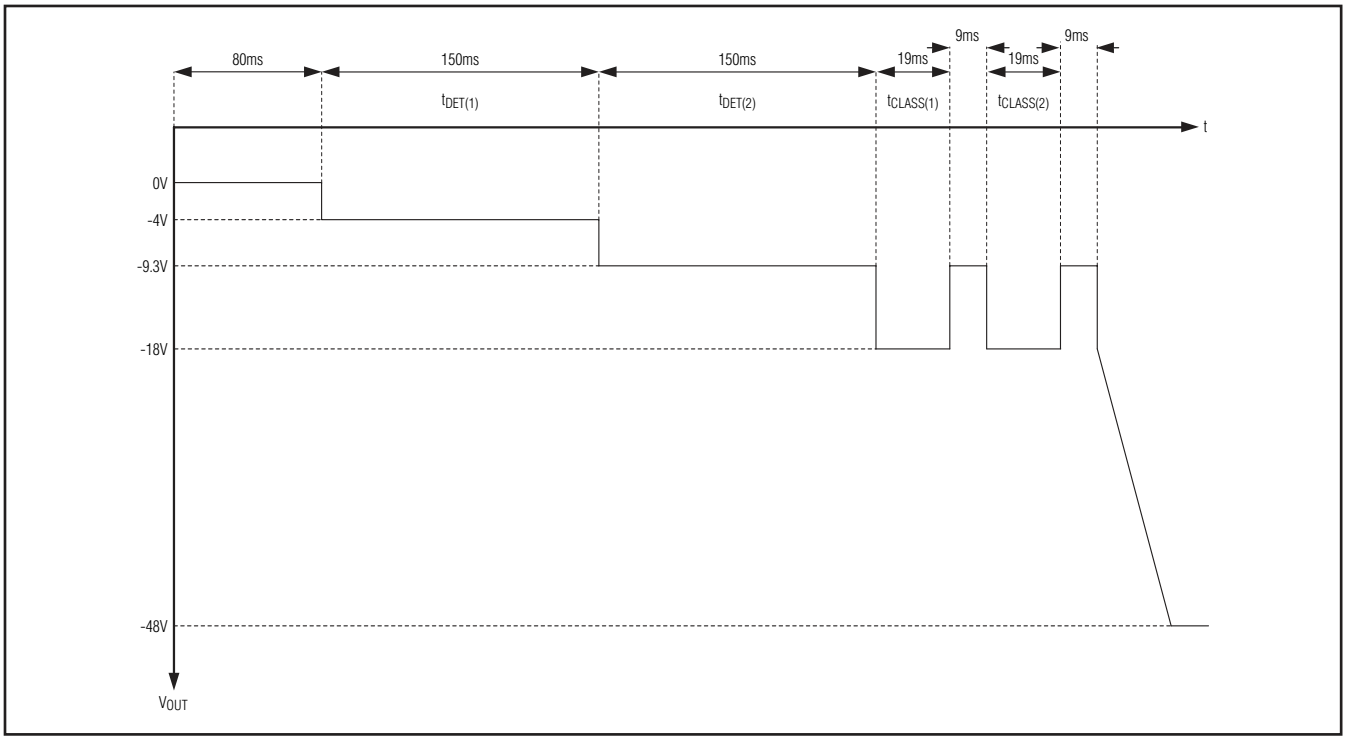

Figure 2. Detection, 2-Event Classification, and Port Power-Up Sequence

Overcurrent Protection

The MAX5971A has an internal sense resistor, R_{SENSE} (see the *Simplified Diagram*), connected between the source of the internal MOSFET and V_{EE} to monitor the load current. Under normal operating conditions, the current through R_{SENSE} (I_{RSENSE}) never exceeds the threshold I_{LIM}. If I_{RSENSE} exceeds I_{LIM}, an internal current-limiting circuit regulates the gate voltage of the internal MOSFET, limiting the current. During transient conditions, if I_{RSENSE} exceeds I_{LIM} by more than 2A, a fast pulldown circuit activates to quickly recover from the current overshoot.

In the normal powered state, the MAX5971A checks for overcurrent conditions, as determined by I_{CUT} = ~88% of I_{LIM}. The t_{FAULT} counter sets the maximum allowed continuous overcurrent period. This timer is incremented both in startup and in normal powered state, but under different conditions. During startup, the counter increases when I_{RSENSE} exceeds I_{LIM}, while in the normal powered state the counter increases when I_{RSENSE} exceeds I_{CUT}. It decreases at a slower pace when I_{RSENSE} drops below I_{LIM} or I_{CUT}. A slower decrement for the t_{FAULT} counter allows for detection of repeated short-duration overcurrent events. When the counter reaches the t_{FAULT} limit, the MAX5971A powers down the port. For a continuous overstress, a fault occurs exactly after a period of t_{FAULT}.

After a power-off due to an overcurrent fault, the t_{FAULT} timer is not immediately reset but starts decrementing. The MAX5971A allows the port to be powered on only when the t_{FAULT} counter reaches zero. This feature sets an automatic port power duty-cycle protection to the internal MOSFET to avoid overheating.

In the normal powered state, the I_{LIM} and I_{CUT} thresholds are set automatically according to the classification result (see Table 2 for classification results based on detection current, and the *Electrical Characteristics* table for the corresponding thresholds). During startup, I_{LIM} is always set to 420mA regardless of the detected class.

Foldback Current

During startup and normal operation, an internal circuit senses the port voltage and reduces the current-limit value and the overcurrent threshold when (V_{AGND} - V_{OUT}) < 27V. The foldback function helps to reduce the power dissipation on the internal MOSFET. The current limit eventually reduces down to I_{TH_FB} when (V_{AGND} - V_{OUT}) < 10V (see Figure 3).

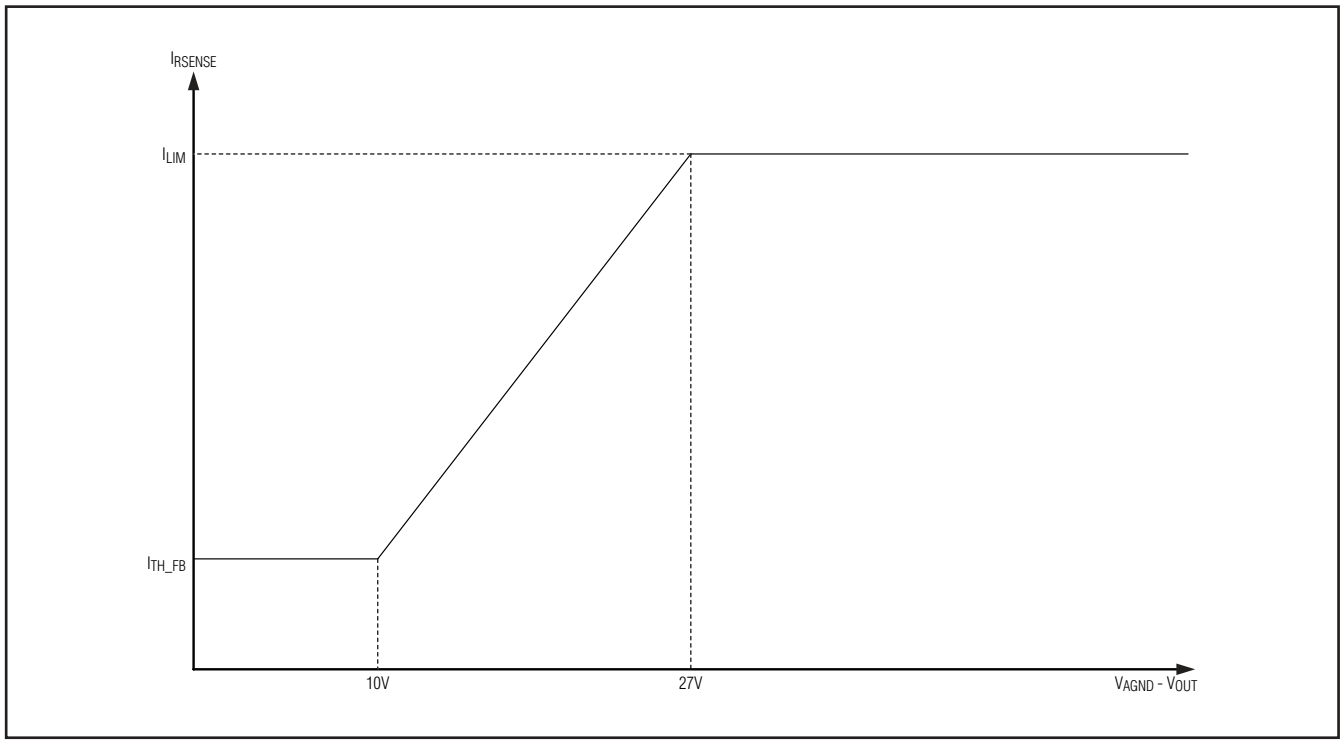

Figure 3. Foldback Current Characteristics

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Digital Logic

The MAX5971A internally generates digital supplies (referenced to V_{EE}) to power the internal logic circuitry. All logic inputs and outputs are referenced to V_{EE}. See the *Electrical Characteristics* table for digital input thresholds. If digital logic inputs are driven externally, the nominal digital logic level is 3.3V.

Undervoltage and Overvoltage Protection

The MAX5971A contains undervoltage and overvoltage protection features. An internal V_{EE} undervoltage lockout (V_{EE_UVLO}) circuit keeps the port off and the MAX5971A in reset until V_{AGND} - V_{EE} exceeds 28.5V (typ) for more than 2.5ms. An internal V_{EE} overvoltage (V_{EE_OV}) circuit shuts down the port when (V_{AGND} - V_{EE}) exceeds 62.5V (typ).

DC Disconnect Monitoring

Force OSC to V_{EE} and power or reset the device to activate DC load-disconnect monitoring. If I_{RSENSE} (the current across R_{SENSE}) falls below the DC load-disconnect threshold, I_{DCTH}, for more than t_{DISC}, the device turns off port power.

AC Disconnect Monitoring

The MAX5971A features AC load-disconnect monitoring. Bypass OSC with a 100nF (±10% tolerance) external capacitor to V_{EE} and power or reset the device to enable AC disconnect. When AC disconnect is enabled, a blocking diode in series to OUT and an RC circuit in parallel to the DET diode must be used, as shown in the typical operating circuit of Figure 7.

The AC disconnect uses an internal triangle wave generator to supply the probing signal. Then the resulting $4V_{P-P}$ amplitude wave is forced on DET. The common mode of the output signal probed on DET is 5V below AGND. If the AC current peak into DET falls below I_{ACTH} for more than t_{DISC}, the device powers down the port.

PWM and LED Signals

The MAX5971A includes a multifunction LED driver to inform the user of the port status. LED is an open-drain, multifunction output referenced to V_{EE} and can sink up to 10mA (typ) while driving an external LED. The LED is turned on when the port is connected to a valid PD and powered. If the port is not powered or is disconnected, the LED will be off.

For two other conditions, the MAX5971A blinks a code to communicate the port status. A series of two flashes indicates an overcurrent fault occurred during port power-on, and has a timing characteristic detailed by Figure 4. A series of five flashes indicates that during detection an invalid low or high discovery signature resistance was detected and has a timing characteristic detailed by Figure 5.

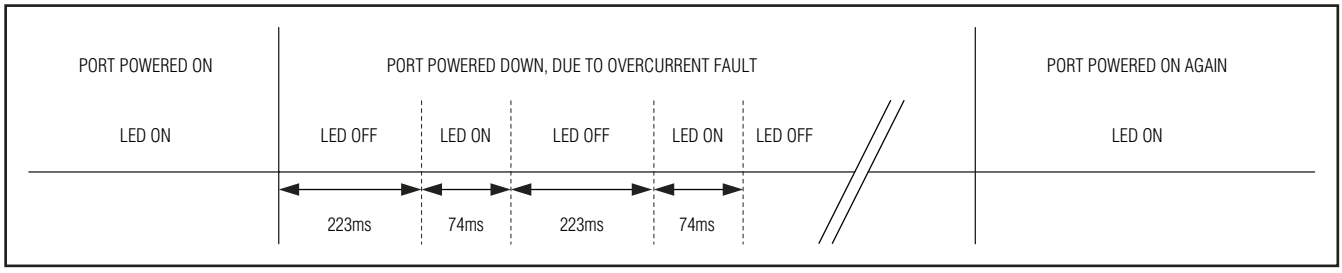

Figure 4. LED Code Timing for Overcurrent Fault During Port Power-On

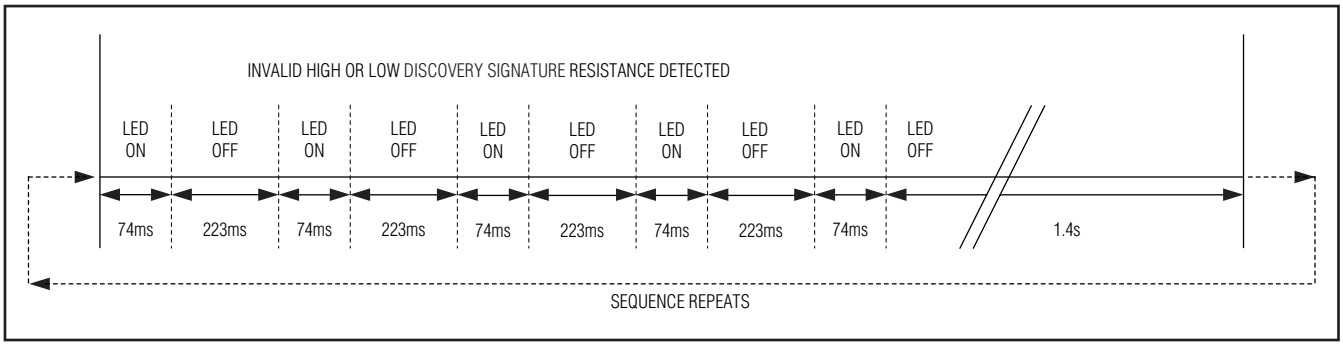

Figure 5. LED Code Timing for Detection Fault Due to High- or Low-Discovery Signature Resistance

The MAX5971A also contains an internal square wave, PWM signal generator. The PWM runs at a typical frequency of 25kHz with an approximate typical duty cycle of 6.25%. PWMEN is used to enable or disable the PWM. PWMEN is internally pulled up to the digital supply, and can be left unconnected to enable the internal PWM. When enabled, the LED pulses are driven by the PWM to reduce the power dissipation and increase the system efficiency. Force PWMEN low to disable the internal PWM; the LED is then driven directly.

Thermal Shutdown

If the MAX5971A die temperature reaches 150°C, an overtemperature fault is generated and the device shuts down. The die temperature must cool down below 130°C to remove the overtemperature fault condition. After a thermal shutdown condition clears, the device is reset.

Applications Information

Layout Procedure

Careful PCB layout is critical to achieve high efficiency and low EMI. Follow these layout guidelines for optimal performance.

1) Place the input bypass capacitance and the output bypass capacitor (0.1µF ceramic capacitor from AGND to OUTP) as close to the MAX5971A as possible.
2) Use large SMT component pads for power dissipating devices such as the MAX5971A and the external diodes in the high-power path.
3) Use short, wide traces whenever possible for high-power paths.
4) Use the MAX5971 Evaluation Kit as a design and layout reference.
5) The exposed pad (EP) must be soldered evenly to the PCB ground plane for proper operation and power dissipation. Use multiple vias beneath the exposed pad for maximum heat dissipation. A 1.0mm to 1.2mm pitch is the recommended spacing for these vias and they should be plated (1oz copper) with a small barrel diameter (0.30mm to 0.33mm).

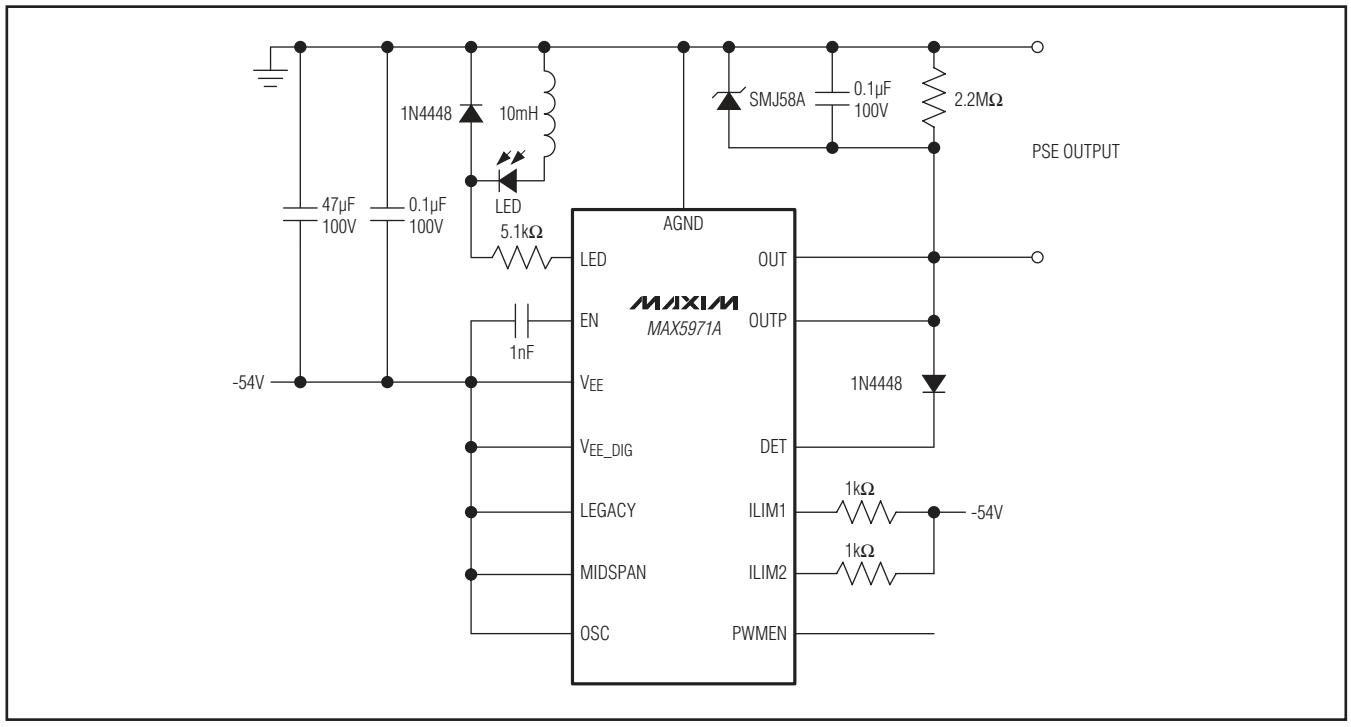

Figure 6. Typical Operating Circuit 1 (DC Load Removal Detection, Internal PWM Enabled for LED Indication, and Class 5 Detection Enabled)

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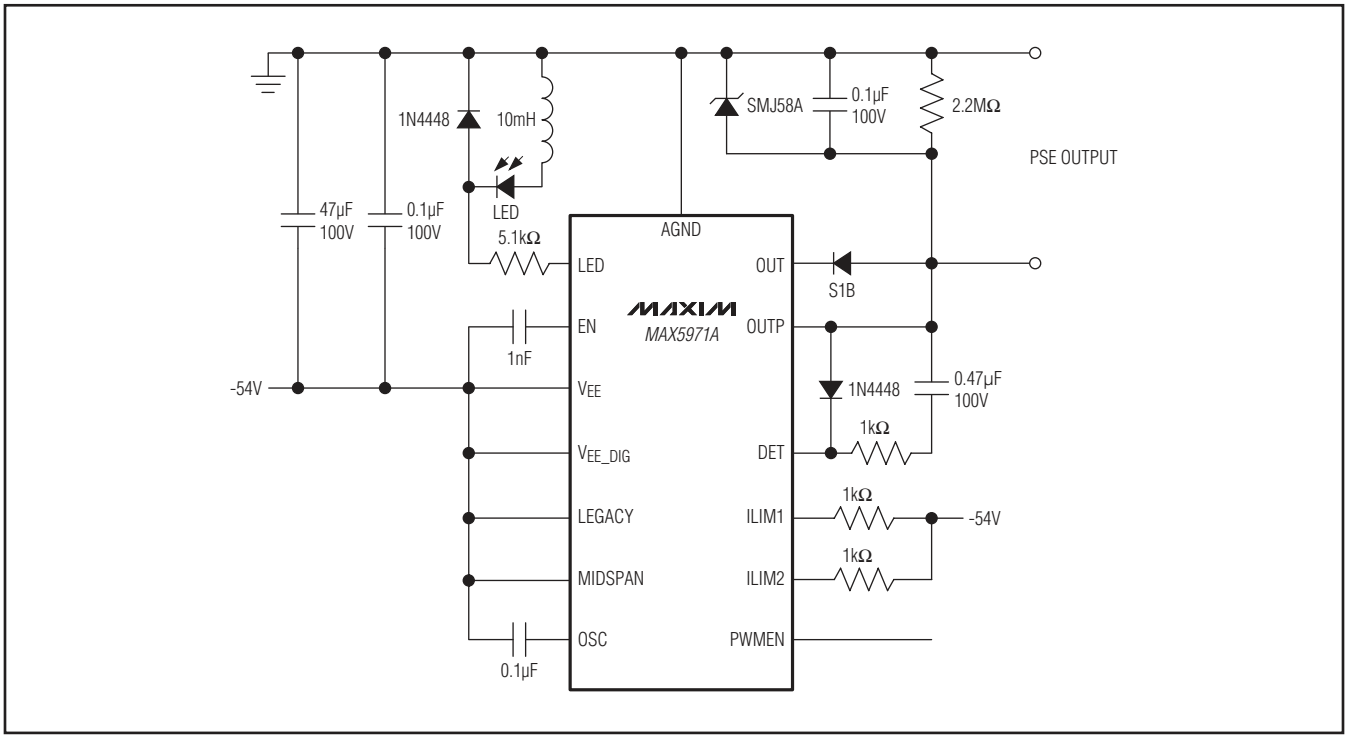

Figure 7. Typical Operating Circuit 2 (AC Load Removal Detection, Internal PWM Enabled for LED Indication, and Class 5 Detection Enabled)

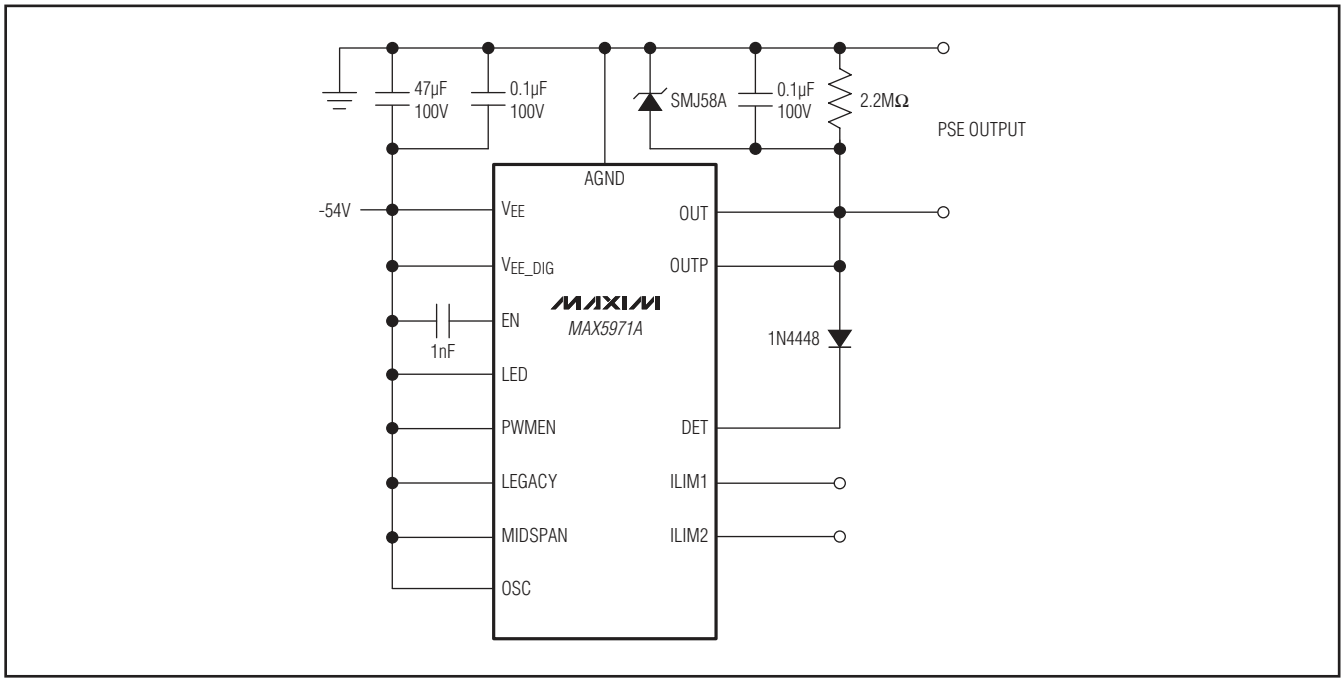

Figure 8. Typical Operating Circuit 3 (IEEE 802.3at Compliant, Minimal Application Circuit with DC Load Removal Detection and No LED Indication)

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Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T2855+6	21-0140	90-0026

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/10	Initial release	—
1	9/10	Updated the *Electrical Characteristics*.	4