

HA-2640, HA-2645

4MHz, High Supply Voltage Operational Amplifiers

FN2904
Rev 6.00
August 7, 2015

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

These amplifiers deliver $\pm 35V$ common mode input voltage range, $\pm 35V$ output voltage swing, and up to $\pm 40V$ supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and $5V/\mu s$ slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excitation designs.

Features

- Output Voltage Swing $\pm 35V$
- Supply Voltage $\pm 10V$ to $\pm 40V$
- Offset Current. 5nA
- Bandwidth 4MHz
- Slew Rate. $5V/\mu s$
- Common Mode Input Voltage Range. $\pm 35V$
- Output Overload Protection

Applications

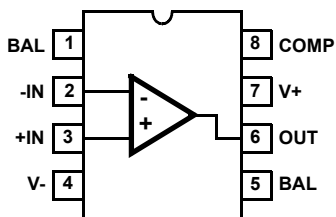
- Industrial Control Systems
- Power Supplies
- High Voltage Regulators
- Resolver Excitation
- Signal Conditioning

Ordering Information

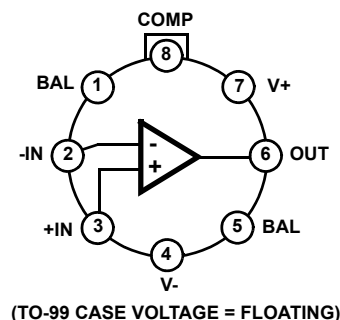
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA2-2640-2	HA2-2640-2	-55 to 125	8 Pin Metal Can	T8.C
HA7-2640-2	HA7-2640-2	-55 to 125	8 Ld CERDIP	F8.3A
HA2-2645-5 (No longer available or supported)	HA2-2645-5	0 to 75	8 Pin Metal Can	T8.C
HA7-2645-5 (No longer available or supported)	HA7-2645-5	0 to 75	8 Ld CERDIP	F8.3A

Pinouts

HA-2640/2645
(CERDIP)
TOP VIEW



HA-2640/2645
(METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 100V
 Differential Input Voltage Range 37V
 Output Current Full Short Circuit Protection

Operating Conditions

Temperature Range
 HA-2640-2 -55°C to 125°C
 HA-2645-5 0°C to 75°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W) θ_{JC} (°C/W)
 CERDIP Package 135 50
 Metal Can Package 165 80
 Maximum Junction Temperature 175°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C

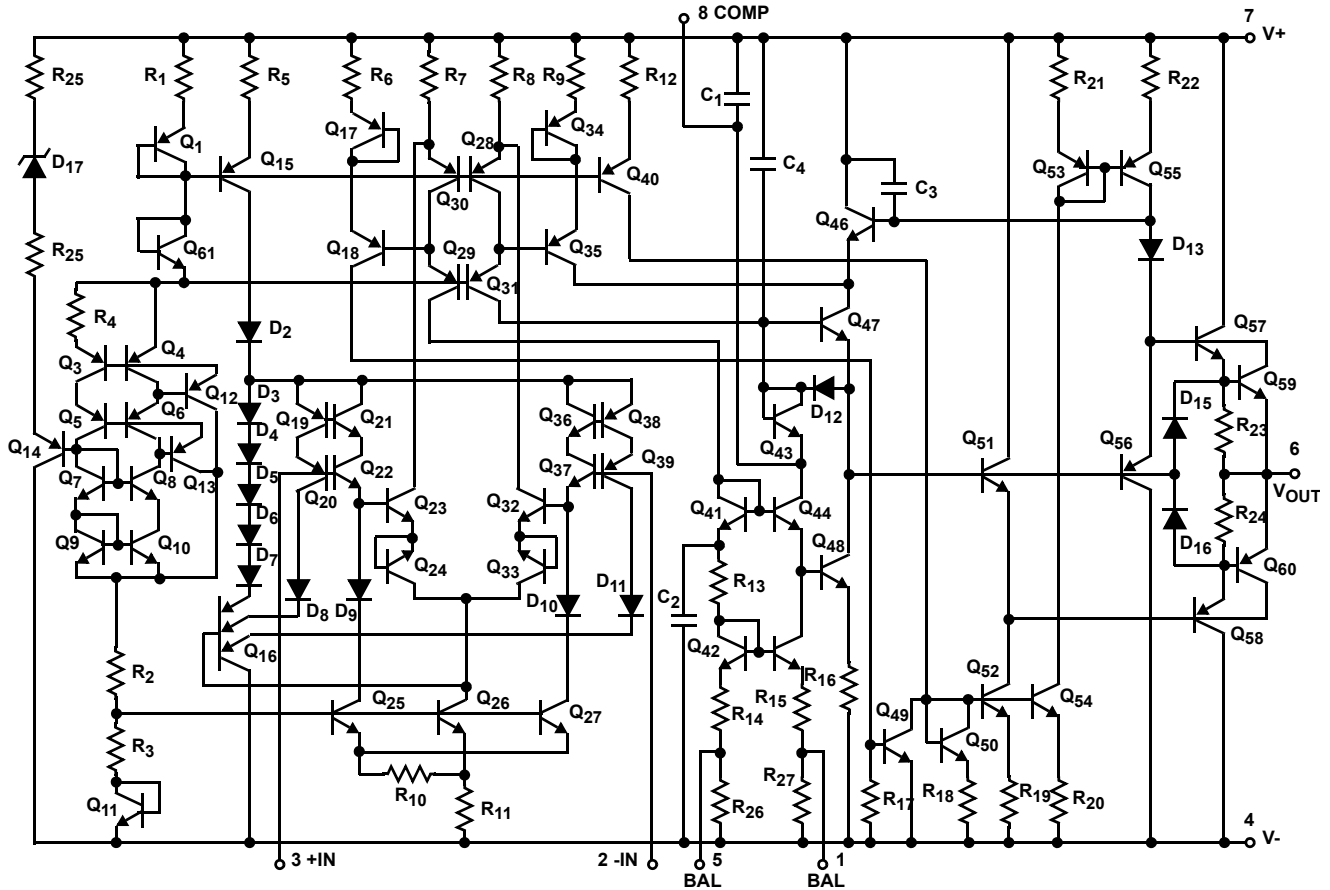
Electrical Specifications $V_{SUPPLY} = \pm 40V$, $R_L = 5k\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-2640-2			HA-2645-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	2	4	-	2	6	mV
		Full		-	6	-	-	7	mV
Average Offset Voltage Drift		Full	-	15	-	-	15	-	$\mu V/^\circ C$
Bias Current		25	-	10	25	-	12	30	nA
		Full	-	-	50	-	-	50	nA
Offset Current		25	-	5	12	-	15	30	nA
		Full	-	-	35	-	-	50	nA
Input Resistance (Note 2)		25	50	250	-	40	200	-	M Ω
Common Mode Range		Full	± 35	-	-	± 35	-	-	V
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$V_{OUT} = \pm 30V$	25	100	200	-	100	200	-	kV/V
		Full	75	-	-	75	-	-	-
Common Mode Rejection Ratio	$V_{CM} = \pm 20V$	Full	80	100	-	74	100	-	dB
Minimum Stable Gain		25	1	-	-	1	-	-	V/V
Unity Gain Bandwidth	$V_{OUT} = 90mV$	25	-	4	-	-	4	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing		Full	± 35	-	-	± 35	-	-	V
Output Current	$R_L = 1k\Omega$	25	± 12	± 15	-	± 10	± 12	-	mA
Output Resistance	Open Loop	25	-	500	-	-	500	-	Ω
Full Power Bandwidth (Note 3)	$V_{OUT} = \pm 35V$	25	-	23	-	-	23	-	kHz
TRANSIENT RESPONSE $A_V = +1$, $C_L = 50pF$, $R_L = 5k\Omega$									
Rise Time	$V_{OUT} = \pm 200mV$	25	-	60	135	-	60	135	ns
Overshoot	$V_{OUT} = \pm 200mV$	25	-	15	30	-	15	40	%
Slew Rate		25	± 3	± 5	-	± 2.5	± 5	-	V/ μs
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	3.2	3.8	-	3.2	4.5	mA
Supply Voltage Range		Full	± 10	-	± 40	± 10	-	± 40	V
Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 40V$	Full	80	90	-	74	90	-	dB

NOTES:

2. This parameter is based upon design calculations.
3. Full Power Bandwidth guaranteed based upon slew rate measurement: $FPBW = S.R./2\pi V_{PEAK}$; $V_{PEAK} = 35V$.

Schematic Diagram



Test Circuits and Waveform

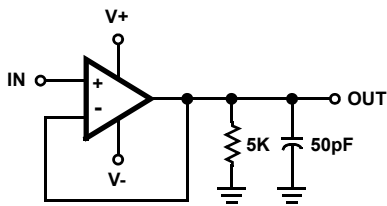
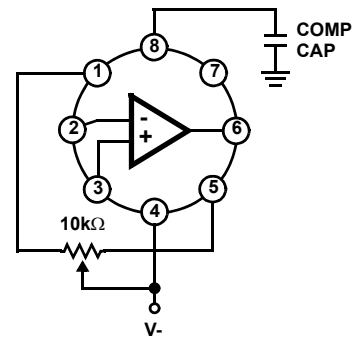


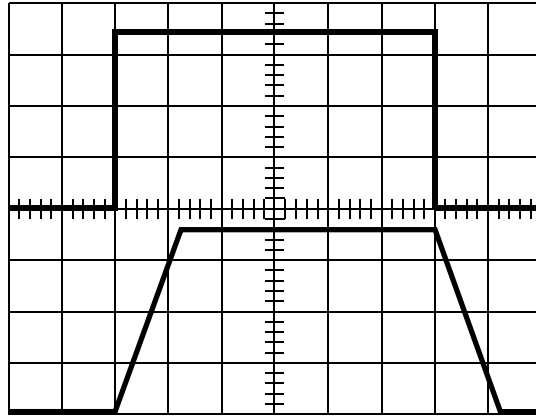
FIGURE 1. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



NOTE: Tested offset adjustment range is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is $\pm 20mV$ with $R_T = 10k\Omega$.

FIGURE 2. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

Test Circuits and Waveform (Continued)



Vertical = 10V/Div., Horizontal = 5μs/Div.

NOTE: $R_L = 5k\Omega$, $C_L = 50pF$, $T_A = 25^\circ C$, $V_S = \pm 40V$

FIGURE 3. VOLTAGE FOLLOWER PULSE RESPONSE

Typical Performance Curves $V_S = \pm 40V$, $T_A = 25^\circ C$, Unless Otherwise Specified

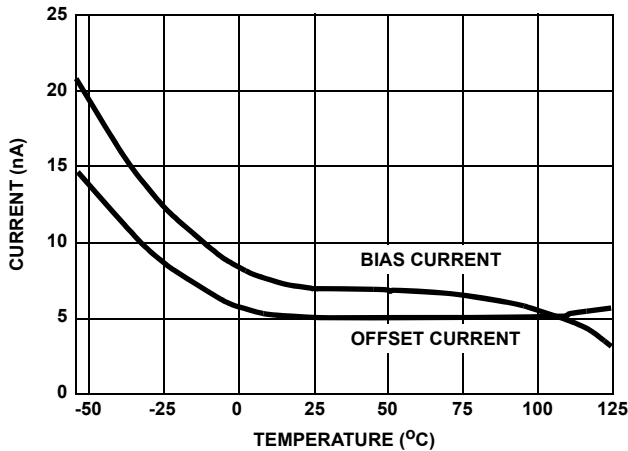


FIGURE 4. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

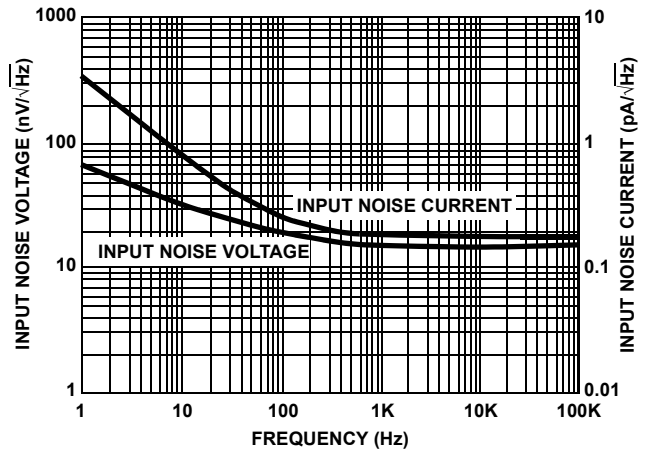


FIGURE 5. INPUT NOISE CHARACTERISTICS

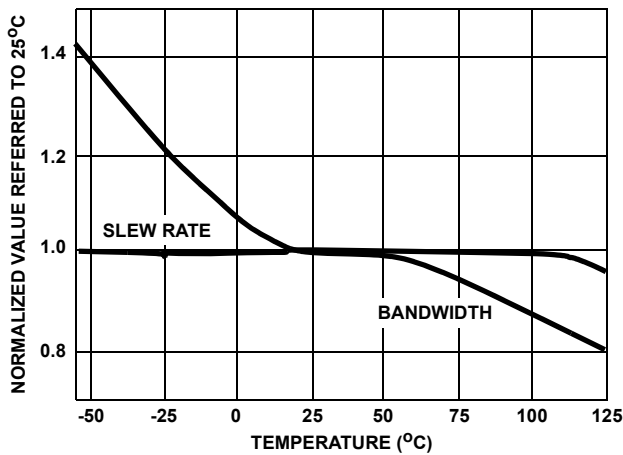


FIGURE 6. NORMALIZED AC PARAMETERS vs TEMPERATURE

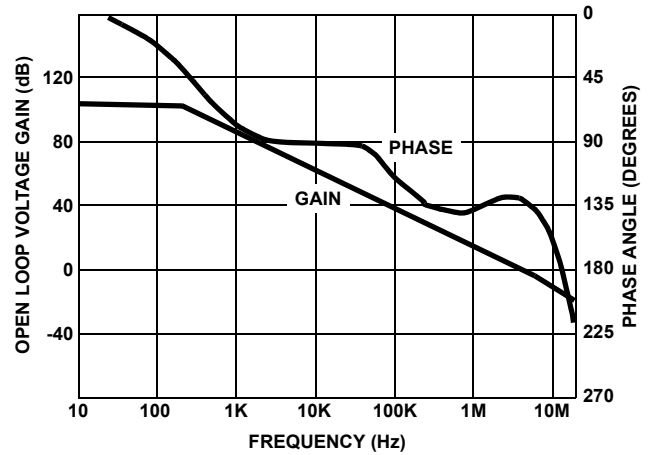


FIGURE 7. OPEN LOOP FREQUENCY RESPONSE

Typical Performance Curves $V_S = \pm 40V$, $T_A = 25^\circ C$, Unless Otherwise Specified (Continued)

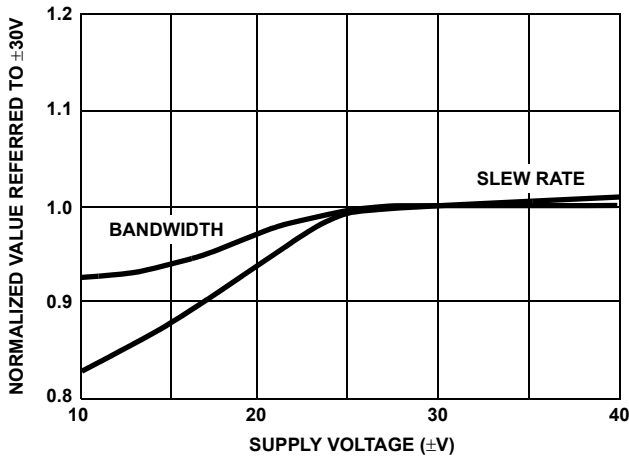


FIGURE 8. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT 25°C

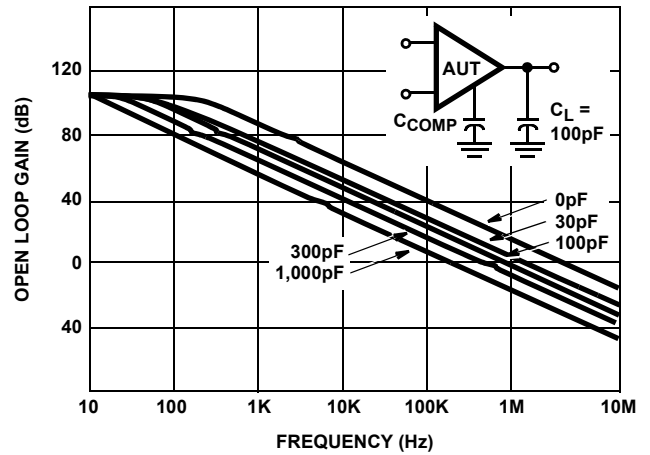


FIGURE 9. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

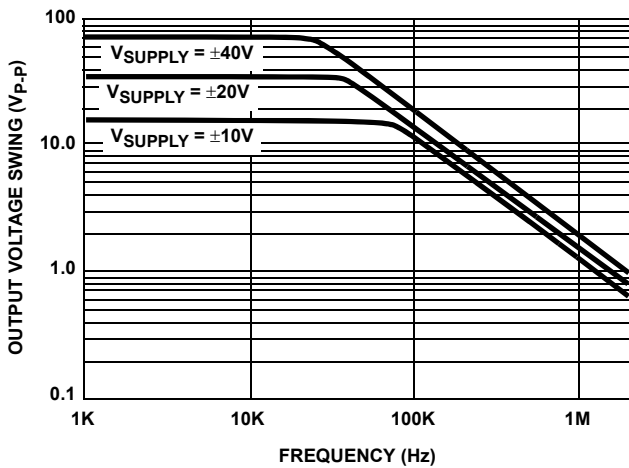


FIGURE 10. OUTPUT VOLTAGE SWING vs FREQUENCY

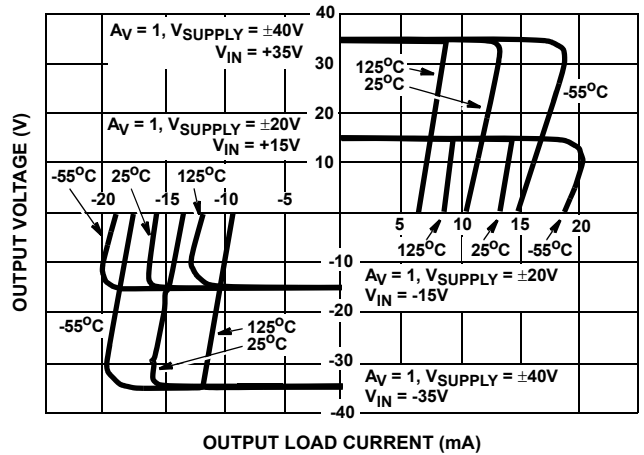


FIGURE 11. OUTPUT CURRENT CHARACTERISTIC

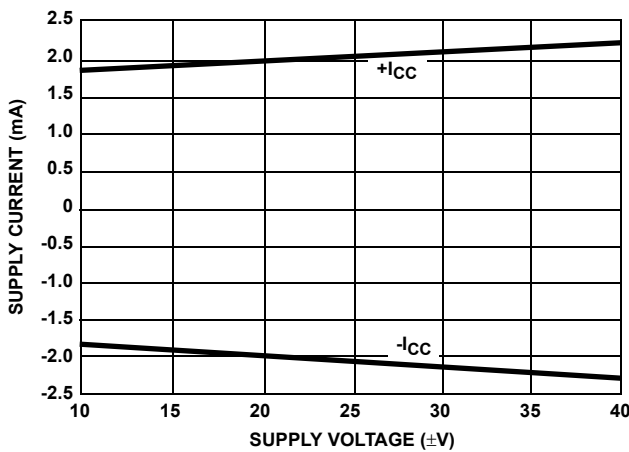


FIGURE 12. SUPPLY CURRENT vs SUPPLY VOLTAGE

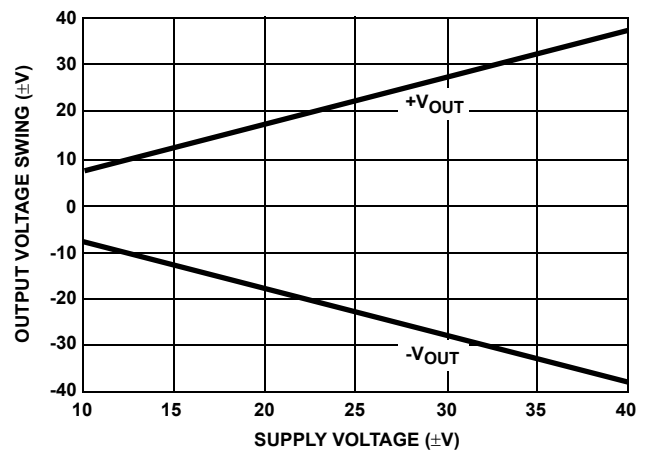


FIGURE 13. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (Powered Up):

Unbiased

TRANSISTOR COUNT:

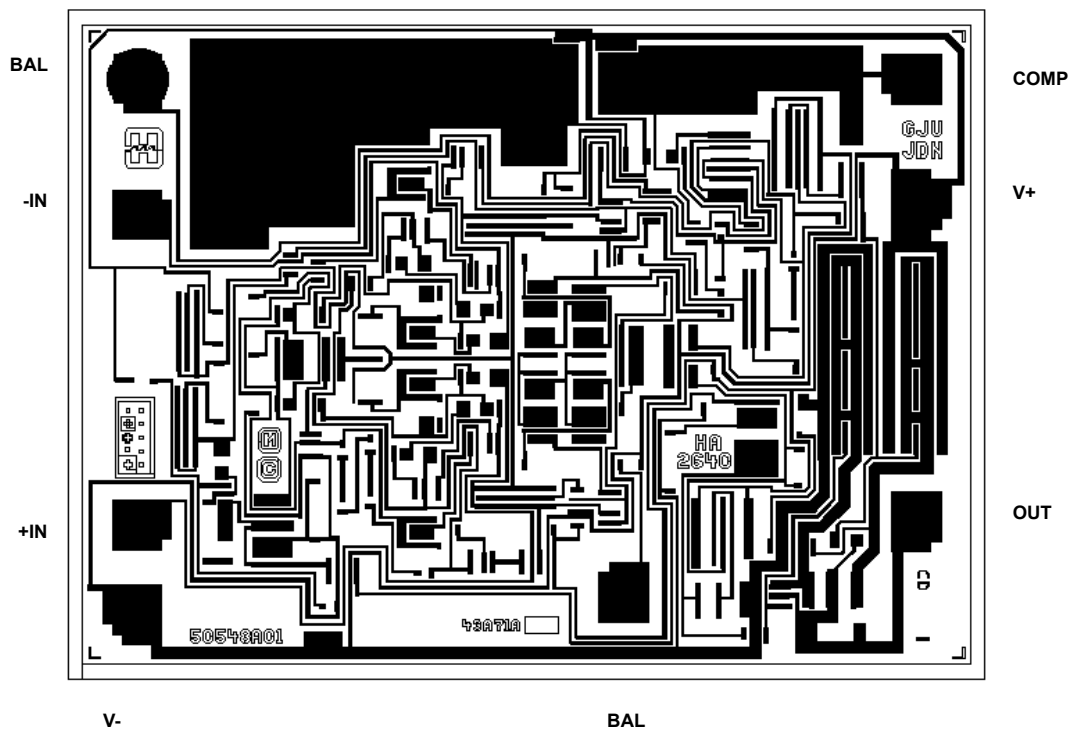
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PROCESS:

HV200 Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2640, HA-2645



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 7, 2015	FN2904.6	Page 1, Ordering Information table: HA2-2645-5 and HA7-2645-5 no longer available or supported. Added Revision History and About Intersil.

About Intersil

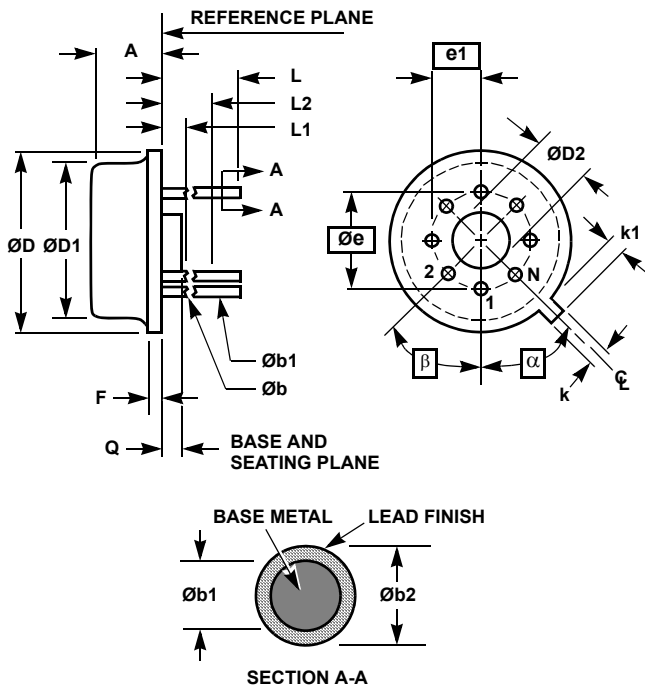
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Metal Can Packages (Can)



NOTES:

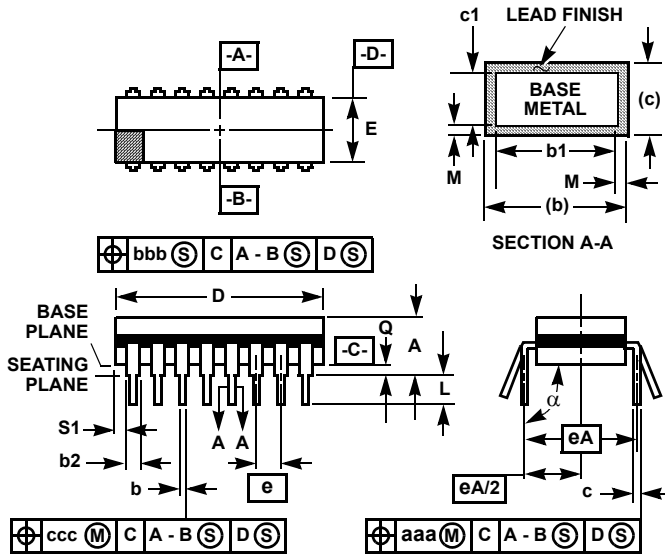
1. (All leads) $\varnothing b$ applies between $L1$ and $L2$. $\varnothing b1$ applies between $L2$ and 0.500 from the reference plane. Diameter is uncontrolled in $L1$ and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position ($N - 1$ places) from α , looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

**T8.C MIL-STD-1835 MACY1-X8 (A1)
8 LEAD METAL CAN PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
$\varnothing b$	0.016	0.019	0.41	0.48	1
$\varnothing b1$	0.016	0.021	0.41	0.53	1
$\varnothing b2$	0.016	0.024	0.41	0.61	-
$\varnothing D$	0.335	0.375	8.51	9.40	-
$\varnothing D1$	0.305	0.335	7.75	8.51	-
$\varnothing D2$	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45° BSC		45° BSC		3
β	45° BSC		45° BSC		3
N	8		8		4

Rev. 0 5/18/94

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

**F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

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