AFCT-57F5ATMZ

Digital Diagnostic SFP+, 1310 nm, 16 GFC [14.025/8.5/4.25 GBd]
Fibre Channel Optical Transceiver
Temperature Range 0 to 85 °C T_{case}

Data Sheet

Description

Avago Technologies' AFCT-57F5ATMZ optical transceiver supports high speed serial links over single mode optical fiber at signalling rates up to 14.025 Gb/s (the serial line rate of 16 GFC). The product is compliant with Small Form Pluggable industry agreements SFP and SFP+ for mechanical and low speed electrical specifications. High speed electrical and optical specifications are compliant with ANSI Fibre Channel FC-PI-5.

The AFCT-57F5ATMZ is a multi-rate 1310 nm transceiver which ensures compliance with FC-PI-5 16 GFC, 8 GFC and 4 GFC specifications. Per the requirements of 16 GFC, an internal clock and data recovery circuit (CDR) is present on the electrical output of this transceiver. This CDR will lock at 14.025Gb/s (16 GFC) but must be bypassed for operation at 8.5Gb/s (8 GFC) and 4.25Gb/s (4 GFC), accomplished by using Rate Select inputs to configure transmit and receive sides. Transmitter and receiver can operate at different data rates, as is often seen during Fibre Channel speed negotiation.

Digital diagnostic monitoring information (DMI) is present in the AFCT-57F5ATMZ per the requirements of SFF-8472, providing real time monitoring information of transceiver laser, receiver and environment conditions over a SFF-8431 2-wire serial interface.

Related Products

- AFBR-57F5TPZ: 850 nm SFP for 16G/8G/4G Fibre Channel
- AFBR-57D7APZ: 850 nm SFP for 8G/4G/2G Fibre Channel
- AFCT-57D5ATPZ: 1310 nm SFP for 8G/4G/2G Fibre Channel
- AFCT-57D5ANPZ: 1310 nm SFP for 8G/4G/2G Fibre Channel
- AFBR-57R5APZ: 850 nm SFP for 4G/2G/1G Fibre Channel
- AFCT-57R5APZ: 1310 nm SFP for 4G/2G/1G Fibre Channel
- AFCT-57R5ATPZ: 1310 nm SFP for 4G/2G/1G Fibre Channel
- AFCT-57R5ANPZ: 1310 nm SFP for 4G/2G/1G Fibre Channel

Features

- Compliant to RoHS directives
- 1310nm Distributed Feedback Laser (DFB)
- Class 1 eye safe per IEC60825-1 and CDRH
- Wide temperature range (0 °C to 85 °C)
- LC duplex connector optical interface conforming to ANSI TIA/EIA604-10 (FOCIS 10A)
- Diagnostic features per SFF-8472 "Diagnostic Monitoring Interface for Optical Transceivers"
- Enhanced operational features including EWRAP, OWRAP and variable electrical EQ/emphasis settings
- Real-time monitoring of:
  - Transmitter average optical power
  - Received average optical power
  - Laser bias current
  - Temperature
  - Supply Voltage
- SFP+ mechanical specifications per SFF-8432
- Pull Tab delatch mechanism
- SFP+ compliant low speed interface
- Fibre Channel FC-PI-5 compliant high speed interface
  - 1600- SM-LC-L, 800- SM-LC-L, 400-SM-LC-L
- Fibre Channel FC-PI-5 compliant 10km link distances

Applications

- Fibre Channel switches (director, stand alone, blade)
- Fibre Channel Host Bus Adapters
- Fibre Channel RAID controllers
- Fibre Channel tape drive
- Port side connections
- Inter-switch or inter-chassis aggregated links

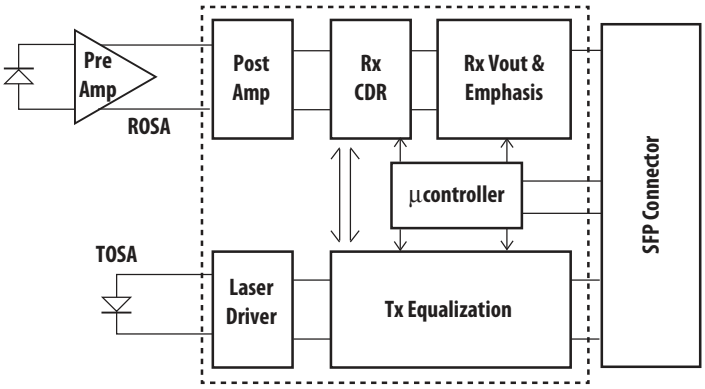


Figure 1. Transceiver functional diagram

Transmitter Section

The transmitter section includes a Transmitter Optical SubAssembly (TOSA), laser driver circuit and an electrical input stage with variable equalization controls. The TOSA contains a 1310nm Distributed Feedback Laser (DFB) light source with integral light monitoring function and imaging optics to assure efficient optical coupling to the LC connector interface. The TOSA is driven by a laser driver IC, which uses the differential output from an integral Tx equalization stage to modulate and regulate DFB optical power. Between the SFP electrical connector and Laser Driver is a variable, I^2C-bus controlled, equalization circuit to optimize SFP performance with non-ideal incoming electrical waveforms.

Receiver Section

The receiver section includes a Receiver Optical SubAssembly (ROSA), pre-amplification and post-amplification circuit, Clock and Data Recovery Circuit and an electrical output stage with variable emphasis controls. The ROSA, containing a high speed PIN detector, pre-amplifier and imaging optics efficiently couple light from the LC connector interface and perform an optical to electrical conversion. The resulting differential electrical signal passes through a post amplification circuit and into a Clock and Data Recovery circuit (CDR) for cleaning up accumulated jitter. The resulting signal is passed to a high speed output line driver stage with variable, I^2C-bus controlled, emphasis settings allowing the host to optimize signal characteristics between the SFP and host ASIC. Note the Rx CDR is engaged only with Rx_RATE=high (16 GFC) and bypassed with Rx_RATE=low (8G/4G).

Digital Diagnostics

The AFCT-57F5ATPZ is compliant to the Diagnostic Monitoring Interface (DMI) defined in document SFF-8472. These features allow the host to access, via I^2C-bus, real time diagnostic monitors of transmit optical power, received optical power, temperature, supply voltage and laser operating current.

Low Speed Interfaces

Conventional low speed interface I/Os are available as defined in documents SFF-8074 and SFF-8431 to manage coarse and fine functions of the optical transceiver. On the transmit side, a Tx_DISABLE input is provided for the host to turn on and off the outgoing optical signal. A transmitter rate select control input, Tx_RATE, is provided to configure the transmitter stages for 16 GFC, 8 GFC or 4 GFC operation (logic HIGH , reserved for 16 GFC, logic LOW , reserved for 8 GFC and 4 GFC). A transmitter fault indicator output, Tx_FAULT, is available for the SFP to signal a host of a transmitter operational problem. A receiver rate select control input, Rx_RATE, is provided to configure receiver stages for 16 GFC, 8 GFC or 4 GFC operation (logic HIGH reserved for 16 GFC, logic LOW reserved for 8 GFC and 4 GFC). A received optical power loss of signal indicator, RX_LOS, is available to advise the host of a receiver operational problem.

Regulatory Compliance

The AFCT-57F5ATMZ complies with all applicable laws and regulations as detailed in Table 1. Certification level is dependent on the overall configuration of the host equipment. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

The AFCT-57F5ATMZ is compatible with ESD levels found in typical manufacturing and operating environments as described in Table 1. In the normal handling and operation of optical transceivers, ESD is of concern in two circumstances.

The first case is during handling of the transceiver before it is inserted into an SFP compliant cage. To protect the device, it is important to use normal ESD handling precautions. These include use of grounded wrist straps, work-benches and floor wherever a transceiver is handled.

The second case to consider is static discharges to the exterior of the host equipment chassis after installation. If the optical interface is exposed to the exterior of host equipment cabinet, the transceiver may be subject to system level ESD requirements.

Electromagnetic Interference (EMI)

Equipment incorporating gigabit transceivers is typically subject to regulation by the FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. The AFCT-57F5ATMZ's compliance to these standards is detailed in Table 1. The metal housing and shielded design of the AFCT-57F5ATMZ minimizes the EMI challenge facing the equipment designer.

EMI Immunity (Susceptibility)

Due to its shielded design, the EMI immunity of the AFCT-57F5ATMZ exceeds typical industry standards.

Flammability

The AFCT-57F5ATMZ optical transceiver is made of metal and high strength, heat resistant, chemical resistant and UL 94 flame retardant plastic.

Table 1. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	JEDEC A114	Class 1 (> 2000 V) >1000 V for high speed signal pins TD+/-, RD+/-
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	Variation of IEC 61000-4-2	Typically, no damage occurs with 25 kV when the duplex LC connector receptacle is contacted by a Human Body Model probe.
	GR1089	10 contacts of 8 kV on the electrical faceplate with device inserted into a panel.
Electrostatic Discharge (ESD) to the Optical Connector	Variation of IEC 801-2	Air discharge of 15 kV (min.) contact to connector without damage.
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22A) VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 10 V/m field swept from 10 MHz to 1 GHz.
Laser Eye Safety and Equipment Type Testing	US FDA CDRH EN 60825-1:2007 EN 60950-1:2006+A11+A1+A12	Class 1 Laser product
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL file 173874
RoHS Compliance		Less than 1000 ppm of cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl ethers.

Special Operation Functions

Electrical and optical high speed data "wrap" functions are enabled to assist with local host or remote diagnostic and optimization sequences. Optical data wrap (OWRAP) takes a received optical signal through a CDR jitter cleanup and retransmits it optically out. Electrical data wrap (EWRAP) takes an incoming electrical signal through a CDR jitter cleanup and retransmits it electrically out. An optional pass-through function is available to transmit outbound the wrapped information, controlled through I²C-bus commands.

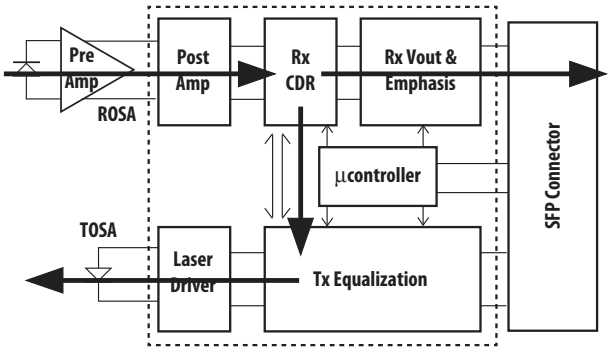


Figure 2a. OWRAP Functionality (I²C-bus controlled)

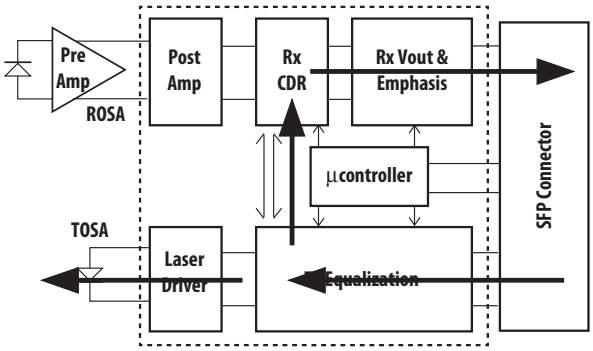


Figure 2b. EWRAP Functionality (I²C-bus controlled)

The electrical SFP input stage (TD +/-) has been enhanced with features to allow host control and optimization of the transceiver's input equalization settings. The host can then select, in situ, the most appropriate SFP setting for a given interconnect scenario.

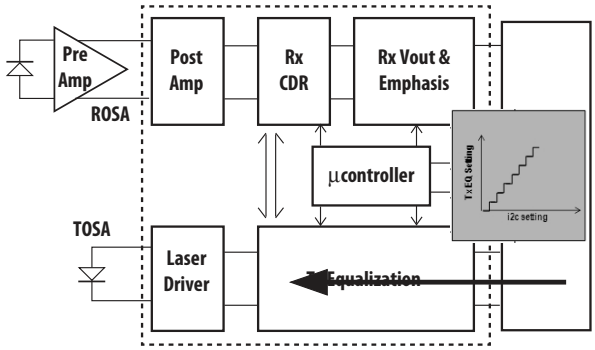


Figure 2c. SFP Tx Variable Input Electrical EQ (I²C-bus controlled)

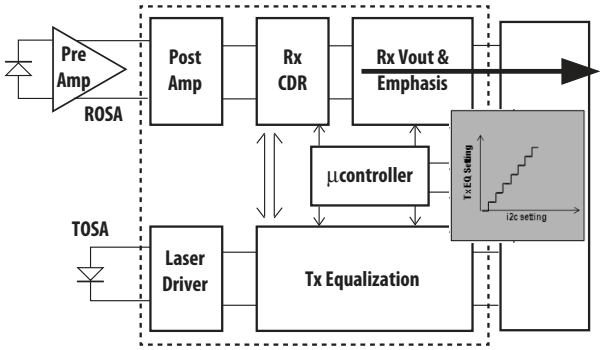


Figure 2d. SFP Rx Variable Output Electrical Emphasis (I²C-bus controlled)

The SFP electrical output stage (RD+/-) has been enhanced with variable output emphasis features to allow host control and optimization of the receiver's output settings. The host can then select, in situ, the most appropriate SFP setting for a given interconnect scenario. To assist with optimizing the receiver output setting, the user can have data transmitted by the SFP to a host ASIC by using EWRAP to loop back host generated traffic or can use a remotely generated optical signal as a data source for SFP and interconnect training.

Table 2. Rate Select Function

Function	State	Explanation
Rx Rate Select RS(0)	High	Receive Rate Select HIGH engages the internal Rx CDR. The CDR will look for valid 16 GFC traffic (14.025Gb/s coded with 64b/66b) and lock within 500 µs when found. Due to differences in coding and bit rate, this CDR will not be able to lock on valid 8 GFC or 4 GFC traffic.
	Low	Receive Rate Select LOW bypasses the internal Rx CDR. This is intended for use only with 8 GFC and 4 GFC traffic. When set low, the SFP behaves like a legacy SFP.
Tx Rate Select RS(1)	High	Transmit Rate Select HIGH optimizes the transmitter performance for 16 GFC traffic.
	Low	Transmit Rate Select LOW optmizes the transmitter performance for 4 GFC and 8 GFC traffic.

Note: During Fibre Channel Link Speed Negotiation sequences, the host will control Tx Rate and Rx Rate inputs separately to accomplish link initialization. Once speed negotiation is complete, it is expected both Tx Rate and Rx Rate will be placed in the same state by the host.

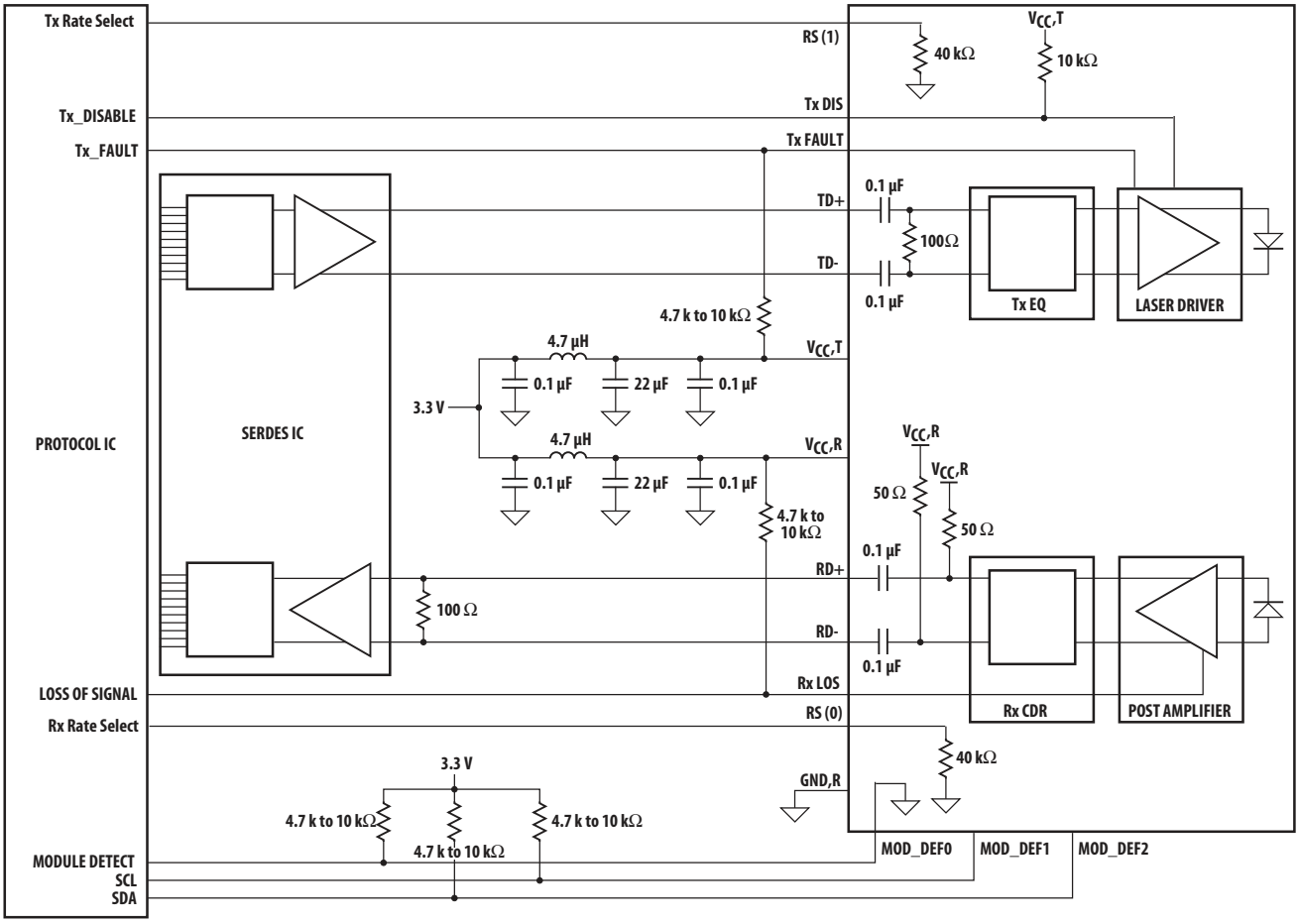
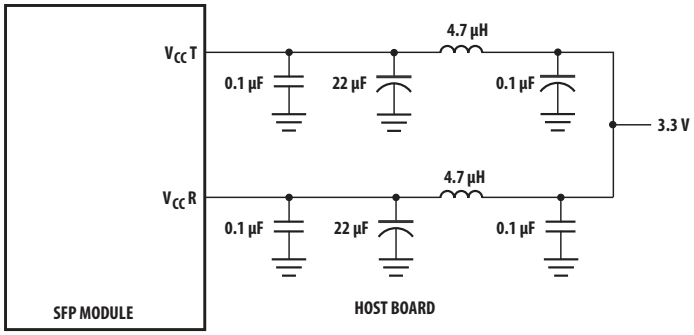


Figure 3. Typical application configuration.



NOTE: INDUCTORS MUST HAVE LESS THAN 1Ω SERIES RESISTANCE TO LIMIT VOLTAGE DROP TO THE SFP MODULE.

Figure 4. Recommended power supply filter.

Table 3. Pin Description

Pin	Name	Function/Description	Notes
1	VeeT	Transmitter Ground	
2	TX_FAULT	Transmitter Fault Indication – High indicates a fault condition	Note 1
3	TX_DISABLE	Transmitter Disable – Module electrical input disables on high or open	Note 2
4	MOD-DEF2	Module Definition 2 – Two wire serial ID interface data line (SDA)	Note 3
5	MOD-DEF1	Module Definition 1 – Two wire serial ID interface clock line (SCL)	Note 3
6	MOD-DEF0	Module Definition 0 – Grounded in module (module present indicator)	Note 3
7	Rx Rate Select RS(0)	Receiver rate select. Logic High = 14.025 Gb/s, Logic Low = 8.5 Gb/s and 4.25 Gb/s	Note 8
8	RX_LOS	Loss of Signal – High indicates loss of received optical signal	Note 4
9	Tx Rate Select RS(1)	Transmitter rate select. Logic High = 14.025 Gb/s, Logic Low = 8.5 Gb/s and 4.25 Gb/s	Note 8
10	VeeR	Receiver Ground	
11	VeeR	Receiver Ground	
12	RD-	Inverse Received Data Out	Note 5
13	RD+	Received Data Out	Note 5
14	VeeR	Receiver Ground	
15	VccR	Receiver Power + 3.3 V	Note 6
16	VccT	Transmitter Power + 3.3 V	Note 6
17	VeeT	Transmitter Ground	
18	TD+	Transmitter Data In	Note 7
19	TD-	Inverse Transmitter Data In	Note 7
20	VeeT	Transmitter Ground	

Notes:

1. TX_FAULT is an open collector/drain output, which must be pulled up with a 4.7 k – 10 kΩ resistor on the host board. When high, this output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to < 0.8 V.
2. TX_DISABLE is an input that is used to shut down the transmitter optical output. It is internally pulled up (within the transceiver) with a 6.8 kΩ resistor.
   - Low (0 – 0.8 V): Transmitter on
   - Between (0.8 V and 2.0 V): Undefined
   - High (2.0 – Vcc max) or OPEN: Transmitter Disabled
3. The signals Mod-Def 0, 1, 2 designate the two wire serial interface pins. They must be pulled up with a 4.7 k – 10 kΩ resistor on the host board.
   - Mod-Def 0 is grounded by the module to indicate the module is present
   - Mod-Def 1 is serial clock line (SCL) of two wire serial interface
   - Mod-Def 2 is serial data line (SDA) of two wire serial interface
4. RX_LOS (Rx Loss of Signal) is an open collector/drain output that must be pulled up with a 4.7 k – 10 kΩ resistor on the host board. When high, this output indicates the received optical power is below the worst case receiver sensitivity (as defined by the standard in use). Low indicates normal operation. In the low state, the output will be pulled to < 0.8 V.
5. RD-/+ designate the differential receiver outputs. They are AC coupled 100 Ω differential lines which should be terminated with 100 Ω differential at the host SERDES input. AC coupling is done inside the transceiver and is not required on the host board. The voltage swing on these lines will be between 370 and 850 mV differential (185 – 425 mV single ended) when properly terminated.
6. VccR and VccT are the receiver and transmitter power supplies. They are defined at the SFP connector pin. The maximum supply current is 300 mA and the associated in-rush current will typically be no more than 30 mA above steady state after 2 microseconds.
7. TD-/+ designate the differential transmitter inputs. They are AC coupled differential lines with 100 Ω differential termination inside the module. The AC coupling is done inside the module and is not required on the host board. The inputs will accept differential swings of 180 – 1200 mV (90 – 600 mV single ended)
8. Rate_Select is an input that is used to control transmit and receive high speed parametric optimizaton. It is internally pulled down (within the transceiver) with a 40kOhm resistor.
   - Low (0 - 0.8V) or Open: Rate is set to 8.5Gb/s and below optimization. For Rx Rate_Select, the internal CDR is bypassed.
   - Between (0.8V and 2.0V) Undefined
   - High (2.0 - Vcc max): Rate is set to 14.025Gb/s optimization. For Rx Rate_Select, the internal CDR is engaged.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Storage Temperature	T_S	-40	85	C	Note 1, 2
Case Operating Temperature	T_C	-40	85	C	Note 1, 2
Relative Humidity	RH	5	95	%	Note 1
Supply Voltage	$Vcc_{T, R}$	-0.5	3.8	V	Note 1, 2, 3
Low Speed Input Voltage	V_{IN}	-0.5	Vcc+0.5	V	Note 1

Notes;

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur if these limits are exceeded for other than a short period of time. See Reliability Data Sheet for specific reliability performance.
2. Between Absolute Maximum Ratings and the Recommended Operating Conditions functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time.
3. The module supply voltages, $V_{CC}T$ and $V_{CC}R$ must not differ by more than 0.5 V or damage to the device may occur.

Table 5. Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Case Operating Temperature	T_C	0	85	°C	Note 1, 2
Supply Voltage	$Vcc_{T, R}$	3.135	3.465	V	Note 2
Data Rate		4.25	14.025	Gb/s	Note 2

Notes:

1. The Ambient Operating Temperature limitations are based on the Case Operating Temperature limitations and are subject to the host system thermal design.
2. Recommended Operating Conditions are those values for which functional performance and device reliability is implied.

Table 6. Transceiver Electrical Characteristics
(T_C = 0 °C to 85 °C, V_{ccT}, V_{ccR} = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
AC Electrical Characteristics						
Power Supply Noise Rejection (peak-peak)	PSNR	100			mV	Note 1
DC Electrical Characteristics						
Module Supply Current	I_{CC}			330	mA	
Low Speed Outputs:	V_{OH}	2.0		$V_{ccT,R}$+0.3	V	Note 2
Transmit Fault (TX_FAULT), Loss of Signal (RX_LOS), MOD-DEF 2	V_{OL}			0.8	V	
Low Speed Inputs:	V_{IH}	2.0		Vcc	V	Note 3
Transmit Disable (TX_DIS), MOD-DEF 1, MOD-DEF2, RS(0), RS(1)	V_{IL}	0		0.8	V	

Notes:

1. Filter per SFP specification is required on host board to remove 10 Hz to 2 MHz content.
2. Pulled up externally with a 4.7 k – 10 kΩ resistor on the host board to 3.3 V.
3. Mod-Def1 and Mod-Def2 must be pulled up externally with a 4.7 k – 10 kΩ resistor on the host board to 3.3 V.

Table 7. Transmitter and Receiver Electrical Characteristics

(T_c = 0 °C to 85 °C, V_{ccT}, V_{ccR} = 3.3 V ± 5%)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
High Speed Data Input Transmitter Differential Input Voltage (TD+/-)	V_I	180		1200	mV	Note 1
High Speed Data Output Receiver Differential Output Voltage (RD+/-)	V_o	370		850	mV	Note 2
Receiver Total Jitter (14.025 Gb/s)	TJ			0.36	UI	Note 3, Rx_Rate = high
Receiver Total Jitter (8.5 Gb/s)	TJ			0.71	UI	Note 4, Rx_Rate = low
Receiver Contributed Total Jitter (4.25 Gb/s)	TJ			0.26	UI	Note 4, Rx_Rate = low
Receiver Deterministic Jitter (14.025 Gb/s)	DJ			0.22	UI	Note 3, Rx_Rate = high
Receiver Deterministic Jitter (8.5 Gb/s)	DJ			0.42	UI	Note 4, Rx_Rate = low
Receiver Contributed Deterministic Jitter (4.25 Gb/s)	DJ			0.10	UI	Note 4, Rx_Rate = low
Receiver Data Dependent Pulse Width Shrinkage (14.025 Gb/s)	DDPWS			0.14	UI	Note 3, Rx_Rate = high
Receiver Data Dependent Pulse Width Shrinkage (8.5 Gb/s)	DDPWS			0.36	UI	Note 4, Rx_Rate = low

Notes:
1. Internally ac coupled and terminated (100Ω differential).
2. Internally ac coupled but requires an external load termination (100Ω differential).
3. CDR is engaged with Rx_Rate = high. Received output jitter for 14.025 Gb/s.
4. CDR is not engaged with Rx_Rate = low (ie. Bypassed). Receiver output jitter for 8.5 Gb/s and 4.25Gb/s.

Table 8. Transmitter Optical Characteristics

(T_c = 0 °C to 85 °C, V_{ccT}, V_{ccR} = 3.3V ± 5%)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Modulated Optical Output Power (OMA) (Peak to Peak) 14.025 Gb/s	Tx,OMA	631			uW	TxRate=High
Modulated Optical Output Power (OMA) (Peak to Peak) 8.5 Gb/s, 4.25 Gb/s	Tx,OMA	290			uW	TxRate=Low
Average Optical Output Power 14.025 Gb/s	P_{out}	-5.0			dBm	Note 1, TxRate=High
Average Optical Output Power 8.5 Gb/s, 4.25 Gb/s	P_{out}	-8.4			dBm	Note 1, TxRate=Low
Center Wavelength	λ_c	1295		1325	nm	
-20 dB Spectral Width	-20 dB			1.0	nm	
Side Mode Suppression		30			dB	
RIN12 (OMA)	RIN			-130	dB/Hz	
Transmitter Distortion Penalty, 14.025 Gb/s	TDP			4.4	dB	TxRate=High
Transmitter Distortion Penalty, 8.5 Gb/s	TDP			3.2	dB	TxRate=Low
Tx Optical Rise/Fall Time (20% - 80%), 4.25Gb/s	T_r, T_f			90	ps	TxRate=Low
Transmitter Contributed Jitter, 4.25 Gb/s	T_J			0.25	UI	TxRate=Low
P_{out} Tx_DISABLE Asserted	P_{off}			-35	dBm	

Notes:
1. Max P_{out} is the lesser of Class 1 safety limits (CDRH and EN 60825) or received power, max.

Table 9. Receiver Optical and Electrical Characteristics

(T_c = 0 °C to 85 °C, V_{ccT}, V_{ccR} = 3.3 V ± 5%)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver Optical Center Wavelength	λc	1260		1370	nm	
Optical Input Power, 14.025 Gb/s	P_{IN}			+2.0	dBm,avg	RxRate=High
Optical Input Power, 8.5 Gb/s	P_{IN}			+0.5	dBm,avg	RxRate=Low
Optical Input Power, 4.25 Gb/s	P_{IN}			-1.0	dBm,avg	RxRate=Low
Input Optical Modulation Amplitude, 14.025 Gb/s (Peak to Peak) [Unstressed Sensitivity]	OMA	63			uW,OMA	Note 1
Input Optical Modulation Amplitude, 8.5 Gb/s (Peak to Peak) [Unstressed Sensitivity]	OMA	42			uW,OMA	Note 1
Input Optical Modulation Amplitude, 4.25 Gb/s (Peak to Peak) [Unstressed Sensitivity]	OMA	29			uW,OMA	Note 1
Return Loss		12			dB	
Loss of Signal – Assert	P_a	-28			dBm,OMA	
Loss of Signal – De-asserted	P_D			-16	dBm,OMA	
Loss of Signal – Hysteresis	$P_A – P_D$	0.5			dB	

Notes:

1. Input Optical Modulation Amplitude (commonly known as sensitivity] requires a valid Fibre Channel encoded input.

Table 10. Transceiver DIAGNOSTIC Timing Characteristics

(T_C = 0 °C to 85 °C, V_{ccT}, V_{ccR} = 3.3 V ± 5%)

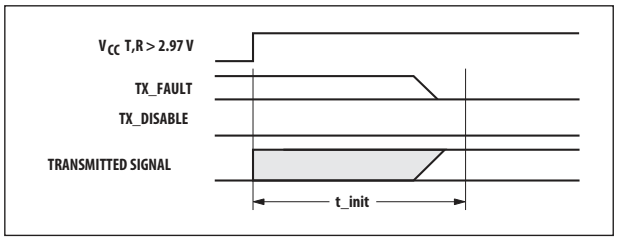
Parameter	Symbol	Minimum	Maximum	Unit	Notes
Hardware TX_DISABLE Assert Time	t_off		10	µs	Note 1
Hardware TX_DISABLE Negate Time	t_on		1	ms	Note 2
Time to initialize, including reset of TX_FAULT	t_init		300	ms	Note 3
Hardware TX_FAULT Assert Time	t_fault		1000	µs	Note 4
Hardware TX_DISABLE to Reset	t_reset	10		µs	Note 5
Hardware RX_LOS Deassert Time	t_loss_on		100	µs	Note 6
Hardware RX_LOS Assert Time	t_loss_off		100	µs	Note 7
Software TX_DISABLE Assert Time	t_off_soft		100	ms	Note 8
Software TX_DISABLE Negate Time	t_on_soft		100	ms	Note 9
Software Tx_FAULT Assert Time	t_fault_soft		100	ms	Note 10
Software Rx_LOS Assert Time	t_loss_on_soft		100	ms	Note 11
Software Rx_LOS Deassert Time	t_loss_off_soft		100	ms	Note 12
Analog parameter data ready	t_data		1000	ms	Note 13
Serial bus hardware ready	t_serial		300	ms	Note 14
Serial Bus Buffer Time	t_buf	20		µs	Note 16
Write Cycle Time	t_write		40	ms	Note 15
Serial ID Clock Rate	f_serial_clock		400	kHz	

Notes:
1. Time from rising edge of TX_DISABLE to when the optical output falls below 10% of nominal.
2. Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal.
3. Time from power on or falling edge of Tx_Disable to when the modulated optical output rises above 90% of nominal.
4. From power on or negation of TX_FAULT using TX_DISABLE.
5. Time TX_DISABLE must be held high to reset the laser fault shutdown circuitry.
6. Time from loss of optical signal to Rx_LOS Assertion.
7. Time from valid optical signal to Rx_LOS De-Assertion.
8. Time from two-wire interface assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the optical output falls below 10% of nominal. Measured from falling clock edge after stop bit of write transaction.
9. Time from two-wire interface de-assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the modulated optical output rises above 90% of nominal.
10. Time from fault to two-wire interface TX_FAULT (A2h, byte 110, bit 2) asserted.
11. Time for two-wire interface assertion of Rx_LOS (A2h, byte 110, bit 1) from loss of optical signal.
12. Time for two-wire interface de-assertion of Rx_LOS (A2h, byte 110, bit 1) from presence of valid optical signal.
13. From power on to data ready bit asserted (A2h, byte 110, bit 0). Data ready indicates analog monitoring circuitry is functional.
14. Time from power on until module is ready for data transmission over the serial bus (reads or writes over A0h and A2h).
15. Time from stop bit to completion of a 1 – 4 byte write command. Write cycle time is 80 ms max. for a 5 – 8 byte write.
16. Time between STOP and START Commands.

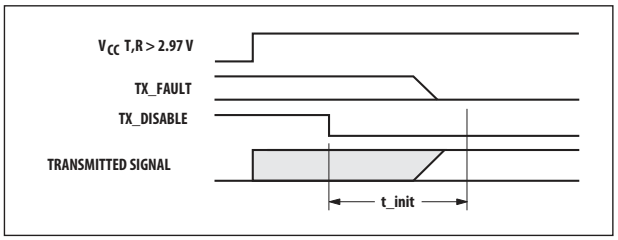
Table 11. Transceiver Digital Diagnostic Monitor (Real Time Sense) Characteristics

(T_C = 0 °C to 85 °C, V_{ccT}, V_{ccR} = 3.3 V ± 5%)

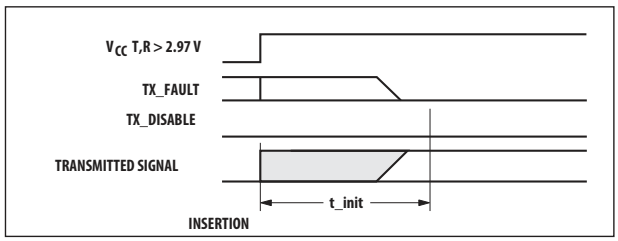
Parameter	Symbol	Min.	Units	Notes
Transceiver Internal Temperature Accuracy	T_{INT}	±3.0	°C	Temperature is measured internal to the transceiver. Valid from = 0 °C to 85 °C case temperature.
Transceiver Internal Supply Voltage Accuracy	V_{INT}	±0.1	V	Supply voltage is measured internal to the transceiver and can, with less accuracy, be correlated to voltage at the SFP Vcc pin. Valid over 3.3 V ± 5%.
Transmitter Laser DC Bias Current Accuracy	I_{INT}	±10	%	I_{INT} is better than ±10% of the nominal value.
Transmitted Average Optical Output Power Accuracy	P_T	±3.0	dB	Coupled into single-mode fiber. Valid from 144 µW to 1584 µW, avg.
Received Average Optical Input Power Accuracy	P_R	±3.0	dB	Coupled from single-mode fiber. Valid from 24 µW to 1584 µW, avg.



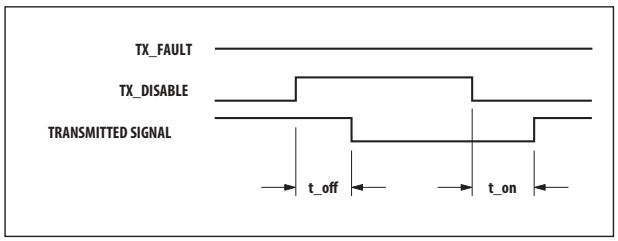
t-init: TX DISABLE NEGATED



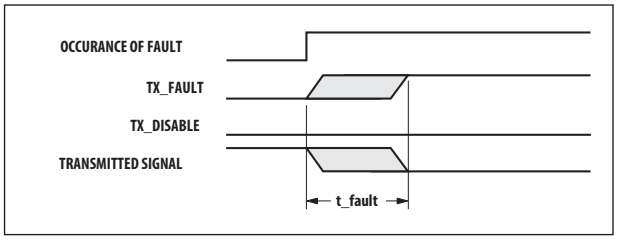
t-init: TX DISABLE ASSERTED



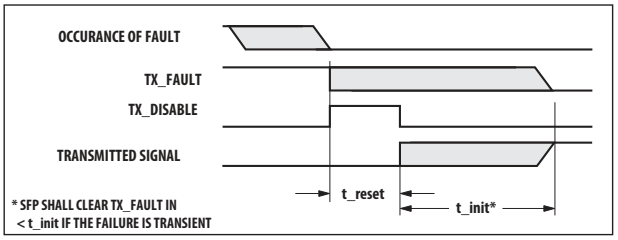
t-init: TX DISABLE NEGATED, MODULE HOT PLUGGED



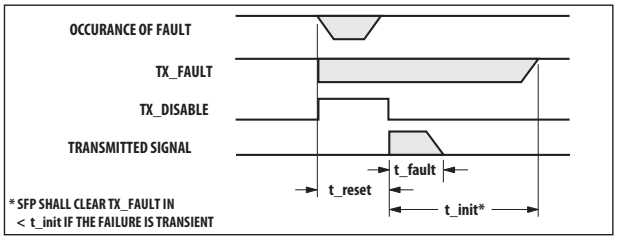
t-off & t-on: TX DISABLE ASSERTED THEN NEGATED



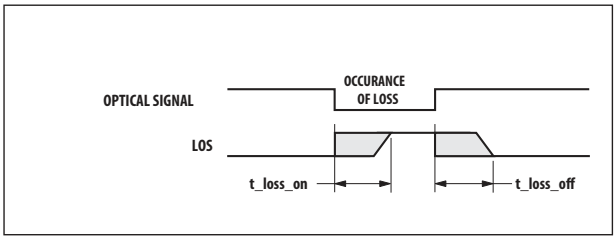
t-fault: TX FAULT ASSERTED, TX SIGNAL NOT RECOVERED



t-reset: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL RECOVERED



t-fault: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL NOT RECOVERED



t-loss-on & t-loss-off

Figure 4. Transceiver timing diagrams (module installed except where noted).

Table 12. EEPROM Serial ID Memory Contents – Base SFP Memory (Address A0h)

Byte # Decimal	Data Hex	Notes	Byte # Decimal	Data Hex	Notes
0	03	SFP physical device	37	00	Hex Byte of Vendor OUI [2]
1	04	SFP function defined by serial ID only	38	17	Hex Byte of Vendor OUI [2]
2	07	LC optical connector	39	6A	Hex Byte of Vendor OUI [2]
3	00		40	41	"A" - Vendor Part Number ASCII character
4	00		41	46	"F" - Vendor Part Number ASCII character
5	00		42	43	"C" - Vendor Part Number ASCII character
6	00		43	54	"T" - Vendor Part Number ASCII character
7	12	Long distance (per FC-PI-5), Longwave Laser (LC)	44	2D	"-" - Vendor Part Number ASCII character
8	00		45	35	"5" - Vendor Part Number ASCII character
9	01	Single mode optical media	46	37	"7" - Vendor Part Number ASCII character
10	70	400, 800 & 1600 Mbyte/s FC-PI-5 speed [1]	47	46	"F" - Vendor Part Number ASCII character
11	06	64b/66b for 16 GFC & 8b/10b for 8 GFC and 4 GFC	48	35	"5" - Vendor Part Number ASCII character
12	8C	140 x 100 Mbit/s nominal bit rate (14.025 Gbit/s)	49	41	"A" - Vendor Part Number ASCII character
13	0A	16/8/4G Independent Tx and Rx Rate Selects	50	54	"T" - Vendor Part Number ASCII character
14	0A	10km of single mode fiber	5A	4D	"M" - Vendor Part Number ASCII character
15	64	10km of single mode fiber	52	5A	"Z" - Vendor Part Number ASCII character
16	00		53	20	" " - Vendor Part Number ASCII character
17	00		54	20	" " - Vendor Part Number ASCII character
18	00		55	20	" " - Vendor Part Number ASCII character
19	00		56	20	" " - Vendor Part Number ASCII character
20	41	"A" - Vendor Part Number ASCII character	57	20	" " - Vendor Part Number ASCII character
21	56	"V" - Vendor Part Number ASCII character	58	20	" " - Vendor Part Number ASCII character
22	41	"A" - Vendor Part Number ASCII character	59	20	" " - Vendor Part Number ASCII character
23	47	"G" - Vendor Part Number ASCII character	60	05	Hex Byte of Laser Wavelength [3]
24	4F	"O" - Vendor Part Number ASCII character	61	1E	Hex Byte of Laser Wavelength [3]
25	20	" " - Vendor Name ASCII character	62	00	
26	20	" " - Vendor Name ASCII character	63		Checksum for Bytes 0-62 [4]
27	20	" " - Vendor Name ASCII character	64	00	
28	20	" " - Vendor Name ASCII character	65	3A	Hardware SFP TX_DISABLE, TX_FAULT & RX_LOS, RATE_SELECT
29	20	" " - Vendor Name ASCII character	66	00	
30	20	" " - Vendor Name ASCII character	67	00	
31	20	" " - Vendor Name ASCII character	68-83		Vendor Serial Number ASCII characters [5]
32	20	" " - Vendor Name ASCII character	84-91		Vendor Date Code ASCII characters [6]
33	20	" " - Vendor Name ASCII character	92	68	Digital Diagnostics, Internal Cal, Rx Pwr Avg
34	20	" " - Vendor Name ASCII character	93	FA	A/W, Soft SFP TX_DISABLE, TX_FAULT & RX_LOS, RATE_SELECT
35	20	" " - Vendor Name ASCII character	94	05	SFF-8472 Compliance to revision 10.5
36	00		95		Checksum for Bytes 64-94 [4]
			96-255	00	

Notes:
1. 16 GFC [1600 MBytes/sec] is a serial bit rate of 14.025 Gb/s with 64b/66b. 8 GFC [800 Mbyte/s] is 8.5Gb/s and 4 GFC [400 Mbyte/s] is 4.25 Gb/s with 8b/10b.
2. The IEEE Organizationally Unique Identifier (OUI) assigned to AVAGO Technologies is 00-17-6A (3 bytes of hex).
3. Laser wavelength is represented in 16 unsigned bits. The hex representation of 1310 (nm) is 051E.
4. Addresses 63 and 95 are checksums calculated (per SFF-8472 and SFF-8074) and stored prior to product shipment.
5. Addresses 68-83 specify the AFCT-57F5ATMZ ASCII serial number and will vary on a per unit basis.
6. Addresses 84-91 specify the AFCT-57F5ATMZ ASCII date code and will vary on a per date code basis.

Table 13. EEPROM Serial ID Memory Contents - Enhanced SFP Memory (Address A2h)

Byte # Decimal	Notes	Byte # Decimal	Notes	Byte # Decimal	Notes
0	Temp H Alarm MSB [1]	23	Tx Bias L Warning LSB [3]	99	Real Time Vcc LSB [2]
1	Temp H Alarm LSB [1]	24	Tx Power H Alarm MSB [4]	100	Real Time Tx Bias MSB [3]
2	Temp L Alarm MSB [1]	25	Tx Power H Alarm LSB [4]	101	Real Time Tx Bias LSB [3]
3	Temp L Alarm LSB [1]	26	Tx Power L Alarm MSB [4]	102	Real Time Tx Power MSB [4]
4	Temp H Warning MSB [1]	27	Tx Power L Alarm LSB [4]	103	Real Time Tx Power LSB [4]
5	Temp H Warning LSB [1]	28	Tx Power H Warning MSB [4]	104	Real Time Rx Power MSB [5]
6	Temp L Warning MSB [1]	29	Tx Power H Warning LSB [4]	105	Real Time Rx Power LSB [5]
7	Temp L Warning LSB [1]	30	Tx Power L Warning MSB [4]	106	Reserved
8	Vcc H Alarm MSB [2]	31	Tx Power L Warning LSB [4]	107	Reserved
9	Vcc H Alarm LSB [2]	32	Rx Power H Alarm MSB [5]	108	Reserved
10	Vcc L Alarm MSB [2]	33	Rx Power H Alarm LSB [5]	109	Reserved
11	Vcc L Alarm LSB [2]	34	Rx Power L Alarm MSB [5]	110	Status/Control – See Table 14
12	Vcc H Warning MSB [2]	35	Rx Power L Alarm LSB [5]	111	Status/Control – See Table 15
13	Vcc H Warning LSB [2]	36	Rx Power H Warning MSB [5]	112	Flag Bits – See Table 16
14	Vcc L Warning MSB [2]	37	Rx Power H Warning LSB [5]	113	Flag Bits – See Table 16
15	Vcc L Warning LSB [2]	38	Rx Power L Warning MSB [5]	114	Reserved
16	Tx Bias H Alarm MSB [3]	39	Rx Power L Warning LSB [5]	115	Reserved
17	Tx Bias H Alarm LSB [3]	40-55	Reserved	116	Flag Bits – See Table 16
18	Tx Bias L Alarm MSB [3]	56-94	External Calibration Constants [6]	117	Flag Bits – See Table 16
19	Tx Bias L Alarm LSB [3]	95	Checksum for Bytes 0-94 [7]	118	Status/Control – See Table 17
20	Tx Bias H Warning MSB [3]	96	Real Time Temperature MSB [1]	119-127	Reserved
21	Tx Bias H Warning LSB [3]	97	Real Time Temperature LSB [1]	128-247	Customer Writable – See Table 18
22	Tx Bias L Warning MSB [3]	98	Real Time Vcc MSB [2]	248-255	Vendor Specific

Notes:
1. Temperature (Temp) is decoded as a 16 bit signed two's complement integer in increments of 1/256 °C.
2. Supply Voltage (V_{cc}) is decoded as a 16 bit unsigned integer in increments of 100 V.
3. Tx bias current (Tx Bias) is decoded as a 16 bit unsigned integer in increments of 2 A.
4. Transmitted average optical power (Tx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 W.
5. Received average optical power (Rx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 W.
6. Bytes 56-94 are not intended for use, but have been set to default values per SFF-8472.
7. Byte 95 is a checksum calculated (per SFF-8472) and stored prior to product shipment.

Table 14. EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, Byte 110)

Bit #	Status/Control Name	Description	Notes
7	TX_DISABLE State	Digital state of TX_DISABLE Input Pin (1 = TX_DISABLE asserted)	Note 1
6	Soft TX_DISABLE Control	Read/write bit for changing digital state of TX_DISABLE function	Note 1, 2
5	RS(1) State	Digital state of TX Rate_Select Input Pin RS(1) (1 = Rate High asserted)	
4	RS(0) State	Digital state of RX Rate_Select Input Pin RS(0) (1 = Rate High asserted)	
3	Soft RS(0) Control	Read/write bit for changing digital state of Rx Rate_Select RS(0) function	Note 3
2	TX_FAULT State	Digital state of TX_FAULT Output Pin (1 = TX_FAULT asserted)	Note 1
1	RX_LOS State	Digital state of SFP RX_LOS Output Pin (1 = RX_LOS asserted)	Note 1
0	Data Ready (Bar)	Indicates transceiver is powered and real time sense data is ready (0 = Data Ready)	

Notes:
1. The response time for soft commands of the AFCT-57F5ATMZ is 100 msec as specified by MSA SFF-8472.
2. Bit 6 is logic OR'd with the SFP TX_DISABLE input pin 3 …. either asserted will disable the SFP transmitter.
3. Bit 3 is logic OR'd with the SFP RS(0) RX Rate_Select input pin 7 …. either asserted will set receiver to Rate = High.

Table 15. EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, Byte 111)

Byte 111 <3:0> (Bin)	Name	Description
1100	OWRAP FORWARD	When enabled, OWRAP FORWARD routes incoming SFP Rx optical data to both the Tx optical output and the Rx electrical output.
0100	OWRAP	When enabled, OWRAP routes incoming SFP Rx optical data to the Tx optical output.
0011	EWRAP FORWARD	When enabled, EWRAP FORWARD routes incoming SFP Tx electrical data to both Rx electrical utput and Tx optical output.
0001	EWRAP	When enabled, EWRAP routes incoming SFP Tx electrical data to the Rx electrical output.
0000	RESET	Disable any EWRAP/OWRAP mode.
Any settings other than those reported above	Invalid	Any invalid setting is ignored and leaves unchanged the previous EWRAP/OWRAP mode.

Table 16. EEPROM Serial ID Memory Contents – Alarms and Warnings (Address A2h, Bytes 112, 113, 116, 117)

Byte	Bit	Flag Bit Name	Description
112	7	Temp High Alarm	Set when transceiver internal temperature exceeds high alarm threshold
	6	Temp Low Alarm	Set when transceiver internal temperature exceeds low alarm threshold
	5	Vcc High Alarm	Set when transceiver internal supply voltage exceeds high alarm threshold
	4	Vcc Low Alarm	Set when transceiver internal supply voltage exceeds low alarm threshold
	3	Tx Bias High Alarm	Set when transceiver laser bias current exceeds high alarm threshold
	2	Tx Bias Low Alarm	Set when transceiver laser bias current exceeds low alarm threshold
	1	Tx Power High Alarm	Set when transmitted average optical power exceeds high alarm threshold
	0	Tx Power Low Alarm	Set when transmitted average optical power exceeds low alarm threshold
113	7	Rx Power High Alarm	Set when received average optical power exceeds high alarm threshold
	6	Rx Power Low Alarm	Set when received average optical power exceeds low alarm threshold
	0-5	Reserved	
116	7	Temp High Warning	Set when transceiver internal temperature exceeds high warning threshold
	6	Temp Low Warning	Set when transceiver internal temperature exceeds low warning threshold
	5	Vcc High Warning	Set when transceiver internal supply voltage exceeds high warning threshold
	4	Vcc Low Warning	Set when transceiver internal supply voltage exceeds low warning threshold
	3	Tx Bias High Warning	Set when transceiver laser bias current exceeds high warning threshold
	2	Tx Bias Low Warning	Set when transceiver laser bias current exceeds low warning threshold
	1	Tx Power High Warning	Set when transmitted average optical power exceeds high warning threshold
	0	Tx Power Low Warning	Set when transmitted average optical power exceeds low warning threshold
117	7	Rx Power High Warning	Set when received average optical power exceeds high warning threshold
	6	Rx Power Low Warning	Set when received average optical power exceeds low warning threshold
	0-5	Reserved	

Table 17. EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, Byte 118).

Bit #	Status/Control Name	Description	Notes
4-7	Reserved		
3	Soft RS(1) Control	Read/write bit for changing digital state of Tx Rate_Select RS(1) function	Note 1
2	Reserved		
1	Power Level State	Always set to zero., which indicates Power Level 1 operation (1 W max)	
0	Power Level Select	Unused. This device supports power level zero (1 W max) only.	

Notes:
1. Bit 3 is logic OR'd with the SFP RS(1) TX Rate_Select input pin 9 …. either asserted will set transmitter to Rate = High.

Table. 18. Signal Integrity Feature Configuration Bytes (2-Wire Address A2h)

Byte	Name	Description
40	Tx Input EQ Setting for RS(1) = High	Defines SFP incoming electrical Tx equalization setting for Tx_Rate = High [i.e., RS(1)=High] The SFP transceiver will support 8 EQ settings in the lower 3 bits of this byte. EQ can be varied from 0 dB to 9 dB gain at 7 GHz in eight non-linear steps. The value of 0 results in 0 dB emphasis. Writing FFh to this byte and power cycling both reset the byte to factory settings, which is 02h.
41	Tx Input EQ Setting for RS(1) = Low	Defines SFP incoming electrical Tx equalization setting for Tx_Rate = Low [i.e., RS(1)=Low] The SFP transceiver will support 8 EQ settings in the lower 3 bits of this byte. EQ can be varied from 0 dB to 9 dB gain at 7 GHz in eight non-linear steps. The value of 0 results in 0 dB emphasis. Writing FFh to this byte and power cycling both reset the byte to factory settings, which is 04h.
42	Rx Output Pre Emphasis Setting for RS(0) = High	Defines SFP output electrical Rx pre-emphasis setting for Rx_Rate = High [i.e., RS(0)=High] The SFP transceiver will support 16 Pre Emphasis settings in the lower 4 bits of this byte. Emphasis can be varied from 0 dB to 9 dB in sixteen non-linear steps. The value of 0 results in 0 dB emphasis. Writing FFh to this byte resets to factory settings. Writing FFh to this byte and power cycling both reset the byte to factory settings, which is 04h.
43	Rx Output Pre Emphasis Setting for RS(0) = Low	Defines SFP output electrical Rx pre-emphasis setting for Rx_Rate = Low [i.e., RS(0)=Low] The SFP transceiver will support 16 Pre Emphasis settings in the lower 4 bits of this byte. Emphasis can be varied from 0 dB to 9 dB in sixteen non-linear steps. The value of 0 results in 0 dB emphasis. Writing FFh to this byte resets to factory settings. Writing FFh to this byte and power cycling both reset the byte to factory settings, which is 02h.
44-55	Unallocated	Contents 00h.

Note: Checksum at address A2h byte 95 will be updated within 100 ms of a value change in these bytes.

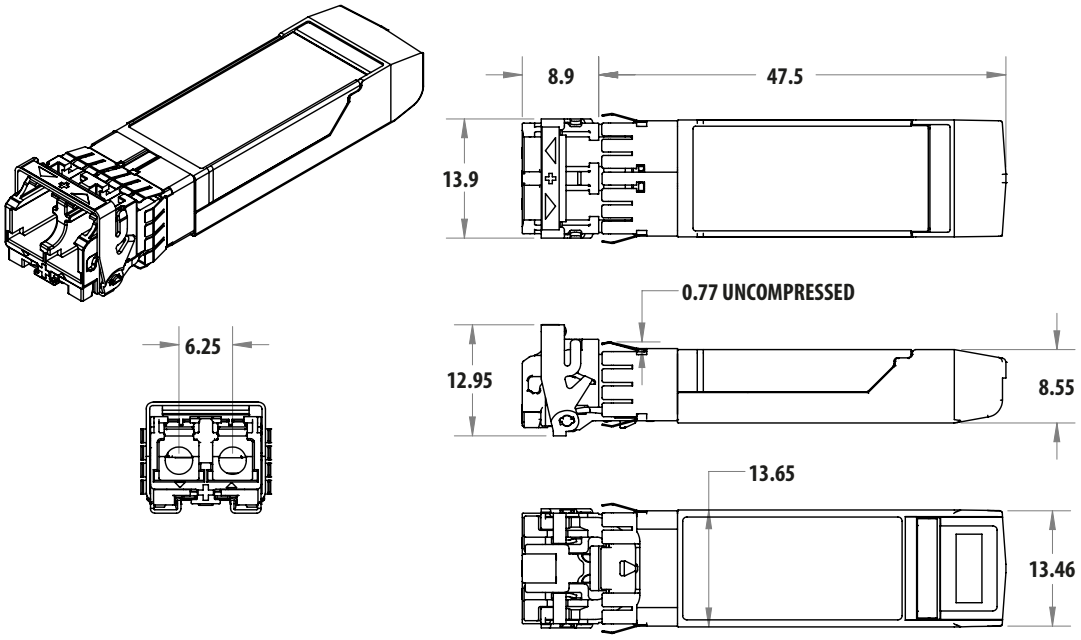


Figure 6. Module drawing

Figure 7. Product Label

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

AV02-3556EN - May 6, 2014