LVPECL Divide by 2 Divider

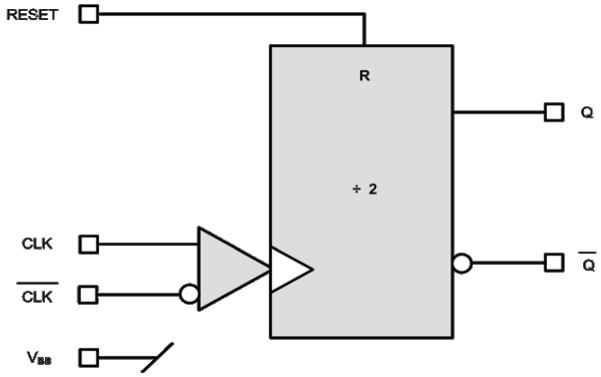
MLP8, MSOP8, SOIC8

Not recommended for new designs

FEATURES

- 3.0+ GHz Toggle Frequency
- 470ps Propagation Delay
- Internal Input Pull-down Resistors
- 3.0V to 5.5V Power Supply
- RoHS Compliant Pb Free Packages

BLOCK DIAGRAM



DESCRIPTION

The CTS100LVEL32 is an integrated ÷2 divider. The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flop will attain a random logic state; the reset allows for the synchronization of multiple CTS100LVEL32's in a system.

The CTS100LVEL32 is a direct replacement for the On Semiconductor MC100EL/LVEL32.

ENGINEERING NOTES

The CTS100LVEL32 provides a V_{BB} output for single-ended use or a DC bias reference for AC coupling to the device. For single-ended input applications, the V_{BB} reference should be connected to one side of the CLK/$\overline{CLK}$ differential input pair. The input signal is then fed to the other CLK/$\overline{CLK}$ input. The V_{BB} pin should be used only as a bias for the CTS100LVEL32 as its sink/source capability is limited. When used, the V_{BB} pin should be bypassed to ground via a 0.01μF capacitor.

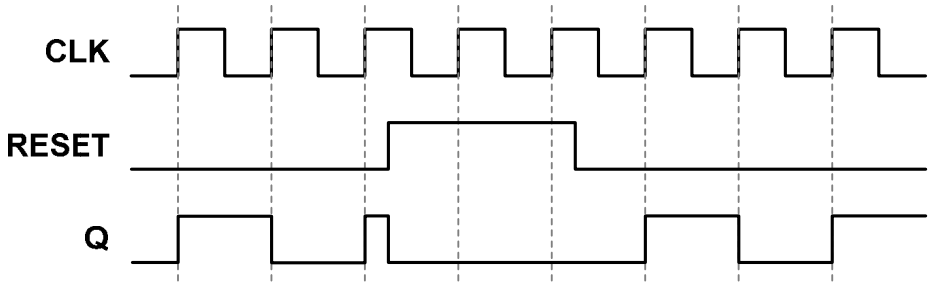


Figure 1 - Timing Diagram

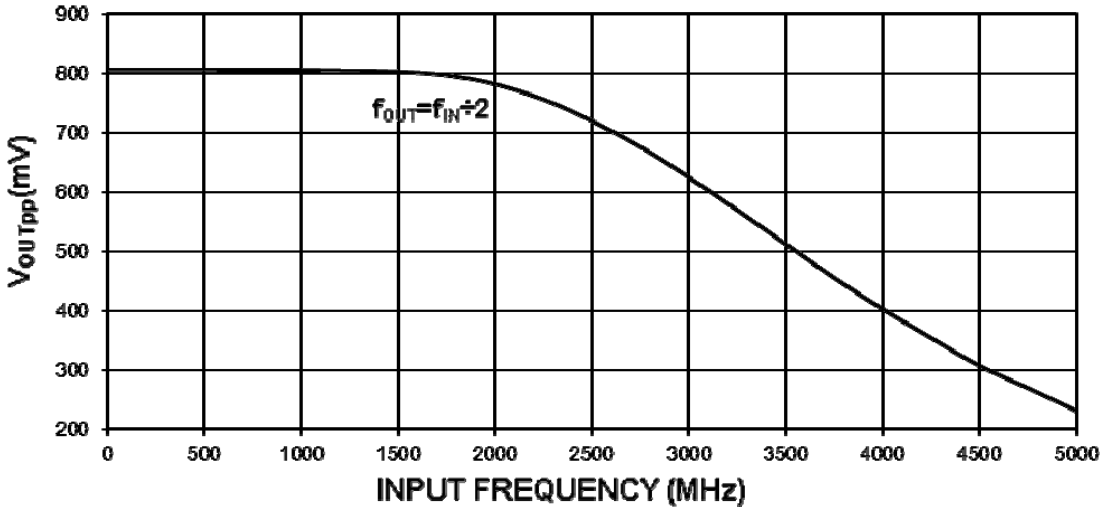


Figure 2 - Typical Large Signal Output Swing
Measured with 750mV input, output terminated to V_{CC}-2V via 50Ω resistors.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	V_{EE} = 0V	0 to + 6.0	V
V_{I_PECL}	PECL Input Voltage	V_{EE} = 0V	0 to + 6.0	V
V_{EE}	ECL Power Supply	V_{CC} = 0V	-6.0 to 0	V
V_{I_ECL}	ECL Input Supply	V_{CC} = 0V	-6.0 to 0	V
I_{OUT}	Output Current	Continuous	50	mA
		Surge	100	
T_A	Operating Temperature Range	-	-40 to +85	°C
T_{STG}	Storage Temperature Range	-	-65 to +150	°C
ESD_{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD_{MM}	Machine Model Electro Static Discharge	-	200	V
ESD_{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

ECL DC Characteristics (VEE = -3.0V to -5.5V, VCC = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1]	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V_{OL}	Output LOW Voltage[1]	-1830	-1555	-1810	-1620	-1810	-1620	-1810	-1620	mV
V_{IH}	Input HIGH Voltage	-1165	-880	-1165	-880	-1165	-880	-1165	-880	mV
V_{IL}	Input LOW Voltage	-1810	-1475	-1810	-1475	-1810	-1475	-1810	-1475	mV
V_{BB}	Reference Voltage	-1380	-1260	-1380	-1260	-1380	-1260	-1380	-1260	mV
I_{IH}	Input HIGH Current		150		150		150		150	µA
I_{IL}	Input LOW Current CLK	-150		-150		-150		-150		µA
	Input LOW Current RESET	0.5		0.5		0.5		0.5		
I_{EE}	Power Supply Current		30		30		30		35	mA

1 Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

LVPECL DC Characteristics (VEE = GND, VCC = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2215	2420	2275	2420	2275	2420	2275	2420	mV
V_{OL}	Output LOW Voltage[1,2]	1470	1745	1490	1680	1490	1680	1490	1680	mV
V_{IH}	Input HIGH Voltage[1]	2135	2420	2135	2420	2135	2420	2135	2420	mV
V_{IL}	Input LOW Voltage[1]	1490	1825	1490	1825	1490	1825	1490	1825	mV
V_{BB}	Reference Voltage[1]	1920	2040	1920	2040	1920	2040	1920	2040	mV
I_{IH}	Input HIGH Current		150		150		150		150	µA
I_{IL}	Input LOW Current CLK	-150		-150		-150		-150		µA
	Input LOW Current RESET	0.5		0.5		0.5		0.5		
I_{EE}	Power Supply Current		30		30		30		35	mA

1 For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

2 Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

PECL DC Characteristics (VEE = GND, VCC = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3915	4120	3975	4120	3975	4120	3975	4120	mV
V_{OL}	Output LOW Voltage[1,2]	3170	3445	3190	3380	3190	3380	3190	3380	mV
V_{IH}	Input HIGH Voltage[1]	3835	4120	3835	4120	3835	4120	3835	4120	mV
V_{IL}	Input LOW Voltage[1]	3190	3525	3190	3525	3190	3525	3190	3525	mV
V_{BB}	Reference Voltage[1]	3620	3740	3620	3740	3620	3740	3620	3740	mV
I_{IH}	Input HIGH Current		150		150		150		150	µA
I_{IL}	Input LOW Current CLK	-150		-150		-150		-150		µA
	Input LOW Current RESET	0.5		0.5		0.5		0.5		
I_{EE}	Power Supply Current		30		30		30		35	mA

1 For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

2 Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

AC Characteristics (VEE = -3.0V to -5.5V; VCC=GND or VEE=GND; VCC = +3.0V to +5.5V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency	2.6			2.6			2.6			2.6			GHz
t_{PLH}/t_{PHL}	$\overline{CLK}$ to $\overline{Q}$	360	450	540	370	460	550	380	470	560	400	490	580	ps
	RESET to $\overline{Q}$	390	540	690	440	540	640	440	540	640	450	550	650	ps
t_{SKEW}	Duty Cycle Skew		5	20		5	20		5	20		5	20	ps
V_{PP} (AC)	Input Swing													
	Differential	150		1000	150		1000	150		1000	150		1000	mV
	Single Ended	300		2000	300		2000	300		2000	300		2000	mV
V_{CMR}	Common Mode Range	V_{EE}+		V_{CC}-	V_{EE}+		V_{CC}-	V_{EE}+		V_{CC}-	V_{EE}+		V_{CC}-	
	V_{PP} < 500mV	1.2		0.4	1.1		0.4	1.1		0.4	1.1		0.4	V
	V_{PP} ≥ 500mV	1.4		0.4	1.3		0.4	1.3		0.4	1.3		0.4	V
t_R/t_F	Output Rise/Fall (20%-80%)	100		260	100		260	100		260	100		260	ps

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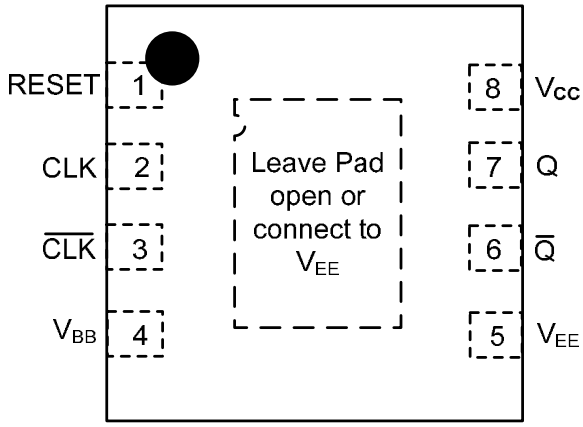
Pin Description and Configuration

Pin Assignments for CTS100LVEL32N

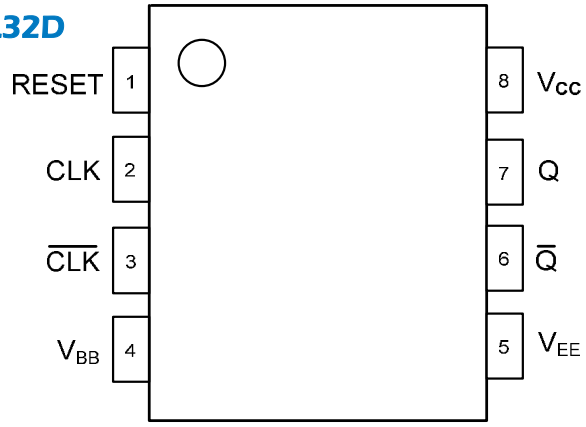
Pin	Name	Type	Function
1	RESET	Input	Asynchronous Reset
2	CLK	Input	Clock Input
3	$\overline{CLK}$	Input	Inverting Clock Input
4	V_{BB}	Output	Reference Voltage
5	V_{EE}	Power	Negative Supply
6	$\overline{Q}$	Output	Inverting PECL Output
7	Q	Output	PECL Output
8	V_{CC}	Power	Positive Supply



CTS100LVEL32N

Pin Assignments for CTS100LVEL32T & CTS100LVEL32D

Pin	Name	Type	Function
1	RESET	Input	Asynchronous Reset
2	CLK	Input	Clock Input
3	$\overline{CLK}$	Input	Inverting Clock Input
4	V_{BB}	Output	Reference Voltage
5	V_{EE}	Power	Negative Supply
6	$\overline{Q}$	Output	Inverting PECL Output
7	Q	Output	PECL Output
8	V_{CC}	Power	Positive Supply

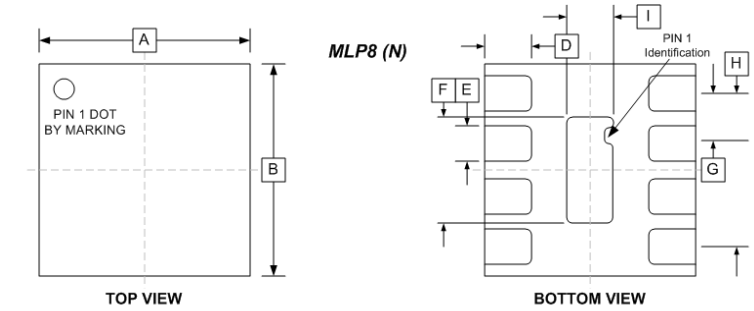


CTS100LVEL32T & CTS100LVEL32D

Not recommended for new designs

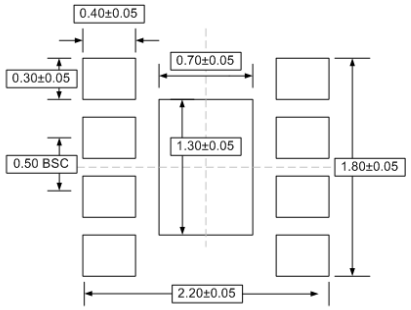
PACKAGE DIMENSIONS

MLP8 (N)

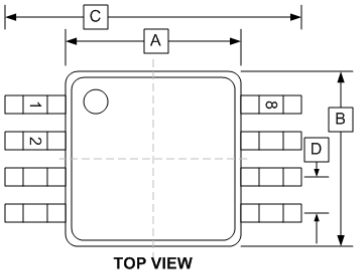


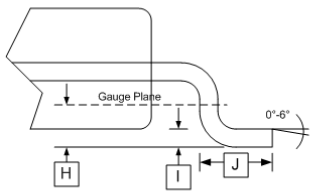
	MILLIMETERS	
DIM	MIN	MAX
A	2.00±0.050	
B	2.00±0.050	
C	0.75±0.050	
C_1	0.00	0.05
C_2	0.203 Ref.	
D	0.35±0.050	
E	0.25±0.050	
F	1.20±0.050	
G	0.500 BSC	
H	1.500 REF	
I	0.60±0.050	

PCB LAND PATTERN/FOOTPRINT



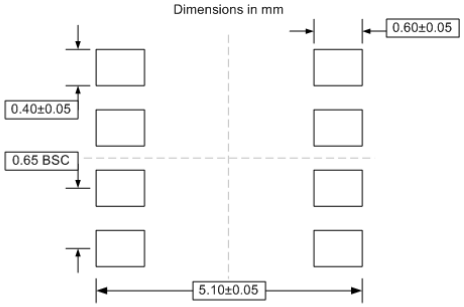
MSOP8 (T)



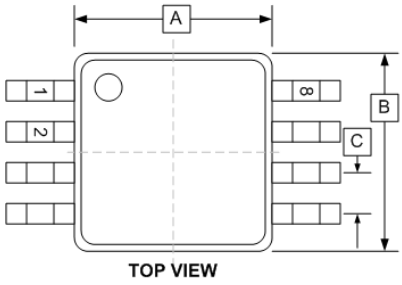


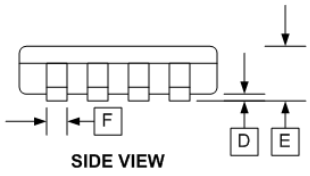
	INCHES	
DIM	MIN	MAX
A	0.118±0.004	
B	0.118±0.004	
C	0.192±0.008	
D	0.0256 TYP	
E	0.004±0.002	
F	0.034±0.002	
G	0.009±0.014	
H	0.010	
I	0.006±0.002	
J	0.021±0.004	

PCB LAND PATTERN/FOOTPRINT
Dimensions in mm

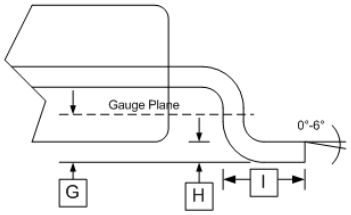


PACKAGE DIMENSIONS





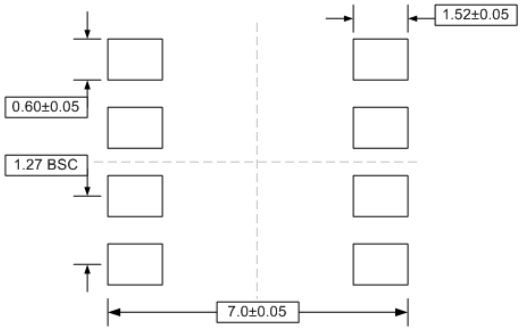
SOIC8 (D)



	mm	
DIM	MIN	MAX
A	3.81	3.99
B	4.80	4.98
C	1.27 BSC	
D	0.10	0.25
E	1.37	1.68
F	0.36	0.48
G	0.25	
H	0.19	0.25
I	0.41	0.86

PCB LAND PATTERN/FOOTPRINT

Dimensions in mm



PART ORDERING INFORMATION

Part Number	Package	Marking
CTS100LVEL32NG	MLP8	C2G / YWW
CTS100LVEL32TG	MSOP8	HL32G / YYWW
CTS100LVEL32DG	SOIC8	CTS100G / LVEL32 / YYWW