*User's Guide*

# *DAC12DL3200 Evaluation Module*


**ABSTRACT**

The DAC12DL3200 evaluation module (EVM) is used to evaluate the DAC12DL3200 digital-to-analog converter (DAC) from Texas Instruments. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the DAC12DL3200EVM.


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## 1 Introduction

The DAC12DL3200 is a very low latency, dual-channel, 12-bit RF sampling digital-to-analog converter (DAC), capable of operating at sampling rates up to 3.2 Giga-samples per second (GSPS) in dual-channel mode, or 6.4 GSPS in single-channel mode. The DAC can transmit signal bandwidths beyond 2 GHz at carrier frequencies approaching 8 GHz when using multi-Nyquist output modes. The DAC12DL3200EVM device input data is transmitted over a high-speed LVDS interface. This evaluation board also includes the following important features:

- Transformer-coupled output allowing for a single-ended 50-Ω output signal up to 8 GHz
- The LMX2592 clock synthesizer as an option to generate the DAC sampling clock
- Transformer-coupled input clock option (board default setup) for quick setup with external clock sources
- LMK04828 clock synthesizer for DAC SYSREF and FPGA reference clock source
- Device register programming through USB connector and FTDI USB-to-SPI bus translator
- High-speed LVDS data input over a 400-pin FMC interface connector


**Figure 1-1. DAC12DL3200EVM**

The TI TSW14DL3200EVM pattern generator, when used with the TI High-Speed-Data-Converter (HSDC) Pro Software GUI, is used to send LVDS data test patterns to the DAC12DL3200EVM.

With proper hardware selection in the HSDC Pro software, the TSW14DL3200EVM is automatically configured to support the different modes of operation of the DAC12DL3200. The interface provides LVDS output data up to 1600 MSPS.

## 1.1 Low Latency Evaluation of Receive and Transmit

The TSW14DL3200EVM is designed for plug-and-play evaluation with the DAC12DL3200EVM and ADC12DL3200EVM. This provides a capability for prototyping or testing a low-latency LVDS-based DAC transmitter or ADC receiver, or both simultaneously.

TI takes two approaches for measuring the overall end-to-end latency of the DAC12DL3200 device.

Approach 1: Figure 1-2 illustrates this approach where the test signal is fed into the front end of the ADC12DL3200 device and the samples are extracted and collected by the FPGA. These samples are then forwarded to the DAC12DL3200 which generates the resultant output signal (delayed version of the input test signal). The IO architecture of the Xilinx UltraScale enables extremely high-speed data rates by trading off latency for throughput. At bit-rates over 1.2Gbps, the SERDES blocks in the FPGA implement asynchronous clock domain crossing (both at the ADC and the DAC side). In addition, there is a possibility of bit-slips between data lanes of the ADC and the outputs of the receiving SERDES blocks in the FPGA. These are compensated for with an additional layer of buffering inside the FPGA. The total sum of all of these domain crossing and data-ordering-related delays result in an end-to-end latency of 285 ns. Of this, the DAC12DL3200 contributes approximately 6 ns of latency (see the data sheet spec), while the ADC12DL3200 adds a latency of approximately 8 ns. The remaining delay is from the FPGA logic used.

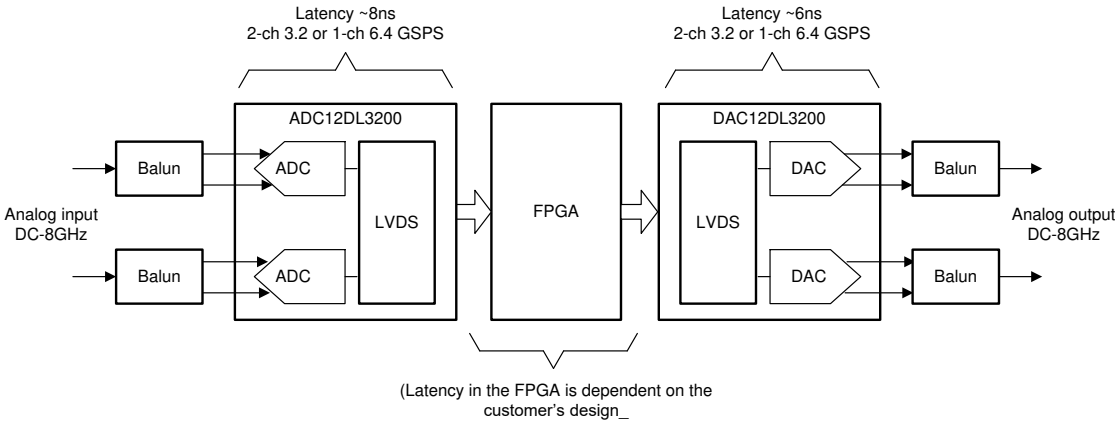


**Figure 1-2. Low Latency LVDS-Based ADC Receiver and DAC Transmitter**

Approach 2: To minimize the delay through the FPGA and obtain a true representation of the latency of the data converters, a simplified setup is created, where the FPGA is used as a combinatorial pass-through device. The FPGA logic passes just the MSB output of the ADC (through the FPGA) to the MSB input of the DAC. The FPGA does not carry out any re-timing of the signals to avoid any non-deterministic delays on account of clock domain crossing. Using this setup, the measured combined latency of ADC12DL3200 + FPGA + DAC12DL3200 + Device EVM routing is 32.8 ns .


**Figure 1-3. Low Latency ADC EVM, Capture Card and Pattern Generator, and DAC EVM**

## 1.2 Related Documentation

### Technical Reference Documents

- Texas Instruments, *DAC12DL3200 6.4-GSPS Single Channel or 3.2-GSPS Dual Channel, 12-bit DAC Data Sheet*
- Texas Instruments, *TSW14DL3200 High-Speed LVDS Data Capture and Pattern Generator User's Guide*
- Texas Instruments, *High Speed Data Converter Pro GUI User's Guide* (also available in the help menu of the software)
- Texas Instruments, *LMX2582 High Performance, Wideband PLLatinum™ RF Synthesizer With Integrated VCO Data Sheet*
- Texas Instruments, *LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner With Dual Loop PLLs Data Sheet*
- *FTDI USB to Serial Driver Installation Manual*

### TSW14DL3200EVM and ADC12DL3200EVM Operation

Refer to the *TSW14DL3200EVM User's Guide* and *ADC12DL3200EVM User's Guide* for configuration and status information.

# 2 Equipment

This section describes the equipment needed to evaluate the full performance of the DAC12DL3200 device.

## 2.1 Evaluation Board Feature Identification Summary

Figure 2-1 shows the EVM features.

**Note**

The EVM does not have any power sequencing as the EVM was designed before this requirement was added to the data sheet. TI recommends using power sequencing per the *Power Supply Recommendations* section of the *DAC12DL3200 6.4-GSPS Single Channel or 3.2-GSPS Dual Channel, 12-bit DAC Data Sheet*.

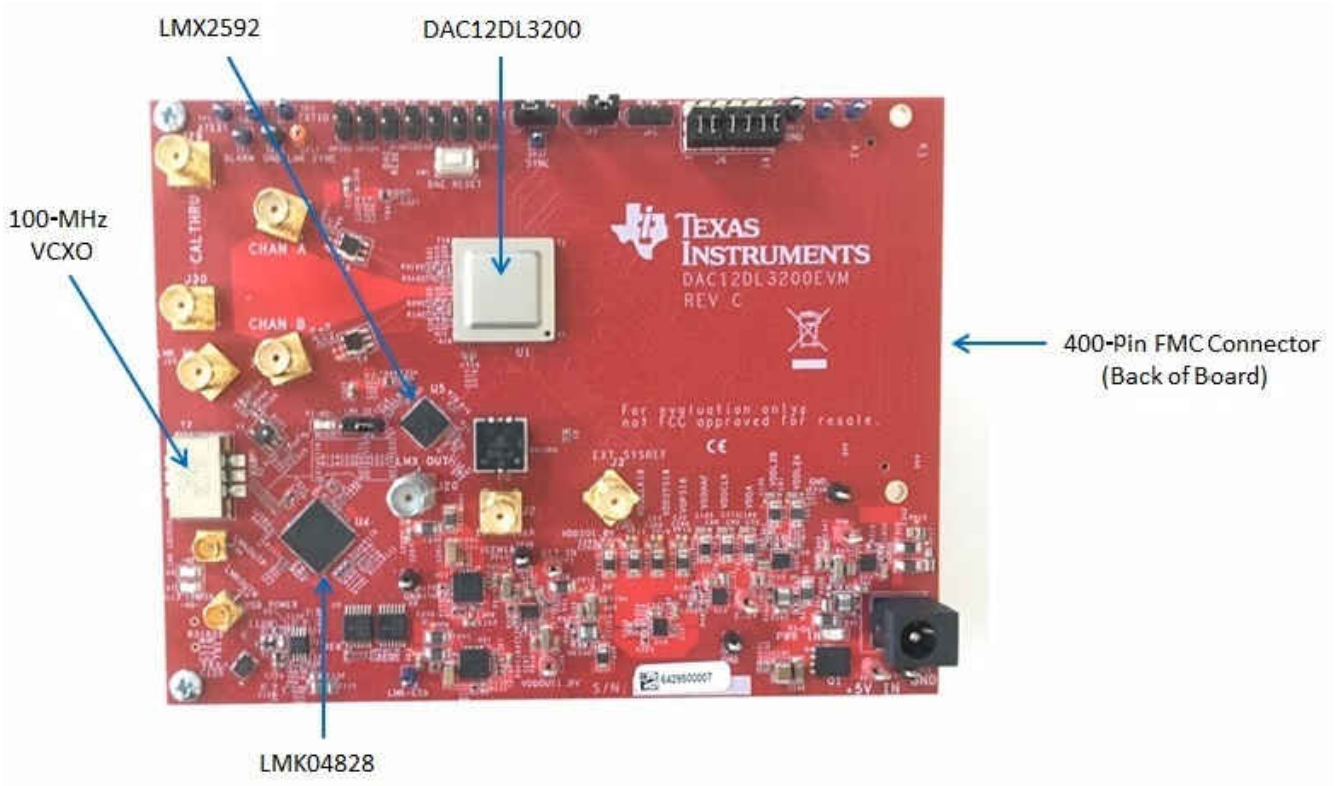


**Figure 2-1. DAC12DL3200EVM Features**

## 2.2 Required Equipment

The following equipment is included in the EVM evaluation kit:

- DAC12DL3200 Evaluation Module (EVM)
- Mini-USB cable
- Power cable

The following equipment is *not* included in the EVM evaluation kit, but is required for evaluation of this product:

- TSW14DL3200EVM pattern generator board, power cable, and USB3.0 cable
- HSDC Pro software
- Computer (PC) running the Microsoft® Windows® operating system (XP, 7, 8, or 10)
- Two synchronized low-noise signal generators for clock inputs. TI recommends the following:
  - Rohde & Schwarz® SMA100A or SMA100B
- Spectrum Analyzer
  - Rohde & Schwarz® FSQ with 20 GHz of bandwidth or equivalent
- Signal-path cables, SMA-to-SMA
- 12-V DC power source, capable of providing 3 A (TSW14DL3200EVM)
- 5-V DC power source capable of providing 4 A (DAC12DL3200EVM)

By default, the DAC12DL3200EVM uses an external clocking solution. A few small board modifications enable the onboard clocking solution. If onboard clocking is used, no signal generators are required.

# 3 Setup Procedure

This section describes how to set up the DAC12DL3200EVM on the bench with the proper equipment to evaluate the full performance of the DAC device. Figure 3-1 shows the EVM test setup.

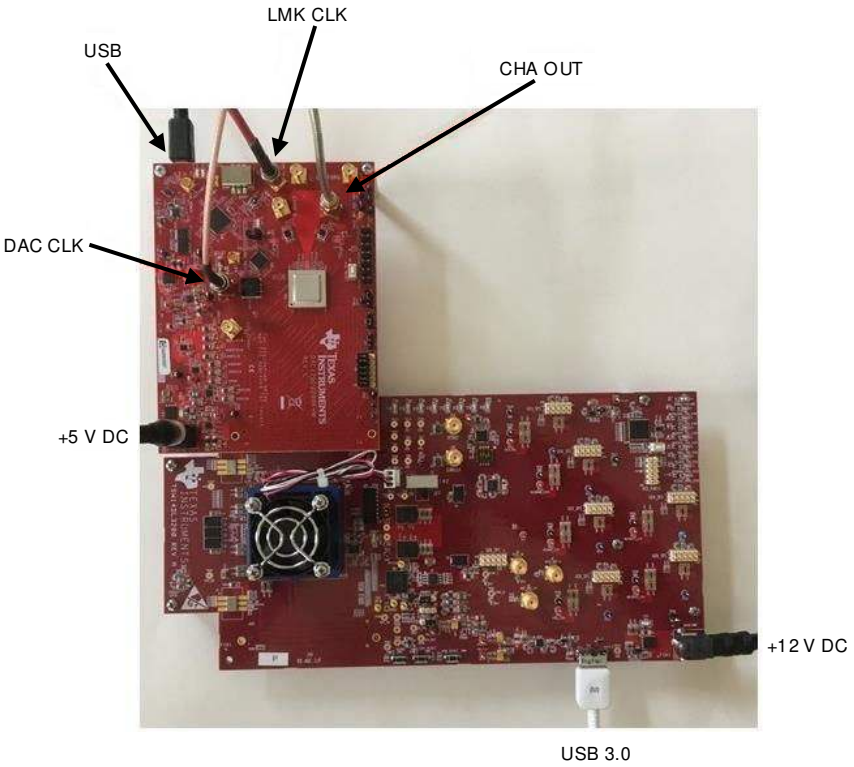


**Figure 3-1. EVM Test Setup**

**Note**

The HSDC Pro software must be installed before connecting the TSW14DL3200EVM to the PC for the first time.

### 3.1 Install the High Speed Data Converter (HSDC) Pro Software

Download the most recent version of the HSDC Pro software from www.ti.com/tool/dataconverterpro-sw. Follow the installation instructions to install the software.

### 3.2 Install the Configuration GUI Software

1. Download the configuration graphical user interface (GUI) software from the EVM tool folder at http://www.ti.com/tool/DAC12DL3200EVM.
2. Extract files from the compressed zip file.
3. Run the executable file ( `setup.exe` ), and follow the instructions.

### 3.3 Connect the DAC12DL3200EVM and TSW14DL3200EVM

With the power off, connect the DAC12DL3200EVM to the TSW14DL3200EVM through the FMC connector as shown in Figure 3-1. Make sure that the standoffs provide the proper height for robust connector connections.

Ensure the board jumpers are configured as follows:

- JP1 (TXENB) pins 1–2. This enables the DAC outputs.
- JP2 (SLEEP) pins 2–3. This places the DAC out of sleep mode.
- JP3 (SYNC) No shunt. This input has an internal pullup. When high, the DAC uses the DxSTRB inputs for strobe. When low, the DAC uses the data LSB as strobe. See the data sheet for more information.
- JP6 (LMX_CE) pins 1–2. This places the LMX in power down mode (board default).
- J6 (DAC NCO select) pins 1–2, 4–5, 7–8, 10–11, 13–14, 16–17. Default is all inputs tied to GND.
- J5, J7–J12 (FTDI Spare GPIOs) No shunt. Default is all inputs disconnected. These jumpers allow for FTDI to control NCO select inputs when installed.

### 3.4 Connect the Power Supplies to the Boards (Power Off)

1. Confirm that the power switch on the TSW14DL3200EVM is in the off position. Connect the power cable to a 12-V DC (minimum 3 A) power supply. Make sure of the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 12 V. Connect the power cable to the EVM power connector.
2. Connect the power cable to a 5-V DC (minimum 4 A) power supply for the DAC12DL3200EVM. Make sure of the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 5 V. Connect the power cable to the EVM power connector.

**CAUTION**

Make sure that the power connections to the EVMs are the correct polarity. Failure to do so may result in immediate damage.

Make sure that the 12-V power supply is connected to the TSW14DL3200EVM and not the DAC12DL3200EVM. Providing the DAC12DL3200EVM with 12-V may result in immediate damage.

Leave the TSW14DL3200EVM power switch in the off position.

## 3.5 Connect the Signal Generators to the EVM (*RF Outputs Disabled Until Directed)

Connect a signal generator to the EXT_DACCLK input of the DAC12DL3200EVM using SMA connector J2. This must be a low-noise signal generator. Configure the signal generator for 6.4 GHz, 12 dBm.

Connect a second signal generator that is synchronized to the DACCLK signal generator to LMK_IN of the DAC12DL3200EVM, using SMA J25. Configure the signal generator for 1.6 GHz, 12 dBm.

### 3.5.1 If External Clocking is Used (Optional)

To operate the EVM using the onboard clocking solution, do the following:

1. Remove the shunt on LMX_CE jumper J6
2. Move C7 to C277
3. Move C6 to C278
4. Install FB28 with MuRata BLM18AG121TN1D or equivalent. This is located on the bottom of the board under Y2.
5. Instructions on GUI settings are provided in Appendix B regarding operating in this mode.

## 3.6 Turn On the TSW14DL3200EVM 12-V Power and Connect to the PC

Use the following steps to turn on the TSW14DL3200EVM with 12-V power and connect to the PC

1. Turn on the 12-V power supply connected to the TSW14DL3200EVM.
2. Connect a mini USB 3.0 cable from the PC to the TSW14DL3200EVM.
3. If this is the first time connecting the TSW14DL3200EVM to the PC, follow the on-screen instructions to automatically install the device drivers. See the TSW14DL3200EVM user's guide for specific instructions.

## 3.7 Turn On the DAC12DL3200EVM 5-V Power Supply and Connect to the PC

Use the following steps to turn on the DAC12DL3200EVM 5-V power supply and connect to the PC.

1. Connect the DAC12DL3200EVM to the PC with the mini USB cable.
2. Turn on the 5-V power supply to power up the EVM.
3. Press the DAC RESET switch SW1.
4. Turn on the power switch on the TSW14DL3200EVM

## 3.8 Turn On the Signal Generator RF Outputs

Turn on the signal output of the two signal generators connected to the DAC12DL3200EVM.

## 3.9 Open the DAC12DL3200EVM GUI and Program the DAC and Clocks for Single Channel, NRZ Mode 2 Operation

The device configuration GUI is installed separately from the HSDC Pro installation and is a stand-alone GUI.

Figure 3-2 shows the GUI open to the *LMK04828* tab. Tabs at the top of the panel organize the configuration into device and EVM features, with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has three configurable devices: the DAC12DL3200, LMK04828, and LMX2592. The register map for each device is provided in the device data sheets.

Figure 3-2 illustrates the DAC12DL3200EVM GUI showing the USB status is connected to a PC.

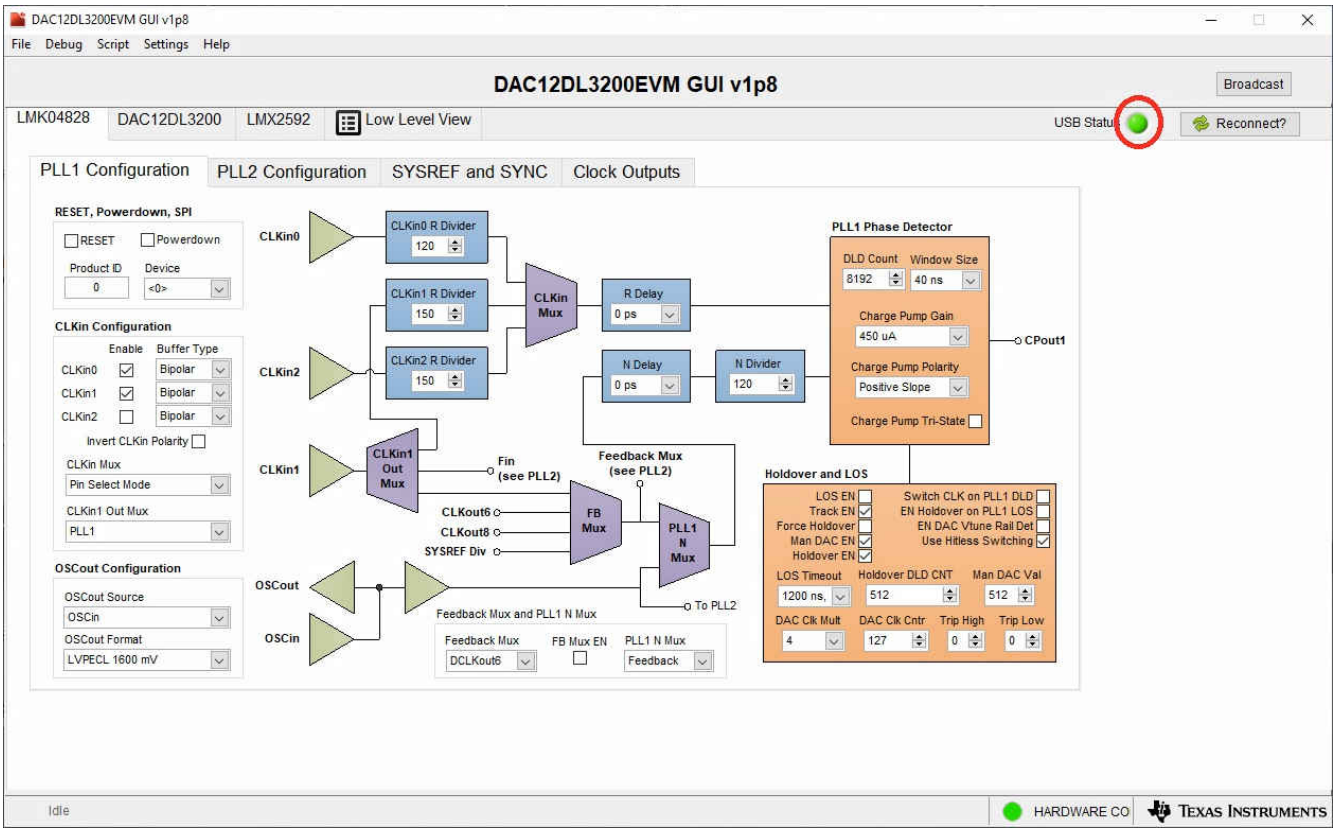


**Figure 3-2. Configuration GUI: LMK04828 Tab**

1. Open the DACDL3200EVM GUI by clicking on the DAC12DL3200 GUI icon and run as administrator.
2. Verify the USB has connected to the board. This is indicated by a green USB Status indicator in the top right corner of the GUI. If this is not lit, click on the *Reconnect?* button until it does illuminate.
3. Click on the *Low Level View* tab.

Figure 3-3 illustrates loading a register configuration file to the EVM.

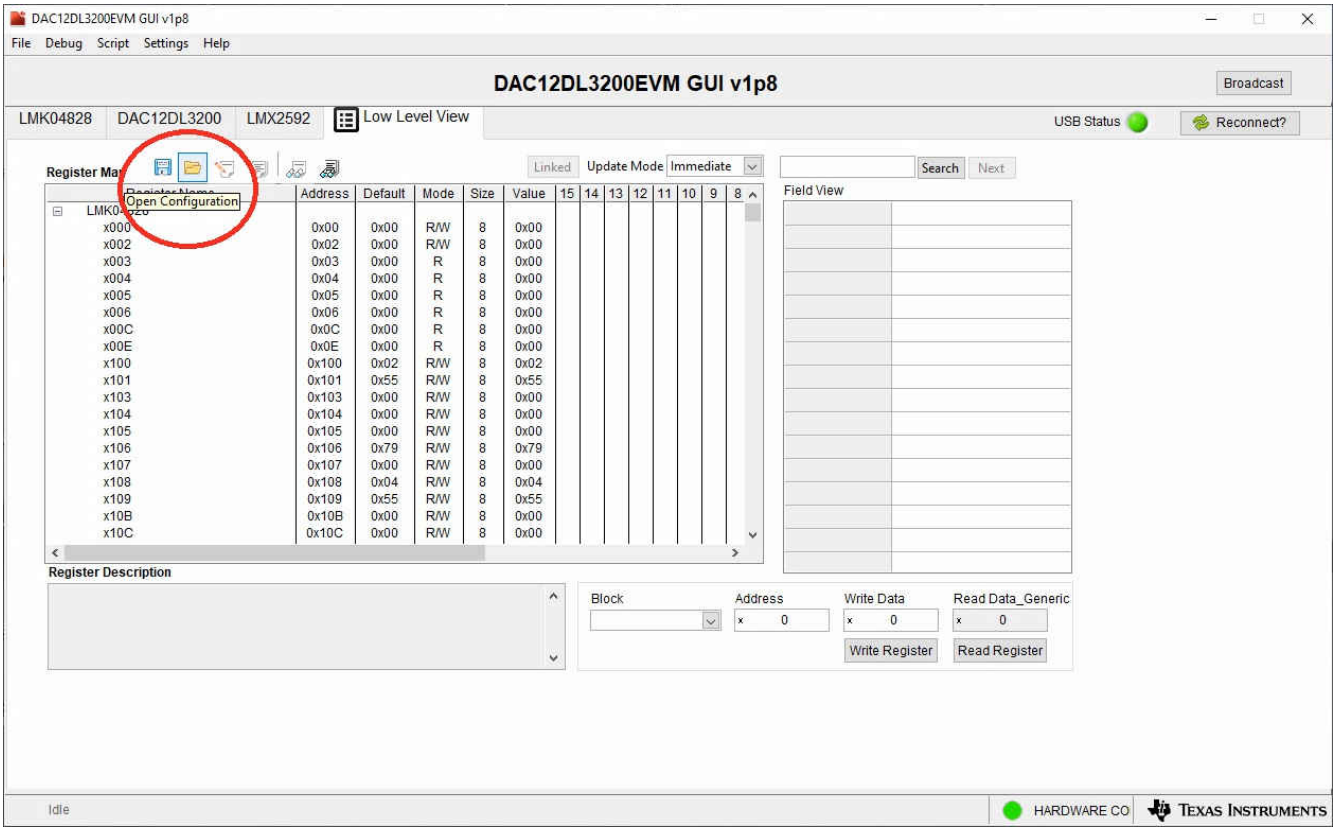


**Figure 3-3. Low Level View Tab**

4. Click on the *File* icon and navigate to “EXT_CLK_Mode2_NRZ_Single_DAC.cfg” and click on the *OK* button to load the LMK and DAC registers, see Figure 3-4.

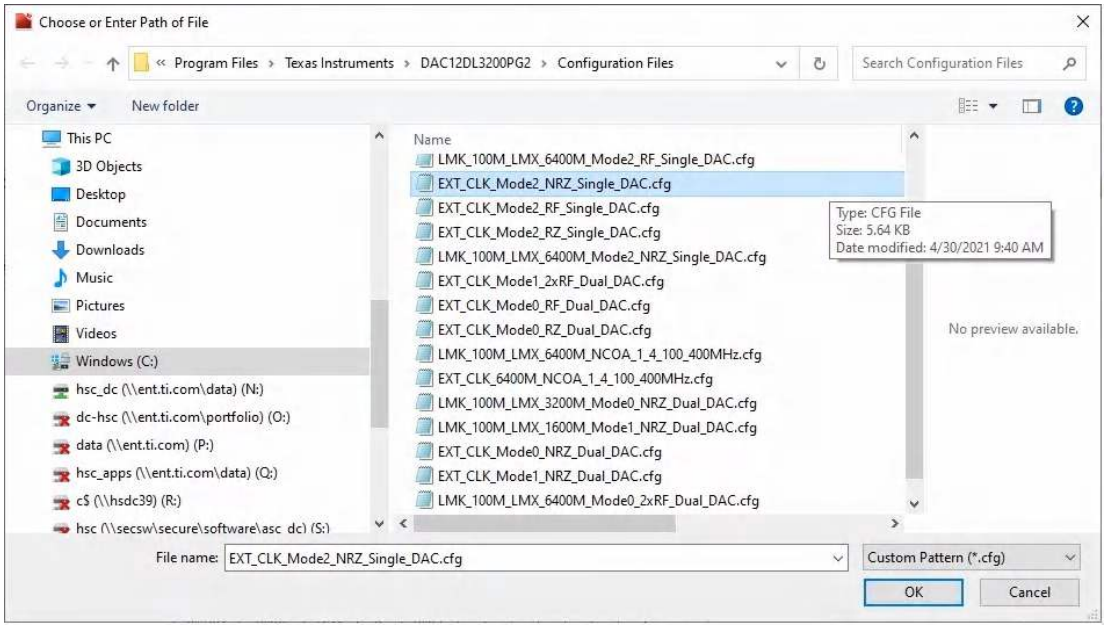


**Figure 3-4. Selecting Configuration File**

This configuration file sets up the DAC to operate in a single-channel mode with the output available only on CHA. The same output is available on CHB in this mode if desired, but the configuration file has CHB powered down by default.

### 3.10 Open the HSDC Software and Load the FPGA Image to the TSW14DL3200EVM

Use the following steps to open the HSDC software and load the FPGA image to the TSW14DL3200EVM:

1. Open the HSDC Pro software.

   Click *OK* to confirm the serial number of the TSW14DL3200EVM device. If multiple TSWxxxxx boards are connected, select the model and serial number for the one connected to the DAC12DL3200EVM. When the EVM powers up, there is no firmware loaded in the FPGA. Click the *OK* button on the *No firmware. Please select a device to load firmware into the board.* message.

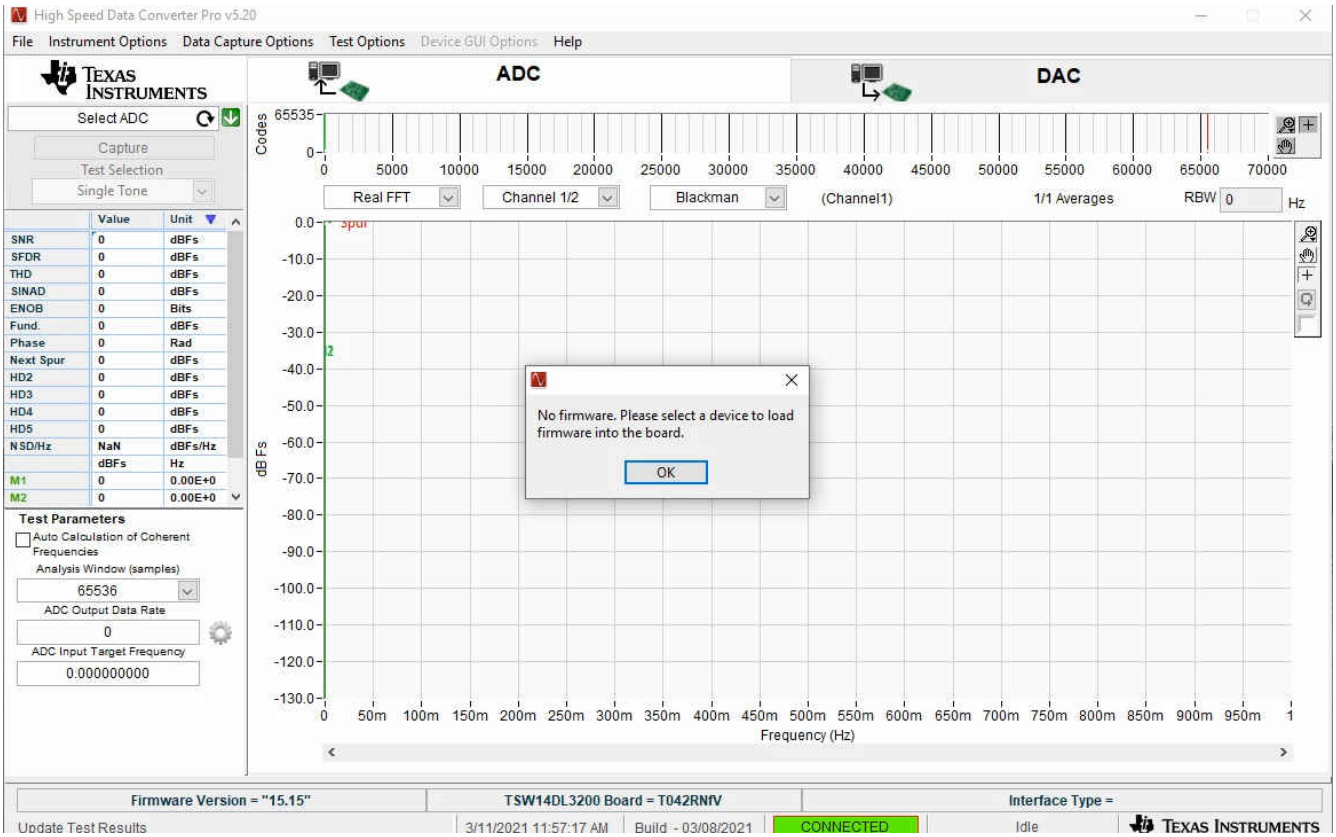


**Figure 3-5. No Firmware Loaded**

2. Click on the *DAC* tab in the top right of the GUI.

   In the device drop-down menu, select "DAC12DL3200_MODE2_12b_sync_istrb" as illustrated in Figure 3-6.

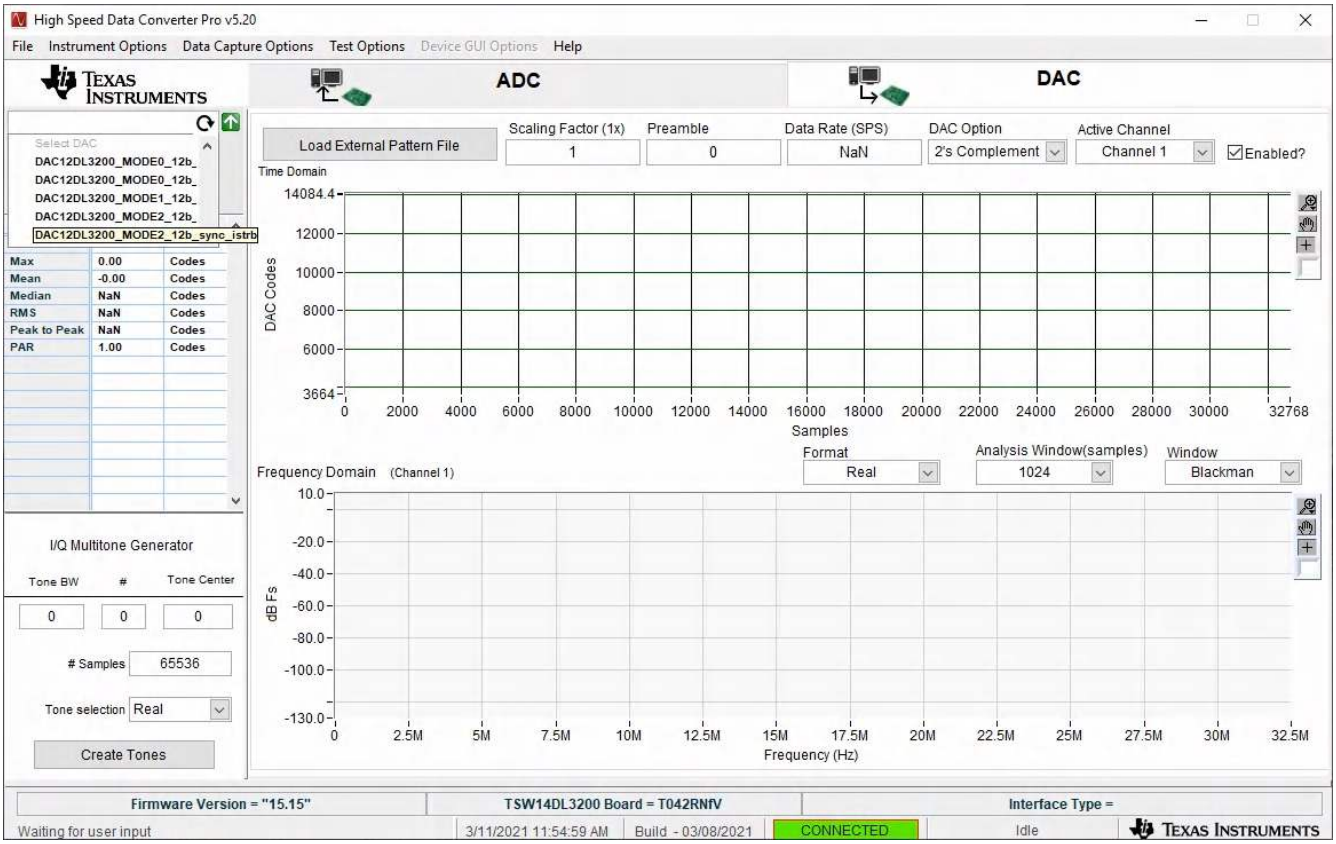


**Figure 3-6. Selecting DAC Mode 2**

3. When prompted, click *Yes* to update the firmware. After the firmware is downloaded, the *configuration done LED D22* illuminates on the TSW14DL3200EVM. This is located next to the FPGA. Status LEDs D1–D5 also illuminate.
4. In the top middle of the GUI, enter "6.4G" for the *Data Rate*.
5. Set the tone center "1GHz" in the *I/Q Multitone Generator* window in the lower left of the GUI, .
6. Enter the # of tones "1", also in the *I/Q Multitone Generator* window
7. Click the *Create Tones* button.

The setup looks as shown in Figure 3-7.

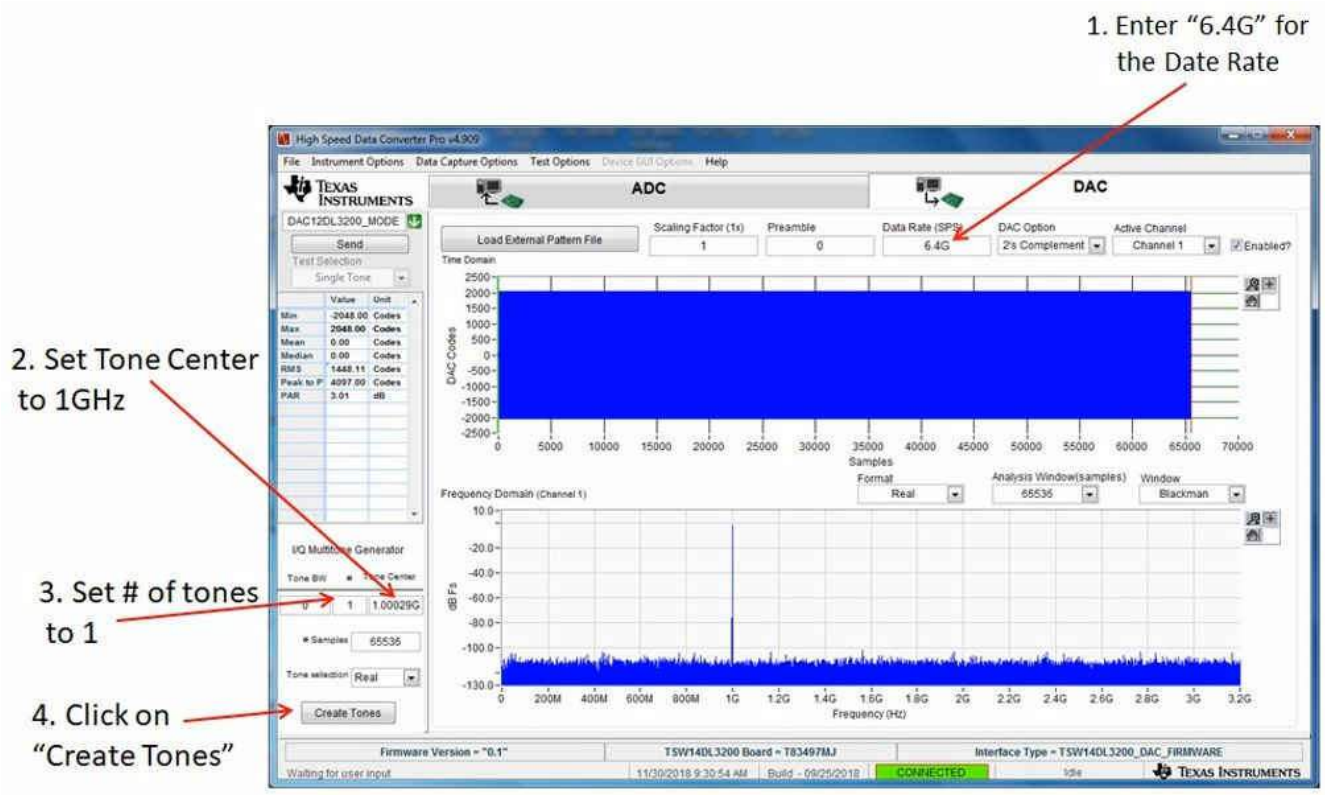


**Figure 3-7. HSDC Pro GUI Setup**

## 3.11 DxSTRB Timing Adjustment

1. By default, the current firmware used by HSDC Pro sends a square wave instead of a pulse for the DxSTR signals. The DAC requires a pulse for DxSTR that needs to be a width that is a multiple of 4 LVDS clock cycles. To correct for this, do the following in HSDC Pro GUI:
   a. Click on the *Instrument Options* tab located in the top left of the DAC main page.
   b. Click on *IO Delay*.


**Figure 3-8. IO Delay**

   c. Click the *Debug Features* button.
   d. Enter x10000004 for the Reg Address and x8000 for the Data in the Write section as shown in Figure 3-9. Click the *Write Registers* button. Enter x10000004 for the RegAddress in the Read section. Click the *Read Registers* button. Verify x8000 was written to this address. Close this window.

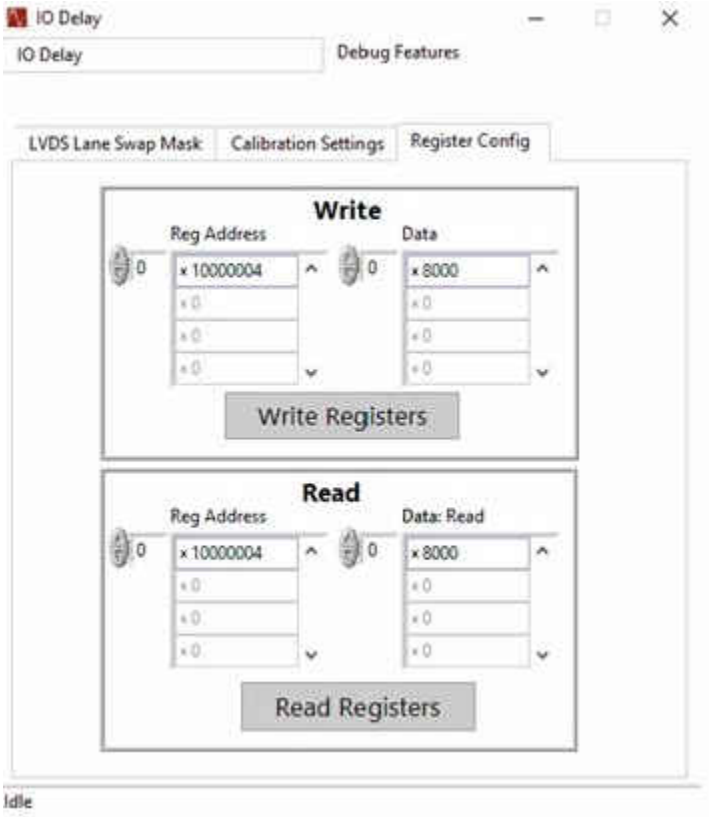


**Figure 3-9. IO Delay Register Write**

**Note**

These steps only need to be done once after the firmware has been loaded. If you send another pattern, you do not have to do these steps. If the TSWS14DL3200EVM is powered down or firmware is reloaded, these steps must be repeated.

e. In the HSDC Pro GUI main page, click the *Send* button in the upper left to send the test tone to the DAC EVM.
f. There should now be a 1-GHz output tone on CHA SMA connector J1.

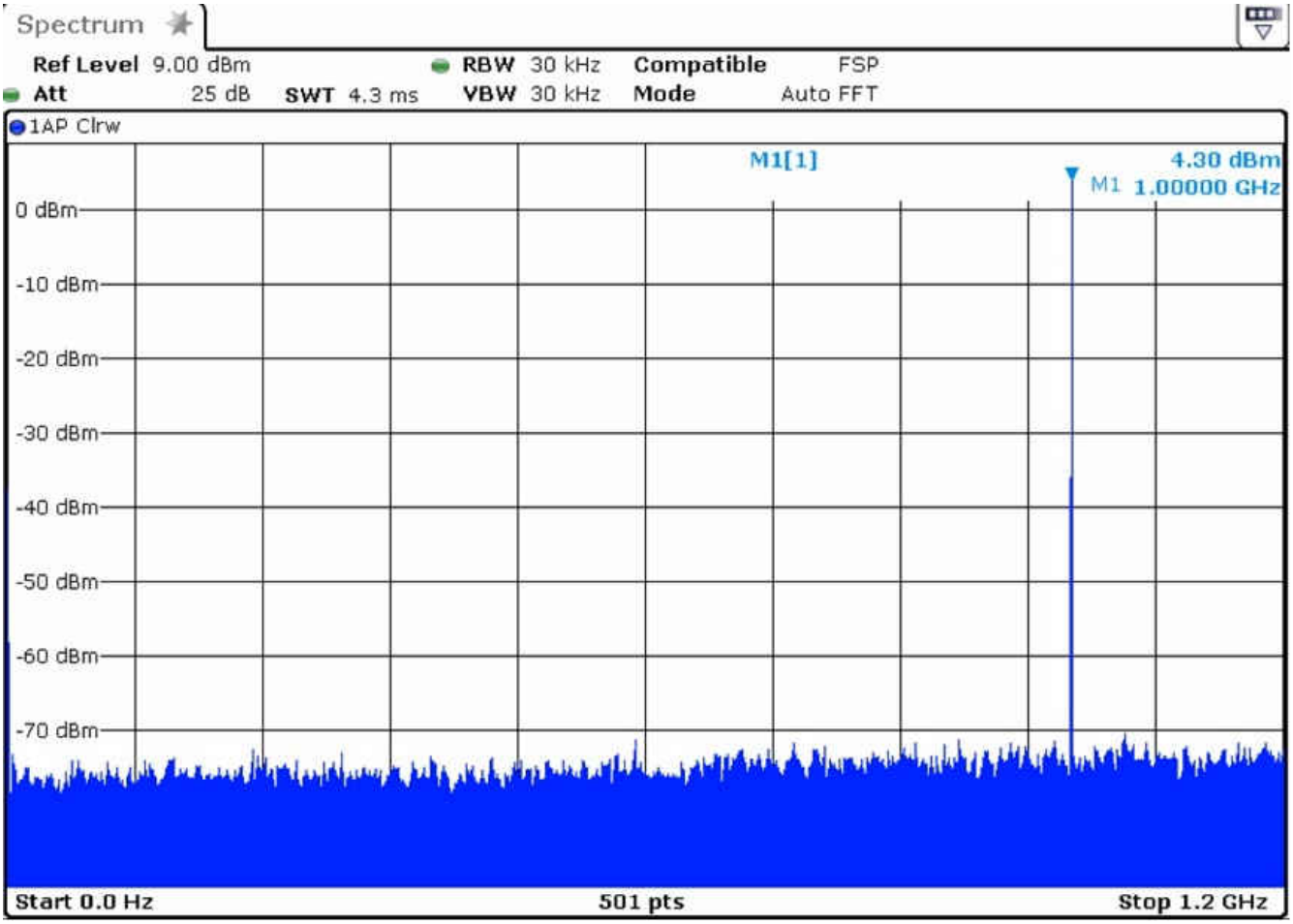


**Figure 3-10. DAC Channel A Output**

# 4 Other Modes of Operation

## 4.1 Single-Channel RF Mode 2 (2nd Nyquist Zone)

In the DAC GUI, click on the *DAC12DL3200 → DACA* tab. For single DAC operation in the 2nd Nyquist zone, in the *DACA_output mode* box, select *RF mode*. With the DAC sampling at 6.4 GHz, and with an input tone at 2.6 GHz, the image will be located at 3.8 GHz in the 2nd Nyquist.

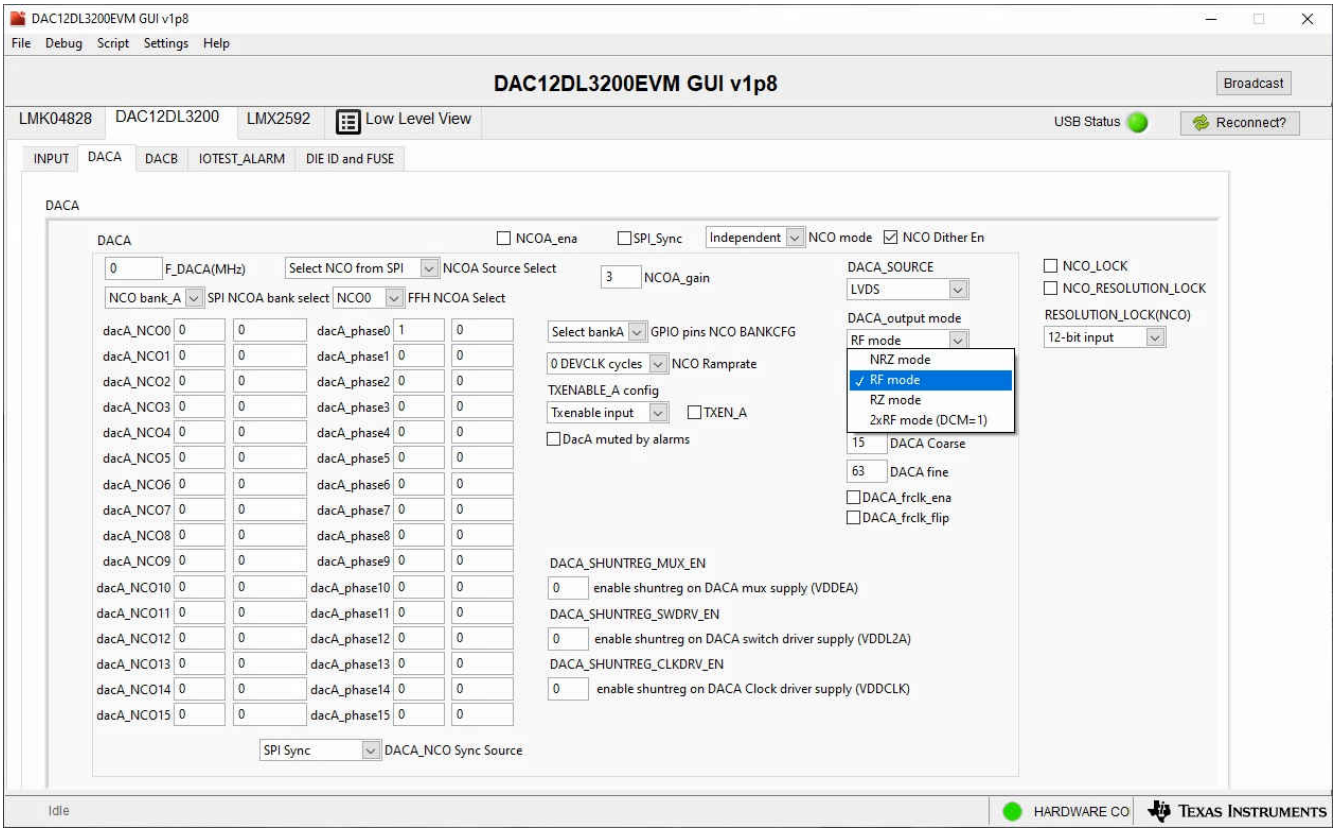


**Figure 4-1. 2nd Nyquist Zone Testing**

## 4.2 Dual-Channel Output Mode 0

Complete the following steps to work in dual-channel output mode 0:

1. Change the frequency of the signal generator connected to EXT_DACCLK (SMA J2) to 3.2 GHz.
2. Select the *DAC RESET* switch.
3. Click on the DAC12DL3200EVM *Low Level View* tab.
4. Click on the *File* icon and navigate to “EXT_CLK_Mode0_NRZ_Dual_DAC.cfg” and click the *OK* button to load the LMK and DAC registers.

   This configuration file will setup the DAC to operate in dual-channel mode with outputs available on CHA and CHB.
5. In the HSDC Pro GUI, in the device drop-down menu, select "DAC12DL3200_MODE0_12b_sync_istrb”. If the firmware is already loaded, skip the next step.
6. When prompted, click the *Yes* button to update the firmware. After the firmware is downloaded, do the DxSTR register write mentioned in the DxSTRB Timing Adjustment section.
7. Enter "3.2GHz" for the *Data Rate*.
8. In the *I/Q Multitone Generator* window in the lower left of the GUI, enter the following parameters: # of tones "1", tone center "1GHz" then click the *Create Tones* button.
9. Click the *Send* button in the upper left of the main GUI page to send the test tone to the DAC EVM. There should now be a 1-GHz output tone on CHA SMA connector J1 and CHB SMA connector J4.

## 4.3 Dual Channel Mode1 Setup

Use the following list to setup the dual DAC one data bank per channel:

1. Change the frequency of the signal generator connected to EXT_DACCLK (SMA J2) to 1.6 GHz. Change the frequency of the signal generator connected to LMK IN (SMA J25) to 400 MHz.
2. Press the DAC RESET switch.
3. Click on the DAC12DL3200EVM *Low Level View* tab.
4. Click on the “File” icon and navigate to “EXT_CLK_Mode1_NRZ_Dual_DAC.cfg” and click on “OK” to load the LMK and DAC registers.

   This configuration file will setup the DAC to operate in dual channel mode, 1 bank of LVDS data only for each DAC, with outputs available on CHA and CHB.
5. In the HSDC Pro GUI, in the device drop-down menu, select "DAC12DL3200_MODE1_12b_sync_istrb”. If the firmware is already loaded, skip the next step.
6. When prompted, click *Yes* to update the firmware. After the firmware is downloaded, do the DxSTR register write mentioned in the DxSTRB Timing Adjustment section.
7. Enter 1.6 GHz for the Data Rate.
8. In the *I/Q Multitone Generator* window in the lower left of the GUI, enter the following parameters: # of tones "1", tone center "500 MHz" then click "Create Tones".
9. Click on "Send" in the upper left of the main GUI page to send the test tone to the DAC EVM. There should now be a 1 GHz output tone on CHA and CHB SMA connectors J1 and J4.

## 4.4 Dual-Channel 2xRF Mode 0 DAC Setup

This mode provides optimized output data in the 3rd, 4th, and 5th Nyquist regions:

1. Change the frequency of the signal generator connected to EXT_DACCLK (SMA J2) to 6.4 GHz. Set the frequency of the signal generator connected to LMK IN (SMA J25) to 1.6 GHz.
2. Press the *DAC RESET* switch.
3. Click on the DAC12DL3200EVM *Low Level View* tab.
4. Click on the *File* icon and navigate to “EXT_CLK_Mode0_2xRF_Dual_DAC.cfg” and click the *OK* button to load the LMK and DAC registers.

   This configuration file sets up the DAC to operate in dual channel mode, 2 banks of LVDS data per DAC, with the output available on CHA and CHB.
5. In the HSDC Pro GUI, in the device drop-down menu, select "DAC12DL3200_MODE0_12b_sync_istrb”. If the firmware is already loaded, skip the next step.
6. When prompted, click *Yes* to update the firmware. After the firmware is downloaded, do the DxSTR register write mentioned in the DxSTRB Timing Adjustment section.
7. Enter "3.2 GHz" for the Data Rate.
8. In the *I/Q Multitone Generator* window in the lower left of the GUI, enter the following parameters: # of tones "1", tone center "1 GHz" then click "Create Tones".
9. Click the *Send* button in the upper left of the main GUI page to send the test tone to the DAC EVM. There should now be a 1-GHz output tone on CHA and CHB SMAs. The image of this tone is optimized for 3rd Nyquist, which is located at 7.4 GHz and 11.8 GHz in the 4th Nyquist zone.

## 4.5 Direct Digital Synthesis Mode

The DAC12DL3200 contains two numerically controlled oscillators (NCOs) that can optionally be used for direct digital synthesis of tones for each DAC. There are two NCO banks, each with 16 separate 32-bit NCOs. The banks can be used separately for each DAC, or together to provide 32 NCOs for one DAC. The two NCOs can be summed as a two tone source for both DACs. The NCO frequencies are set using the dac_A/B_NCO column in the DACA and DACB tabs. The phase is set using the dacA/B_phase column.

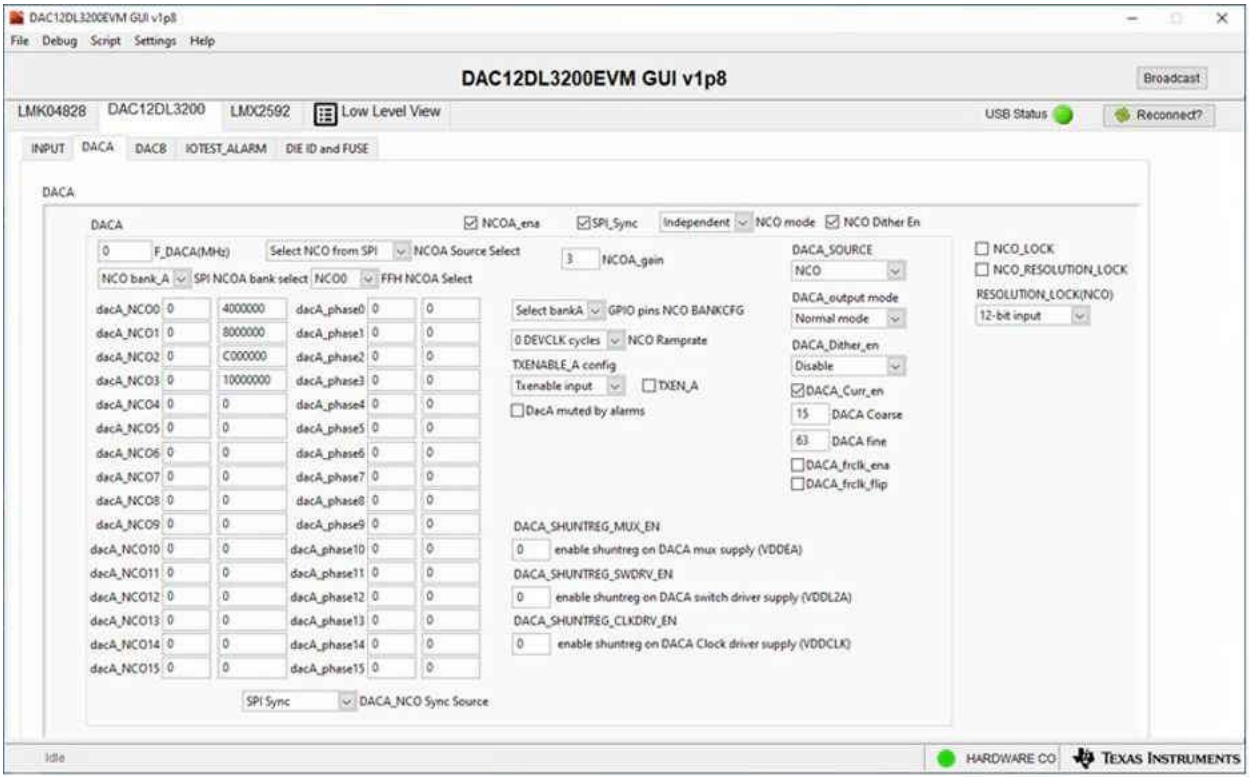


**Figure 4-2. DACA Tab With NCO settings**

The GUI comes with two default NCO setting configuration files. One called "EXT_CLK_6400M_NCOA_1_4_100_400MHz.cfg" which sets the first 4 DAC NCOs to 100 MHz, 200 MHz, 300 MHz, and 400 MHz. With a 6.4-GHz external clock provided to the EVM and this configuration file loaded, the user can select any one of these four NCOs to be sent to the CHA output. The GUI box labeled SPI NCOA bank select determines which NCO is used.

The second configuration file called "LMK_100M_LMX_6400M_NCOA_1_4_100_400MHz" loads the same parameters but is used with the EVM setup in onboard clock mode.

The digital input data is not used in the NCO mode. The TSW14DL3200EVM is not required.

To enter the desired NCO frequency and phase settings, the user must first enter the DAC sample rate in the box labeled as F_DACA(MHz). The value entered is in megahertz.

The user then selects which NCOs they plan on using and enter the NCO frequency in megahertz in the first column. After entering the value, clicking anywhere in the GUI or pressing enter on the keyboard will load the required registers and update the second column with the actual register setting used to generate this frequency. The same instructions apply for setting the NCO phase. The value to be entered for phase is in radians. The valid entries are from –3.1416 to 3.1416. The equation for this setting can be found in the device data sheet.

Figure 4-3 illustrates a setting with the DAC sampling at 6400 MHz and NCO0, NCO1, NCO2 and NCO3 set to 100 MHz, 200 MHz, 300 MHz, and 400 MHz.

If using the SPI_SYNC for the NCO SYNC source, after making any changes to the NCO settings, click on the SPI_SYNC button twice to synchronize the two NCOs.

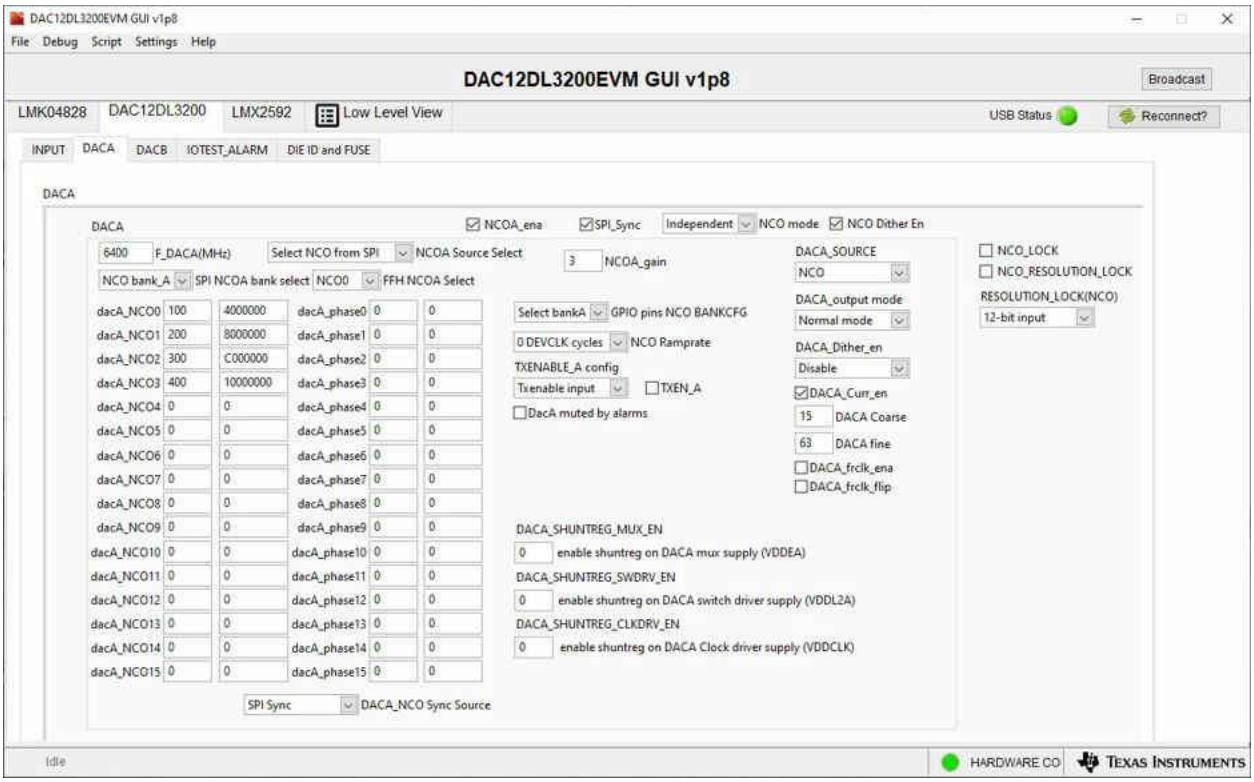


**Figure 4-3. NCOA Calculation**

# 5 Register Log File

Double clicking near the text *Idle* in the lower left of the GUI opens a log file. Every time a user enters a new value or clicks on a button in the GUI, the log file updates and shows the actual register address and data value that was written to the DAC12DL3200, LMK04828, or LMX2592. This log file information can be saved by first highlighting the register settings to be saved then double clicking inside the log file and selecting *Save Selected*.

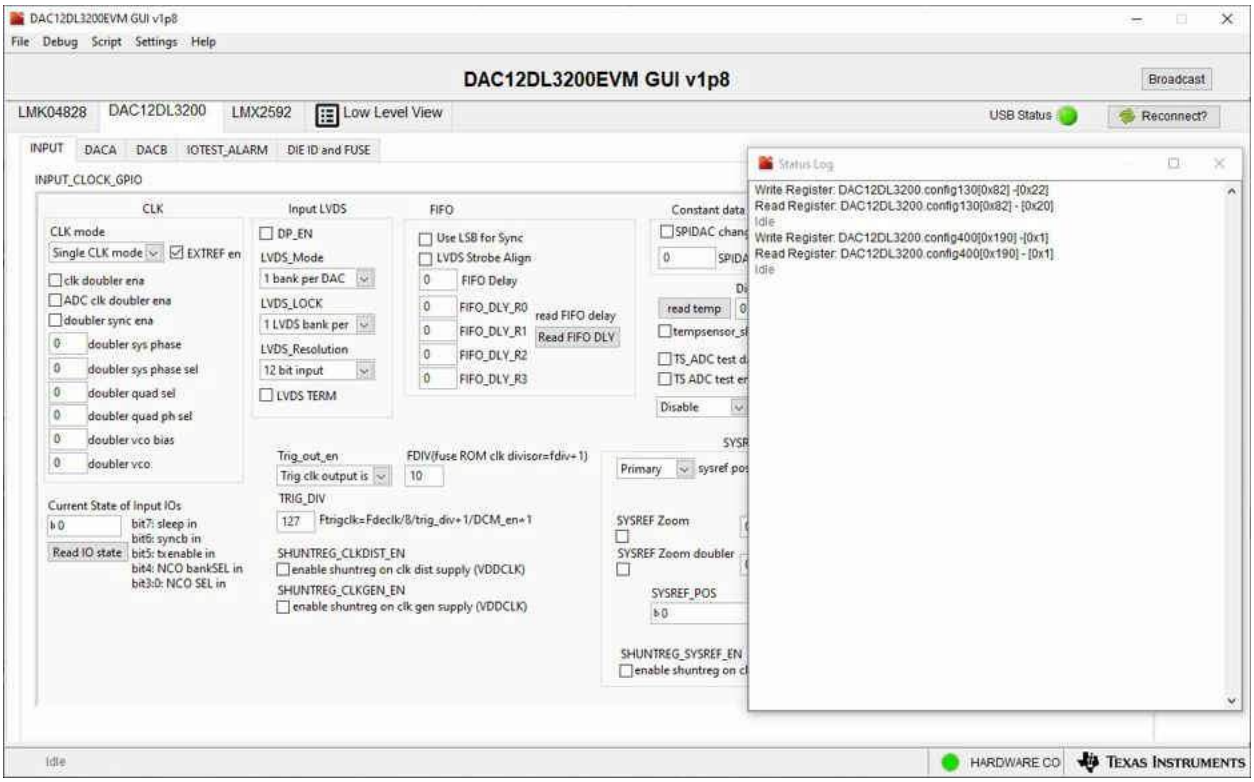


**Figure 5-1. Register Log file**

# 6 Device Configuration

The DAC device is programmable through the serial programming interface (SPI) bus accessible through the FTDI USB-to-SPI converter located on the EVM. The GUI is used to write instructions on the bus and program the registers of the DAC12DL3200, LMK04828, and LMX2592 devices.

For more information about the registers in the DAC device, see the *DAC12DL3200 6.4-GSPS Single Channel or 3.2-GSPS Dual Channel, 12-bit DAC Data Sheet*.

## 6.1 Tab Organization

Control of the DAC device features are available in the *INPUT*, *DACA, DACB, IOTEST_ALARM*, and *DIE ID and FUSE* configuration tabs.

Control of the LMK0428 device features are available in the *PLL1 Configuration*, *PLL2 Configuration, SYSREF and SYNC, and Clock Outputs* configuration tabs under the LMK04828 tab.

Control of the LMX2592 device features are available under the LMX2592 tab.

## 6.2 Low-Level Control

The *Low Level View* tab illustrated in Figure 6-1, allows configuration of the devices at the bit-field level. At any time, use the controls in Table 6-1 to configure or read from the device.

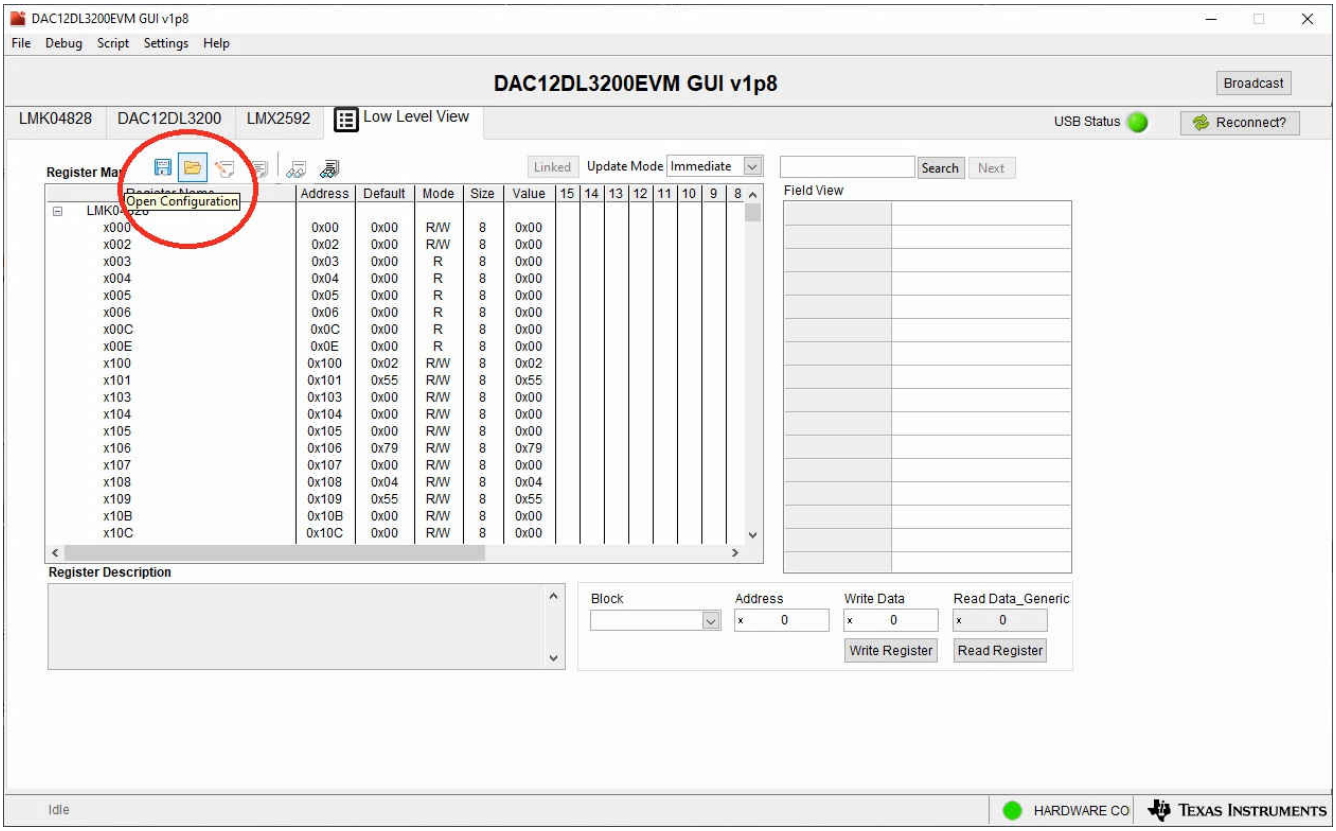


**Figure 6-1. Configuration GUI: Low-Level View Tab**

**Table 6-1. Low-Level Controls**

| Control | Description |
|---|---|
| Register map summary | Displays the devices on the EVM, registers for those devices, and the states of the registers<br>• Clicking on a register field allows individual bit manipulation in the register data cluster<br>• The value column shows the value of the register at the time the GUI was last updated |
| Write register button | Write to the register highlighted in the register map summary with the value in the *Write Data* field |
| Write all button | Update all registers shown in the register map summary with the values shown in the *Register Map* summary |
| Read register button | Read from the register highlighted in the *Register Map* summary and display the results in the *Read Data* field<br>Can be used to synchronize the GUI with the state of the hardware |
| Read-all button | Read from all registers in the *Register Map* summary and display the current state of the hardware |
| *Load Configuration* button | Load a configuration file from disk and register address/data values in the file |
| *Save Configuration* button | Save a configuration file to disk that contains the current state of the configuration registers |
| *Register Data* cluster | Manipulate individual accessible bits of the register highlighted in the register map summary |
| Individual register cluster with read or write register buttons | Perform a generic read or write command to the device shown in the *Block* drop-down menu using the address and write data information |

# A Troubleshooting the DAC12DL3200EVM

Table A-1 lists some troubleshooting procedures.

**Table A-1. Troubleshooting**

| Issue | Troubleshoot |
|---|---|
| General problems | • Verify the test setup shown in Figure 3-1, and repeat the setup procedure as described in this document.<br>• Check power supply to EVM and TSW14DL3200EVM. Verify that the power switch is in the on position.<br>• Check signal and clock connections to EVM.<br>• Visually check the top and bottom sides of the board to verify that nothing looks discolored or damaged.<br>• Make sure the board-to-board FMC connection is secure.<br>• After changing the DAC configuration, click *Instrument Options* → *Download Firmware* and download *TSW14DL3200_DAC_FIRMWARE.bin*.<br>• Power cycle the external power supply to the DAC EVM, and reprogram the LMK and DAC devices.<br>• Ensure jumpers are set properly. |
| TSW14DL3200 EVM LEDs are not correct | • Verify the installed jumpers on the TSW14DL3200EVM.<br>JP2 pins 1–2, JP4 pins 2–3, and JP3 open.<br>• Verify that the clock going to the CLK inputs of the DAC EVM are connected.<br>• Verify that the DAC and LMK internal registers are configured properly.<br>• Click *Instrument Options* → *Download Firmware* and download *TSW14DL3200_DAC_FIRMWARE.bin*. |
| Configuration GUI is not working properly | • Verify that the USB cable is plugged into the EVM and the PC.<br>• Check the computer device manager and verify that a *USB serial device* is recognized when the EVM is connected to the PC.<br>• Verify that the green *USB Status* LED light in the top right corner of the GUI is lit. If it is not lit, click the *Reconnect FTDI* button.<br>• Close and start the configuration GUI. |
| Configuration GUI is not able to connect to the EVM | • Use the free FT_PROG software from FTDI chip and verify that the onboard FTDI chip is programmed with the product description *DAC12DL3200*. |
| HSDC Pro software is not sending data. | • Verify that the TSW14DL3200EVM is properly connected to the PC with a mini USB 3.0 cable and that the board serial number is properly identified by the HSDC software.<br>• Check that the DAC device mode selected matches the HSDC Pro ini file selected.<br>• Check that the data rate parameter is correct. This should have a "M" for megahertz or "G" for gigahertz after the frequency number. |
| HSDC Pro software gives a time-out error when User clicks on *SEND*. | • Verify that the DAC data rate parameter is correctly set in the HSDC software.<br>• Select *Instrument Options* → *Download Firmware* and download *TSW14DL3200_DAC_FIRMWARE.bin*. Try sending the test pattern again.<br>• Verify both clocks are enabled, synchronized and the correct frequency going to the DAC EVM. |
| Sub-optimal measured performance | • Make sure the DAC reset button was pressed before loading the DAC configuration file.<br>• Ensure all SMA connections are secure.<br>• Make sure FMC connectors are fastened together properly. |

# B DAC12DL3200EVM Onboard Clocking Configuration

This appendix provides settings for modifying the EVM for onboard clocking mode. In this mode, no external clocks are required. The LMK04828 uses the onboard 100-MHz VCXO and the internal PLL2 to provide the required clocks along with the LMX2592.

The DAC12DL3200EVM GUI provides 12 configuration files to be used with this mode. The following list describes a few of them:

1. **LMK_100M_LMX_6400M_Mode2_NRZ_Single_DAC.cfg**: Operates the DAC in mode 2 with a sample rate of 6.4 GHz.
2. **LMK_100M_LMX_3200M_Mode0_NRZ_Dual_DAC.cfg**: Operates the DAC in mode 0 with a sample rate of 3.2 GHz.
3. **LMK_100M_LMX_1600M_Mode1_NRZ_Dual_DAC.cfg**: Operates the DAC in mode 1 with a sample rate of 1.6 GHz.
4. **LMK_100M_LMX_6400M_Mode0_2xRF_Dual_DAC.cfg**: Operates the DAC in mode 0 with a sample rate of 6.4 GHz.
5. **LMK_100M_LMX_6400M_NCOA_1_4_100_400MHz.cfg**: Operates the DAC in NCO mode with CHA output options of 100 MHz, 200 MHz, 300 MHz, and 400 MHz.

When using the "LMK_100M_LMX_6400M_Mode2_NRZ_Single_DAC.cfg" configuration file, the LMK04828 provides a 100-MHz reference clock to the LMX2592, a 50-MHz SYSREF clock to the DAC and a 400-MHz reference clock to the FPGA on the TSW14DL3200EVM.

The LMX2592 uses a 100-MHz reference clock from the LMK04828 and an internal PLL to provide the 6.4-GHz clock to the DAC. All clocks are synchronized to the 100-MHz VCXO.

To configure the DAC12DL3200EVM to use onboard clock mode, complete the following steps:

1. Remove C7 and C6, and populate C277 and C278.
2. Install FB28 with MuRata BLM18AG121TN1D or equivalent. This is located on the bottom of the board under Y2.
3. Remove the shunt on the LMX_CE jumper J6.


**Figure B-1. Onboard Clocking Setup**

4. Remove the signal generators.
5. Program the DAC using the DAC12DL3200 GUI.
   a. Press the DAC RESET switch on the EVM.
   b. In the DAC GUI *Low Level View* tab, select the configuration file called "LMK_100M_LMX_6400M_Mode2_NRZ_Single_DAC.cfg".
6. Send a test pattern using HSDC Pro GUI.

The LMK04828 routes a spare clock (DCLK10) to SMBs J26 and J28 that can be used to verify LMK operation. By default, the GUI has this clock disabled. Use the *LMK04828 Clock Outputs* tab to enable this clock. Set CLKout 10 and 11 DCLK Type to "LVPECL 2000 mV" and DCLK Divider to "24" to provide a 100-MHz clock to these SMBs (LMKOUTP, LMKOUTN).

The LMX2592 routes a spare clock (RFOUTB) to SMB J20 that can be used to verify LMX operation. By default, the GUI has this clock disabled. Click on the LMX2592 tab and uncheck the OUTB PD box. There is now a 6.4-GHz tone on SMB connector J20 (LMX OUT).

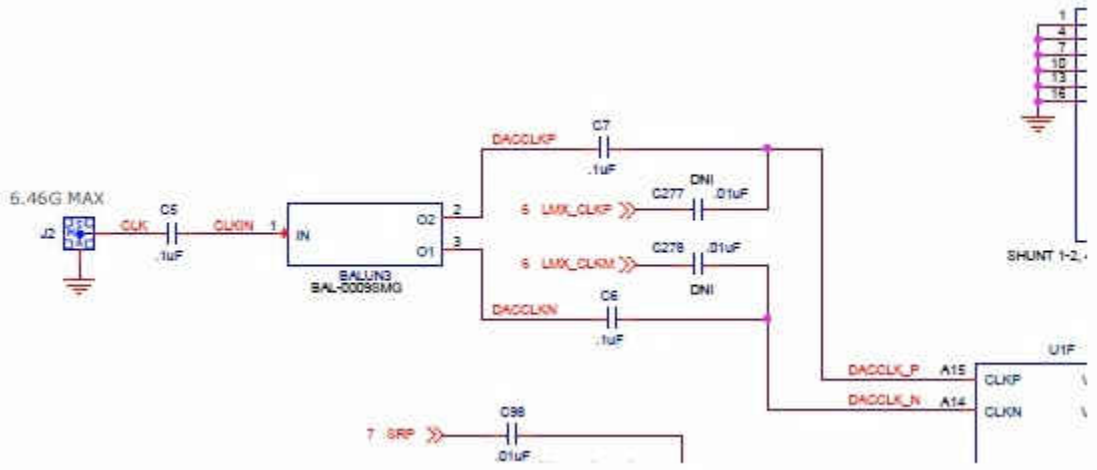


**Figure B-2. Default Board Clock Configuration Circuit (External Clock Mode)**

The LMX2582 and LMK04828 may be reconfigured to exercise more features, but this EVM is not intended to be a full evaluation platform for these devices. For a full evaluation platform, see the LMK04828EVM tool folder and LMX2592EVM tool folder.

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