A DIVISION OF CIRRUS LOGIC

CS5324

120 dB, 500 Hz Oversampling A/D Converter

Features

- Monolithic CMOS A/D converter
- 120 dB Dynamic Range
- dc-500 Hz Bandwidth
- 110 dB Total Harmonic Distortion
- Internal Track-and-Hold Amplifier
- Delta-Sigma Architecture
  - 256X Oversampling
  - Linear Phase Digital Filter
  - Output Word Rate 32 kHz
- Low Power Dissipation: 150 mW
- Evaluation Board Available

Description

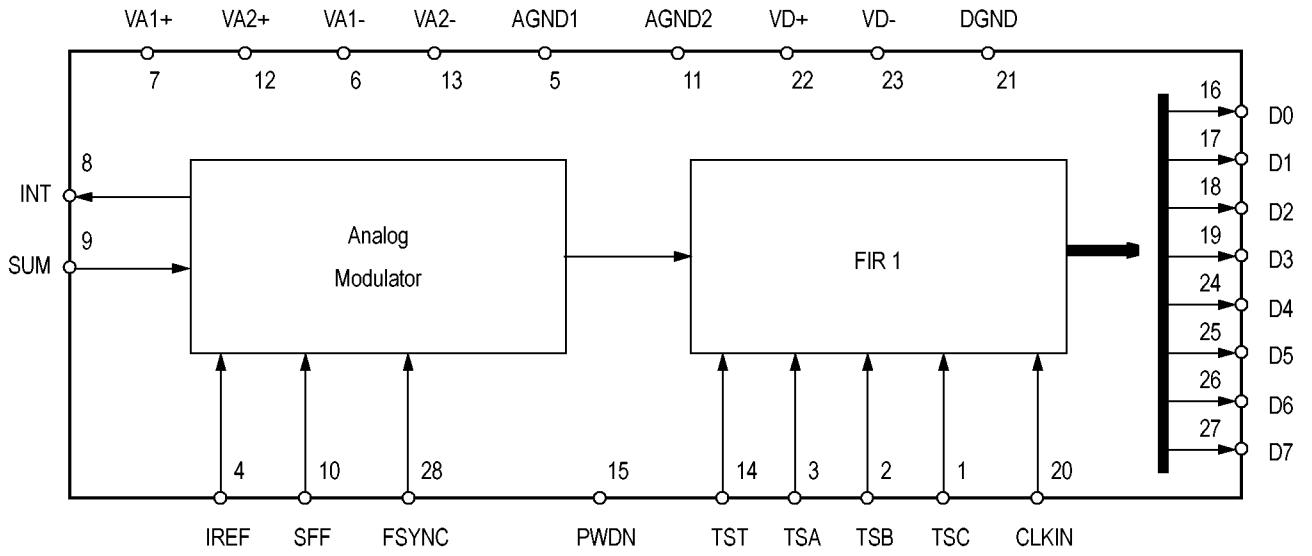
very high resolution A/D converter intended for geophysical and sonar applications. It is a complete analog front end to a Digital Signal Processor and provides the DSP with a low distortion digital input suitable for precision signal analysis. The CS5324 performs sampling, A/D conversion, and anti-alias filtering.

The CS5324 uses delta-sigma modulation to produce highly accurate conversions. The device oversamples at 256X, virtually eliminating the need for external anti-aliasing filters. An on-chip linear-phase FIR digital filter decimates the output to a 32 kHz output word rate. Data is transmitted to the DSP as two, 8-bit bytes. An additional FIR filter in the DSP further decimates the signal to achieve 120 dB dynamic range over 500 Hz bandwidth with signal-to-distortion of 110 dB.

The CMOS design of the CS5324 ensures high reliability and power dissipation of less than 180 mW.

ORDERING INFORMATION

CS5324-BL -40° to +85° C 28-pin PLCC



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ANALOG CHARACTERISTICS (T_A= T_{min} to T_{max} ; VA-=-5V; VA+= 5V; AGND=0V; CLKIN=1.024 MHz Device is connected as shown in Figure 1, the System Connection Diagram. Output data is further processed using off-chip filtering described in Appendix 1.)

Parameter*		Symbol	Min	Typ	Max	Units
Specified Temperature Range			-40	-	+85	°C
Dynamic Performance						
Dynamic Range		DR	116	120	-	dB
Signal-to-Distortion	(Note 1)	SDR	100	110	-	dB
Intermodulation Distortion	(Note 2)		-	110	-	dB
dc Accuracy						
Full Scale Error	(Note 3)		-	-	2	%
Full Scale Drift	(Note 3, 4)		-	0.003	0.006	%/°C
Offset	(Note 3)		-	-	250	mV
Offset Drift	(Note 3, 4)		-	500	750	µV/°C
Input Characteristics						
Input Signal Frequencies	(Note 5)	BW	dc	-	500	Hz
Input Voltage Range	(Note 6)	Vin	-10.0	-	+10.0	V
Power Supplies						
DC Power Supply Currents	(Note 7)					
Positive Supplies			-	12.5	18	mA
Negative Supplies			-	14.5	18	mA
Power Dissipation	(Note 7)					
PWDN Low			-	150	180	mW
PWDN High			-	5	10	mW
Power Supply Rejection						
(dc to 500 Hz) VA+	(Note 8)		-	55	-	dB
VA-			-	45	-	dB
VD+			-	48	-	dB
VD-			-	38	-	dB
(500 Hz to 128 kHz) VA+	(Note 9)		-	60	-	dB
VA-			-	60	-	dB
VD+			-	50	-	dB
VD-			-	55	-	dB

Notes:
1. Tested with full scale input signal of 50 Hz.
2. Tested with input signals of 50 Hz and 90 Hz, each 6 dB down from full scale.
3. Specification is for the parameter over the specified temperature range and is for the CS5324 device only. It does not include the effects of external components.
4. Drift specifications are guaranteed by design and characterization.
5. The upper bandwidth limit is determined by the off-chip digital filter.
6. This input voltage range is for the configuration depicted in Figure 1, the System Connection Diagram.
7. All outputs unloaded. All logic inputs forced to VA+ or GND.
8. Tested with a 100 mVp-p 120 Hz sine wave applied separately to each supply (VA1 and VA2 are considered as one input for this test).
9. Tested with a 100 mVp-p 120 kHz sine wave applied separately to each supply (VA1 and VA2 are considered as one input for this test).

* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS (T_A= T_{min} to T_{max} ; VA+,VD+=5V±5%; VA-, VD- =-5V±5%; Inputs: Logic 0 = 0V Logic 1 = VD+; C_L=50pF. See Note 10.)

Parameter			Symbol	Min	Typ	Max	Units
CLKIN Frequency		(Note 11)	f_c	0.9	1.024	1.1	MHz
CLKIN Duty Cycle				40	-	60	%
CLKIN Jitter				-	-	5	ps
Rise Times:	Any Digital Input Any Digital Output	(Note 12)	t_{rise}	- -	- 50	1.0 200	µs ns
Fall Times:	Any Digital Input Any Digital Output	(Note 12)	t_{fall}	- -	- 50	1.0 200	µs ns
CLKIN Rising Edge to FSYNC Rising		(Note 13)	t_{cf}	70	-	-	ns
FSYNC Rising to CLKIN Falling Edge			t_{fc}	150	-	-	ns
Output Data Delay: CLKIN Rising to Valid Data			t_{dd}	-	200	250	ns
Output Float Delay: CLKIN Rising to Hi-Z			t_{fd}	-	150	250	ns

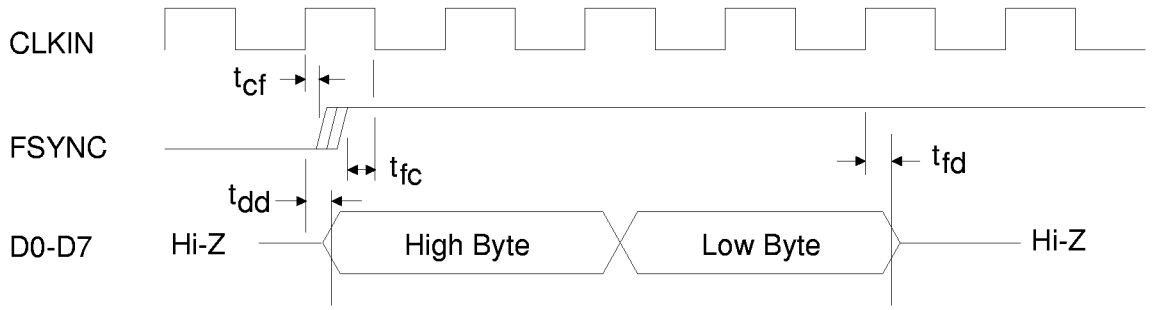
Notes: 10. Guaranteed by design, characterization and/or test.
11. If CLKIN is removed the device will enter the power down mode.
12. Excludes CLKIN input. CLKIN should be driven with a signal having rise and fall times of 25ns or faster.
13. Only the rising edge of FSYNC relative to CLKIN is used to synchronize the device. FSYNC can return low at any time as long as it remains high for at least one CLKIN cycle.

DIGITAL CHARACTERISTICS (T_A= T_{min} to T_{max} ; VA+,VD+ = 5V±5%; VA-,VD- = -5V±5%)

All measurements below are performed under static conditions.

Parameter			Symbol	Min	Typ	Max	Units
High-Level Input Voltage			V_{IH}	(VD+)-1.0V	-	-	V
Low-Level Input Voltage			V_{IL}	-	-	1.0	V
High-Level Output Voltage	I_{OUT} = -600 µA	(Note 14)	V_{OH}	(VD+)-0.4V	-	-	V
Low-Level Output Voltage	I_{OUT} = 800 µA	(Note 14)	V_{OL}	-	-	0.4	V
Input Leakage Current			I_{LKG}	-	-	±10	µA
Tri-State Leakage Current			I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance			C_{OUT}	-	9	-	pF

Notes: 14. The device is designed for low current output drive to minimize induced noise. CMOS interfacing is highly recommended.



Digital Timing Relationships

RECOMMENDED OPERATING CONDITIONS (DGND=0V; AGND=0V. All voltages measured with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Supply						
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	-4.75	-5.0	-5.25	V
	Positive Digital	VD+	4.75	5.0	5.25	V
	Negative Digital	VD-	-4.75	-5.0	-5.25	V

ABSOLUTE MAXIMUM RATINGS (DGND=0V; AGND=OV. All voltages measured with respect to ground.)

Parameter			Symbol	Min	Max	Units
DC Supply	Positive Digital		VD+	-0.3	(VA+)+0.3	V
	Negative Digital		VD-	0.3	-6.0	V
	Positive Analog		VA+	-0.3	6.0	V
	Negative Analog		VA-	0.3	-6.0	V
Input Current, Any Pin Except supplies		(Note 15)	I_{in}	-	±10	mA
Digital Input Voltage			V_{IND}	-0.3	(VA+)+0.3	V
Ambient Operating Temperature			T_A	-55	125	°C
Storage Temperature			T_{stg}	-65	150	°C

Note: 15. Transient currents up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

General Description

The CS5324 is a monolithic CMOS A/D converter designed specifically for very high resolution measurement of signals between dc and 500 Hz. The device consists of a fourth-order delta-sigma modulator followed by an on-chip digital decimation filter.

The modulator of the CS5324 samples the analog input signal at a 256X oversampling rate. This high oversampling rate, along with subsequent digital filtering, enables the CS5324 to achieve a dynamic range which exceeds 120dB. To achieve optimum performance, the CS5324 uses off-chip circuitry to develop the reference and operating currents necessary to set the gain and offset of the modulator portion of the A/D converter. Discrete components are also used for the first stage integrator input resistor and integration capacitor.

The CS5324 performs conversions continuously and outputs twelve data bits for further data decimation by an off-chip digital filter. A separate DSP chip can be utilized to perform the off-chip filtering. A single DSP chip can perform the filter function for several CS5324 devices. For this reason, the CS5324 was designed to output its data in a simple time-division multiplexing (TDM) format. This TDM architecture allows up to eight CS5324 devices to share the same data bus.

Theory of Operation

The CS5324 utilizes a fourth order oversampling delta-sigma architecture to achieve high-resolution A/D conversion. The converter consists of an analog modulator, along with an on-chip digital decimation filter. The modulator consists of a 1-bit A/D converter embedded in a negative feedback loop. The first stage of the fourth order modulator uses discrete components external to the chip to maximize signal performance relative to noise.

The modulator samples at 256 kHz (CLKIN = 1.024 MHz) which is 256X oversampling above two times the maximum signal frequency of 500 Hz. The modulator output is followed by a decimate by 8, fourth-order (sinx)/x filter. The result from this filter is a 12-bit word which is output from the chip at a 32 kHz rate. The 12-bit data is then further filtered by means of an off-chip digital filter. The off-chip filter can be implemented by either a DSP chip or an ASIC designed for this purpose. The exact characteristics of the on-chip filter and some recommended off-chip digital filters are discussed under the Filter Characteristics section of the data sheet. Upon reduction with the off-chip filtering, the data results in resolution which exceeds 20-bits. The final result yields a dynamic range exceeding 120 dB.

The architecture of the CS5324 was chosen to maximize performance. The input integrator uses off-chip discrete components. The chip is designed to use a current-source type reference, rather than a voltage source to minimize noise. In addition, the amount of on-chip digital filtering is minimized to reduce the possibility of the digital noise of the filter coupling into the analog sections of the chip. Configuring the chip to use additional off-chip digital filtering also allows the user maximum flexibility in implementing a filter appropriate to his system requirements.

Signal Input and Current Reference

The CS5324 uses a number of external discrete components to achieve maximum performance. Figure 1 illustrates the recommended circuit configuration for the current reference components and for the signal input components.

The CS5324 is designed to use a current reference of 2 mA into the IREF pin. A current reference rather than a voltage reference was chosen to achieve better noise performance. For optimum performance the dc source impedance at

the IREF pin should be approximately 5 kΩ. This calls for a 10 volt source driving the 5 kΩ (R_6+R_7) resistor to achieve the desired 2 mA current source. The IREF input sets the full scale gain of the A/D converter.

To properly bias the input integrator to a midrange operating point, a current source 1/4 the size of the IREF input current must be sourced into the integrator summing junction at the SUM pin. This requires a 20 kΩ resistance (R4+R5) be placed from the 10 V reference to the SUM pin.

Both the 2 mA IREF current and the 500 µA sources have capacitive filtering to aid in reducing the broadband current noise from the voltage reference. These capacitors should be of quality construction. Particular attention should be paid

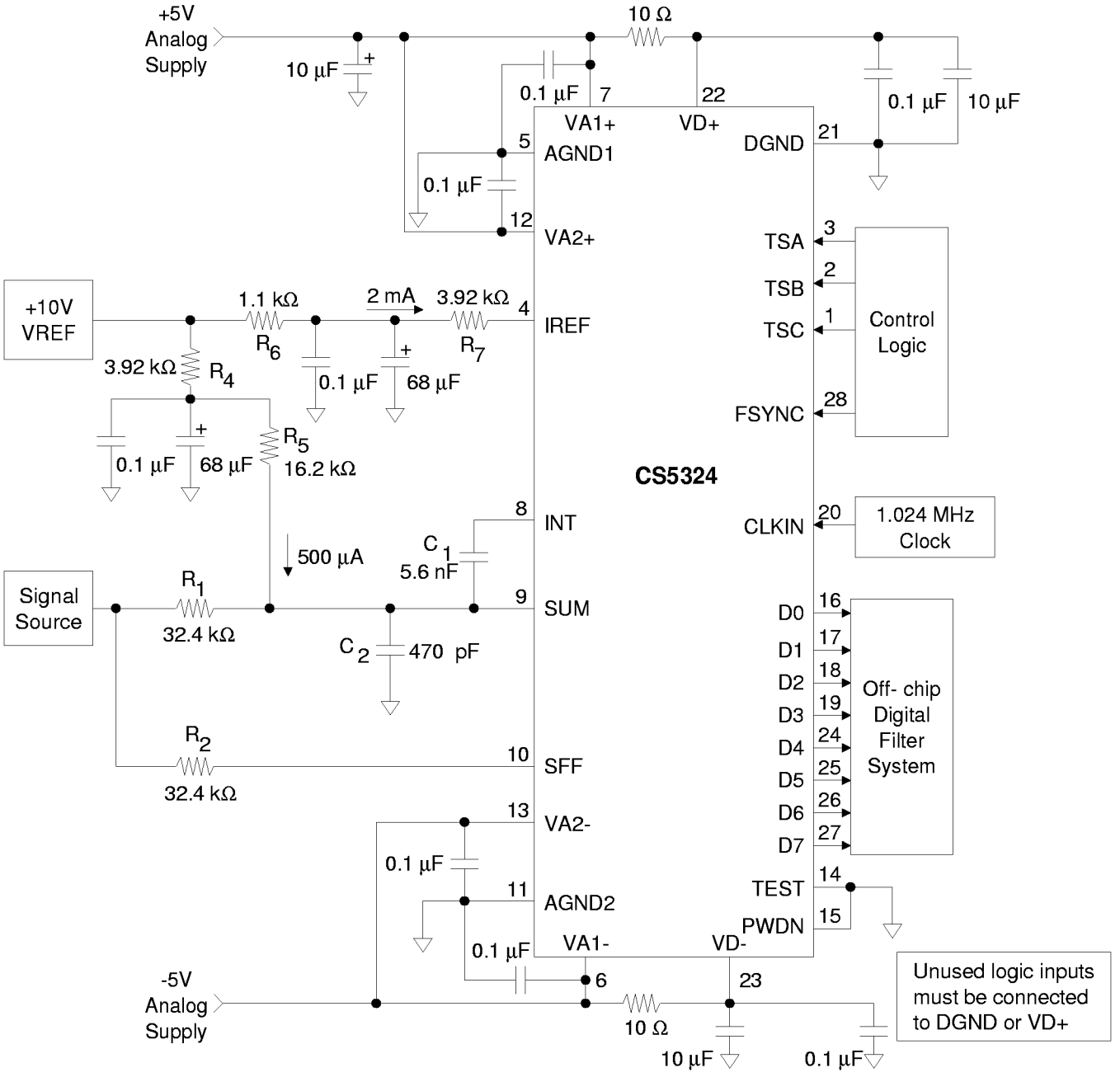


Figure 1. System Connection Diagram

to leakage current variation over the desired operating temperature, as this leakage will affect the system gain.

The signal input pin (SUM) of the CS5324 is the summing junction of the input integrator stage. This integrator is designed to use an external input resistor (R_1) and integrating capacitor (C_1). In addition, a capacitor (C_2) is required at this node for proper phase compensation. The size of the input resistor (R_1) is determined by the magnitude of the signal current. With a maximum input voltage into the resistor, the integrator input current must be set equal to approximately 0.15 the current value injected into the IREF pin. With a 2 mA IREF current, the full scale signal current should be about 300 µA. Additionally, to minimize current noise into the summing junction, the value of the effective input resistance should be above 8 kΩ. Using a 32.4 kΩ resistor for R_1 sets the full scale input voltage into the integrating resistor to a value near 10 volts. The input signal then spans 20 V_{p-p}.

Once the integrator input resistor is chosen, the integrator capacitor can be determined. The resistor and capacitor combination should yield a frequency ($f= 1/(2 \pi R_1C_1)$) between 800 and 900 Hz to achieve maximum performance. This yields a capacitor value near 5.6 nF. The capacitor should be chosen for minimum leakage, minimum dielectric absorption, and minimum voltage coefficient of capacitance. While a teflon foilwrap capacitor is preferred, high quality film capacitors may be acceptable in many applications.

The CS5324 has a second signal input pin called the Signal Feedforward (SFF) pin. The signal into this pin bypasses the input stage of the input integrator, improving signal performance in the passband. The resistor (R_2) used at this input should be identical in value and performance characteristics to the input resistor (R_1).

Digital Output and Data Format

For proper operation the CS5324 must be provided with a CMOS-compatible clock into the CLKIN pin. The normal operating frequency is 1.024 MHz. This clock determines the input sample rate and the output word rate of the converter. The sample rate is CLKIN/4 while the output word rate is at CLKIN/32.

The CS5324 will compute a 12-bit output word at a 32 kHz rate (CLKIN = 1.024 MHz). The data is output from Data Output pins D7-D0 in the form of two eight bit bytes. The first byte is the high order byte with the MSB in the D7 position. The second 8-bit byte is the low order byte, and includes three status bits and an unused bit. The data is in two's complement format. Figure 2 illustrates the format of the output data.

For 12-bit two's complement data the codes range from -2048 to +2047. The output codes from the CS5324 will range from approximately -1280 to +1280 for a full scale sine wave input into the converter as shown in Table 1. There may be typically ±50 codes of noise (p-p) on the data in the 12-bit data output. Off-chip digital filtering is required to achieve the full dynamic range capability of the CS5324.

	D7	D6	D5	D4	D3	D2	D1	D0
Hi Byte	B11	B10	B9	B8	B7	B6	B5	B4
Lo Byte	B3	B2	B1	B0	0	OF	UF	ORST

Data is 2's complement with B11 as sign bit

Figure 2. Output Data Format

Input Signal	Output Code
approx. +16V	0111 1111 1111
+F.S. - 1.5 LSB (approx. +10V)	0101 0000 0000
0V	0000 0000 0000
-F.S. + 0.5 LSB (approx. -10V)	1011 0000 0000
approx. -16V	1000 0000 0000

Notes: 1. Output codes from the on-chip digital filter will typically exhibit ±50 LSB's of noise (p-p).
2. Table depicts output codes for circuit configuration of Figure 1.

Table 1. Output Coding

Status Bits

Three status bits are output from the CS5324. The three status bits are overflow, underflow, and oscillation reset. The overflow and underflow status bits indicate whenever the digital filter accumulator results in an overflow or underflow condition. With the present on-chip digital filter, the underflow condition will never occur. The overflow bit will go high indicating an accumulator overflow only if the input signal to the converter exceeds positive full scale by approximately 1.6X. Upon overflow, the accumulator will contain the value +2047 (or 2048 after underflow). The oscillation reset status bit indicates that output data may be in error. An oscillation detection circuit monitors the modulator loop to see if it is operating within its stable operating range. If the modulator is operating outside its normal operating range the output data may be corrupted. The ORST status bit may go high as a result of power-up, or, if the input signal exceeds the specified full scale input value. If ORST does occur, it will remain high for a total of four update cycles (of 32 kHz) to the output port, while the modulator and the digital filter are reset. Once ORST goes back low, output data will not be valid until the modulator and the digital filter(s) settle.

Initialization and Output Data Sequencing

The CS5324 updates its output register at a 32 kHz rate (CLKIN = 1.024 MHz). Between updates 32 CLKIN cycles occur. The CS5324 is designed such that eight data output time slots occur during these 32 CLKIN cycles. Each time slot lasts for 4 CLKIN cycles. The CS5324 is designed to allow eight devices to share the same 8-bit data bus when each device is set-up to output its data in an individual time slot. The exact time the CS5324 will output data is determined by the TSA, TSB, TSC, and FSYNC inputs. After power is applied to the devices, the FSYNC input must be brought high. When FSYNC is brought high (within the required timing specifications), each chip will be assigned to a data output time slot according to the logic levels of its TSA, TSB, and TSC inputs. Table 2 tabulates the decoding of these inputs.

If all the CS5324s in the system are initialized with the same FSYNC signal, they will all compute filter results in phase with each other and update their output registers at the same time. Only the time slot in which the data is output from the devices is different.

The FSYNC signal used to initialize the CS5324 need only be activated once after power up. In some systems, it may be preferable to have this

TSA	TSB	TSC	Time Slot
0	0	0	TS0
0	0	1	TS1
0	1	0	TS2
0	1	1	TS3
1	0	0	TS4
1	0	1	TS5
1	1	0	TS6
1	1	1	TS7

Table 2. Time - Slot Decoding

signal occur every 32 CLKIN cycles. Only the occurrence of the rising edge of FSYNC is significant in determining the system initialization. Figure 3 illustrates a system configuration using multiple CS5324s interfaced to the same DSP chip.

Four cycles of CLKIN occur during each time slot. During the time slot designated for a CS5324 to output its data, the high-order byte will be output for the first two CLKIN cycles of the time slot. The second byte will be output during the last two CLKIN cycles of the period.

If four or less CS5324's share the same data bus, it is preferable to use alternate time slots (i.e. TS0, TS2, TS4, TS6) to minimize the possibility of bus contention problems. Slight timing differences between chips may result in timing overlap if adjacent time slots are used.

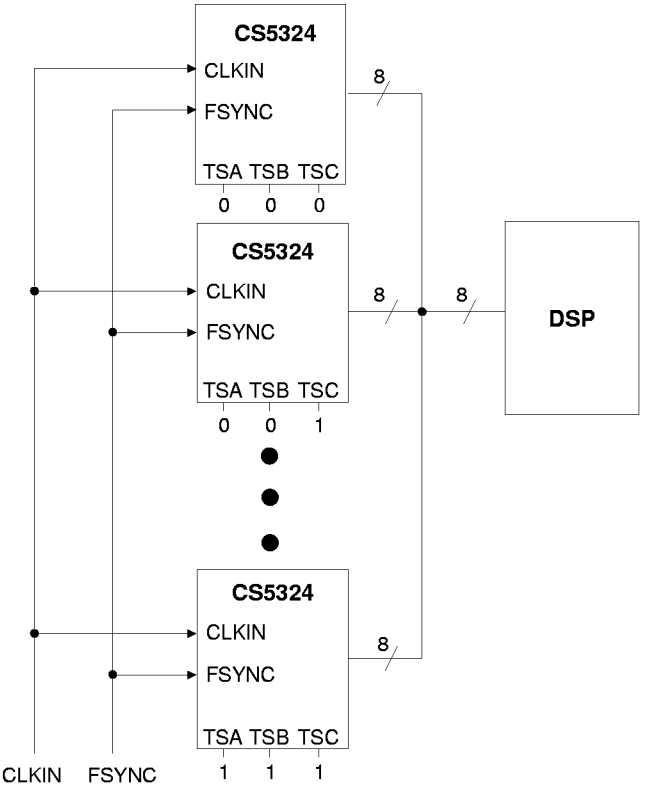


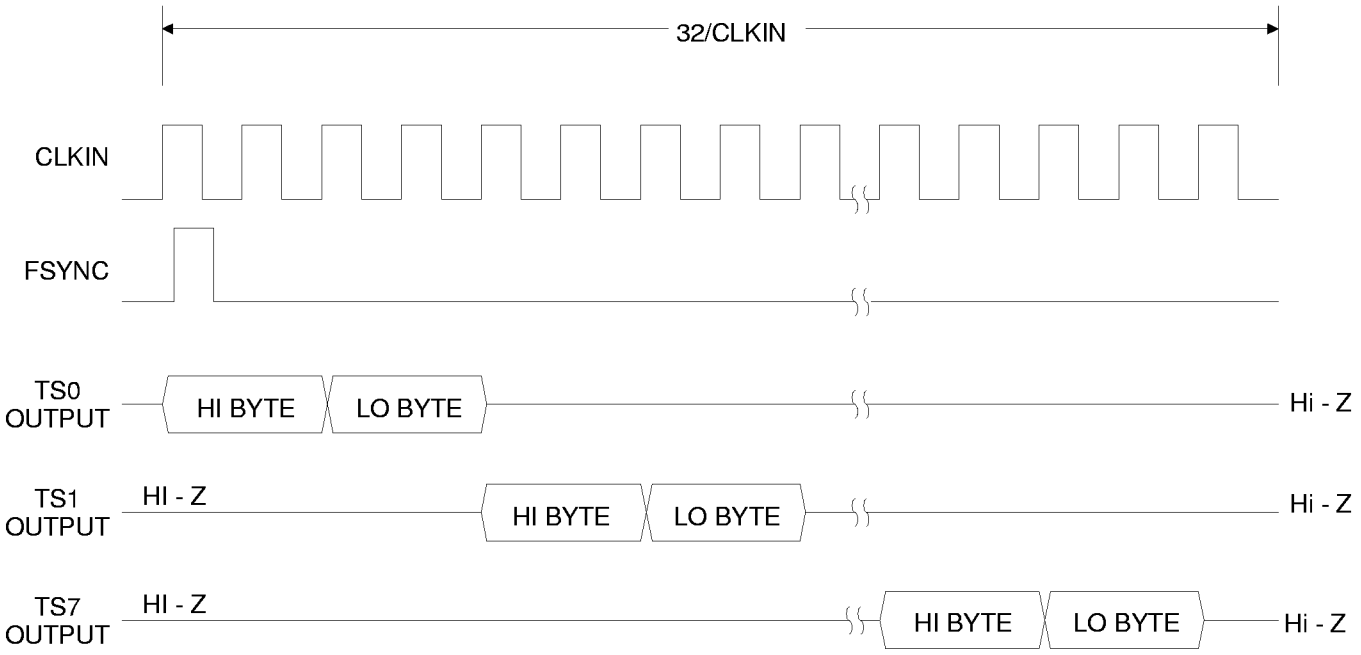
Figure 3. Multiple CS5324 to DSP Interface.

Filter Characteristics

The CS5324 utilizes a fourth-order delta-sigma modulator which has superb linearity. The full capability of the A/D conversion block can be obtained with an appropriate digital filter. Many applications, (seismic applications in particular) require the A/D conversion function to accurately reproduce the pulse shape of the input signal waveform, not just the spectral content. To accurately digitize the shape of the input signal requires a linear phase response in the signal processing system. Any non-linearities in the phase response of the signal processing system will corrupt the true waveshape information. For this reason, the design of the digital filtering to be used with the CS5324 should include particular attention to the phase characteristics of the filter function.

While the on-chip filter is fixed in its characteristics, the off-chip filter will be defined by the system requirements of the particular application. A low pass filter specification to be used with the CS5324 will include the following parameters: Passband ripple (or flatness); group delay or phase characteristics; transition band rolloff; stop band rejection; and filter complexity. All of these parameters are interrelated in any given filter design. There is no one particular solution to be used with the CS5324.

The CS5324 samples the input signal at 256 kHz (CLKIN = 1.024 MHz). With a signal bandwidth of 500 Hz, the output data rate from the A/D system (including the off-chip digital filtering) need only be 1 kHz to adequately represent the input signal. For this reason, it is desirable to decimate the 256 kHz sample rate to 1 kHz. To accomplish this while also providing the necessary low-pass filtering, three stages of filtering are utilized. The first of these is the on-chip filter. This filter is a decimate-by-8 function, and reduces the output word rate from the CS5324 chip to 32 kHz. Two additional filtering stages are to be implemented off-chip with either a DSP, a dedicated ASIC, or another computing device. The first off-chip



Note: Up to eight A/D converters can share the same digital output bus as long as each converter is assigned to put out its data in a different time slot with respect to all other converters on the bus.

Figure 4. Data Output Sequence for Multiple CS5324s.

stage is a decimate-by-8 function, which reduces the output word rate to 4 kHz. The last stage will be a decimate-by-4 function, which will reduce the word rate to 1 kHz. The filter stages are designed so that the first filter has zeroes in its transfer function, such that it rejects the aliased components, due to the first decimate-by-8. The second stage has zeroes such that it rejects the aliased components due to the second decimate-by-8. Neither the on-chip filter, nor the first off-chip stage really affect the passband, but instead, these two stages reduce the output data rate, while at the same time providing anti-alias filtering. The third stage provides the low-pass filtering function.

The CS5324 includes an on-chip 29th-order linear phase FIR (finite-impulse-response) filter and decimator. The response of this filter is illustrated in Figure 5. The filter coefficients are listed in Table 3. The filter performs a fourth-order sinc function, and has a monotonic rolloff in the passband. Attenuation at 500 Hz is 0.0137 dB. The minimum attenuation in the (n x 32 kHz) +/-500 Hz bands is 147 dB. The data output from the on-chip filter has been described in the Data Output and Data Format section above. Data is output at a 32 kHz rate.

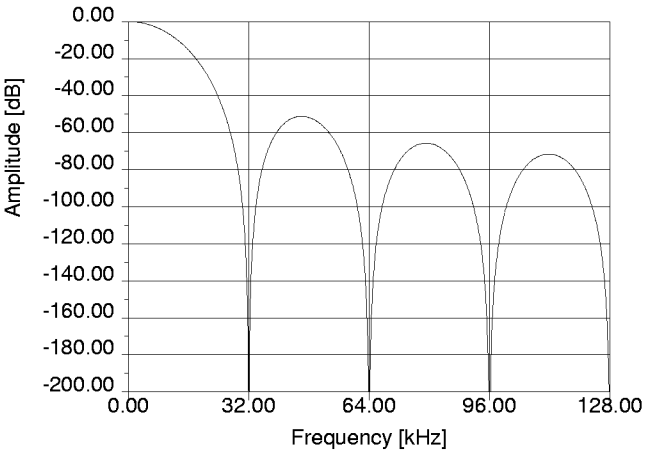


Figure 5. On-chip Filter Response

$$X(z) = \sum_{n=0}^{28} h(n+1)\, z^{-n}$$

Coefficient	Value
h(1) = h(29)	1.00
h(2) = h(28)	4.00
h(3) = h(27)	10.00
h(4) = h(26)	20.00
h(5) = h(25)	35.00
h(6) = h(24)	56.00
h(7) = h(23)	84.00
h(8) = h(22)	120.00
h(9) = h(21)	161.00
h(10) = h(20)	204.00
h(11) = h(19)	246.00
h(12) = h(18)	284.00
h(13) = h(17)	315.00
h(14) = h(16)	336.00
h(15)	344.00

Table 3. On-chip Filter Coefficients

The two proposed off-chip filter stages are as follows: The first off-chip stage is a 43rd-order modified sinc FIR filter. Its coefficients are listed in Appendix 1, along with a plot of its transfer function. Attenuation at 500 Hz (CLKIN = 1.024 MHz) is 1.47 dB. The minimum attenuation in the (n x 4 kHz) +/- 500 Hz bands is 132 dB.

The second off-chip filter stage is a 301st-order FIR filter that performs the necessary low-pass function, with less than 0.00016 dB ripple in the dc-400 Hz band. Attenuation in the region from 500 Hz to 2 kHz is typically greater than 130 dB. The coefficients for the second off-chip filter stage are listed in Appendix 1, along with a plot of its transfer function. An alternate final stage filter is also listed in Appendix 1. It is a 201st-order FIR filter and allows more passband ripple (0.07 dB).

If more ripple or less stop band rejection is acceptable, the off-chip filter complexity can be reduced. The filter examples given have been illustrated only as possible filters which can be utilized with the CS5324 to achieve quality performance from the A/D.

CS5324 Performance

The CS5324 A/D converter is intended for use in seismic and passive sonar applications. These applications require particularly high dynamic range capability. The CS5324 offers high dynamic range without compromising spectral purity. The CS5324 typically achieves 120 dB of dynamic range, while maintaining signal/distortion at 110 dB.

An A/D converter system using the CS5324 A/D converter as its core was tested using Fast Fourier Transform techniques. The CS5324 was connected using the components as shown in the system connection diagram, Figure 1. Data was collected from the CS5324 with the use of a parallel I/O card in a PC-compatible computer. Software was used to implement the two stage digital filtering function. The output from the digital filtering software was submitted to a windowing algorithm and then to the FFT algorithm. Figure 6 illustrates the performance of the CS5324 when tested with a full scale 113 Hz signal. The CS5324 exhibits some second harmonic but no third harmonic. The test frequency of 113 Hz was selected, as this was the center frequency of a bandpass filter, constructed to reject harmonics and line frequencies present at the output of the signal generator. Note that the performance of the CS5324 will generally exceed the capability of most available sine wave test generators for frequencies between 2-500 Hz, as is the case in Figure 6. The excess noise, in this case, is due to the signal source. Figure 7 illustrates the performance of the CS5324 with a -60 dB 100 Hz input signal. The CS5324 is capable of converting with minimal intermodulation distortion as depicted in Figure 8.

Clock Source Considerations

To obtain maximum performance from the CS5324 requires a CLKIN signal which has a low level of clock jitter, i.e., less than 5 picoseconds of jitter. A well-designed crystal-based clock is preferred. The clock oscillator should have a well-regulated supply, with local bypass capacitors at the oscillator. The output from the oscillator should pass through as few logic gates or counter-divider stages as possible, as these can add jitter. Excess clock jitter will reduce the signal/noise performance of the A/D converter.

Power Supply Rejection Ratio

The power supply noise rejection of the CS5324 is frequency dependent. The rejection for frequencies between dc and 500 Hz (CLKIN=1.024 MHz) is nearly constant. Above 500 Hz, the off-chip digital filter will aid in rejecting interference until the frequency of the interference approaches frequencies near CLKIN/21.3 (above 48 kHz for CLKIN=1.024 MHz). Power supply interference above this frequency may cause noise to be modulated into the passband (dc to 500 Hz), degrading the performance of the A/D.

Power Supply Considerations

The system connection diagram, Figure 1, illustrates the recommended power supply arrangements. The CS5324 has two positive analog supply pins and two negative analog supply pins. Multiple pins are used to minimize the possibility of noise coupling on the chip. All six power supply pins should be decoupled to their respective grounds, with a 0.1 uF capacitor located near the device. The digital supplies are decoupled from the analog supplies with 10 ohm resistors to minimize the effects of digital noise in the converter.

The positive digital power supply of the CS5324 must never exceed either positive analog supply by more than a diode drop, or the CS5324 could experience permanent damage. If separate supplies are used for the analog and digital sections of the chip, care must be taken that the analog supply comes up first at power-up. Additionally, the power supplies to the CS5324 should be active before the reference current generator supplies the IREF input current. For proper start-up, the CLKIN signal should be active before IREF is applied. The recommended filter capacitors, which filter the reference currents, will aid

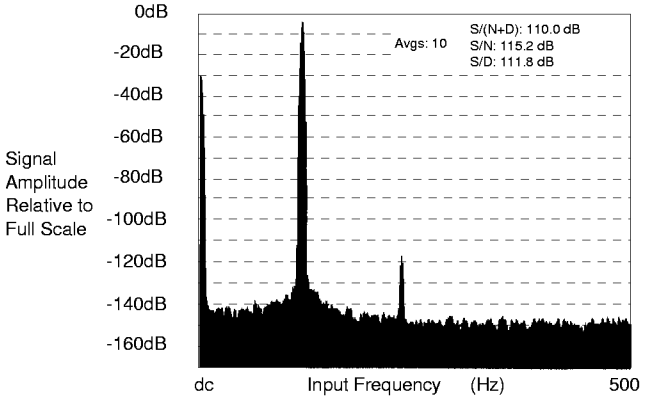


Figure 6. 1024 Point FFT Plot with Full Scale Input, 113 Hz.

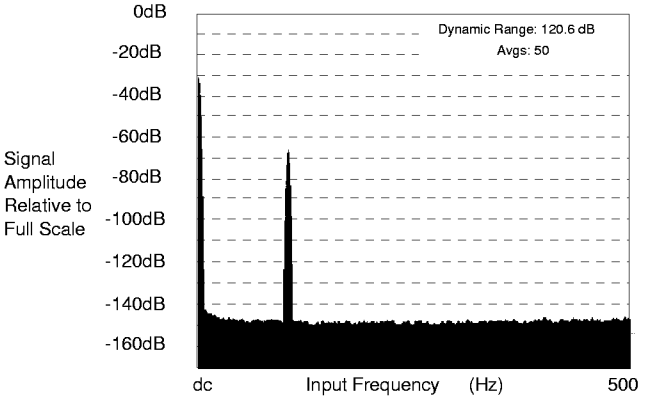
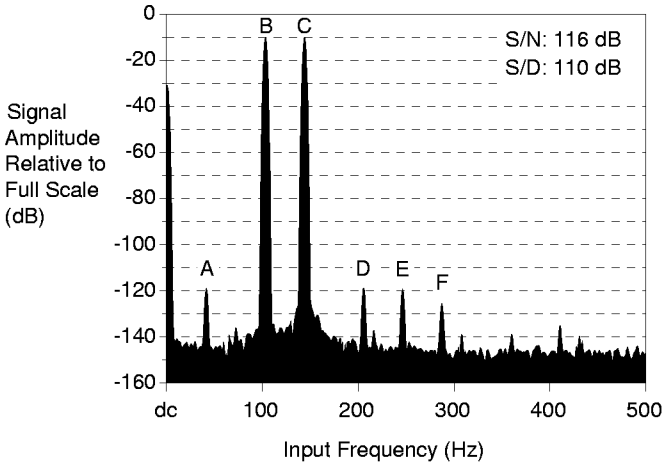


Figure 7. 1024 Point FFT Plot with -60 dB Input, 100 Hz.



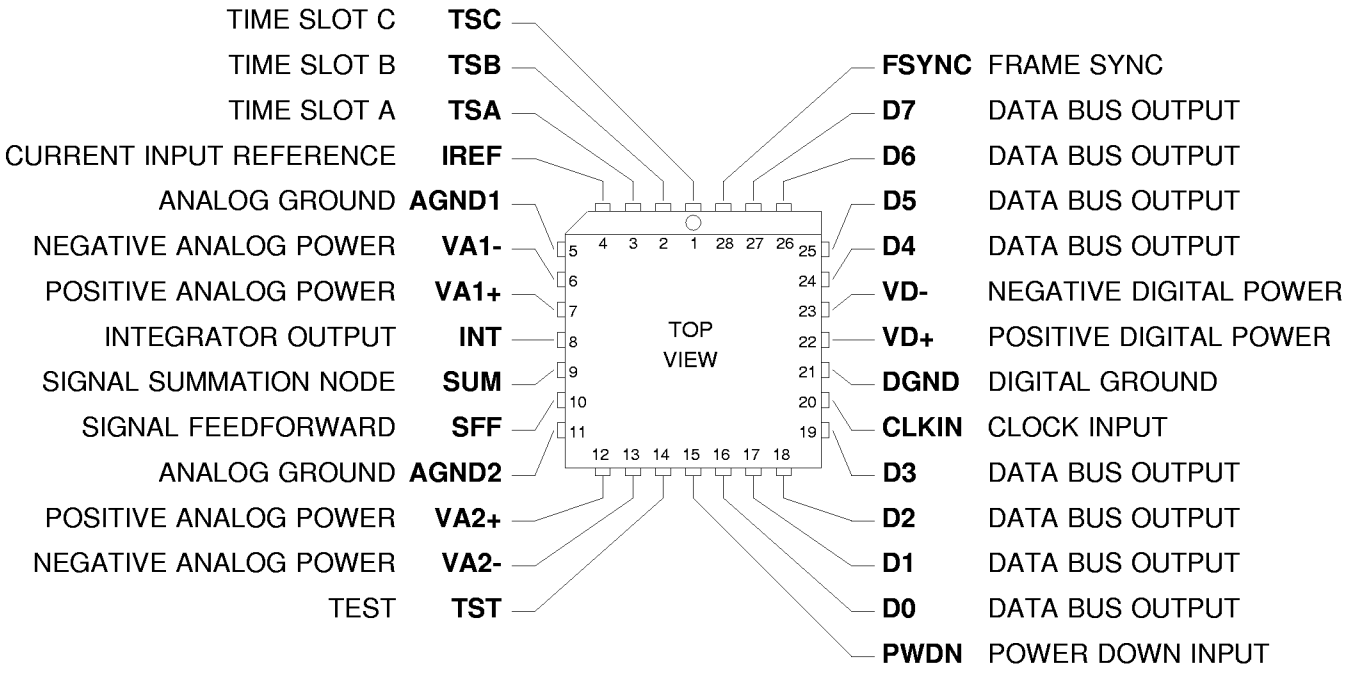
A – 40 Hz Intermodulation Distortion Term
B – 100 Hz Fundamental at 6 dB down
C – 140 Hz Fundamental at 6 dB down
D – 200 Hz Second Order Distortion Term
E – 240 Hz Intermodulation Distortion Term
F – 280 Hz Second Order Distortion Term

Note: S/N noise degradation is due to input signal source.

Figure 8. 1024 Point FFT Plot of Intermodulation Products.

in accomplishing these requirements. Use of good ground plane layout is recommended to achieve maximum performance.

Many seismic or sonar systems are battery powered, and utilize dc-dc converters to generate the necessary supply voltages for the system. To minimize the effects of power supply interference, it is desirable to operate the dc-dc converter at a frequency which is rejected by the digital filtering in the A/D converter. To achieve maximum benefit of the digital filter in the A/D, the dc-dc operating frequency should be located below 48 kHz (see Power Supply Rejection). A synchronous dc-dc converter, whose operating frequency is derived from the 1.024 MHz clock used to drive the CS5324, will minimize the potential for "beat frequencies" appearing in the dc to 500 Hz passband.



PIN DESCRIPTIONS

Power Supplies

VA1+, VA2+ – Positive Analog Power, PINS 7, 12
Positive analog supply voltage. Nominally +5 volts.

VA1-, VA2- – Negative Analog Power, PINS 6, 13
Negative analog supply voltage. Nominally -5 volts.

AGND1, AGND2 – Analog Ground, PINS 5, 11
Analog ground reference.

VD+ – Positive Digital Power, PIN 22
Positive digital supply voltage. Nominally +5 volts.

VD- – Negative Digital Power, PIN 23
Negative digital supply voltage. Nominally -5 volts.

DGND – Digital Ground, PIN 21
Digital ground reference.

Analog Inputs

IREF – Current Input Reference Node, PIN 4

This node accepts a 2 mA reference current to set the signal gain of the A/D converter.

SFF – Signal Feedforward, PIN 10

The input signal is fed forward around the integrator input stage by means of this input pin. This maximizes signal performance.

SUM – Signal Summation node, PIN 9

This is the input integrator virtual ground summing junction. The external integrator input resistor and integrating capacitor are connected to this node, along with a 500 uA bias current network.

INT – Integrator Output, PIN 8

Output pin of the input integrator stage. The external integrating capacitor is connected to this pin for proper operation.

Digital Inputs

CLKIN – Clock Input, PIN 20

A CMOS-compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation of the modulator, digital filter and data output portions of the A/D converter.

PWDN – Power Down Input, PIN 15

When connected to +5 V (VD+) the CS5324 will enter a low-power state. For normal operation this pin should be tied to DGND.

TSA – Time Slot A, PIN 3

See TSC below.

TSB – Time Slot B, PIN 2

See TSC below.

TSC – Time Slot C, PIN1

The TSC input along with TSA and TSB select one of eight possible time periods in which data is output from the CS5324 in a time-multiplexed architecture. Table 2 indicates the decoding of the TSA, TSB, and TSC inputs.

FSYNC – Frame Sync, PIN 28

A transition from a low to high level on this input will re-initialize the CS5324. The digital filter will be initialized and the time-slot counter will be set to zero.

D0 through D7 – Data Bus Outputs, PINS 16-19, 24-27

3-state output pins. Data will be presented out of these pins in the form of two eight-bit bytes during a time slot selected by the TSA, TSB and TSC inputs. The high-order byte with eight data bits will be presented first followed by a second eight-bit byte, which consists of the four low-order data bits, three status bits, and one unused bit.

Miscellaneous

TST – Test, PIN 14

Reserved for production test facility. Should be tied to DGND for normal operation.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full-scale (rms) signal to the broadband noise signal. Broadband noise is measured with the input grounded within the bandwidth of dc to 500 Hz. Units in dB.

Signal-to-Distortion

The ratio of the full-scale (rms) signal to the rms sum of all harmonics up to 500 Hz. Units in dB.

Intermodulation Distortion

The ratio of the rms sum of the two test frequencies (100 and 140 Hz) which are each 6 dB down from full-scale to the rms sum of all intermodulation components within the the bandwidth of dc to 500 Hz. Units in dB.

Full Scale Error

The ratio of the difference between the value of the voltage reference and analog input voltage to the full scale span (two times the voltage reference value). This ratio is calculated after the effects of offset and the external bias components are removed and the analog input voltage is adjusted to yield a code value of 1280 out of the CS5324. Measurement of this parameter uses the circuitry illustrated in the System Connection Diagram. Units in %.

Full Scale Drift

The change in the Full Scale value with temperature. Units in %/°C.

Offset

The difference between the analog ground and the analog voltage necessary to yield an output code from the CS5324 of 00(H). Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in mV.

Offset Drift

The change in the Offset value with temperature. Units in µV/°C.

Appendix 1.

Off-chip Filter Stages

Two stages of off-chip filtering are recommended for use with the CS5324. The first stage is a decimate-by-8 modified-sinc filter with 43 coefficients. Its magnitude response is illustrated in Figure A1.1. Table A1.1 lists its coefficients.

The second filter stage is a 301st-order low-pass filter. Its magnitude plot is illustrated in Figure A1.2 with an expanded view of the passband ripple illustrated in Figure A1.3. Table A1.2 lists the coefficients for this filter.

An alternative second stage filter is also included. It has fewer coefficients, and therefore, is less complex than the previous second stage filter. The magnitude plot of the alternative filter is illustrated in Figure A1.4 with an expanded view of the passband ripple in Figure A1.5. Note that this low-pass function has slightly less out-of-band rejection and somewhat higher passband ripple. The filter coefficients for the alternative final stage are listed in Table A1.3.

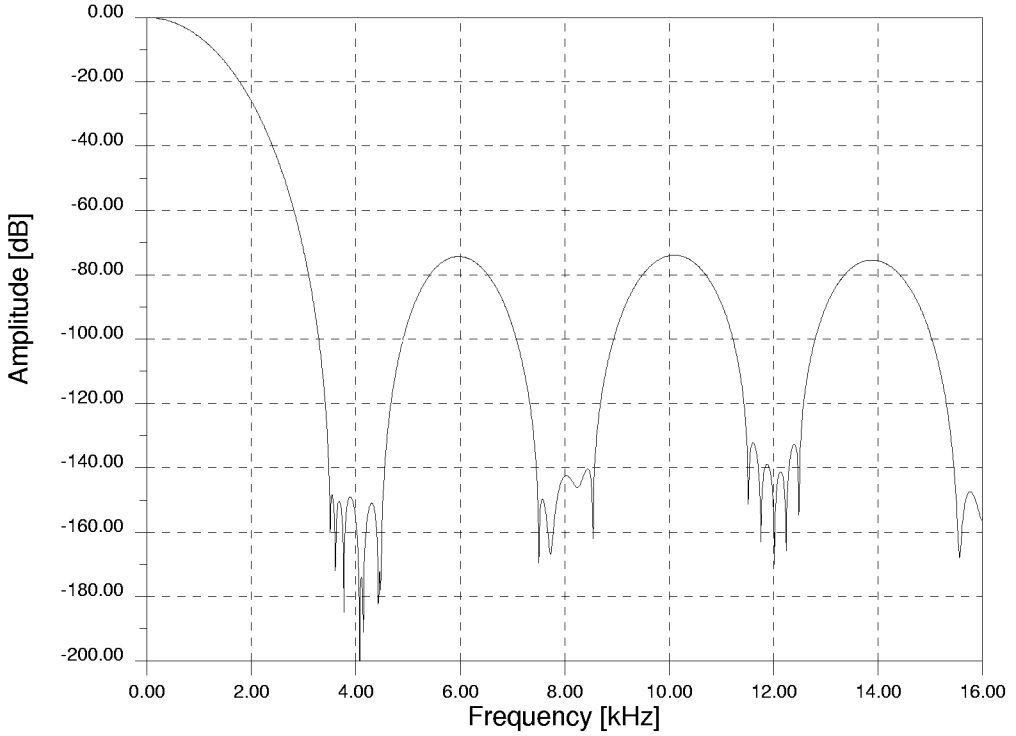


Figure A1.1. First Stage Off-chip Filter – Magnitude Plot

h(1)	= h(43) =	1623	h(12)	= h(32) =	1143595
h(2)	= h(42) =	5137	h(13)	= h(31) =	1494661
h(3)	= h(41) =	12950	h(14)	= h(30) =	1889251
h(4)	= h(40) =	28499	h(15)	= h(29) =	2315005
h(5)	= h(39) =	55210	h(16)	= h(28) =	2752059
h(6)	= h(38) =	99783	h(17)	= h(27) =	3185947
h(7)	= h(37) =	169332	h(18)	= h(26) =	3584677
h(8)	= h(36) =	272838	h(19)	= h(25) =	3926472
h(9)	= h(35) =	414146	h(20)	= h(24) =	4191616
h(10)	= h(34) =	604491	h(21)	= h(23) =	4354400
h(11)	= h(33) =	847470	h(22)	=	4410541

Table A1.1. First Stage Off-chip Filter – 43 Coefficients

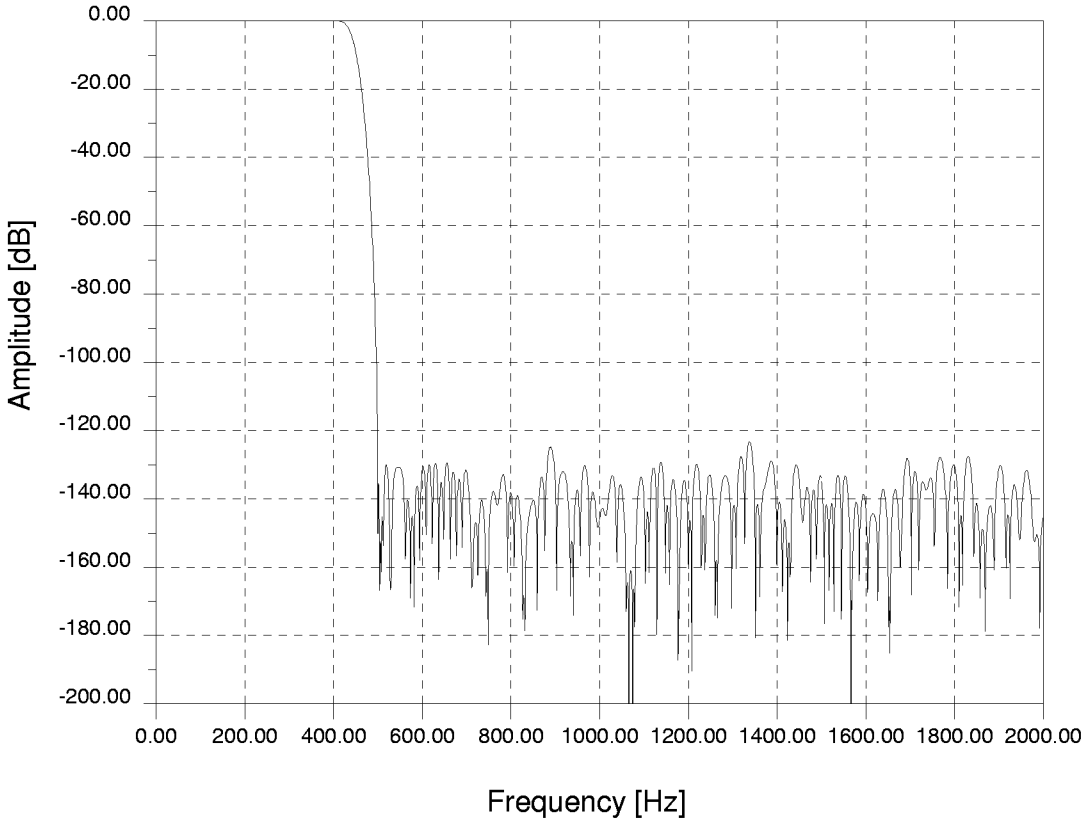


Figure A1.2. Second Stage Off-chip Filter – Magnitude Plot

h(1) = h(301) = 4	h(52) = h(250) = -1711	h(103) = h(199) = 124723
h(2) = h(300) = 6	h(53) = h(249) = -7104	h(104) = h(198) = 145121
h(3) = h(299) = 4	h(54) = h(248) = -9771	h(105) = h(197) = 96333
h(4) = h(298) = -6	h(55) = h(247) = -7963	h(106) = h(196) = -4251
h(5) = h(297) = -28	h(56) = h(246) = -1918	h(107) = h(195) = -112209
h(6) = h(296) = -58	h(57) = h(245) = 5964	h(108) = h(194) = -175323
h(7) = h(295) = -85	h(58) = h(244) = 12013	h(109) = h(193) = -158449
h(8) = h(294) = -93	h(59) = h(243) = 12943	h(110) = h(192) = -62339
h(9) = h(293) = -68	h(60) = h(242) = 7567	h(111) = h(191) = 73359
h(10) = h(292) = -7	h(61) = h(241) = -2315	h(112) = h(190) = 185878
h(11) = h(291) = 75	h(62) = h(240) = -12399	h(113) = h(189) = 217891
h(12) = h(290) = 146	h(63) = h(239) = -17689	h(114) = h(188) = 146090
h(13) = h(289) = 166	h(64) = h(238) = -14905	h(115) = h(187) = -4196
h(14) = h(288) = 108	h(65) = h(237) = -4360	h(116) = h(186) = -166796
h(15) = h(287) = -23	h(66) = h(236) = 9720	h(117) = h(185) = -263179
h(16) = h(286) = -185	h(67) = h(235) = 20798	h(118) = h(184) = -239689
h(17) = h(285) = -302	h(68) = h(234) = 22983	h(119) = h(183) = -96169
h(18) = h(284) = -300	h(69) = h(233) = 14065	h(120) = h(182) = 108776
h(19) = h(283) = -144	h(70) = h(232) = -2922	h(121) = h(181) = 280687
h(20) = h(282) = 130	h(71) = h(231) = -20553	h(122) = h(180) = 331861
h(21) = h(281) = 414	h(72) = h(230) = -30166	h(123) = h(179) = 224879
h(22) = h(280) = 565	h(73) = h(229) = -26027	h(124) = h(178) = -4045
h(23) = h(279) = 467	h(74) = h(228) = -8537	h(125) = h(177) = -255205
h(24) = h(278) = 106	h(75) = h(227) = 15226	h(126) = h(176) = -407467
h(25) = h(277) = -399	h(76) = h(226) = 34244	h(127) = h(175) = -375114
h(26) = h(276) = -826	h(77) = h(225) = 38558	h(128) = h(174) = -153475
h(27) = h(275) = -935	h(78) = h(224) = 24349	h(129) = h(173) = 169870
h(28) = h(274) = -594	h(79) = h(223) = -3468	h(130) = h(172) = 447384
h(29) = h(273) = 127	h(80) = h(222) = -32689	h(131) = h(171) = 536503
h(30) = h(272) = 947	h(81) = h(221) = -49042	h(132) = h(170) = 369619
h(31) = h(271) = 1468	h(82) = h(220) = -43038	h(133) = h(169) = -3865
h(32) = h(270) = 1359	h(83) = h(219) = -15194	h(134) = h(168) = -426733
h(33) = h(269) = 538	h(84) = h(218) = 23126	h(135) = h(167) = -696076
h(34) = h(268) = -725	h(85) = h(217) = 54160	h(136) = h(166) = -655325
h(35) = h(267) = -1882	h(86) = h(216) = 61841	h(137) = h(165) = -276498
h(36) = h(266) = -2320	h(87) = h(215) = 39925	h(138) = h(164) = 307141
h(37) = h(265) = -1673	h(88) = h(214) = -3894	h(139) = h(163) = 839720
h(38) = h(264) = -56	h(89) = h(213) = -50321	h(140) = h(162) = 1044525
h(39) = h(263) = 1898	h(90) = h(212) = -76781	h(141) = h(161) = 751372
h(40) = h(262) = 3264	h(91) = h(211) = -68222	h(142) = h(160) = -3724
h(41) = h(261) = 3239	h(92) = h(210) = -25304	h(143) = h(159) = -953887
h(42) = h(260) = 1580	h(93) = h(209) = 34332	h(144) = h(158) = -1671933
h(43) = h(259) = -1168	h(94) = h(208) = 83049	h(145) = h(157) = -1718209
h(44) = h(258) = -3814	h(95) = h(207) = 95832	h(146) = h(156) = -813868
h(45) = h(257) = -5004	h(96) = h(206) = 62860	h(147) = h(155) = 1027355
h(46) = h(256) = -3886	h(97) = h(205) = -4158	h(148) = h(154) = 3464481
h(47) = h(255) = -631	h(98) = h(204) = -75642	h(149) = h(153) = 5912858
h(48) = h(254) = 3478	h(99) = h(203) = -116939	h(150) = h(152) = 7722306
h(49) = h(253) = 6517	h(100) = h(202) = -104877	h(151) = h(151) = 8388608
h(50) = h(252) = 6784	h(101) = h(201) = -40254	
h(51) = h(251) = 3702	h(102) = h(200) = 50253	

Table A1.2. Second Stage Off-chip Filter – 301 Coefficients

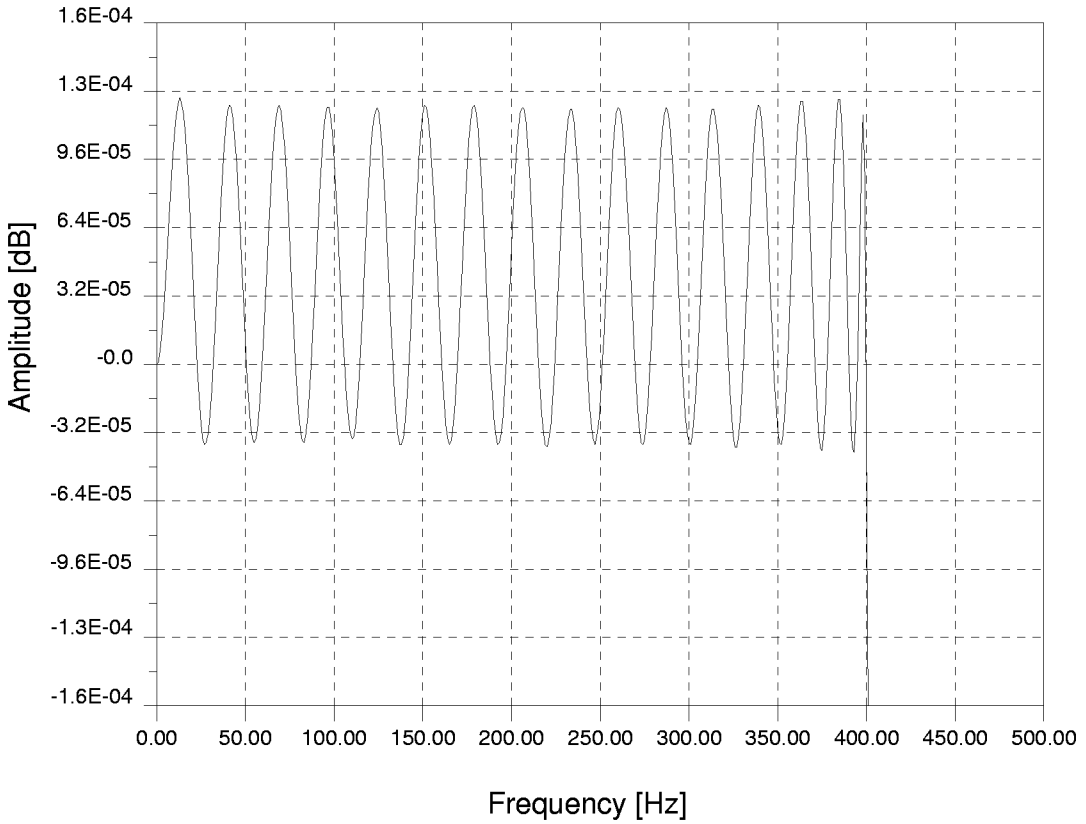


Figure A 1.3. Second Stage Off-chip Filter – Passband Ripple Plot

h(1) = h(201) = -68	h(35) = h(167) = 24059	h(69) = h(133) = 64893
h(2) = h(200) = -266	h(36) = h(166) = -1482	h(70) = h(132) = 229769
h(3) = h(199) = -681	h(37) = h(165) = -29822	h(71) = h(131) = 305309
h(4) = h(198) = -1350	h(38) = h(164) = -48300	h(72) = h(130) = 245984
h(5) = h(197) = -2192	h(39) = h(163) = -47054	h(73) = h(129) = 64260
h(6) = h(196) = -2938	h(40) = h(162) = -24000	h(74) = h(128) = -168625
h(7) = h(195) = -3124	h(41) = h(161) = 13122	h(75) = h(127) = -349221
h(8) = h(194) = -2181	h(42) = h(160) = 49003	h(76) = h(126) = -386474
h(9) = h(193) = 366	h(43) = h(159) = 66874	h(77) = h(125) = -245727
h(10) = h(192) = 4634	h(44) = h(158) = 56133	h(78) = h(124) = 28395
h(11) = h(191) = 10142	h(45) = h(157) = 18103	h(79) = h(123) = 323264
h(12) = h(190) = 15743	h(46) = h(156) = -33025	h(80) = h(122) = 502448
h(13) = h(189) = 19809	h(47) = h(155) = -75161	h(81) = h(121) = 466350
h(14) = h(188) = 20712	h(48) = h(154) = -87623	h(82) = h(120) = 203318
h(15) = h(187) = 17462	h(49) = h(153) = -60982	h(83) = h(119) = -193406
h(16) = h(186) = 10292	h(50) = h(152) = -2877	h(84) = h(118) = -554902
h(17) = h(185) = 889	h(51) = h(151) = 63451	h(85) = h(117) = -704448
h(18) = h(184) = -7915	h(52) = h(150) = 108121	h(86) = h(116) = -538246
h(19) = h(183) = -13029	h(53) = h(149) = 107776	h(87) = h(115) = -84243
h(20) = h(182) = -12292	h(54) = h(148) = 57300	h(88) = h(114) = 490248
h(21) = h(181) = -5542	h(55) = h(147) = -25620	h(89) = h(113) = 932553
h(22) = h(180) = 4957	h(56) = h(146) = -106083	h(90) = h(112) = 1005109
h(23) = h(179) = 15066	h(57) = h(145) = -146288	h(91) = h(111) = 595458
h(24) = h(178) = 20225	h(58) = h(144) = -122895	h(92) = h(110) = -209660
h(25) = h(177) = 17383	h(59) = h(143) = -39611	h(93) = h(109) = -1121850
h(26) = h(176) = 6584	h(60) = h(142) = 71441	h(94) = h(108) = -1730461
h(27) = h(175) = -8560	h(61) = h(141) = 161525	h(95) = h(107) = -1642084
h(28) = h(174) = -21921	h(62) = h(140) = 186220	h(96) = h(106) = -632318
h(29) = h(173) = -27236	h(63) = h(139) = 126698	h(97) = h(105) = 1247052
h(30) = h(172) = -20930	h(64) = h(138) = 1412	h(98) = h(104) = 3649798
h(31) = h(171) = -4177	h(65) = h(137) = -138356	h(99) = h(103) = 6019586
h(32) = h(170) = 16903	h(66) = h(136) = -228840	h(100) = h(102) = 7753188
h(33) = h(169) = 33304	h(67) = h(135) = -222225	h(101) = h(101) = 8388608
h(34) = h(168) = 36843	h(68) = h(134) = -110815	

Table A 1.3. Alternate Second Stage Off-chip Filter – 201 Coefficients

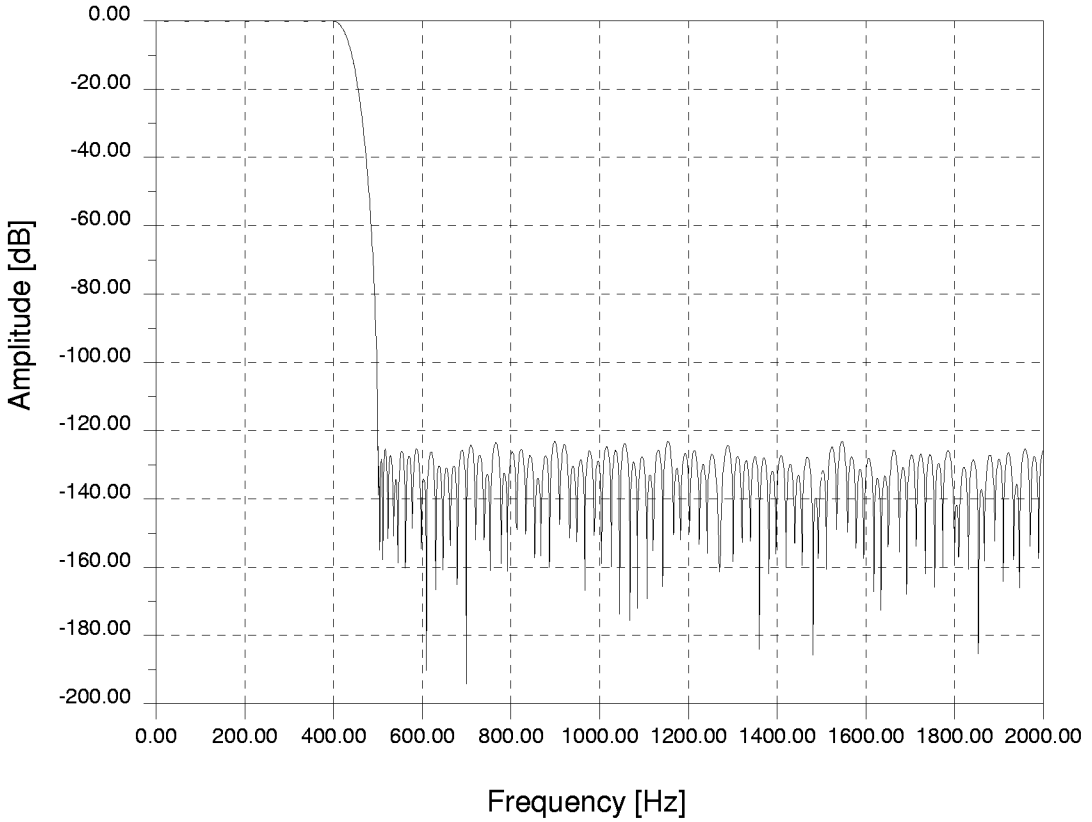


Figure A 1.4 Alternate Second Stage Off-chip Filter – Magnitude Plot

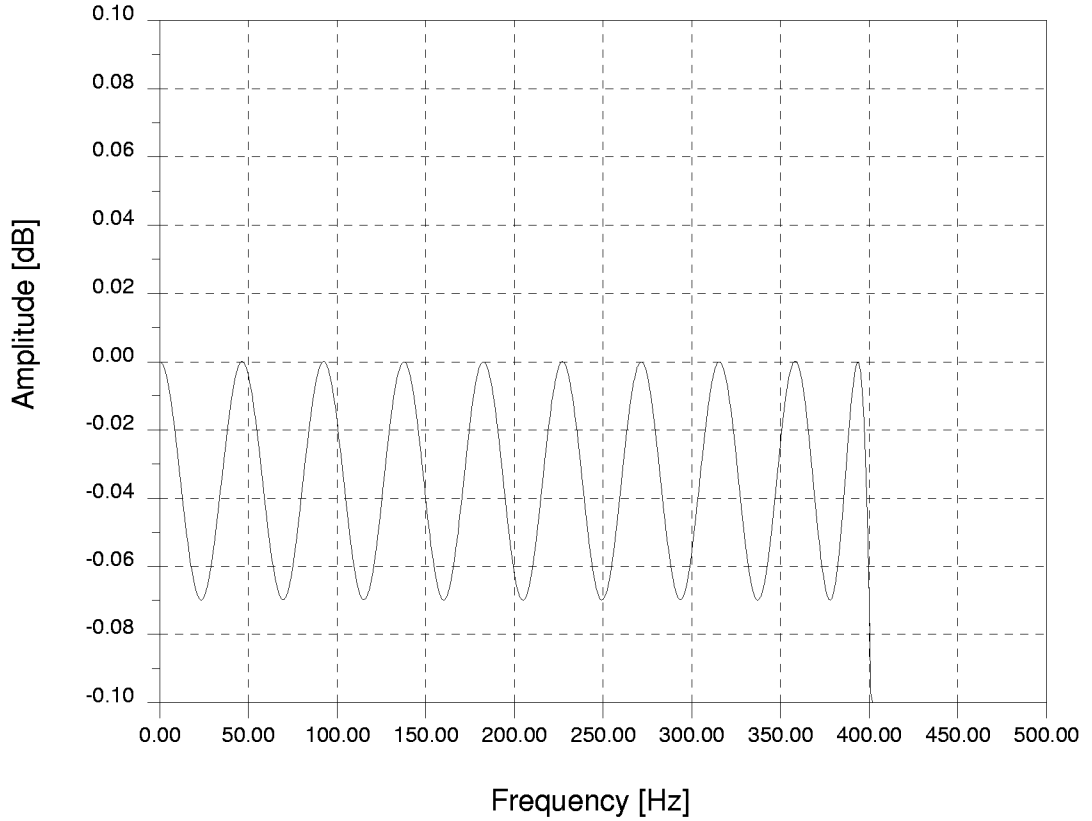


Figure A1.5 Alternate Second Stage Off-chip Filter – Passband Ripple Plot

CRYSTAL
A DIVISION OF CIRRUS LOGIC

CDB5324

Evaluation Board for CS5324

Features

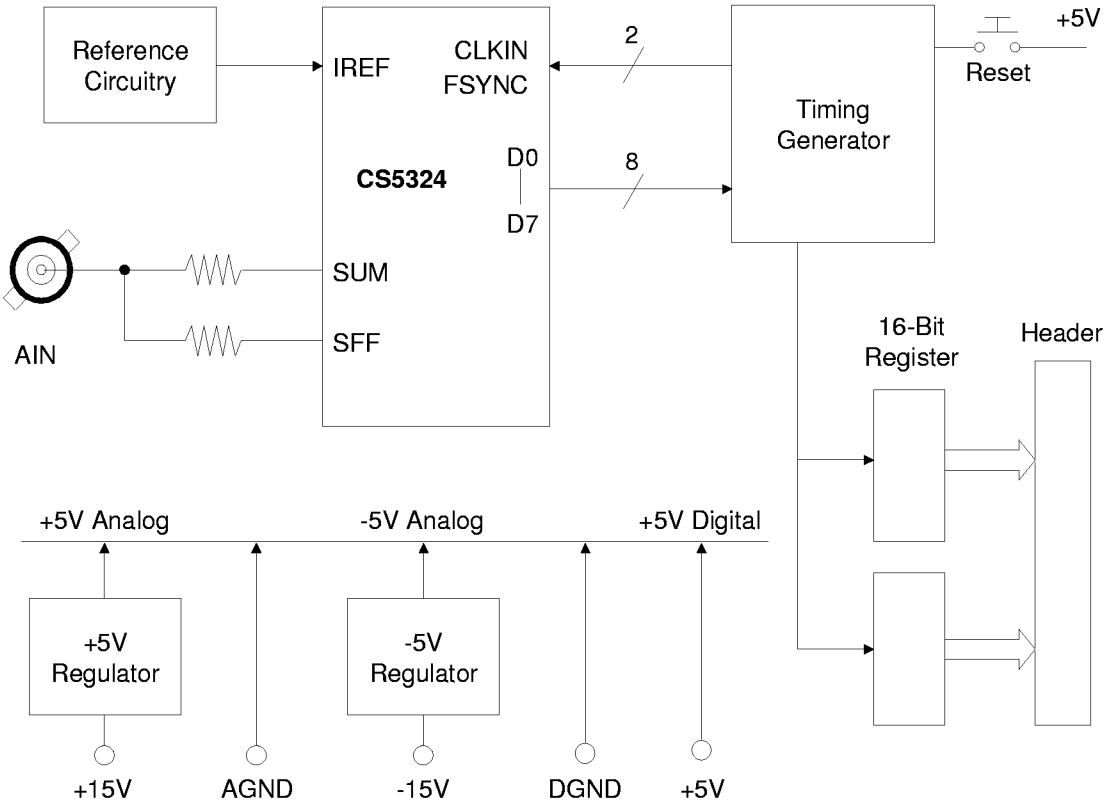
- PC/µP-compatible Header Connection
  - 16 Bit Parallel Data
  - Three-State Output
  - Data Ready Signal
- Analog/Digital Patch Areas
- Analog BNC Input Connector

Description

The CDB5324 is an evaluation board that allows the laboratory characterization of the CS5324 A/D converter. The CS5324 is a 120 dB dynamic range, 500 Hz bandwidth ADC intended for seismic applications. The board supports ±10 volt analog input signals and generates the timing signals which format the output data from the CS5324 into a single 16-bit parallel word.

ORDERING INFORMATION

CDB5324 Evaluation Board



Cirrus Logic, Inc.
Crystal Semiconductor Products Division
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com

Power Supplies and Voltage Reference

The CDB5324 evaluation board requires three separate input voltages for proper operation. Figure 1 illustrates the power supply connections. The required power supply input voltages consist of +5V, +15V, and -15V. The +5V input supplies power to the digital logic portion of the board. The +15V and -15V inputs are regulated down to provide the +5V and -5V supplies necessary for the CS5324. Also included in Figure 1 is a start-up circuit which allows a power-down signal to turn off both the CS5324 and the supply current to the LTC1021 voltage reference. An RC delay is added as part of the start-up circuitry to insure the the +5V digital supply is present before the LTC1021 voltage reference is turned on. The FSYNC and CLKIN signals to the CS5324 must

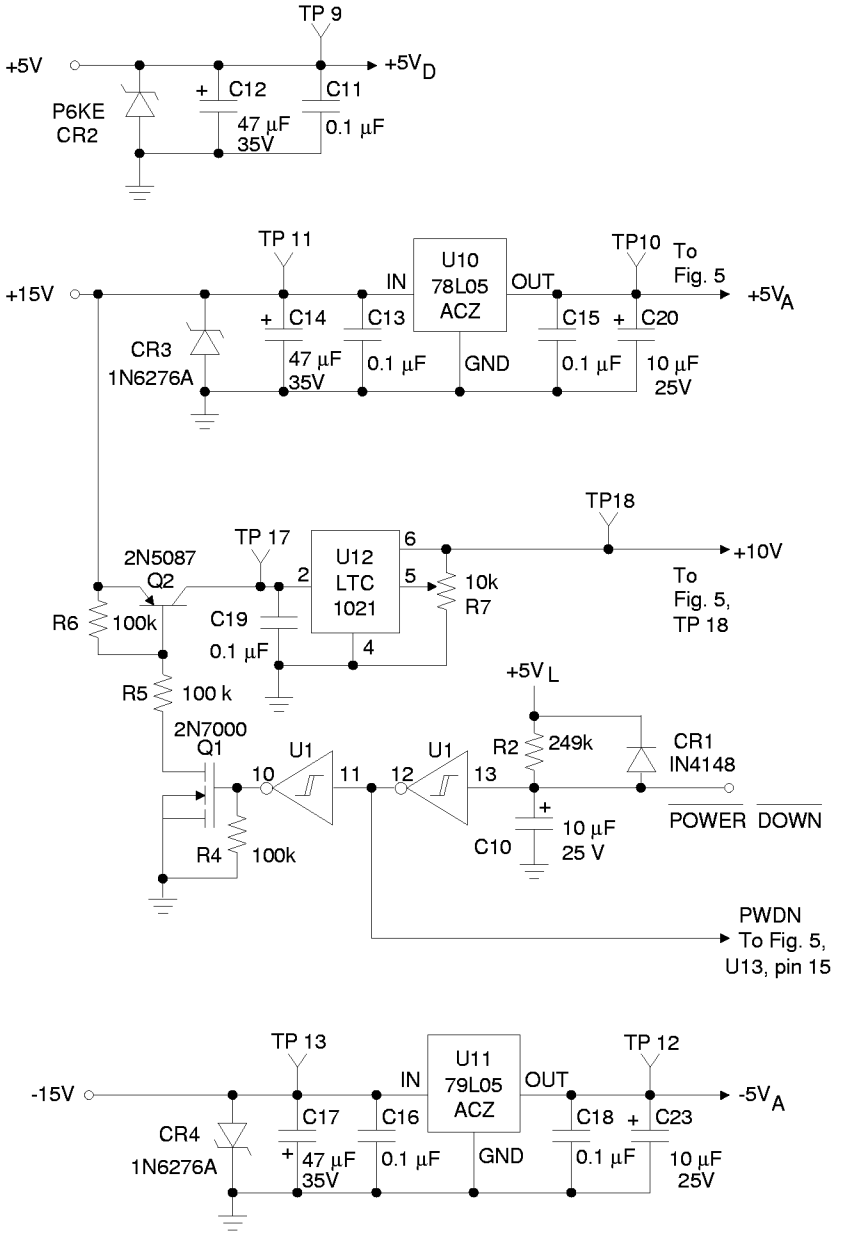


Figure 1. Voltage Regulators and +10V Reference

be furnished by the digital logic whenever the voltage reference is turned on to insure proper start-up of the device. This start-up circuitry is provided on the evaluation board to insure proper start-up of the CS5324 while using separate laboratory supplies which may then be turned on in any sequence. This circuitry is not required if all of the supplies are activated at the same time.

Clock Oscillator/Divider

Figure 2 illustrates the oscillator and clock divider circuitry used to generate the 1 MHz clock for the CS5324 A/D converter. This circuitry is in the digital patch area of the circuit card. The 1 MHz clock to the CS5324 must have low jitter. Jitter on the clock of any high resolution A/D converter

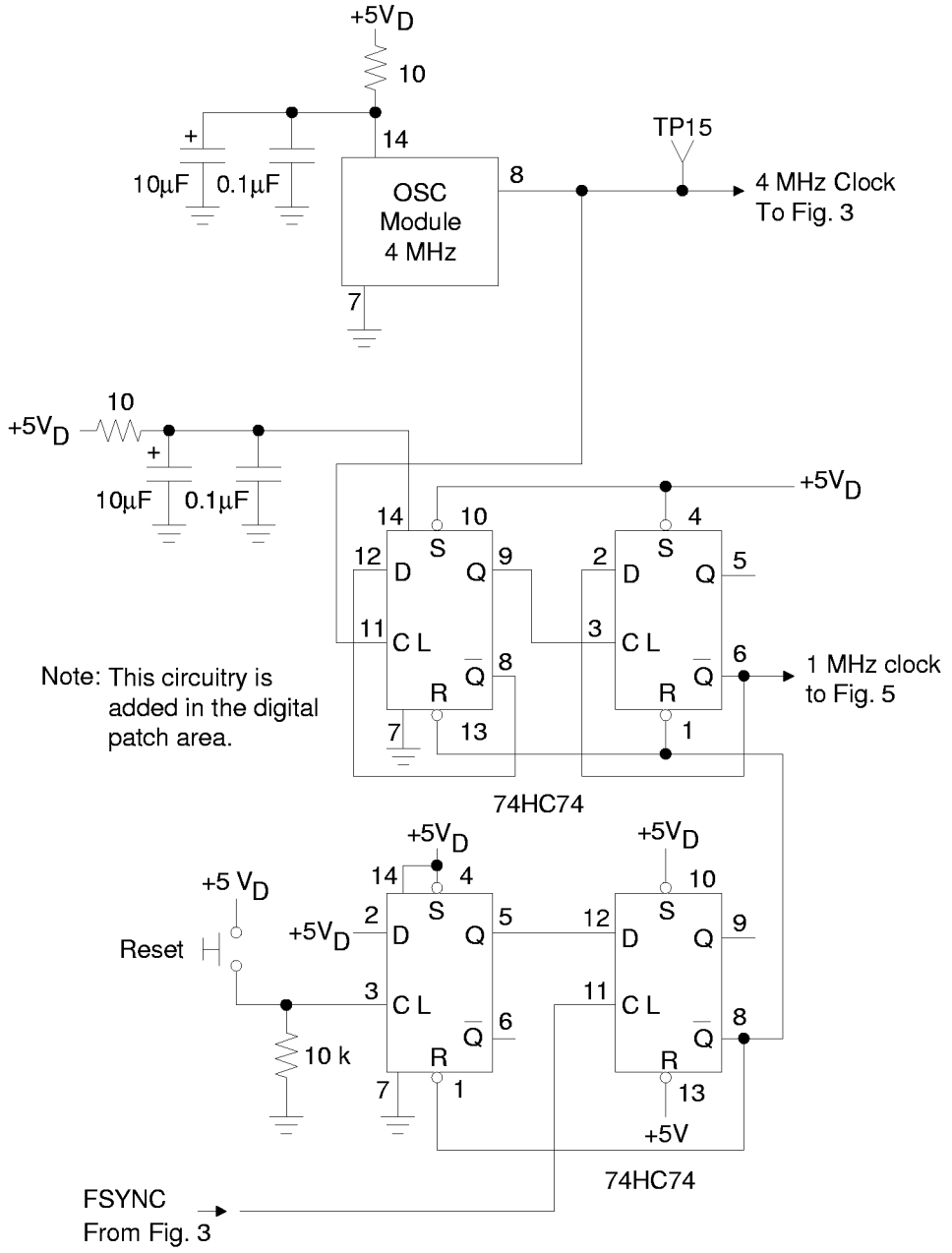


Figure 2. Clock Oscillator/Divider

will reduce the signal-to-noise capability of the device.

Note that both the oscillator and the dual D flip-flop used to divide the oscillator output are individually decoupled from the +5V logic supply. The second dual D flip-flop pair are used to synchronize the 1 MHz from the dual D divider to be in phase with the 1 MHz out of the 74HC590 counter. This synchronization is necessary to insure that the other timing signals derived from the 74HC590 outputs have the proper phase relationship to the 1 MHz clock in the CS5324.

Reset

To insure synchronization of the 1 MHz clock to the CS5324 with the other clock signals in the system, the reset button in the digital patch area of the board must be activated after power is applied to the system.

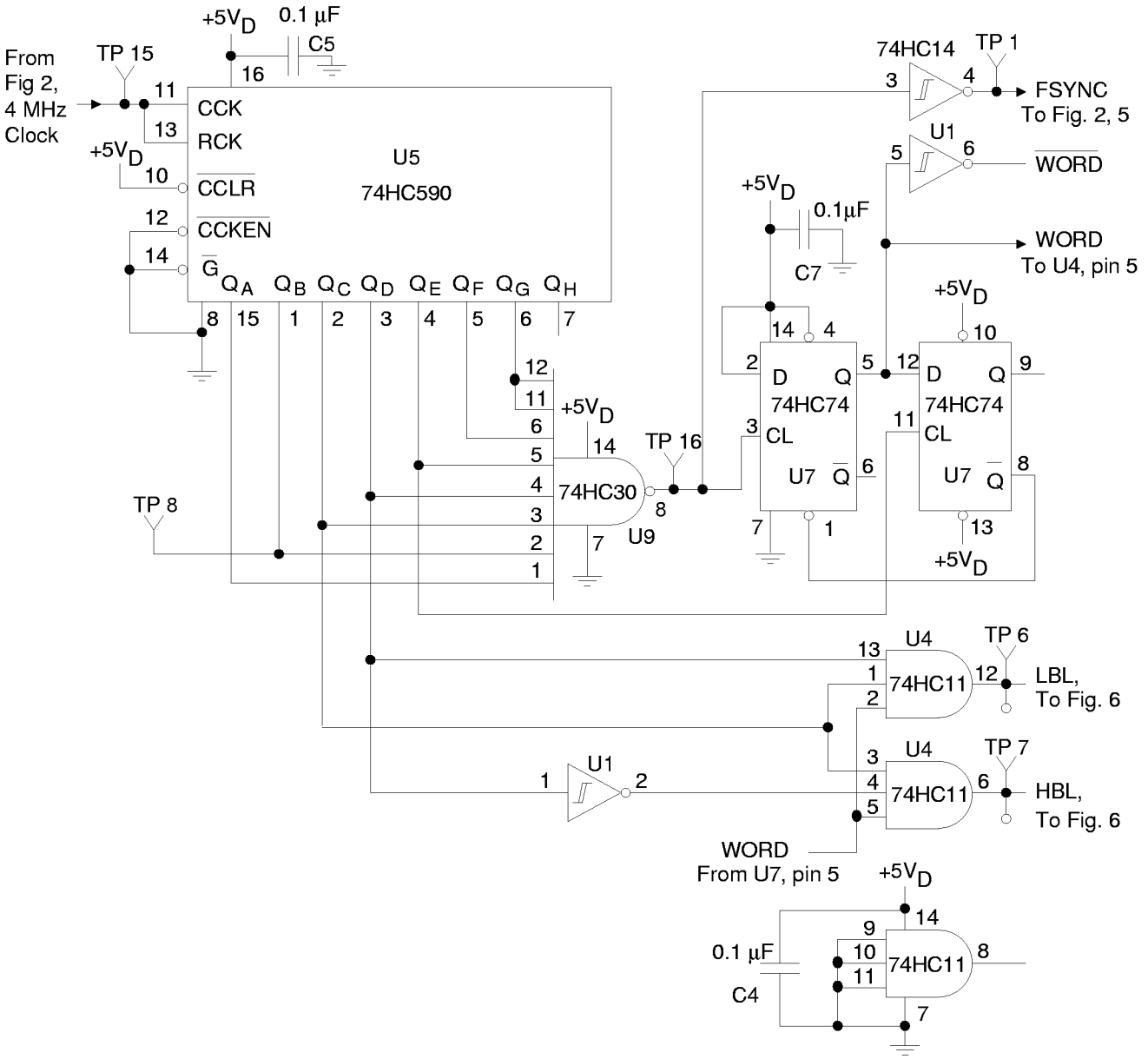


Figure 3. Timing Generator

Timing Generator

Figure 3 illustrates the logic circuitry which generates the timing signals used to latch the data coming out of the CS5324 A/D converter. The outputs from the 74HC590 counter are used to generate FSYNC, HBL (High Byte Latch), LBL (Low Byte Latch), and WORD. Figure 4 illustrates the timing relationships of these signals.

CS5324 A/D Converter

The connections to the CS5324 chip are illustrated in Figure 5. The analog and digital supply voltages are all decoupled close to the device. Included in the schematic are the discrete components used to develop the reference current and signal current inputs to the device. The AIN BNC is the signal input to the evaluation board. The input range is set for 20 volts p-p. Data from the CS5324 is output as two 8-bit bytes. These two bytes are latched into the output registers of Figure 6.

Output Registers/Header Connector

Data from the CS5324 A/D converter is latched into the two 74HC574 octal flip-flops by the HBL and LBL latch signals generated by the timing generator. The outputs of the 74HC574's are then connected to the 40-pin header Connector. Figure 7 identifies the pins on the 40-pin header.

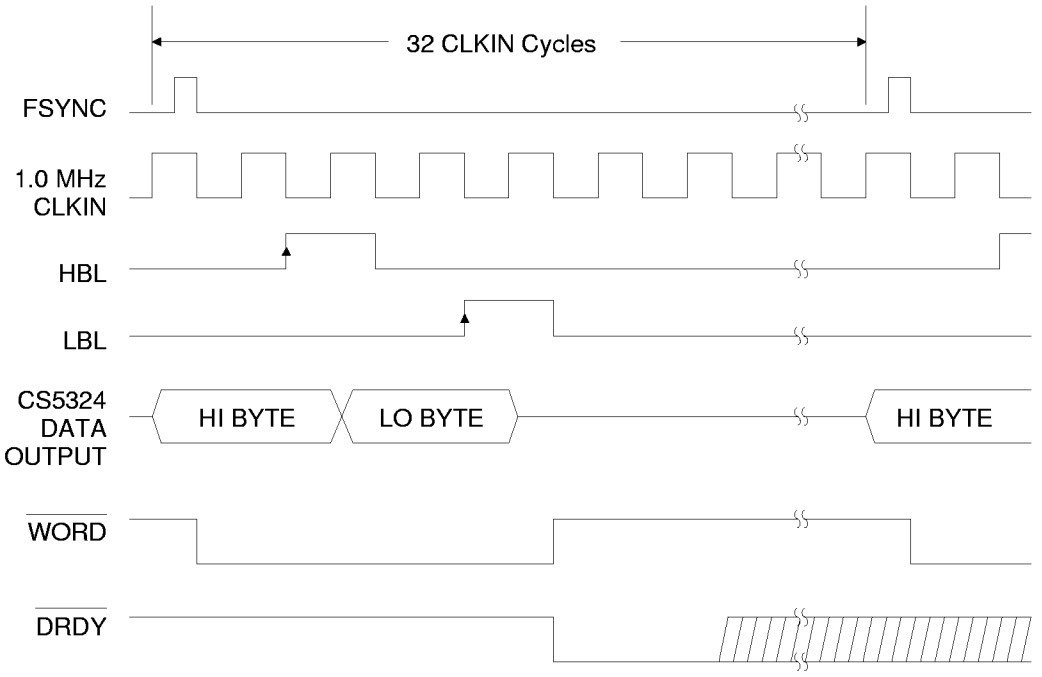


Figure 4. Timing Diagram

Note that each of the data output pins is adjacent to a ground pin on the header. In constructing a cable for interfacing to the evaluation board, twisted-pair ribbon cable (Beldon Vari-Twist 9V28040 or equivalent) should be used. Each twisted pair should include a ground line with the data signal as this minimizes radiated noise.

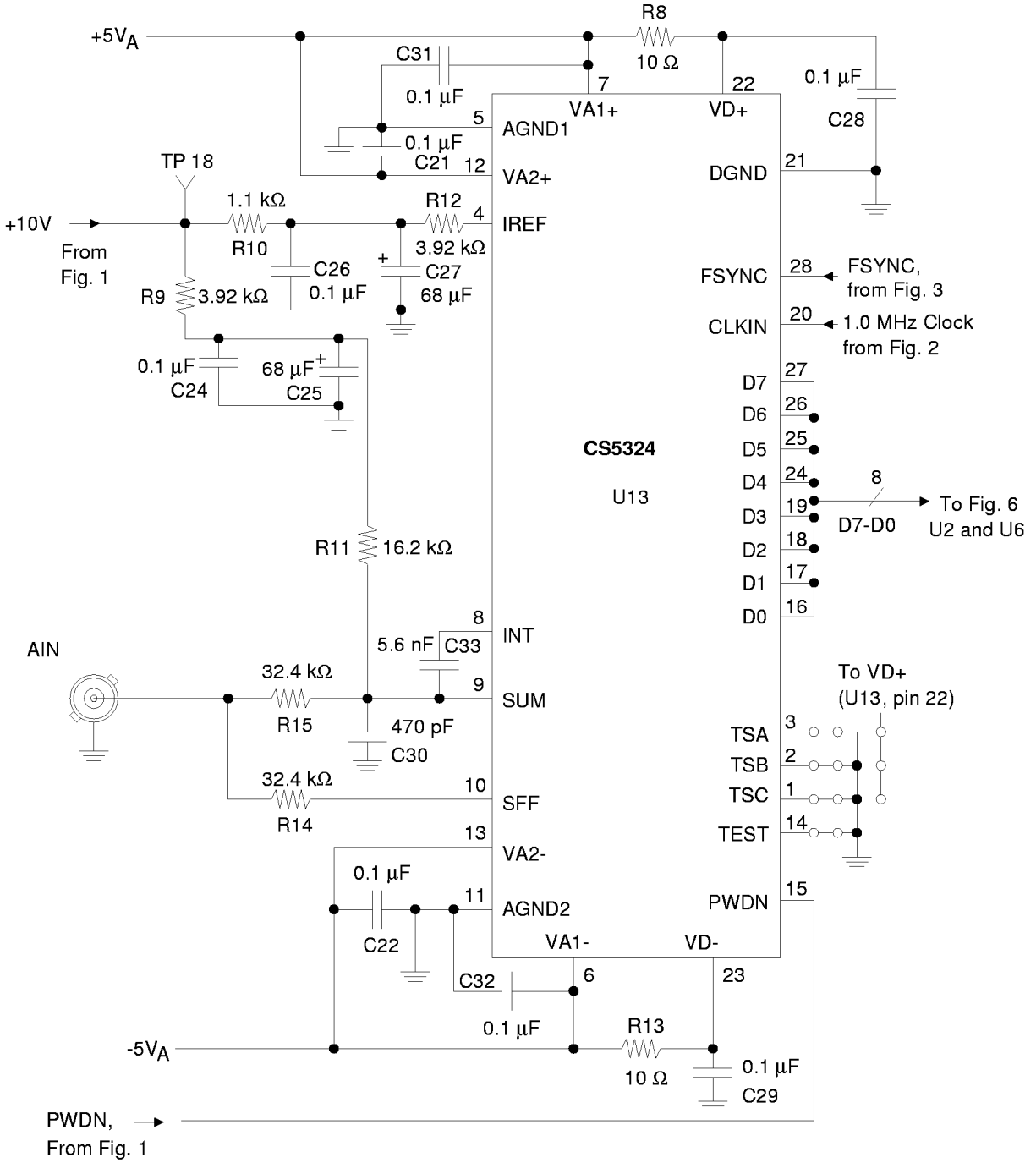


Figure 5. CS5324 A/D Converter

Using the Evaluation Board

Connect the appropriate power supply voltages to the binding posts of the board. Twist the +5V digital supply lead with the digital ground lead from the board to the supply. Also twist the supply leads for the analog voltages. Use a high quality power supply which is low in noise and line frequency (50/60 Hz) interference.

Connect a coaxial cable from the analog BNC to the signal source. Note that the performance of the A/D converter will exceed the capability of

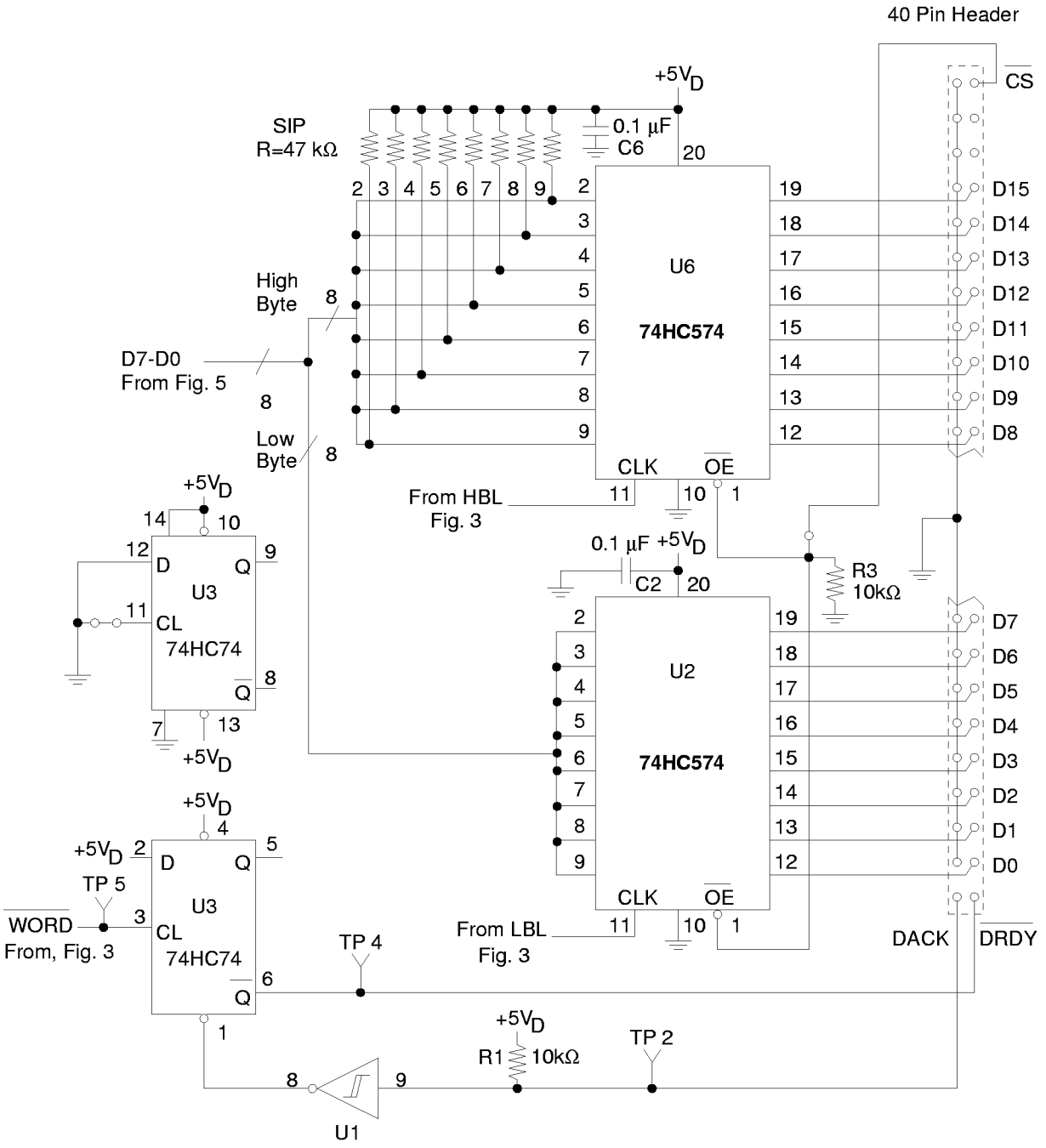


Figure 6. Output Registers/Header Connector

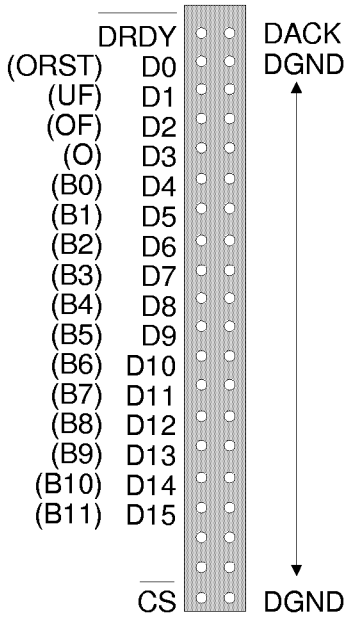


Figure 7. Header Pin Identification

most signal generators, especially with respect to noise and line frequency interference.

Power-up the evaluation board and activate the reset button (located in the digital patch area). The ribbon cable to the 40-pin header should remain disconnected until after power is applied to the board. This is a requirement only if power can be sourced from the data collection equipment to the evaluation board. (In the event that current is sourced through the ribbon cable into the evaluation board, and then power is applied, the evaluation board circuitry may not start-up properly).

Data from the evaluation board must be processed using digital filter functions, such as those found in the Appendix of the CS5324 data sheet to achieve the full 120 dB dynamic range of the A/D.

Evaluation Board Performance

To evaluate the performance of the evaluation board will require a quality signal source. A Khron-Hite 4400A low distortion oscillator can be used if an additional narrowband filter is used to filter out the line frequency interference and broadband noise which is part of the oscillator signal. Note that when using the Khron-Hite oscillator with a 60 Hz line frequency, interference components at 60, 120, 180 and 240 Hz show up as well as the oscillator fundamental. These interference components are generally 105 to 115 dB below full scale and will therefore show up in an FFT plot of the A/D's performance.

With a pure signal source provided to the AIN BNC input, output words are collected and filtered. The resulting data is then windowed and submitted to the FFT algorithm. The results can then be plotted. Performance plots for the CS5324 can be found in the CS5324 data sheet.

Component Layout

Figure 8 illustrates the component layout of the CDB5324 evaluation board. Note that this layout does not include the components added in the digital patch area. The components in the digital patch area are indicated in schematic diagram of Figure 2.

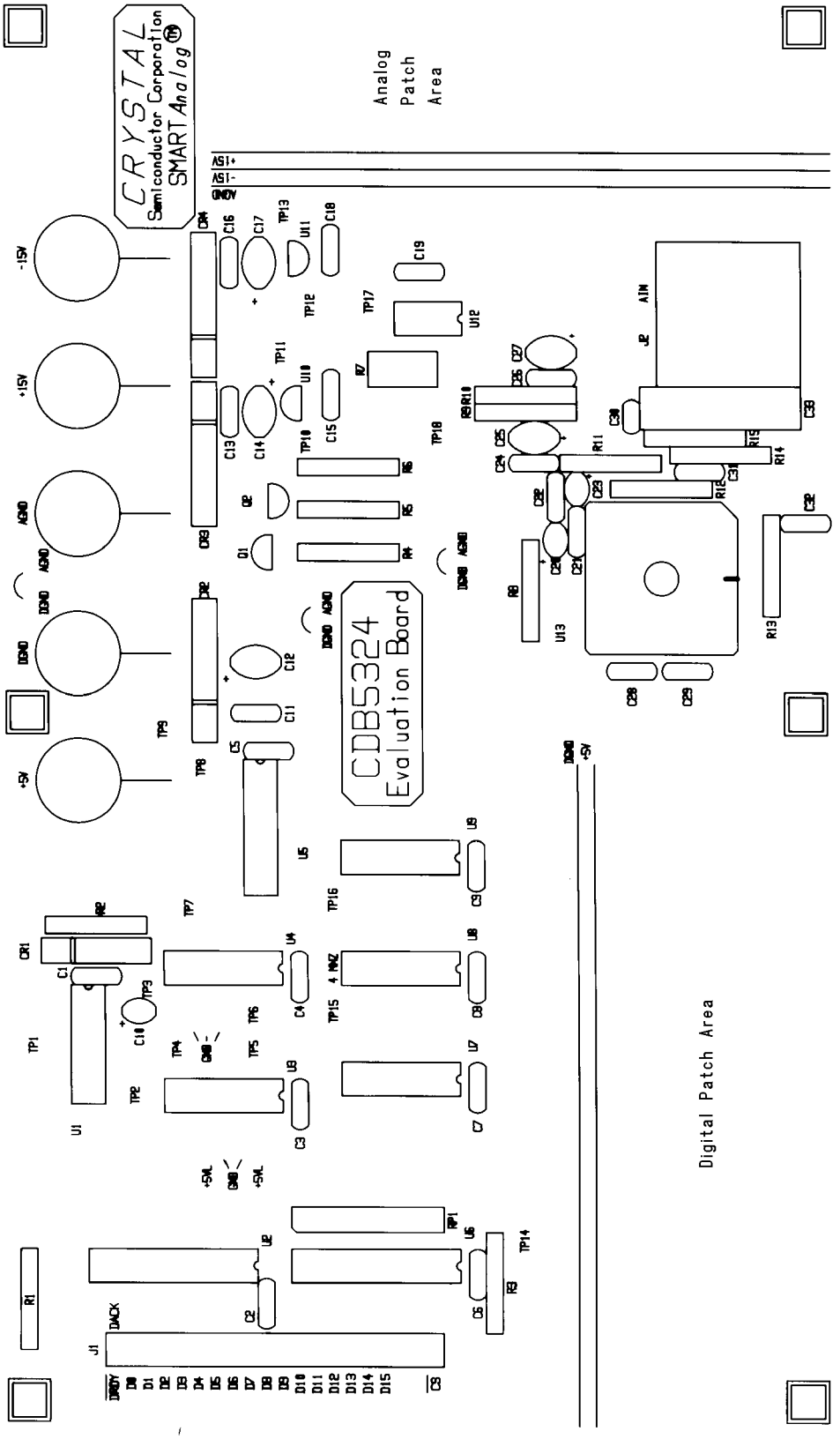


Figure 8. CDB5324 Component Layout