User's Guide

TPS51220A Buck Controller Evaluation Module User's Guide

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1 Introduction

This EVM utilizes Texas Instrument's TPS51220A in a dual output design. The device includes many test points to help the engineer monitor and evaluate the control characteristics of the TPS51220A. The TPS51220A is a dual peak current mode synchronous buck controller with three linear regulators. The EVM also allows the engineer to configure several of the features of the TPS51220A controller.

2 Description

The TPS51220A EVM-476 provides two 8-A outputs: 3.3 V and 5 V. It accepts an input voltage from 8 V to 20 V. Several jumpers and switches allow the user to evaluate various control functions of the TPS51220A. Switches provide an easy method to enable and disable the EVM or each of the two outputs independently. Two jumper blocks allow the user to select the mode of operation of each output. One jumper block allows the engineer to select the control architecture and OVP function. One block allows for selection of overcurrent trip level and if the output is discharged by the converter. See the following sections for more details.

2.1 Typical Applications

- Notebook computers and I/O bus
- Point-of-load in such applications as digital TV and multi-function printers

2.2 Features

- Input range from 8 V to 20 V
- Dual 8-A outputs: 3.3 V and 5 V
- Individual enable function for 3.3-V and 5-V output
- Selectable light load operation
- Selectable control architecture
- Inductor current sensing
- OVP disable function
- Output discharge disable function
- Test points for easy access to measure key parameters

3 Electrical Performance Specifications

Table 3-1. TPS51220A EVM-476 Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Voltage range		8	12	20	V
Maximum input current	12 V_{IN}, both outputs at 8 A		5.8		A
Output Characteristics					
Output voltage, VOUT 1			5		V
Output load current, IOUT1		0		8	A
Output voltage regulation	Line regulation: input voltage = 8 V to 20 V		±0.5%		
	Load regulation: output current = 0 A to 8 A		±1%		
Output voltage ripple	At IOUT1 = 8 A			50	mVpp
Output over current			12		A
Switching frequency			330		kHz
Peak efficiency			97.8%		
Full load efficiency			96.9%		
Output voltage, VOUT 2			3.3		V
Output load current, IOUT2		0		8	A
Output voltage regulation	Line regulation: input voltage = 8 V to 20 V		±0.5%		
	Load regulation: output current = 0 A to 8 A		±1%		
Output voltage ripple	At IOUT = 8 A			50	mVpp
Output over current			12		A
Switching frequency			330		kHz

Table 3-1. TPS51220A EVM-476 Electrical Performance Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Peak efficiency			96%		
Full load efficiency			95%		

4 Schematic

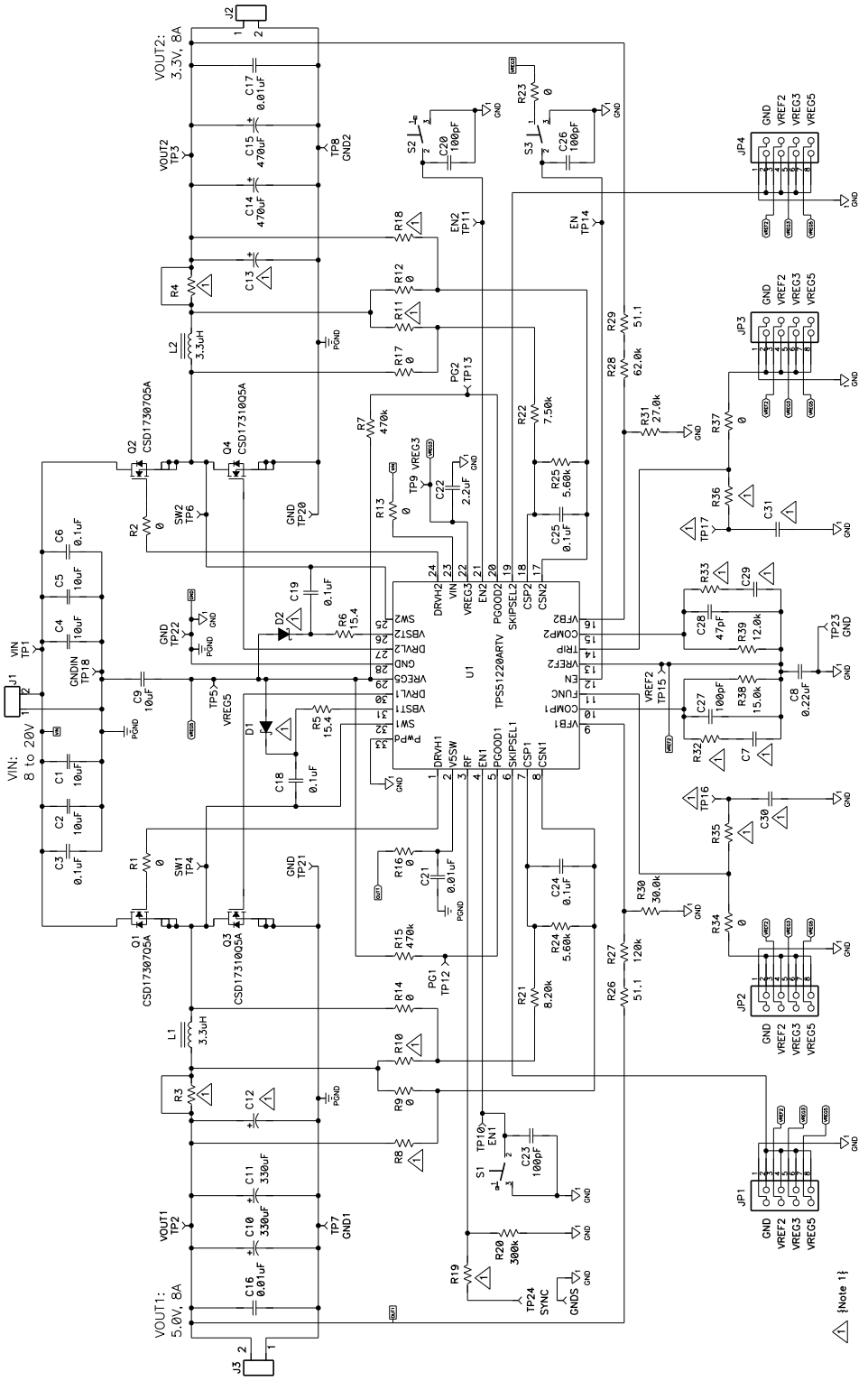

Figure 4-1. TPS51220A EVM-476 Schematic

5 Test Setup

5.1 Test Equipment

Voltage Source: The power source must be capable of supplying 8 VDC to 20 VDC at up to 10 A.

Multimeters: A minimum of three voltage meters are required. Other voltage meters can be used to monitor some of the test points.

Output Load: Two constant current electronic loads are recommended. They must be able to sink up to 10 A when the output is 3.3 V or 5 V.

Oscilloscope: A minimum 50-MHz digital oscilloscope and a voltage probe is required. The scope can be used to measure output ripple and monitor some of the test points.

Fan: A fan is not required when testing the EVM.

Recommended Wire Gauge: Both loads and input should be connected using a minimum gauge wire of AWG#16. Also these connections should be kept as short as possible.

5.2 Recommended Test Setup

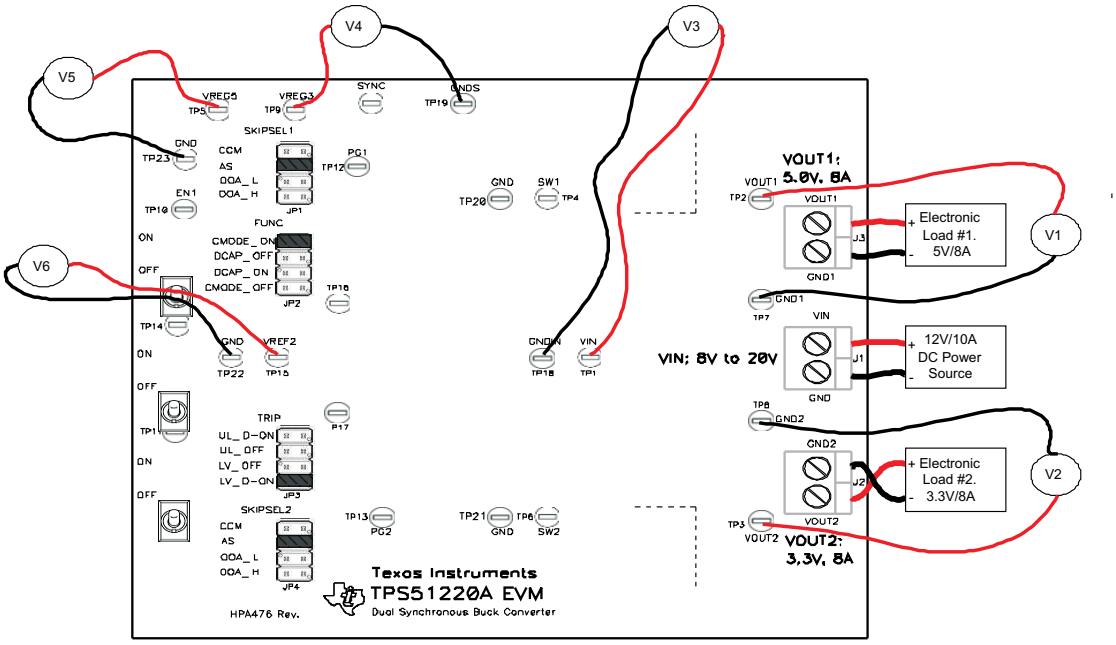

Figure 5-1. TPS51220A EVM-476 Recommended Test Setup

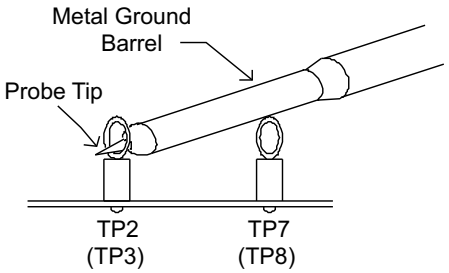

Figure 5-2. Recommended Tip and Barrel Technique to Measure Output Ripple Voltage

5.3 List of Test Points

Table 5-1. Test Point Functions Found on the TPS51220A EVM-476

TEST POINT	NAME	DESCRIPTION
TP1	VIN	Measurement point for input voltage with respect to TP18
TP2	VOUT1	Measurement point for output 1 voltage with respect to TP7
TP3	VOUT2	Measurement point for output 2 voltage with respect to TP8
TP4	SW1	Output 1 switch node with respect to TP20
TP5	VREG5	5-V/100-mA output, enabled EN is high, use switch S3
TP6	SW2	Output 2 switch node with respect to TP21
TP7	GND1	Ground reference for VOUT1
TP8	GND2	Ground reference for VOUT2
TP9	VREG3	3.3-V/10-mA output should be present when input voltage is applied to EVM.
TP10	EN1	Output 1 enable signal, will be high when output is enabled via switch S1
TP11	EN2	Output 2 enable signal, will be high when output is enabled via switch S2
TP12	PG1	Output 1 power good signal, will be high when output is in regulation
TP13	PG2	Output 2 power good signal, will be high when output is in regulation
TP14	EN	5-V and 2-V reference enable signal, high when EVM is enabled with switch S3
TP15	VREF2	2-V internal reference, enabled when EN is high, use switch S3
TP16	–	Not used
TP17	–	Not used
TP18	GNDIN	Ground reference for VIN
TP19	GNDS	General ground
TP20	GND	Ground reference for SW1
TP21	GND	Ground reference for SW2
TP22	GND	General ground
TP23	GND	General ground
TP24	SYNC	Not used

6 Test Procedure

6.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Ensure the switches S1 (EN1), S2 (EN2), and S3 (EN) are in the “OFF” position.
2. Ensure the shunt jumper are set as follows, see Section 6.3, Section 6.4, and Section 6.5 for details on how to change these settings:
   a. JP1 (SKIPSEL1): jumper 3 pin to 4 pin (AS)
   b. JP2 (FUNC): jumper 1 pin to 2 pin (CMODE_ON)
   c. JP3 (TRIP): jumper 7 pin to 8 pin (LV_D-ON)
   d. JP4 (SKIPSEL2): jumper 3 pin to 4 pin (AS)
3. Set the DC power source current limit to 10 A. Increase VIN voltage from 0 V to 8 VDC. V3 should be used to verify VIN.
4. Measure VREG3 (TP9) voltage using V4. It should be between 3.2 V and 3.4 V.
5. Set S3 (EN) to “ON” position. Measure VREG5 (TP5) voltage using V5, it should read between 4.9 V and 5.1 V. Measure VREF2 (TP15) voltage using V6, it should read 1.98 V to 2.02 V.
6. Make sure electronic load #1 is set to sink 0 A. Set S1 (EN1) to “ON” position, S3 remains in “ON” position.
7. Record VOUT1 voltage using V1, IOUT1 current, VIN using V3 and input current from source.
8. Increase electronic load #1’s current in 0.5-A steps from 0 A to 8 A, Record VOUT1 voltage using V1, IOUT1 current, VIN using V3 and input current from source for each step.
9. Set input voltage to 20 V.
10. Reduce the current of electronic load #1 from 8 A to 0 A, the current electronic load #1 in 0.5-A steps from 0 A to 8 A. Record VOUT1 voltage using V1, IOUT1 current, VIN using V3 and input current from source for each step.
11. Similar technique can be used for VOUT2. Use S2 to enable VOUT2.

6.2 Output Ripple Test

1. Use steps 1 to 6 of Section 6.1 to start output.
2. Set up the scope as follows:
   a. HORIZONTAL SWEEP: 2 µs/div
   b. TRIGGER MODE: auto, rising edge
   c. TRIGGER SOURCE: Ch1
   d. CH1: 50 mV/div, AC coupled, bandwidth 20 MHz
3. Use the tip and barrel technique shown in Figure 5-2 to probe VOUT1 and VOUT2 during test procedure.

6.3 Measuring Improved Light Load Efficiency

1. All jumper modifications should be done with no power applied to the EVM
2. SKIPSEL1 and SKIPSEL2 allow the user to select how the EVM operates when in light load. Table 6-1 describes each possible selection.

Table 6-1. SKIPSEL1 or SKIPSEL2 (jumpers JP1 and JP4) Selections

JUMPER LOCATION	MODE	DESCRIPTION
CCM (1 and 2 shorted)	CCM	EVM remains in continuous current mode
AS (3 and 4 shorted) default	Auto-skip	EVM enters auto skip mode at light load, audible noise may be heard.
OOA_L (5 and 6 shorted)	OOA (< 400 kHz)	EVM enters skip mode with no audible noise
OOA_H (7 and 8 shorted)	OOA (> 400 kHz)	Not recommended

3. Once a mode has been selected, efficiency and regulation measurements may be retaken. Repeat steps 3 to 11 of Section 6.1. The engineer should reduce the step current when the output is less than 1 A. Section 7 shows typical data for the various modes of operation

6.4 Control Architecture and OVP Select

1. All jumper modifications should be done with no power applied to the EVM.
2. The FUNC jumper (JP2) allows the user to select the control architecture the EVM uses to control the output. It also enables or disables the OVP function. Table 6-2 describes each possible selection.

Table 6-2. FUNC (jumper JP2) Selections

JUMPER LOCATION	MODE
CMODE_ON (1 and 2 shorted) default	Current mode control and OVP enabled
DCAP_OFF (3 and 4 shorted)	D-Cap mode control and OVP disabled
DCAP_ON (5 and 6 shorted)	D-Cap mode control and OVP enabled
CMODE_OFF (7 and 8 shorted)	Current mode control and OVP disabled

3. Once a mode has been selected efficiency and regulation measurements may be retaken. Repeat steps 3 to 11 of Section 6.1. The engineer should reduce the step current when the output is less than 1 A. Section 7 shows typical data for the various modes of operation

6.5 Overcurrent Trip Level and Output Discharge Select

1. All jumper modifications should be done with no power applied to the EVM.
2. The TRIP jumper (JP3) allows the user to select the voltage level used by the EVM to implement current limit. It also enables or disables the output discharge function. Table 6-3 describes each possible selection.

Table 6-3. TRIP (JP3) Selections

JUMPER LOCATION	MODE
UL_D-ON (1 and 2 shorted)	Overcurrent uses ultra low voltage threshold (31 mV typical) and output discharge is enabled
UL_OFF (3 and 4 shorted)	Overcurrent uses ultra low voltage threshold (31 mV typical) and output discharge is disabled
LV_OFF (5 and 6 shorted)	Overcurrent uses low voltage threshold (60 mV typical) and output discharge is disabled
LV_D-ON (7 and 8 shorted) default	Overcurrent uses low voltage threshold (60 mV typical) and output discharge is enabled

3. Once a mode has been selected efficiency and regulation measurements may be retaken. Repeat steps 3 to 11 of Section 6.1. The engineer should reduce the step current when the output is less than 1 A. Section 7 shows typical data for the various modes of operation

7 Performance Data and Typical Characteristic Curves

7.1 Efficiency

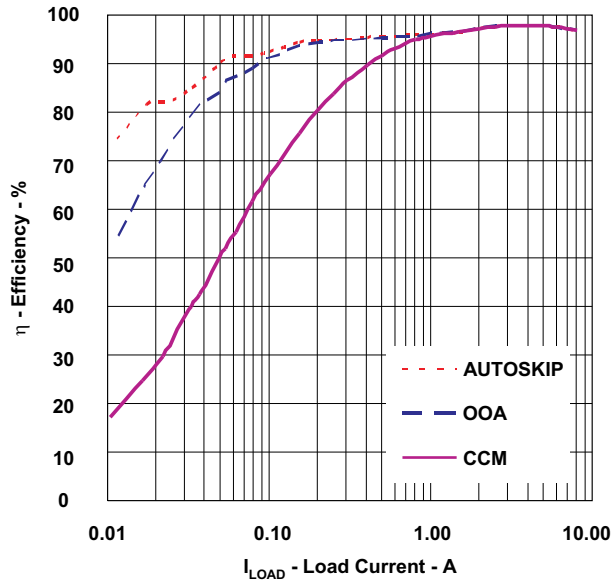

Figure 7-1. Efficiency, 12 V_{IN}, 5.0-V Output

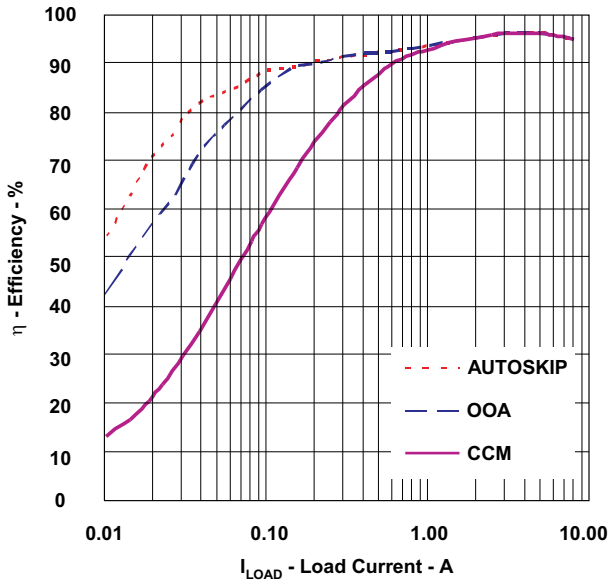

Figure 7-2. Efficiency, 12 V_{IN}, 3.3-V Output

7.2 Load Regulation

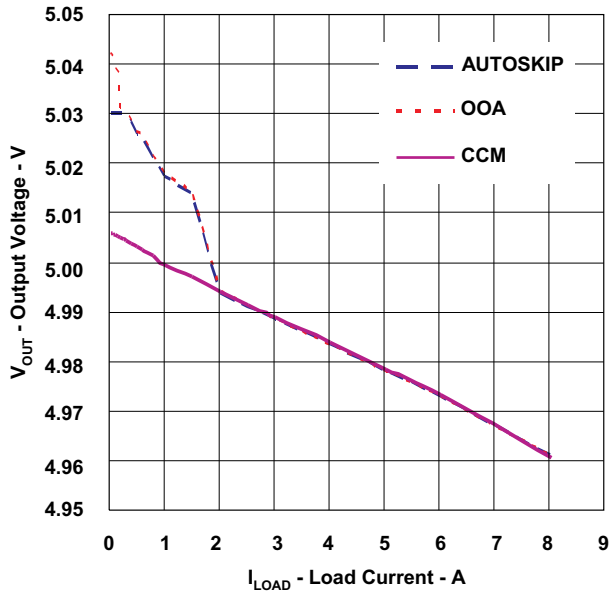

Figure 7-3. 12 V_{IN}, 5.0-V Load Regulation

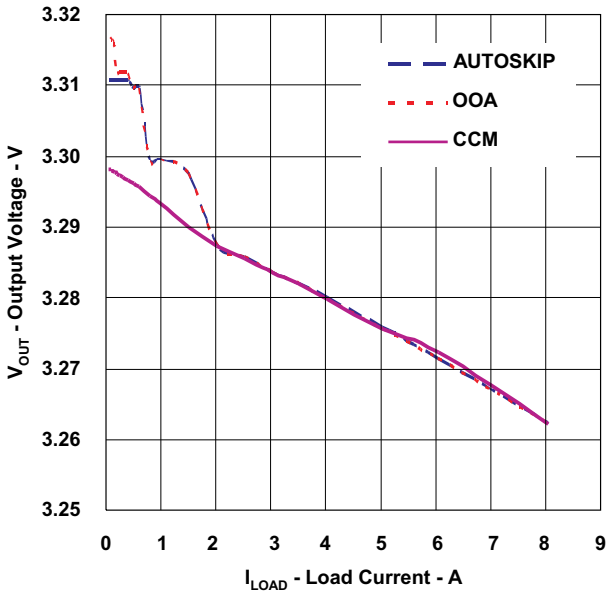

Figure 7-4. 12 V_{IN}, 3.3-V Load Regulation

7.3 Bode Plot

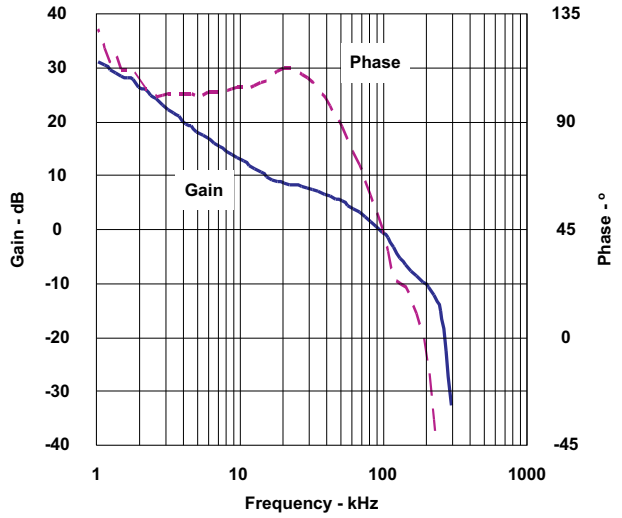

Figure 7-5. CCM mode 5-V Loop Response Gain and Phase, f_{CO} = 95 kHz, PM = 48°

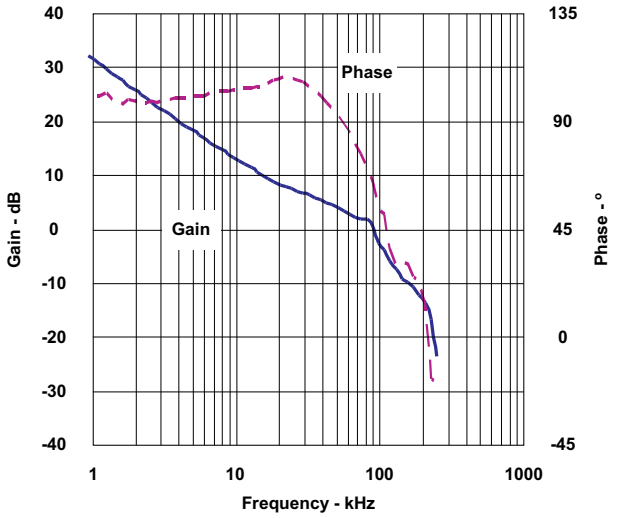

Figure 7-6. CCM mode 3.3-V Loop Response Gain and Phase, f_{CO} = 90 kHz, PM = 63°

7.4 Transient Response

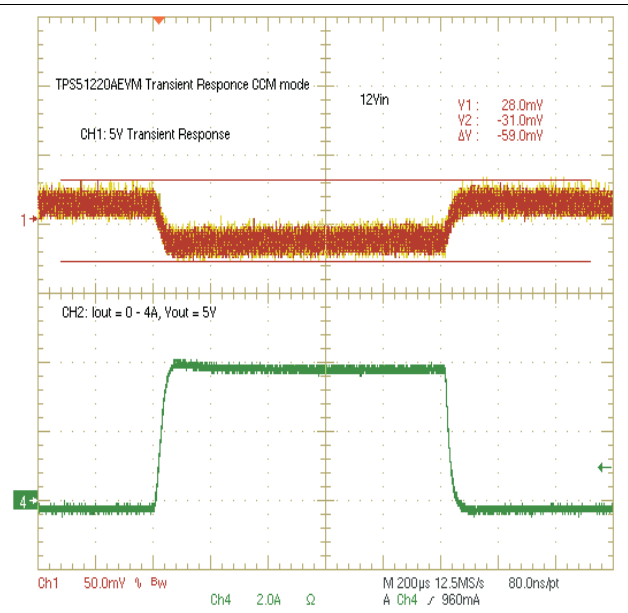

Figure 7-7. 5-V CCM Mode Load Transient

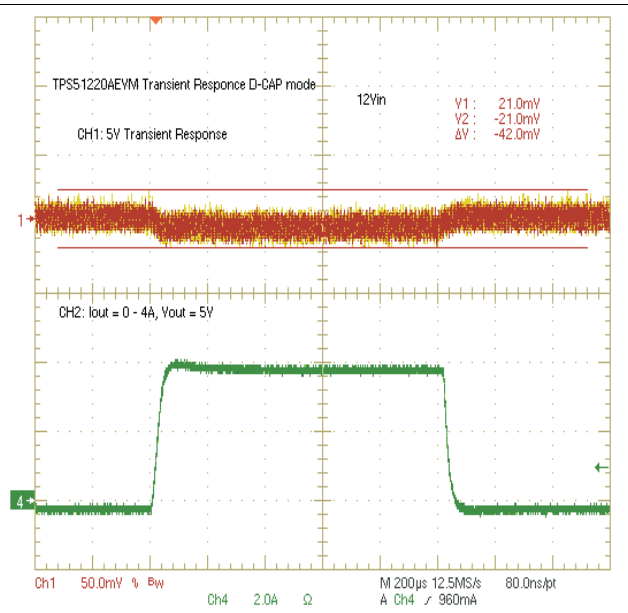

Figure 7-8. 5-V D-CAP Mode Load Transient

7.5 Output Ripple and Switch Node

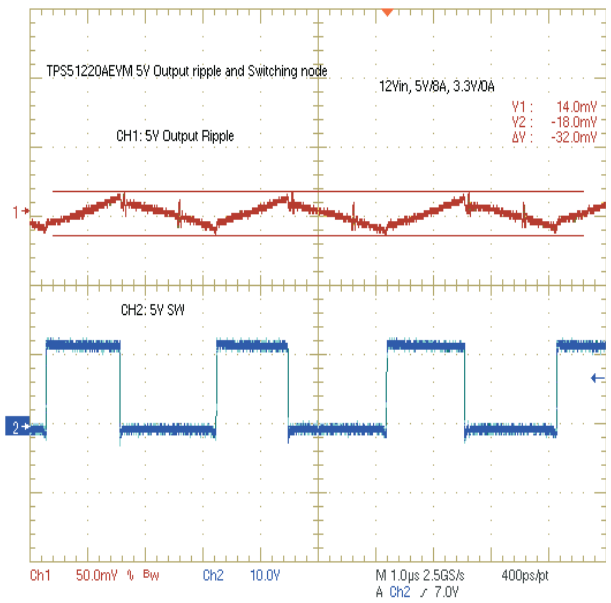

Figure 7-9. 5-V CCM Mode Output Ripple and Switch Node

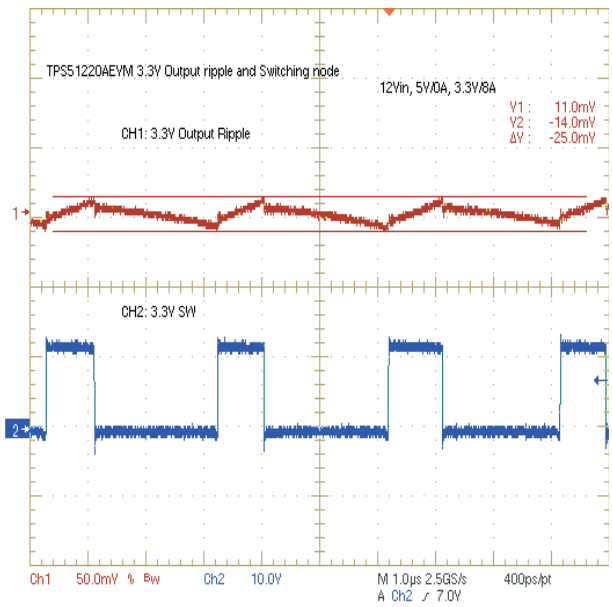

Figure 7-10. 3.3-V CCM Mode Output Ripple

7.6 Turn-On Waveform

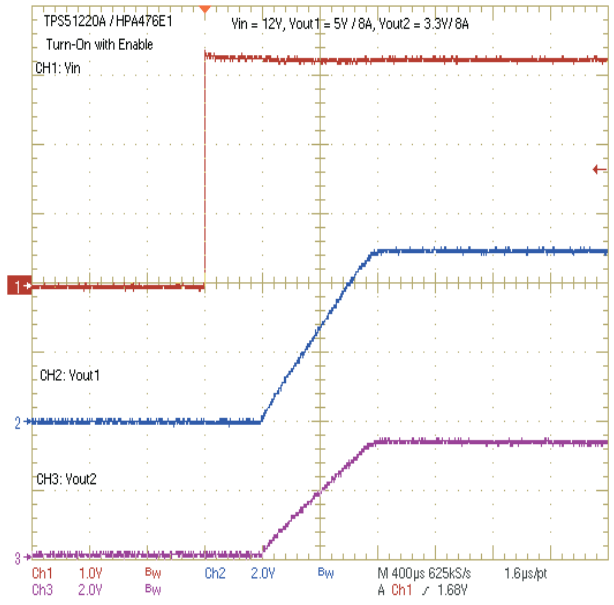

Figure 7-11. Enable Turn-On Waveform

7.7 Turn-Off Waveform

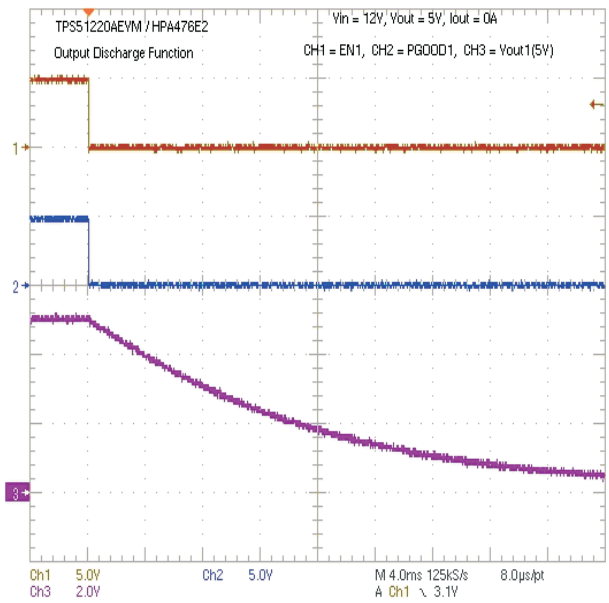

Figure 7-12. Enable Turn-Off With Discharge Waveform

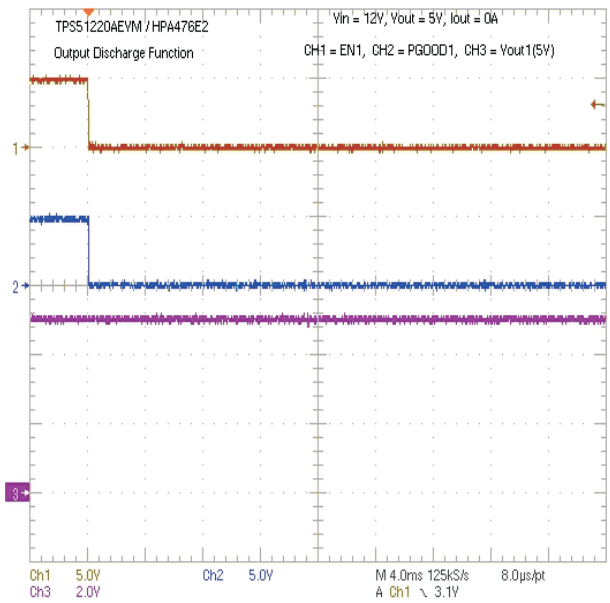

Figure 7-13. Enable Turn-Off Without Discharge Waveform

8 EVM Assembly Drawing and PCB Layout

The following figures (Figure 8-1 through Figure 8-6) show the design of the TPS51220A EVM-476 printed circuit board. The PCB is 0.062” thick. It uses four layers of copper. The two internal layers are 2-oz copper while the external layers are 1-oz copper.

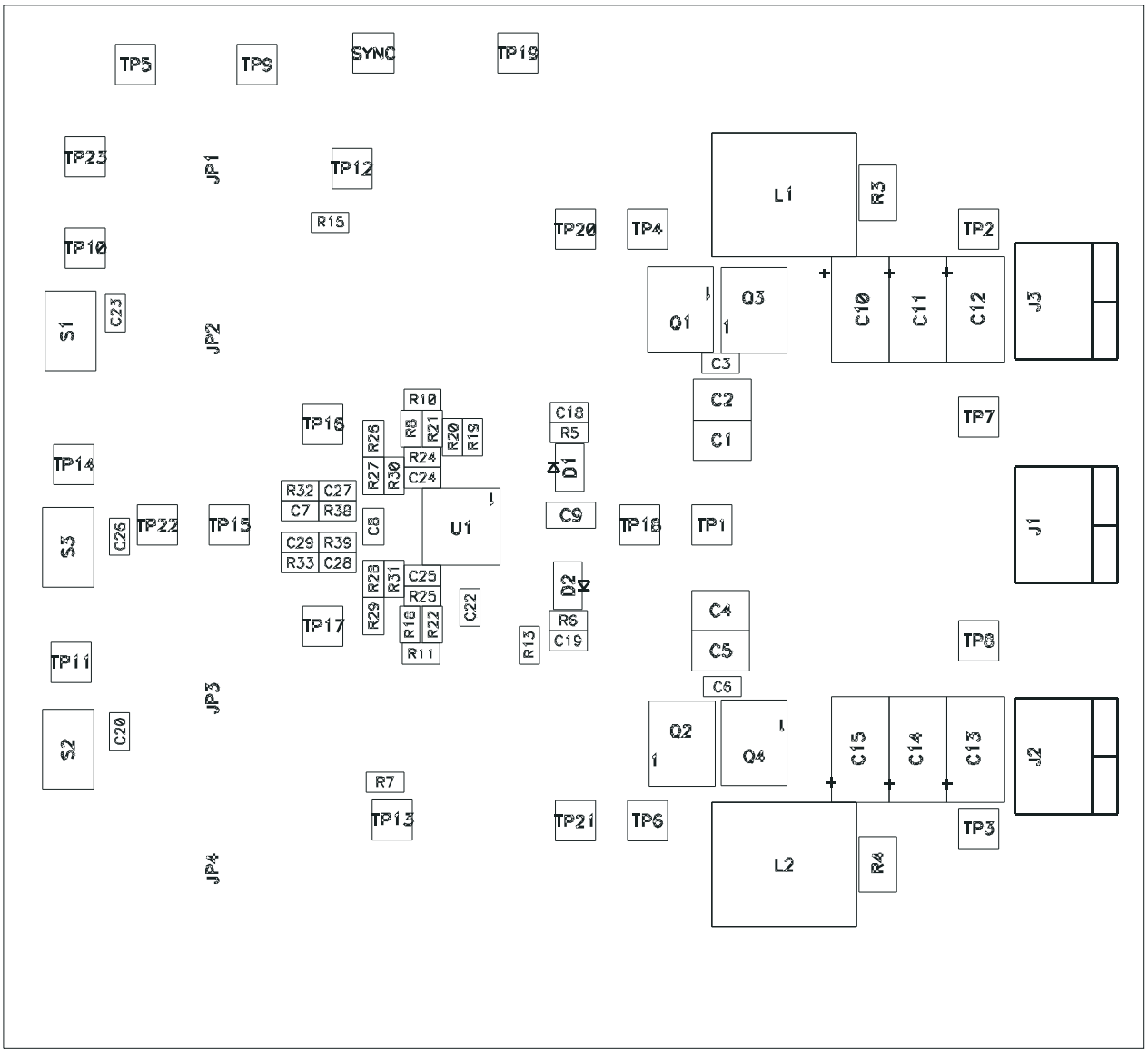

Figure 8-1. Top Layer Assembly Drawing (Top View)

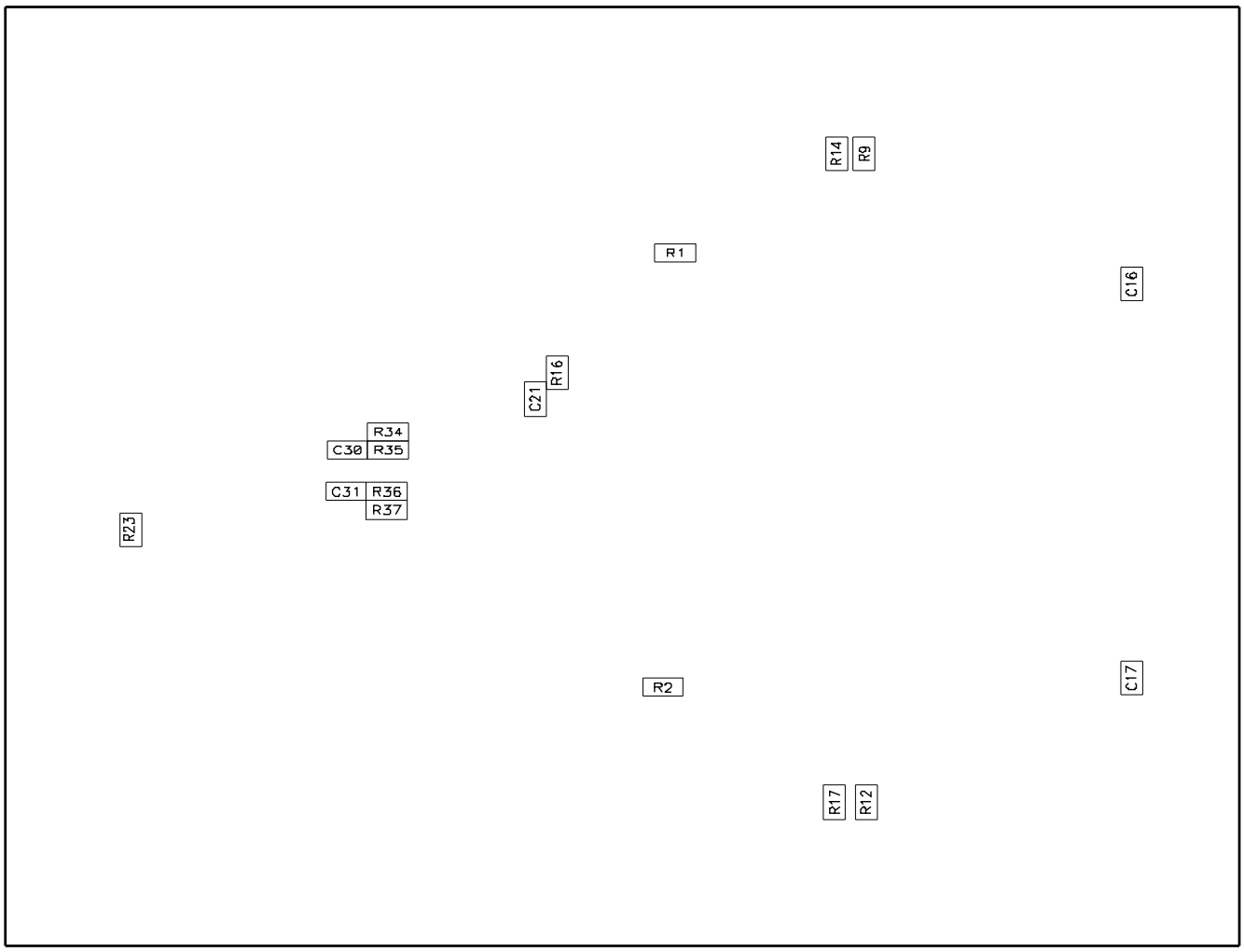

Figure 8-2. Bottom Assembly Drawing (Top View)

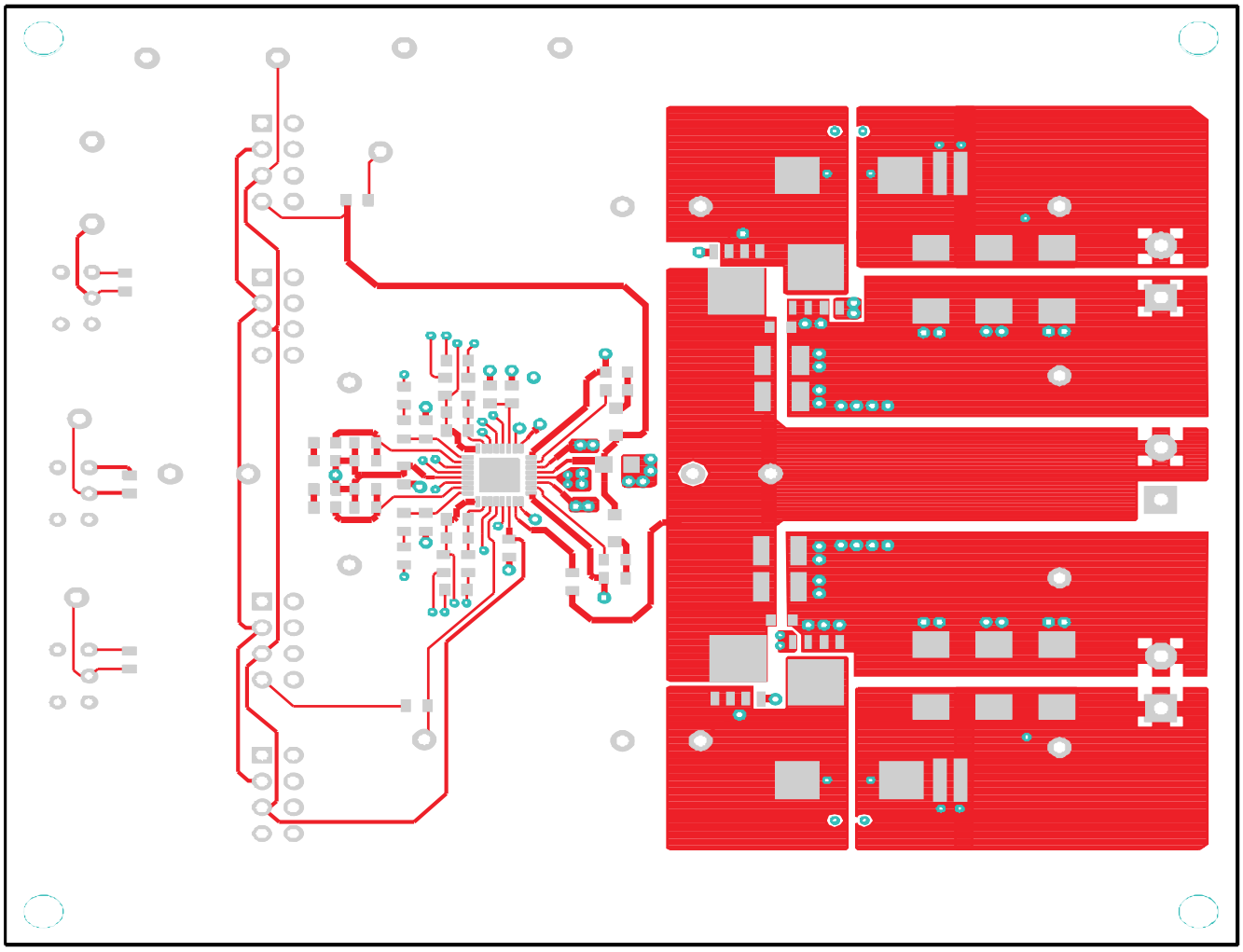

Figure 8-3. Top Copper (Top View)

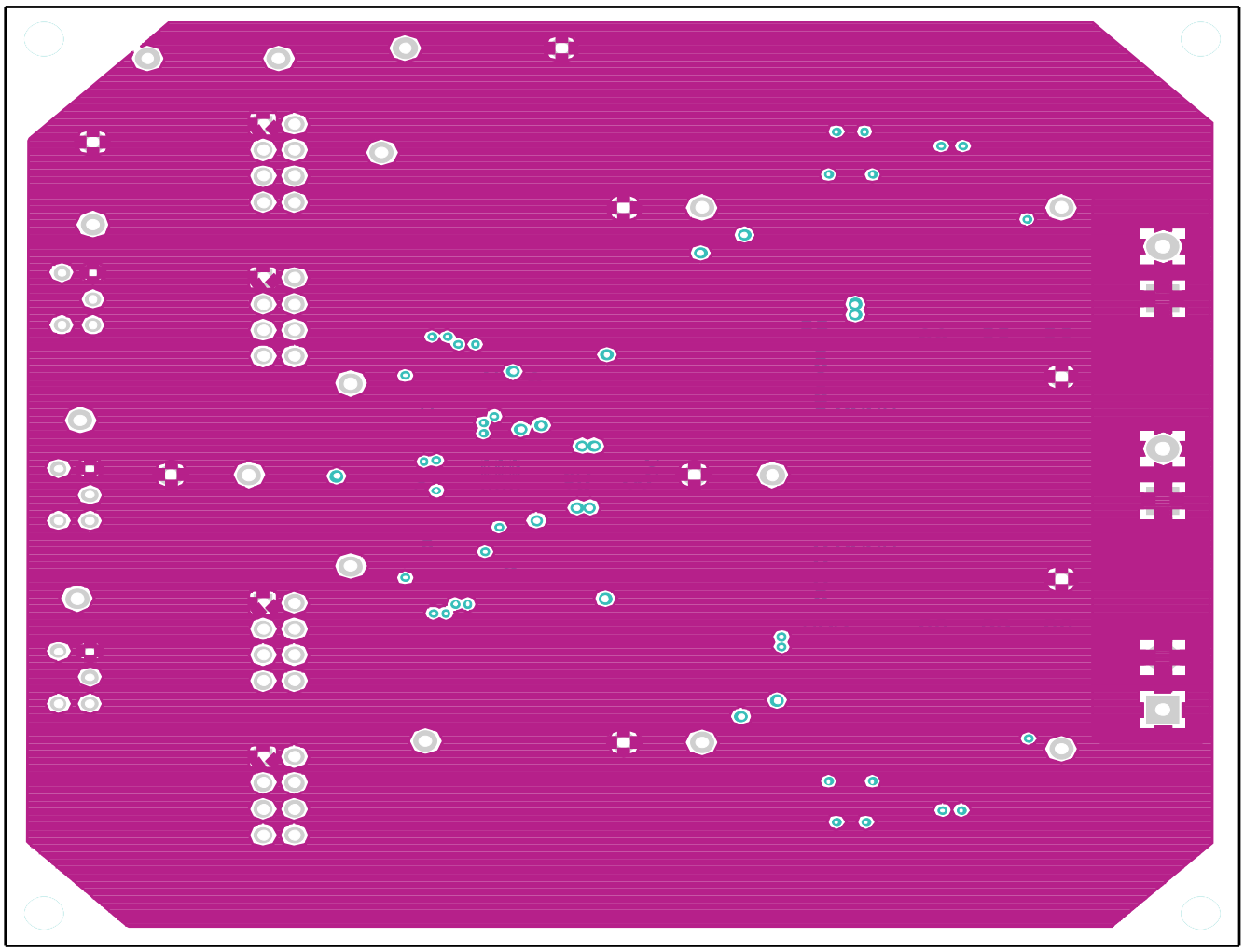

Figure 8-4. Internal Layer 1 (Top View)

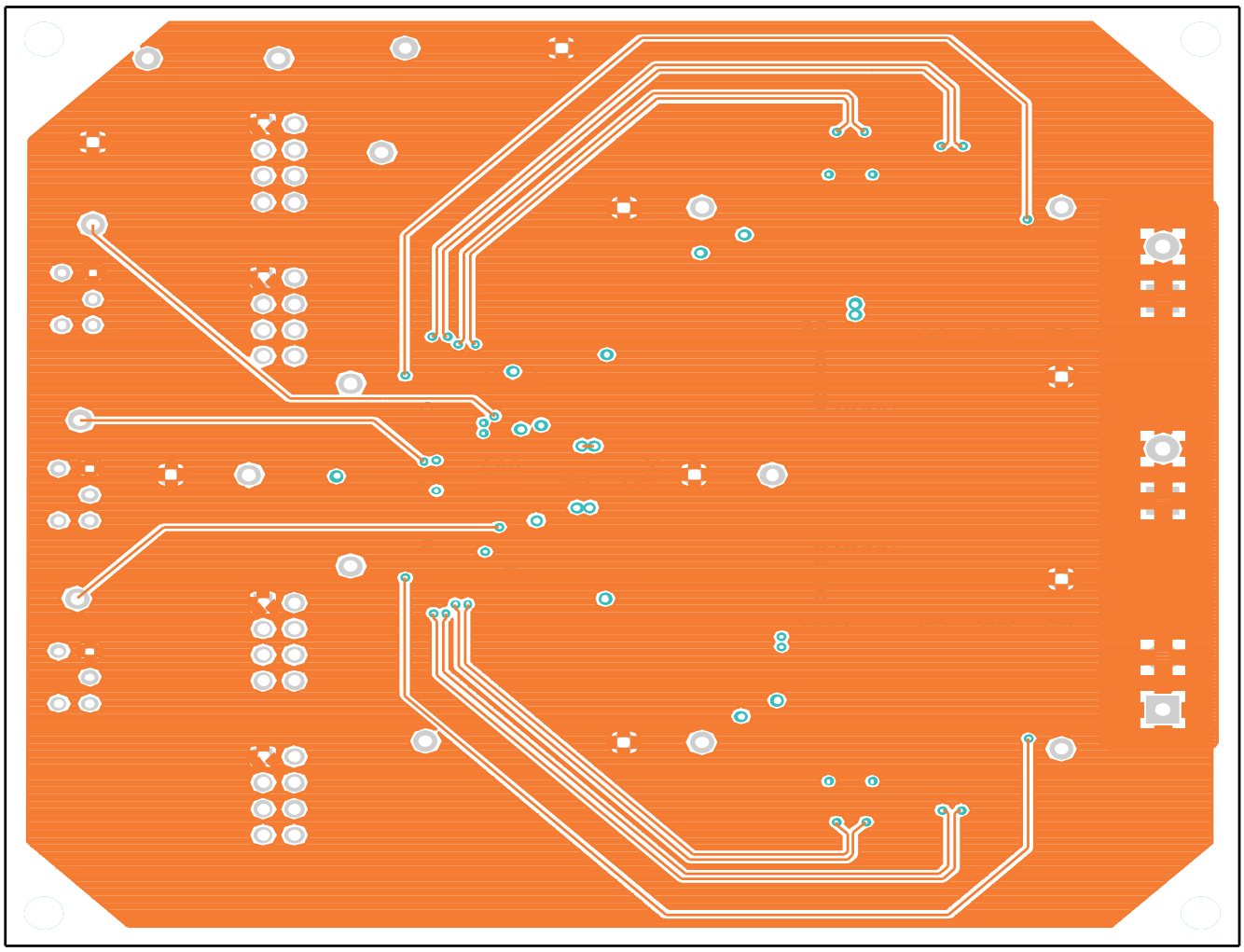

Figure 8-5. Internal Layer 2 (Top View)

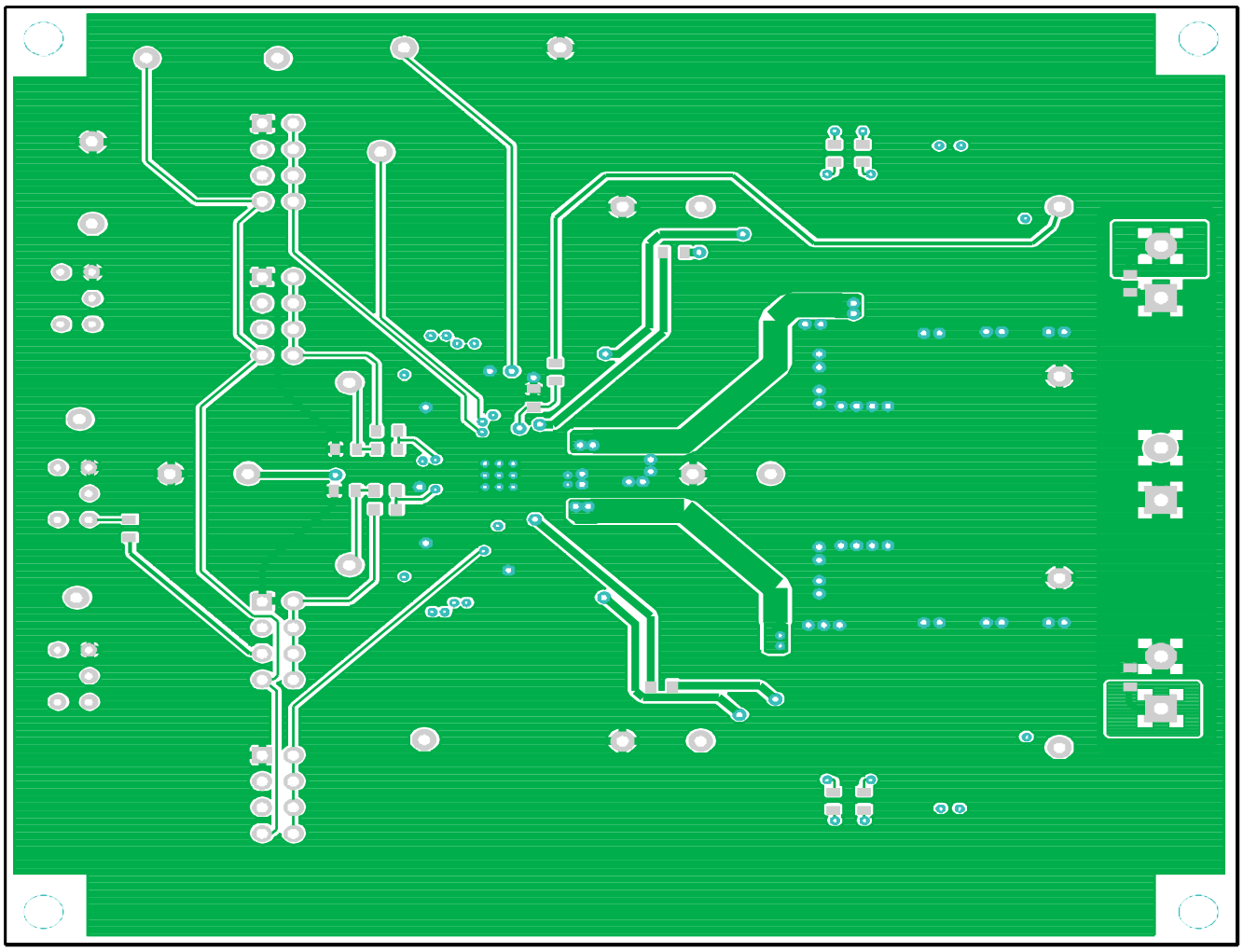

Figure 8-6. Bottom Copper (Top View)

9 List of Materials

Table 9-1. EVM Components List According to Schematic Shown in Figure 4-1

QTY	REFDES	DESCRIPTION	MFR	PART NUMBER
4	C1, C2, C4, C5	Capacitor, ceramic, 10 µF, 25 V, X7R, ±10%, 1210	muRata	GRM32DR71E106K
2	C10, C11	Capacitor, POS-CAP, 330 µF, 6.3 V, 18 mΩ, 20%	SANYO	6TPE330MIL
2	C14, C15	Capacitor, POS-CAP, 470 µF, 4.0 V, 15 mΩ, 20%	SANYO	4TPE470MFL
3	C16, C17, C21	Capacitor, ceramic, 0.01 µF, 50 V, X7R, ±10%, 0603	Std	Std
4	C20, C23, C26, C27	Capacitor, ceramic, 100 pF, 50 V, C0G, ±5%, 0603	Std	Std
1	C22	Capacitor, ceramic, 2.2 µF, 6.3 V, X5R, ±10%, 0603	Std	Std
1	C28	Capacitor, ceramic, 47 pF, 50 V, C0G, ±5%. 0603	Std	Std
6	C3, C6, C18, C19, C24, C25	Capacitor, ceramic, 0.1 µF, 50 V, X7R, ±10%, 0603	Std	Std
1	C8	Capacitor, ceramic, 0.22 µF, 25 V, X7R, ±10%, 0603	Std	Std
1	C9	Capacitor, ceramic, 10 µF, 6.3 V, X5R, ±10%, 0805	TDK	C2012X5R0J106K
2	D1, D2	Diode, Schottky, 40 V, 30 mA, SOD-323	Rohm	RB751x-40
2	L1, L2	Inductor, 3.3-µH, 12 A	Vishay	IHLP5050CEER3R3
2	Q1, Q2	MOSFET, N-ch, 30 V, 14 A, 9.7 mΩ	TI	CSD17307Q5A
2	Q3, Q4	MOSFET, N-ch, 30 V, 21 A, 4.5 mΩ	TI	CSD17310Q5A
11	R1, R2, R9, R12, R13, R14, R16, R17, R23, R34, R37	Resistor, chip, 0 Ω, 1/16 W, ±5%, 0603	Std	Std
1	R20	Resistor, chip, 300 kΩ, 1/16 W, ±1%, 0603	Std	Std
1	R21	Resistor, chip, 8.20 kΩ, 1/16 W, ±1%, 0603	Std	Std
1	R22	Resistor, chip, 7.50 kΩ, 1/16 W, ±1%, 0603	Std	Std
2	R24, R25	Resistor, chip, 5.60 kΩ, 1/16 W, ±1%, 0603	Std	Std
2	R26, R29	Resistor, chip, 51.1 Ω, 1/16 W, ±1%, 0603	Std	Std
1	R27	Resistor, chip, 120 kΩ, 1/16 W, ±1%, 0603	Std	Std
1	R28	Resistor, chip, 62.0 kΩ, 1/16 W, ±1%, 0603	Std	Std
1	R30	Resistor, chip, 30.0 kΩ, 1/16 W, ±1%, 0603	Std	Std
1	R31	Resistor, chip, 27.0 kΩ, 1/16 W, ±1%, 0603	Std	Std
1	R38	Resistor, chip, 15.0 kΩ, 1/16 W, ±1%, 0603	Std	Std
1	R39	Resistor, chip, 12.0 kΩ, 1/16 W, ±1%, 0603	Std	Std
2	R5, R6	Resistor, chip, 15.4 Ω, 1/16 W, ±1%, 0603	Std	Std
2	R7, R15	Resistor, chip, 470 kΩ, 1/16 W, ±1%, 0603	Std	Std
1	U1	Fixed frequency 99% duty cycle, dual buck controller	TI	TPS51220ARTV

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2011) to Revision B (February 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	3
• Updated the user's guide title.	3

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