Document Number: MML09211H
Rev. 1, 9/2014

RoHS

Enhancement Mode pHEMT Technology (E-pHEMT)

Low Noise Amplifier

MML09211HT1

400-1400 MHz, 21.3 dB
22 dBm
E-pHEMT LNA

DFN 2 × 2

The MML09211H is a single-stage low noise amplifier (LNA) with active bias and high isolation for use in cellular infrastructure applications. It is designed for a range of low noise, high linearity applications such as pico cell, femto cell, tower mounted amplifiers (TMA) and receiver front end circuits. It operates from a single voltage supply and is suitable for applications with frequencies from 400 to 1400 MHz such as ISM, GSM, W-CDMA and LTE.

Features

- Ultra Low Noise Figure: 0.52 dB @ 900 MHz
- Frequency: 400-1400 MHz
- Unconditionally Stable over Temperature
- High Reverse Isolation: -35 dB @ 900 MHz
- P1dB: 22 dBm @ 900 MHz
- Small-Signal Gain: 21.3 dB @ 900 MHz (adjustable externally)
- Third Order Output Intercept Point: 32.6 dBm @ 900 MHz
- Single 5 V Supply
- Supply Current: 60 mA
- 50 Ohm Operation (some external matching required)
- Cost-effective 8-pin, 2 mm DFN Surface Mount Plastic Package
- In Tape and Reel. T1 Suffix = 1,000 Units, 12 mm Tape Width, 7-inch Reel.

Table 1. Typical Performance (1)

Characteristic	Symbol	400 MHz	900 MHz	1400 MHz	Unit
Noise Figure (2)	NF	0.54	0.52	0.66	dB
Input Return Loss (S11)	IRL	-19	-23	-17	dB
Output Return Loss (S22)	ORL	-16	-16	-20	dB
Small-Signal Gain (S21)	G_p	26.1	21.3	18.8	dB
Power Output @ 1dB Compression	P1dB	22	22	20	dBm
Third Order Input Intercept Point	IIP3	11	11.3	13.5	dBm
Third Order Output Intercept Point	OIP3	31.5	32.6	32.3	dBm

1. V_{DD} = 5 Vdc, T_A = 25°C, 50 ohm system, application circuit tuned for specified frequency.
2. Noise figure value calculated with connector losses removed.

Table 2. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	6	V
Supply Current	I_{DD}	150	mA
RF Input Power	P_{in}	20	dBm
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	175	°C

Table 3. Thermal Characteristics

Characteristic	Symbol	Value (3)	Unit
Thermal Resistance, Junction to Case Case Temperature 86°C, 5 Vdc, 60 mA, no RF applied	$R_{\theta JC}$	37.5	°C/W

3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

freescale

Table 4. Electrical Characteristics (V_{DD} = 5 Vdc, 900 MHz, T_A = 25°C, 50 ohm system, in Freescale Application Circuit)

Characteristic	Symbol	Min	Typ	Max	Unit
Small-Signal Gain (S21)	G_p	19	21.3	—	dB
Input Return Loss (S11)	IRL	—	-23	—	dB
Output Return Loss (S22)	ORL	—	-16	—	dB
Power Output @ 1dB Compression	P1dB	—	22	—	dBm
Third Order Input Intercept Point	IIP3	—	11.3	—	dBm
Third Order Output Intercept Point	OIP3	—	32.6	—	dBm
Reverse Isolation (S12)	|S12|	—	-35	—	dB
Noise Figure (1)	NF	—	0.52	—	dB
Supply Current (2)	I_{DD}	45	60	90	mA
Supply Voltage	V_{DD}	—	5	—	V

1. Noise figure value calculated with connector losses removed.
2. DC current measured with no RF signal applied.

Table 5. Functional Pin Description

Pin Number	Pin Function
1	RF_{in}
2	RF_{in}
3	RF Input Matching Termination
4	Bias Voltage DC Supply
5	RF Feedback
6	RF_{out}/DC Supply
7	RF_{out}/DC Supply
8	No Connection

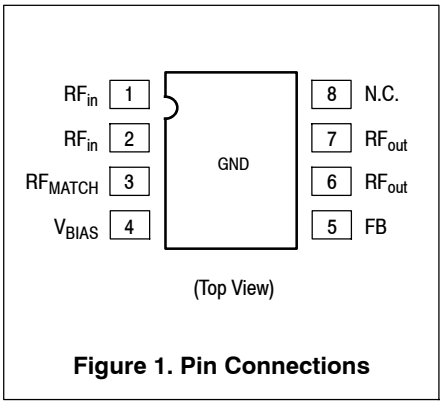


Figure 1. Pin Connections

Table 6. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD 22-A114)	0
Machine Model (per EIA/JESD 22-A115)	A
Charge Device Model (per JESD 22-C101)	IV

Table 7. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	1	260	°C

50 OHM APPLICATION CIRCUIT: 900 MHz

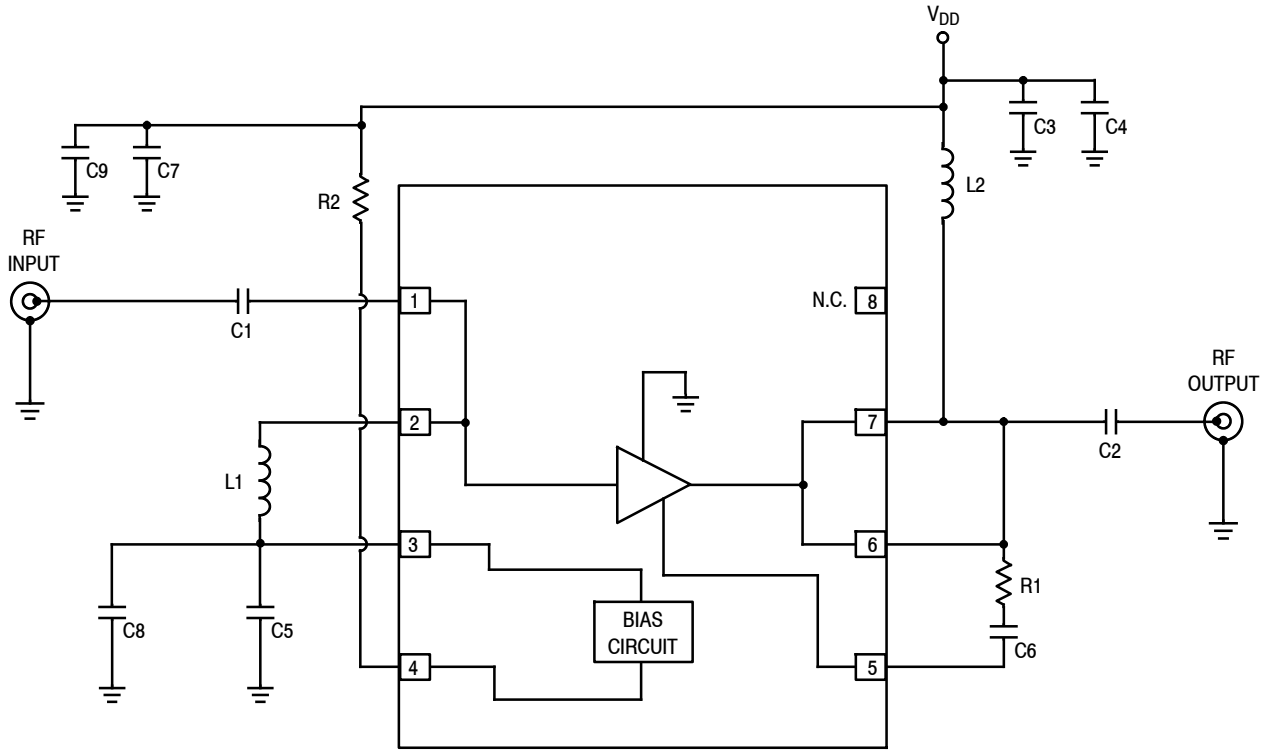
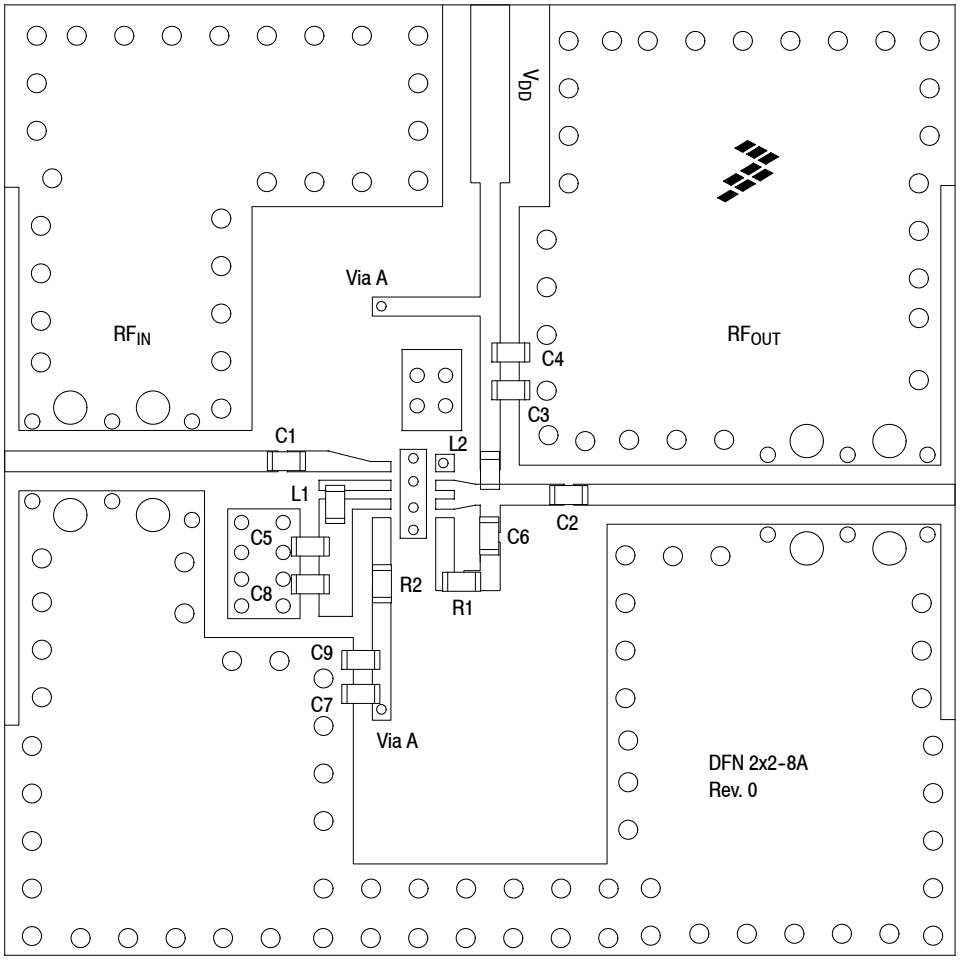


Figure 2. MML09211HT1 Test Circuit Schematic

Table 8. MML09211HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C6, C7	56 pF Chip Capacitors	GRM1555C1H560JZ01D	Murata
C3	100 pF Chip Capacitor	GRM1555C1H101JZ01D	Murata
C4	0.1 μF Chip Capacitor	GRM155R61A104KA01D	Murata
C5	180 pF Chip Capacitor	GRM1555C1H181JZ01D	Murata
C8, C9	0.01 μF Chip Capacitors	GRM155R71E103KA01D	Murata
L1	12 nH Chip Inductor	0402CS-12NXGL	Coilcraft
L2	13 nH Chip Inductor	0402CS-13NXGL	Coilcraft
R1	81 Ω, 1/16 W Chip Resistor	RC0402JR-0782RL	Yageo
R2	1210 Ω, 1/16 W Chip Resistor	RC0402FR-071K21L	Yageo
PCB	0.010″, ε_r = 3.38, Multilayer	IS680-3.38	Isola

50 OHM APPLICATION CIRCUIT: 900 MHz



NOTE: To achieve optimal noise performance, it is critical that proper biasing, input matching, supply decoupling and grounding are employed.

Figure 3. MML09211HT1 Test Circuit Component Layout

Table 8. MML09211HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
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C3	100 pF Chip Capacitor	GRM1555C1H101JZ01D	Murata
C4	0.1 μF Chip Capacitor	GRM155R61A104KA01D	Murata
C5	180 pF Chip Capacitor	GRM1555C1H181JZ01D	Murata
C8, C9	0.01 μF Chip Capacitors	GRM155R71E103KA01D	Murata
L1	12 nH Chip Inductor	0402CS-12NXGL	Coilcraft
L2	13 nH Chip Inductor	0402CS-13NXGL	Coilcraft
R1	81 Ω, 1/16 W Chip Resistor	RC0402JR-0782RL	Yageo
R2	1210 Ω, 1/16 W Chip Resistor	RC0402FR-071K21L	Yageo
PCB	0.010″, ε_r = 3.38, Multilayer	IS680-3.38	Isola

(Test Circuit Component Designations and Values repeated for reference.)

50 OHM TYPICAL CHARACTERISTICS: 900 MHz

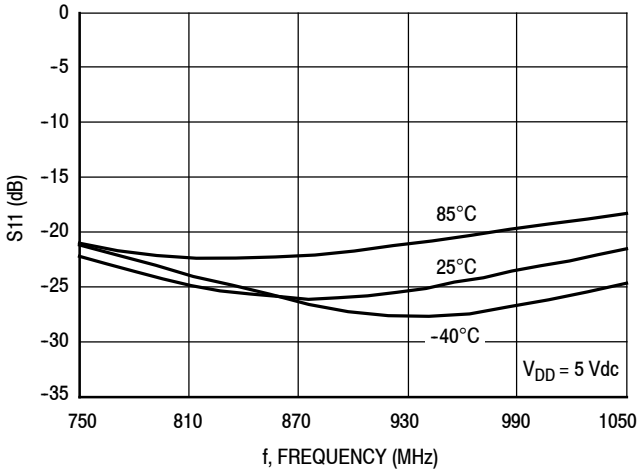


Figure 4. S11 versus Frequency versus Temperature

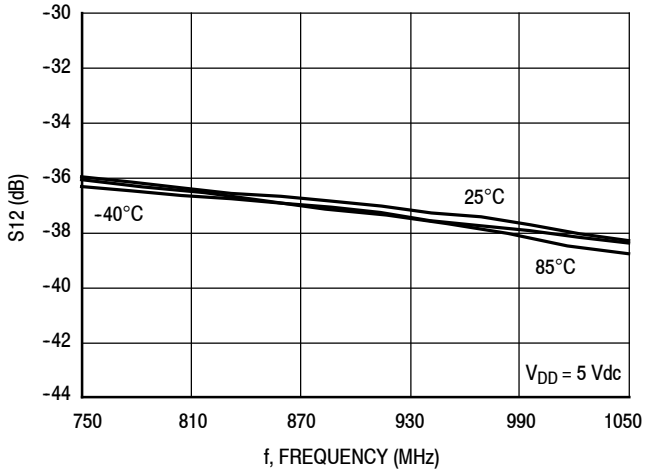


Figure 5. S12 versus Frequency versus Temperature

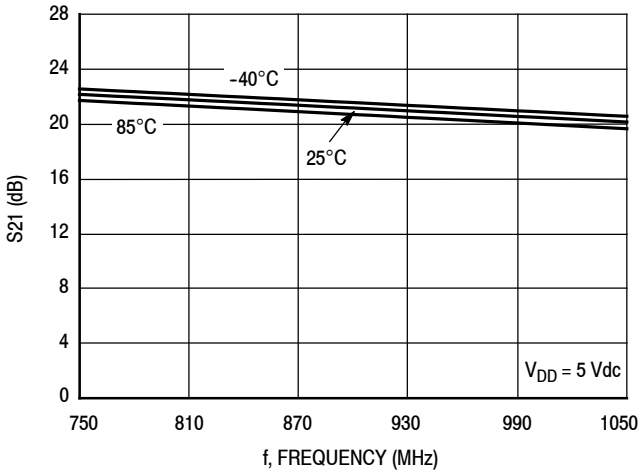


Figure 6. S21 versus Frequency versus Temperature

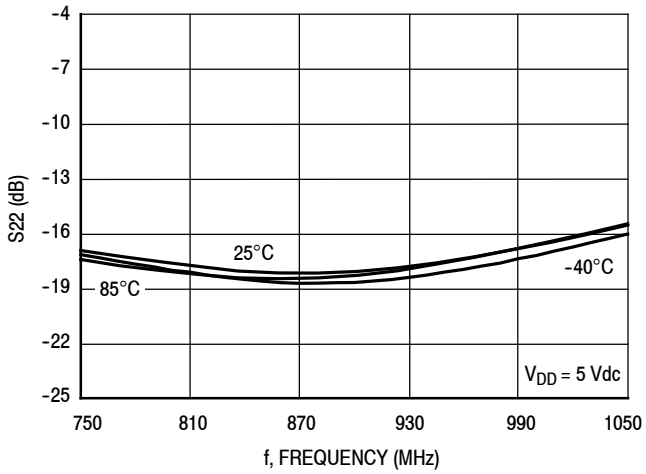


Figure 7. S22 versus Frequency versus Temperature

50 OHM TYPICAL CHARACTERISTICS: 900 MHz

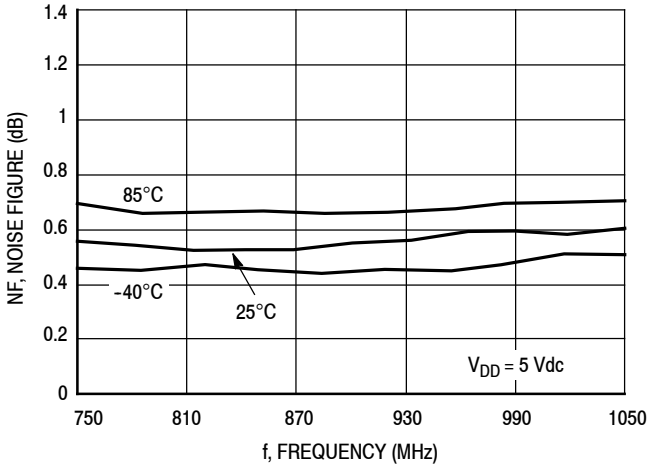


Figure 8. Noise Figure versus Frequency versus Temperature

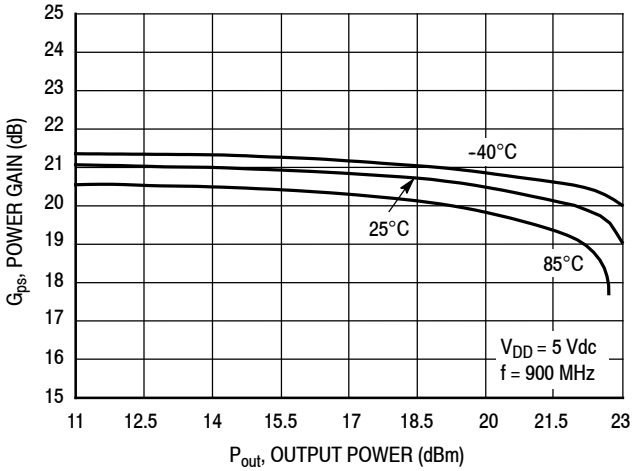


Figure 9. Power Gain versus Output Power versus Temperature, CW

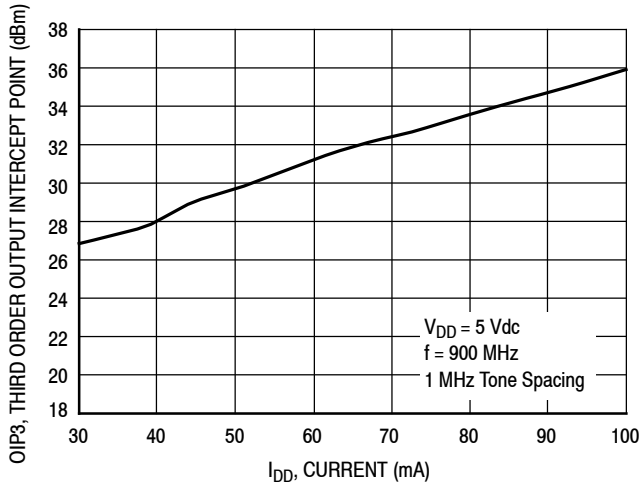


Figure 10. Third Order Output Intercept Point (Two-Tone) versus I_{DD} Current

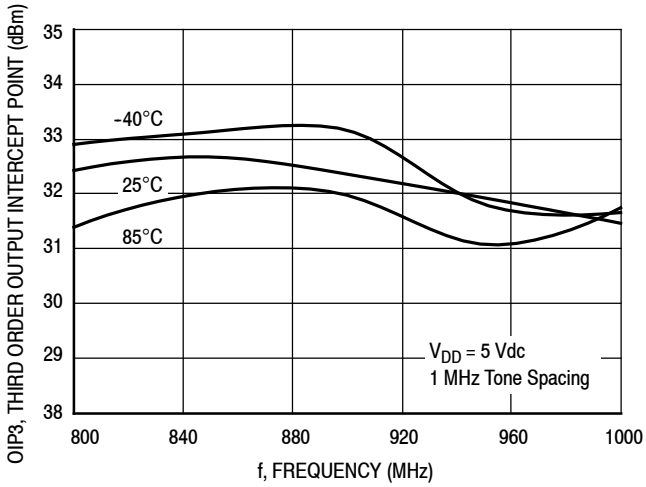


Figure 11. Third Order Output Intercept Point (Two-Tone) versus Frequency versus Temperature

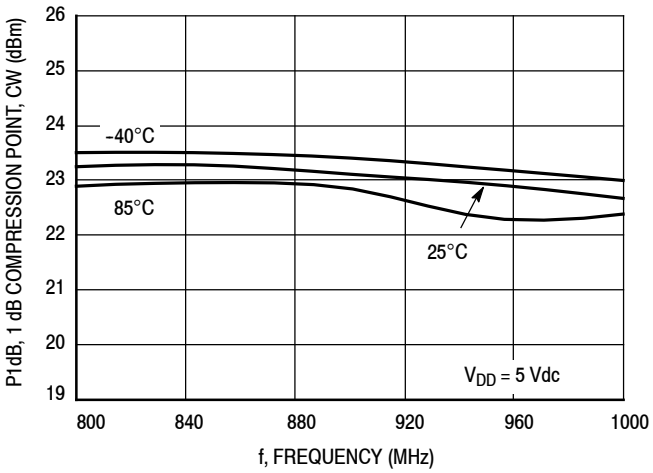


Figure 12. P1dB versus Frequency versus Temperature, CW

50 OHM APPLICATION CIRCUIT: 400 MHz

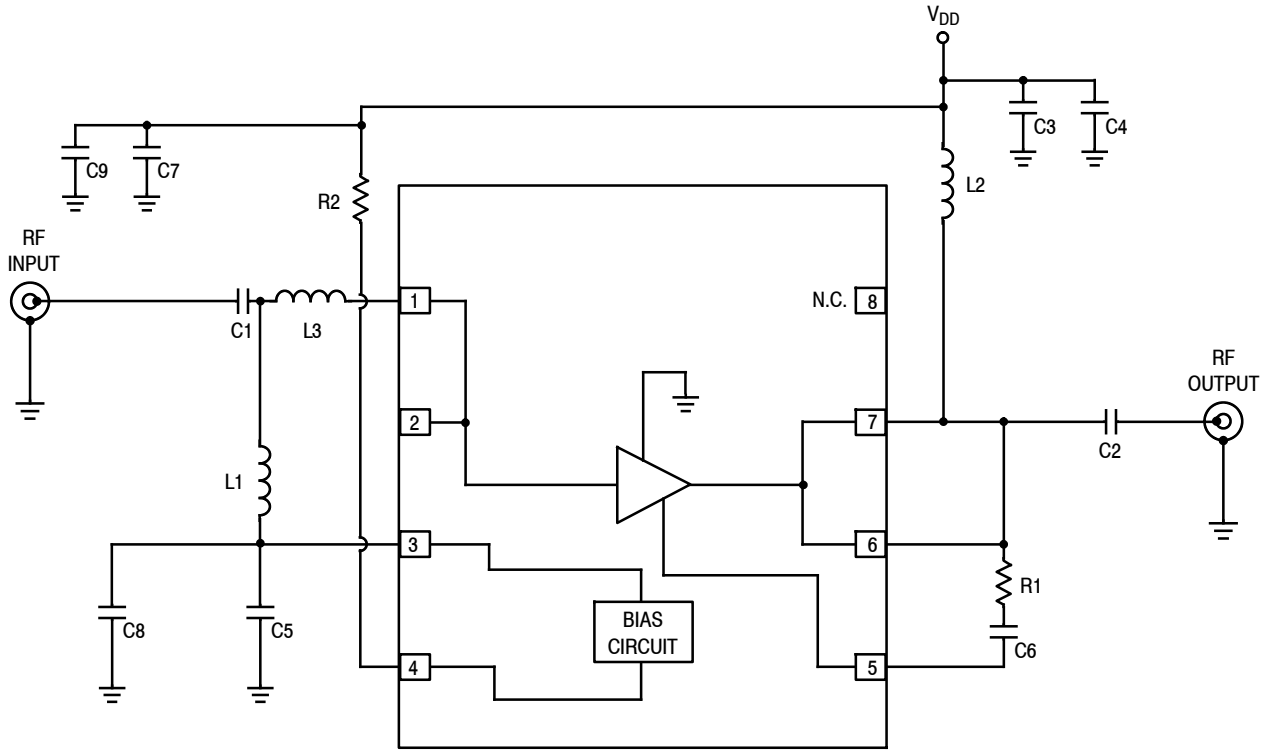
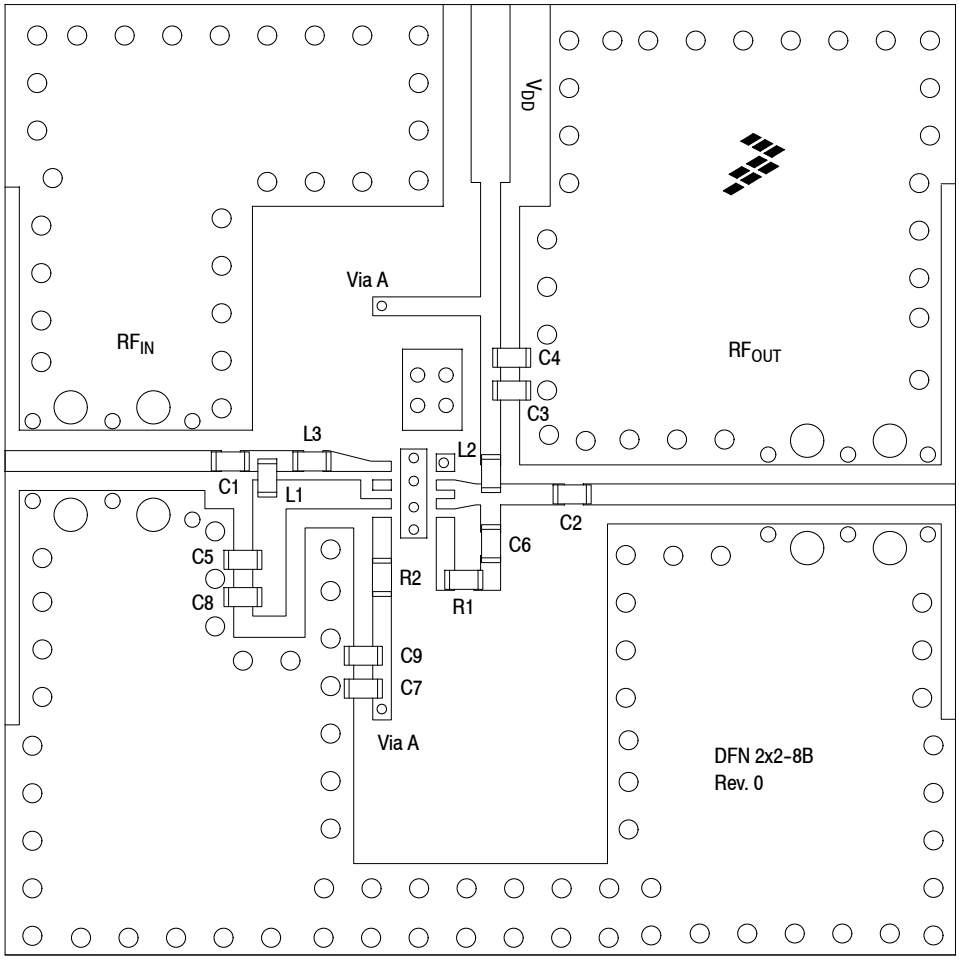


Figure 13. MML09211HT1 Test Circuit Schematic

Table 9. MML09211HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	100 pF Chip Capacitors	GRM1555C1H101JA01D	Murata
C3, C5	390 pF Chip Capacitors	GRM1555C1H391JA01D	Murata
C4	0.1 μF Chip Capacitor	GRM155R71C104KA88D	Murata
C6, C7	56 pF Chip Capacitors	GRM155C1H560JA01D	Murata
C8, C9	0.01 μF Chip Capacitors	GRM155R71E103KA01D	Murata
L1	22 nH Chip Inductor	0402CS-22NXGL	Coilcraft
L2	24 nH Chip Inductor	0402CS-24NXGL	Coilcraft
L3	4.3 nH Chip Inductor	0402CS-4N3XGL	Coilcraft
R1	100 Ω, 1/16 W Chip Resistor	RC0402FR-07100RL	Yageo
R2	1210 Ω, 1/16 W Chip Resistor	RC0402FR-071K21L	Yageo
PCB	0.010″, ε_r = 3.38, Multilayer	IS680-3.38	Isola

50 OHM APPLICATION CIRCUIT: 400 MHz



NOTE: To achieve optimal noise performance, it is critical that proper biasing, input matching, supply decoupling and grounding are employed.

Figure 14. MML09211HT1 Test Circuit Component Layout

Table 9. MML09211HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	100 pF Chip Capacitors	GRM1555C1H101JA01D	Murata
C3, C5	390 pF Chip Capacitors	GRM1555C1H391JA01D	Murata
C4	0.1 μF Chip Capacitor	GRM155R71C104KA88D	Murata
C6, C7	56 pF Chip Capacitors	GRM155C1H560JA01D	Murata
C8, C9	0.01 μF Chip Capacitors	GRM155R71E103KA01D	Murata
L1	22 nH Chip Inductor	0402CS-22NXGL	Coilcraft
L2	24 nH Chip Inductor	0402CS-24NXGL	Coilcraft
L3	4.3 nH Chip Inductor	0402CS-4N3XGL	Coilcraft
R1	100 Ω, 1/16 W Chip Resistor	RC0402FR-07100RL	Yageo
R2	1210 Ω, 1/16 W Chip Resistor	RC0402FR-071K21L	Yageo
PCB	0.010″, ε_r = 3.38, Multilayer	IS680-3.38	Isola

(Test Circuit Component Designations and Values repeated for reference.)

50 OHM TYPICAL CHARACTERISTICS: 400 MHz

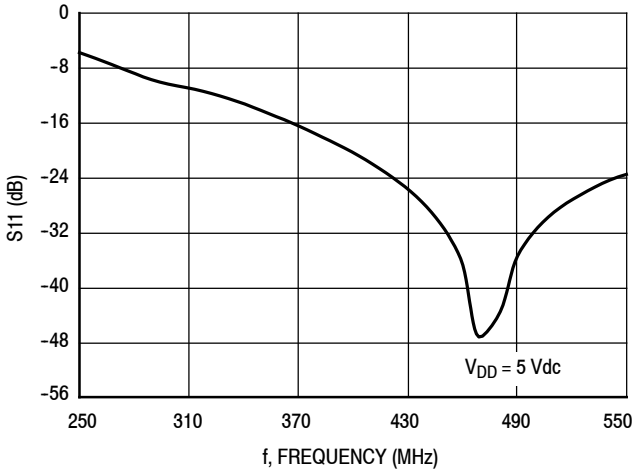


Figure 15. S11 versus Frequency

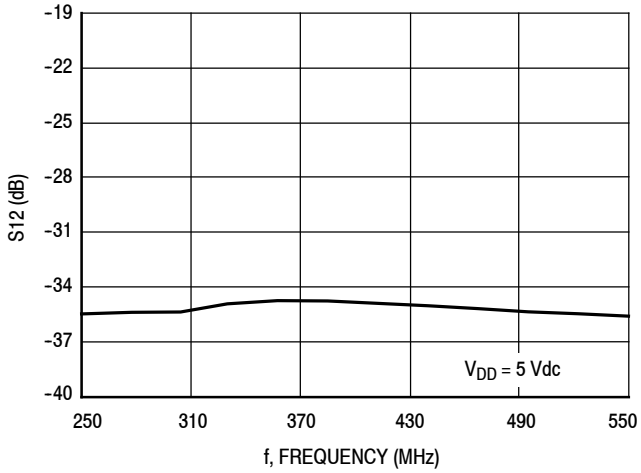


Figure 16. S12 versus Frequency

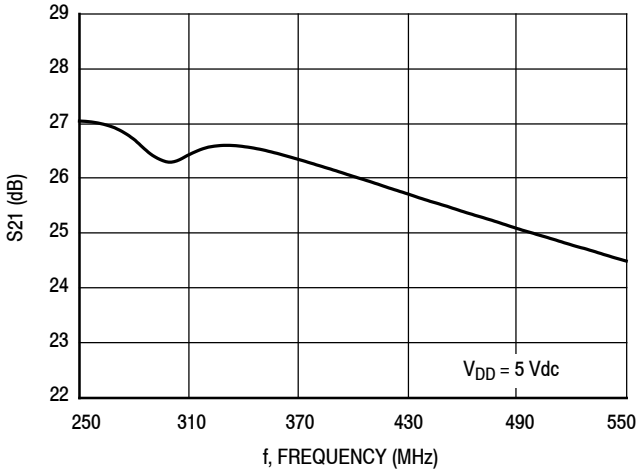


Figure 17. S21 versus Frequency

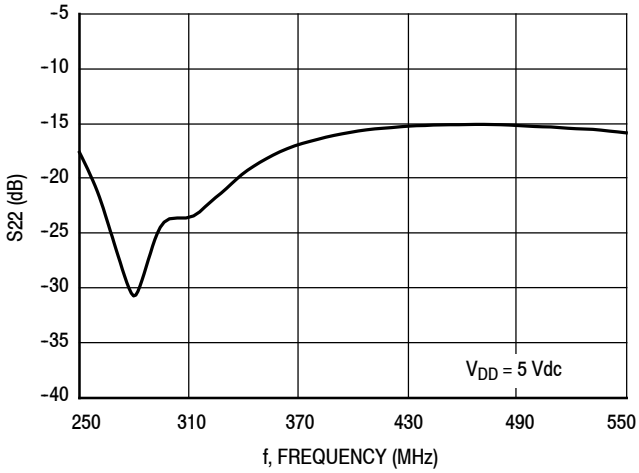


Figure 18. S22 versus Frequency

50 OHM TYPICAL CHARACTERISTICS: 400 MHz

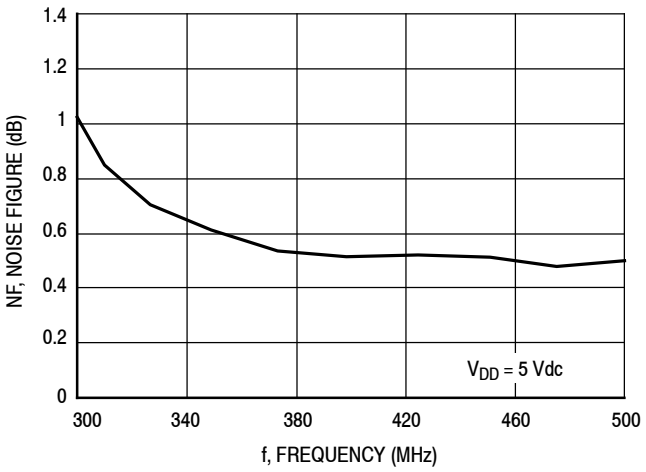


Figure 19. Noise Figure versus Frequency

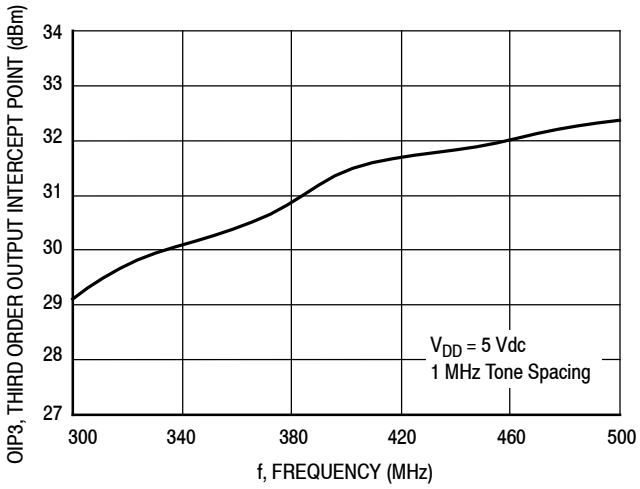


Figure 20. Third Order Output Intercept Point (Two-Tone) versus Frequency

50 OHM APPLICATION CIRCUIT: 1400 MHz

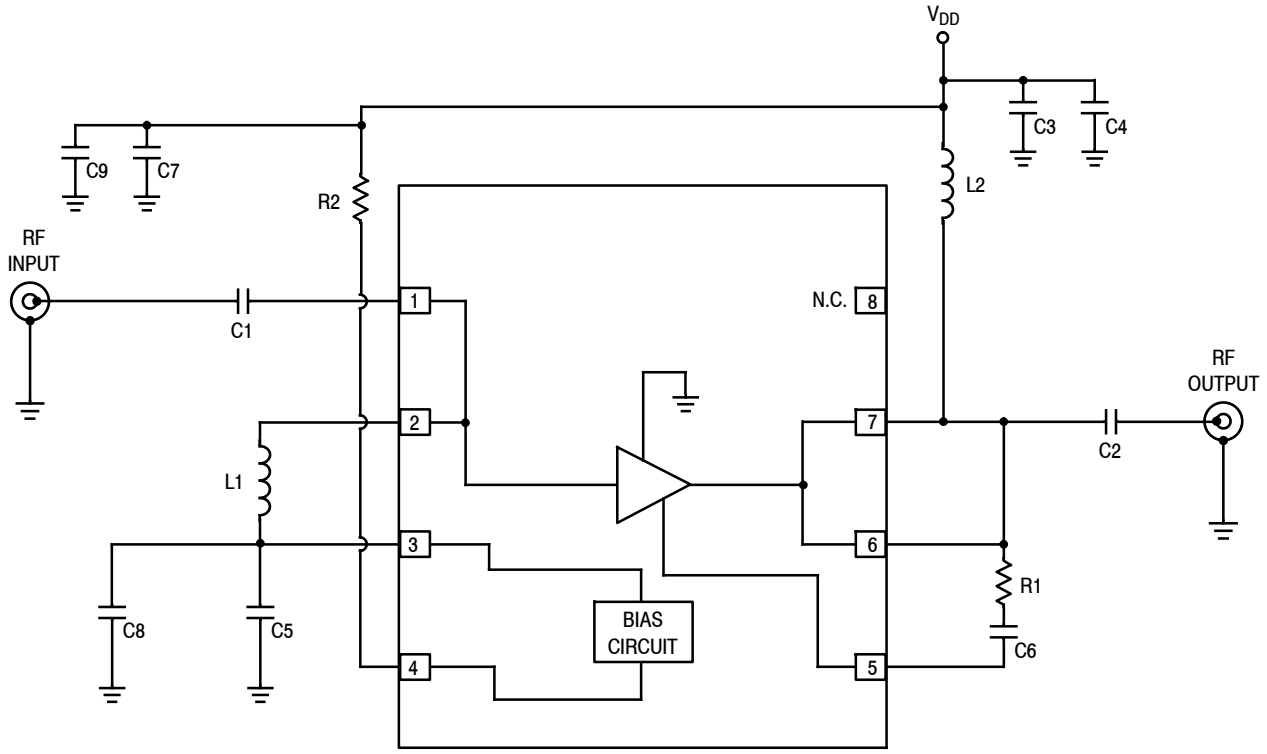
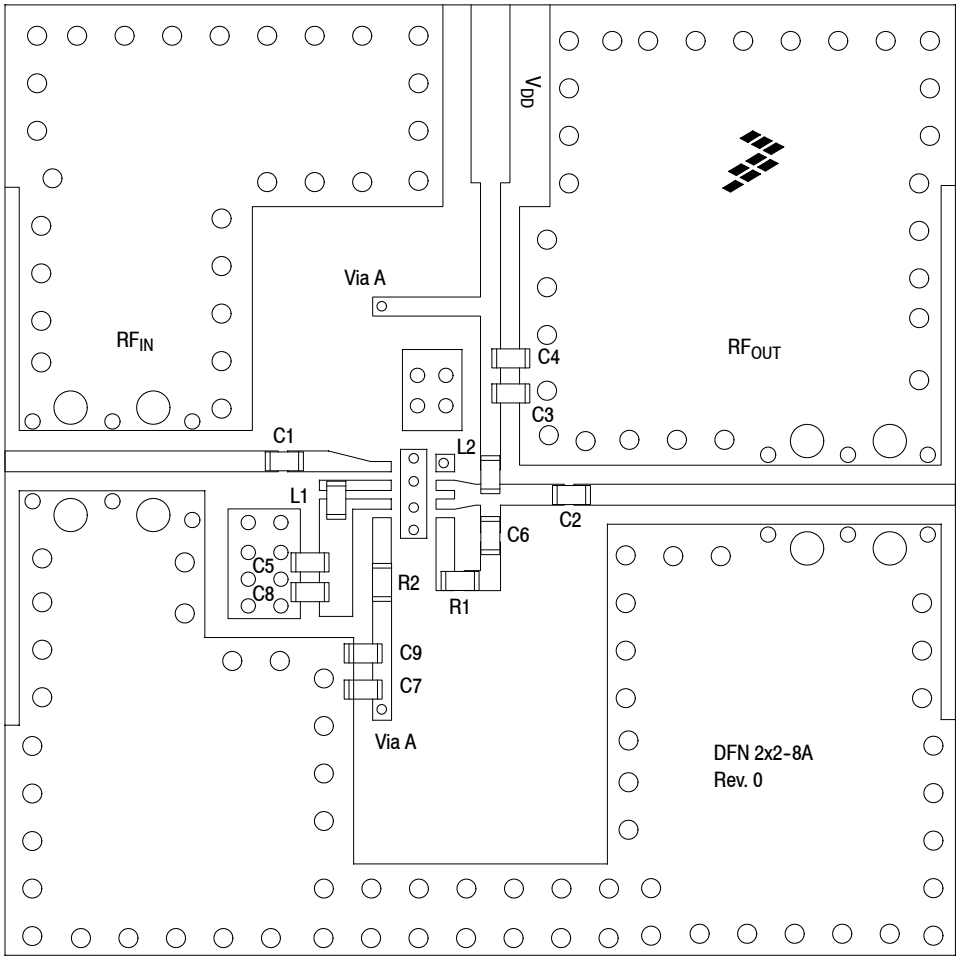


Figure 21. MML09211HT1 Test Circuit Schematic

Table 10. MML09211HT1 Test Circuit Component Designations and Values

C1	220 pF Chip Capacitor	GRM1555C1H221JA01D	Murata
C2	33 pF Chip Capacitor	GRM1555C1H330JA01D	Murata
C3	100 pF Chip Capacitor	GRM1555C1H101JA01D	Murata
C4	0.1 μF Chip Capacitor	GRM155R71C104KA88D	Murata
C5	180 pF Chip Capacitor	GRM1555C1H181JA01D	Murata
C6, C7	56 pF Chip Capacitors	GRM155C1H560JA01D	Murara
C8, C9	0.01 μF Chip Capacitors	GRM155R71E103KA01D	Murata
L1	8.7 nH Chip Inductor	0402CS-8N7XGL	Coilcraft
L2	3.9 nH Chip Inductor	0402CS-3N9XGL	Coilcraft
R1	100 Ω, 1/16 W Chip Resistor	RC0402FR-07100RL	Yageo
R2	1210 Ω, 1/16 W Chip Resistor	RC0402FR-071K21L	Yageo
PCB	0.010″, ε_r = 3.38, Multilayer	IS680-3.38	Isola

50 OHM APPLICATION CIRCUIT: 1400 MHz



NOTE: To achieve optimal noise performance, it is critical that proper biasing, input matching, supply decoupling and grounding are employed.

Figure 22. MML09211HT1 Test Circuit Component Layout

Table 10. MML09211HT1 Test Circuit Component Designations and Values

C1	220 pF Chip Capacitor	GRM1555C1H221JA01D	Murata
C2	33 pF Chip Capacitor	GRM1555C1H330JA01D	Murata
C3	100 pF Chip Capacitor	GRM1555C1H101JA01D	Murata
C4	0.1 μF Chip Capacitor	GRM155R71C104KA88D	Murata
C5	180 pF Chip Capacitor	GRM1555C1H181JA01D	Murata
C6, C7	56 pF Chip Capacitors	GRM155C1H560JA01D	Murara
C8, C9	0.01 μF Chip Capacitors	GRM155R71E103KA01D	Murata
L1	8.7 nH Chip Inductor	0402CS-8N7XGL	Coilcraft
L2	3.9 nH Chip Inductor	0402CS-3N9XGL	Coilcraft
R1	100 Ω, 1/16 W Chip Resistor	RC0402FR-07100RL	Yageo
R2	1210 Ω, 1/16 W Chip Resistor	RC0402FR-071K21L	Yageo
PCB	0.010″, ε_r = 3.38, Multilayer	IS680-3.38	Isola

(Test Circuit Component Designations and Values repeated for reference.)

50 OHM TYPICAL CHARACTERISTICS: 1400 MHz

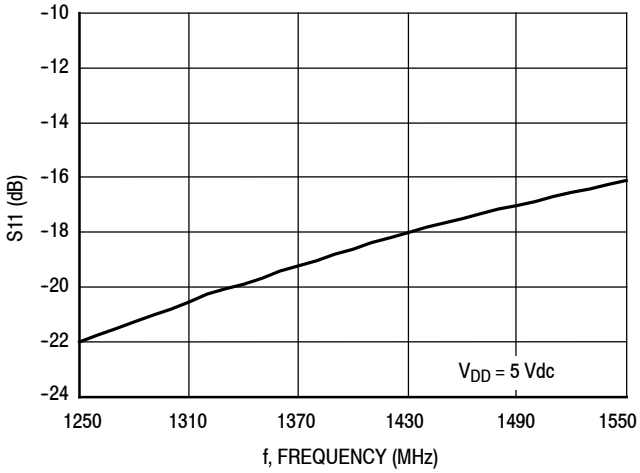


Figure 23. S11 versus Frequency

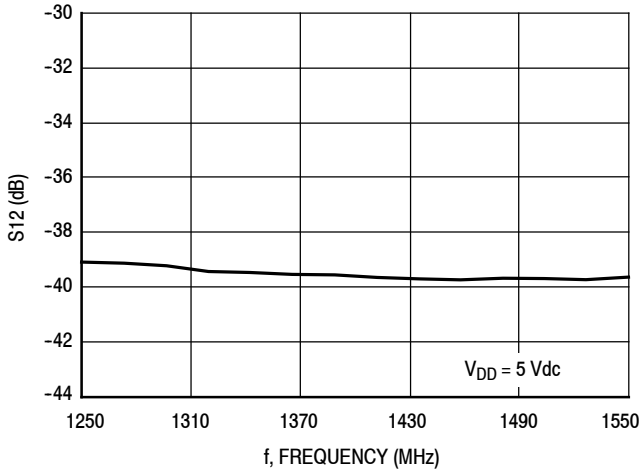


Figure 24. S12 versus Frequency

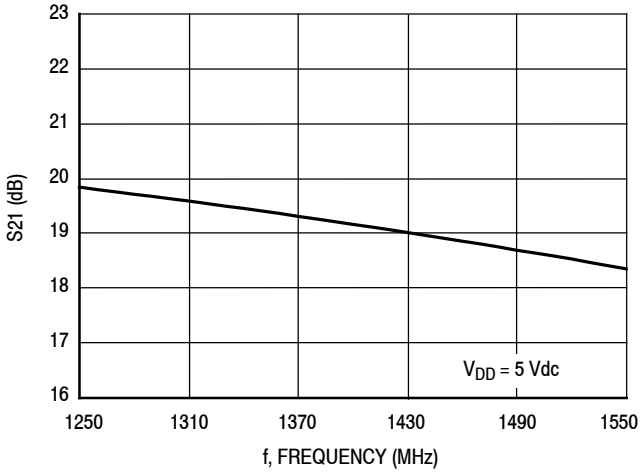


Figure 25. S21 versus Frequency

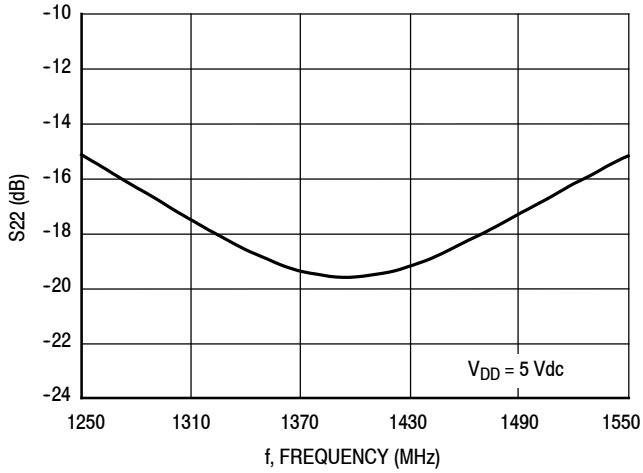


Figure 26. S22 versus Frequency

50 OHM TYPICAL CHARACTERISTICS: 1400 MHz

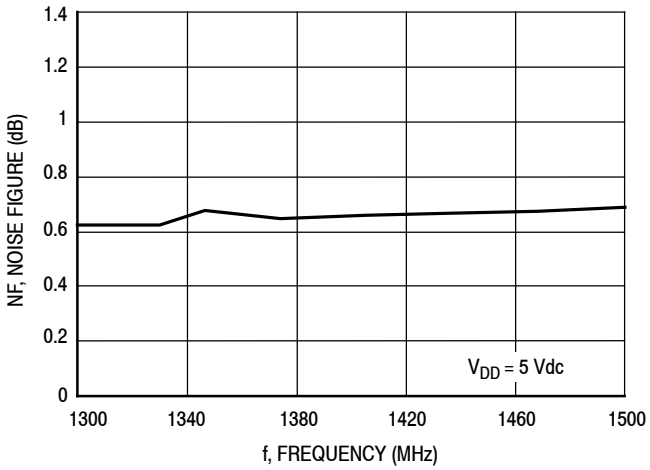


Figure 27. Noise Figure versus Frequency

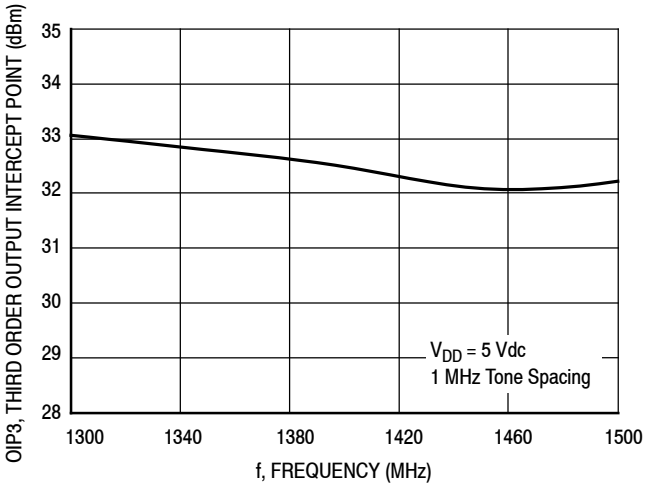


Figure 28. Third Order Output Intercept Point (Two-Tone) versus Frequency

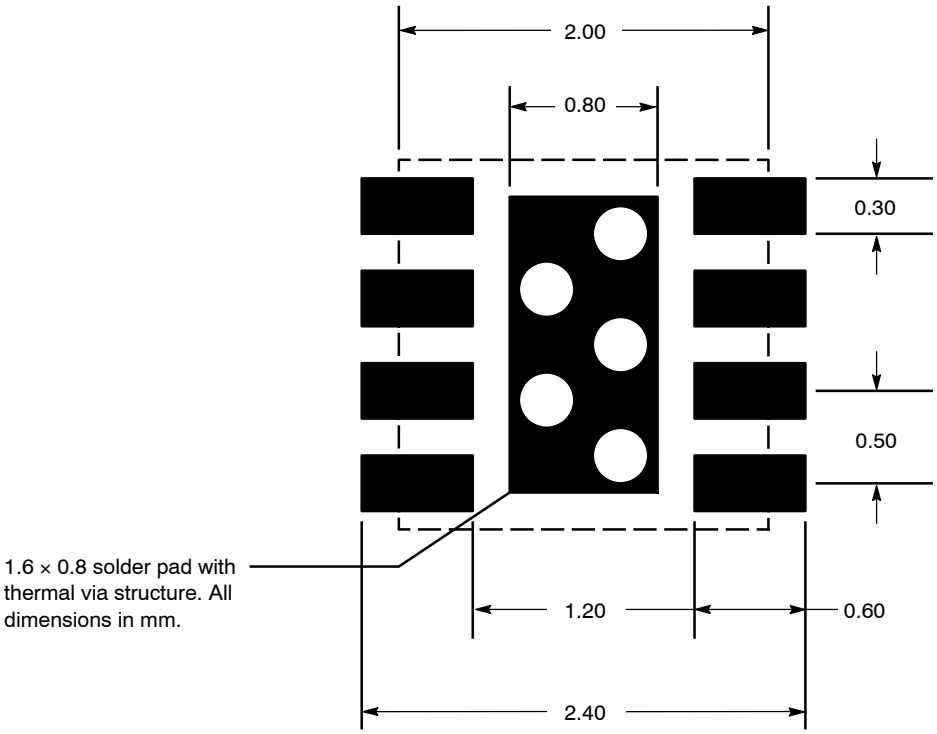


Figure 29. PCB Pad Layout for DFN 2 × 2

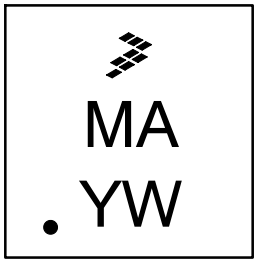
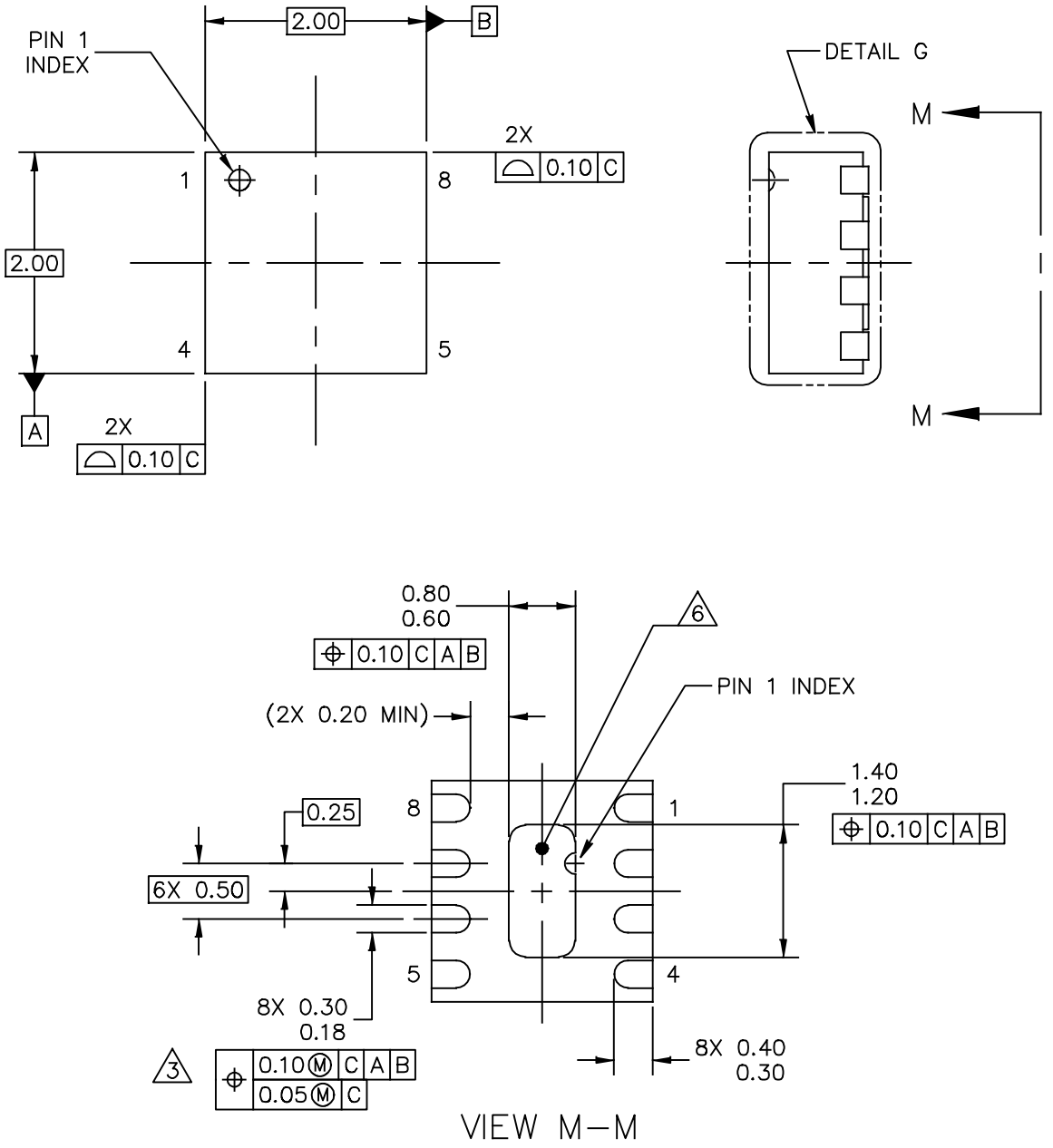


Figure 30. Product Marking

PACKAGE DIMENSIONS



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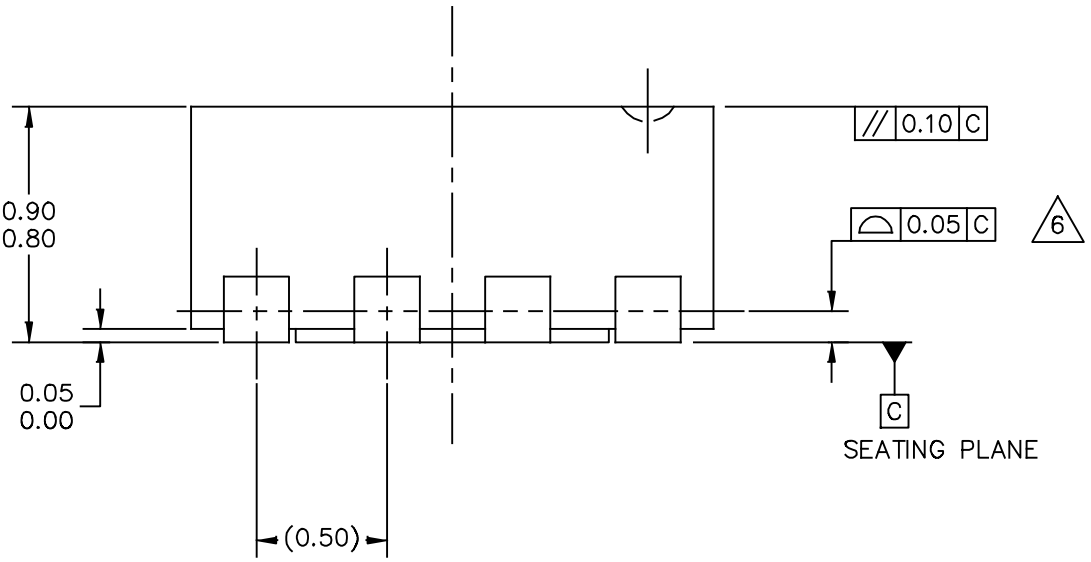
TITLE: THERMALLY ENHANCED DUAL FLAT NON–LEADED PACKAGE (DFN) 8 TERMINAL, 0.5 PITCH (2 X 2 X 0.85)	DOCUMENT NO: 98ASA00228D	REV: O
	CASE NUMBER: 2132–01	14 MAY 2010
	STANDARD: NON–JEDEC	



DETAIL G
VIEW ROTATED 90° CW

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NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5 – 2009

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMIMAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THIS DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

4. MAX. PACKAGE WARPAGE IS 0.05 mm.

5. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.

6. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

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PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to Software & Tools on the part’s Product Summary page to download the respective tool.

FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where Freescale is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local Freescale Sales Office.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2011	• Initial Release of Data Sheet
1	Sept. 2014	• Table 2, Maximum Ratings: updated Junction Temperature from 150°C to 175°C to reflect recent test results of the device, p. 1 • Table 6, ESD Protection Characteristics, removed the word “Minimum” after the ESD class rating. ESD ratings are characterized during new product development but are not 100% tested during production. ESD ratings provided in the data sheet are intended to be used as a guideline when handling ESD sensitive devices, p. 2 • Revised Failure Analysis information, p. 19

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