

NGTG35N65FL2WG

IGBT - Field Stop II

This Insulated Gate Bipolar Transistor (IGBT) features a robust and cost effective Field Stop II Trench construction, and provides superior performance in demanding switching applications, offering both low on state voltage and minimal switching loss. The IGBT is well suited for UPS and solar applications.

Features

- Extremely Efficient Trench with Field Stop Technology
- $T_{Jmax} = 175^{\circ}C$
- Optimized for High Speed Switching
- 5 μs Short-Circuit Capability
- These are Pb-Free Devices

Typical Applications

- Solar Inverters
- Uninterruptible Power Supplies (UPS)
- Welding

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-emitter voltage	V_{CES}	650	V
Collector current @ $T_c = 25^{\circ}C$ @ $T_c = 100^{\circ}C$	I_c	70 35	A
Pulsed collector current, T_{pulse} limited by T_{Jmax}	I_{CM}	120	A
Short-circuit withstand time $V_{GE} = 15 V, V_{CE} = 400 V,$ $T_J \leq +150^{\circ}C$	t_{SC}	5	μs
Gate-emitter voltage	V_{GE}	± 20	V
Transient gate-emitter voltage ($T_{PULSE} = 5 \mu s, D < 0.10$)		± 30	V
Power Dissipation @ $T_c = 25^{\circ}C$ @ $T_c = 100^{\circ}C$	P_D	300 150	W
Operating junction temperature range	T_J	-55 to $+175$	$^{\circ}C$
Storage temperature range	T_{stg}	-55 to $+175$	$^{\circ}C$
Lead temperature for soldering, 1/8" from case for 5 seconds	T_{SLD}	260	$^{\circ}C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



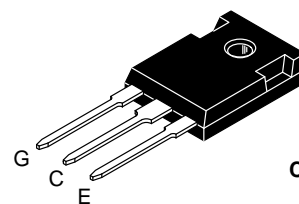
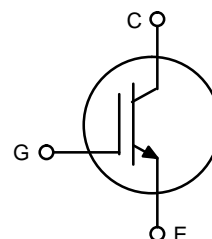
ON Semiconductor[®]

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35 A, 650 V

$V_{CEsat} = 1.70 V$

$E_{OFF} = 0.28 mJ$



**TO-247
CASE 340L
STYLE 4**

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
NGTG35N65FL2WG	TO-247 (Pb-Free)	30 Units / Rail

NGTG35N65FL2WG

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal resistance junction-to-case, for IGBT	$R_{\theta JC}$	0.50	°C/W
Thermal resistance junction-to-ambient	$R_{\theta JA}$	40	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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STATIC CHARACTERISTIC

Collector-emitter breakdown voltage, gate-emitter short-circuited	$V_{GE} = 0\text{ V}, I_C = 500\ \mu\text{A}$	$V_{(BR)CES}$	650	–	–	V
Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}, I_C = 35\text{ A}$ $V_{GE} = 15\text{ V}, I_C = 35\text{ A}, T_J = 175^\circ\text{C}$	V_{CEsat}	1.50 –	1.70 2.20	2.00 –	V
Gate-emitter threshold voltage	$V_{GE} = V_{CE}, I_C = 350\ \mu\text{A}$	$V_{GE(th)}$	4.5	5.5	6.5	V
Collector-emitter cut-off current, gate-emitter short-circuited	$V_{GE} = 0\text{ V}, V_{CE} = 650\text{ V}$ $V_{GE} = 0\text{ V}, V_{CE} = 650\text{ V}, T_J = 175^\circ\text{C}$	I_{CES}	– –	– –	0.5 4.0	mA
Gate leakage current, collector-emitter short-circuited	$V_{GE} = 20\text{ V}, V_{CE} = 0\text{ V}$	I_{GES}	–	–	200	nA

DYNAMIC CHARACTERISTIC

Input capacitance	$V_{CE} = 20\text{ V}, V_{GE} = 0\text{ V}, f = 1\text{ MHz}$	C_{ies}	–	3115	–	pF
Output capacitance		C_{oes}	–	149	–	
Reverse transfer capacitance		C_{res}	–	88	–	
Gate charge total	$V_{CE} = 480\text{ V}, I_C = 35\text{ A}, V_{GE} = 15\text{ V}$	Q_g	–	125	–	nC
Gate to emitter charge		Q_{ge}	–	30	–	
Gate to collector charge		Q_{gc}	–	63	–	

SWITCHING CHARACTERISTIC, INDUCTIVE LOAD

Turn-on delay time	$T_J = 25^\circ\text{C}$ $V_{CC} = 400\text{ V}, I_C = 35\text{ A}$ $R_g = 10\ \Omega$ $V_{GE} = 0\text{ V}/15\text{ V}^*$	$t_{d(on)}$	–	72	–	ns	
Rise time		t_r	–	40	–		
Turn-off delay time		$t_{d(off)}$	–	132	–		
Fall time			t_f	–	75	–	mJ
Turn-on switching loss		E_{on}	–	0.84	–		
Turn-off switching loss		E_{off}	–	0.28	–		
Total switching loss		E_{ts}	–	1.12	–		
Turn-on delay time	$T_J = 150^\circ\text{C}$ $V_{CC} = 400\text{ V}, I_C = 35\text{ A}$ $R_g = 10\ \Omega$ $V_{GE} = 0\text{ V}/15\text{ V}^*$	$t_{d(on)}$	–	70	–	ns	
Rise time		t_r	–	38	–		
Turn-off delay time		$t_{d(off)}$	–	135	–		
Fall time			t_f	–	96	–	mJ
Turn-on switching loss		E_{on}	–	1.05	–		
Turn-off switching loss		E_{off}	–	0.50	–		
Total switching loss		E_{ts}	–	1.55	–		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Includes diode reverse recovery loss using NGTG35N65FL2WG.

NGTG35N65FL2WG

TYPICAL CHARACTERISTICS

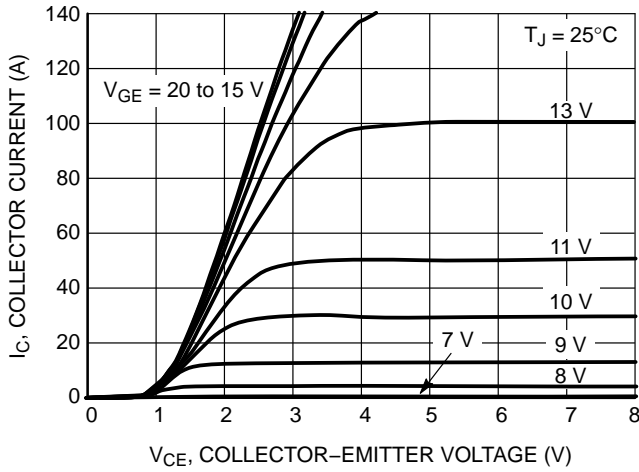


Figure 1. Output Characteristics

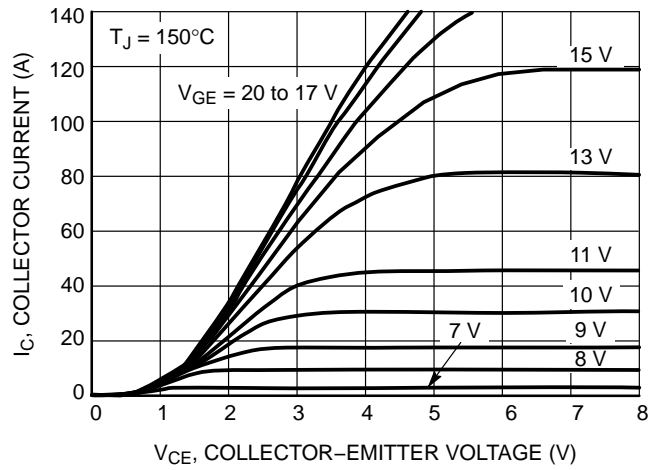


Figure 2. Output Characteristics

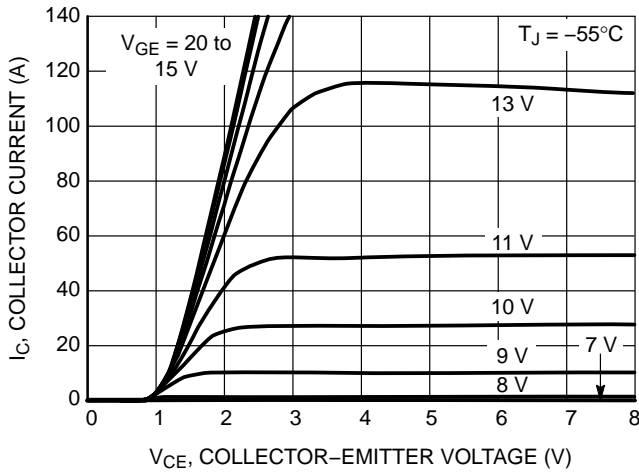


Figure 3. Output Characteristics

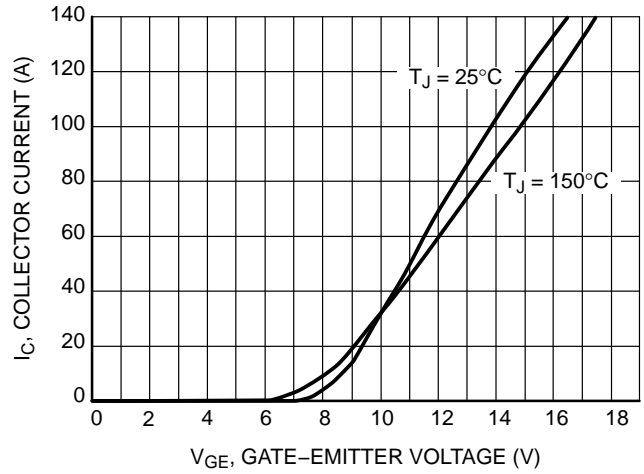


Figure 4. Typical Transfer Characteristics

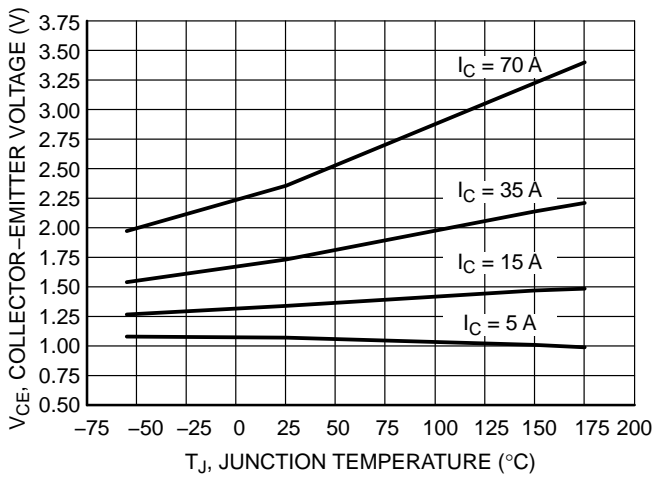


Figure 5. $V_{CE(sat)}$ vs. T_J

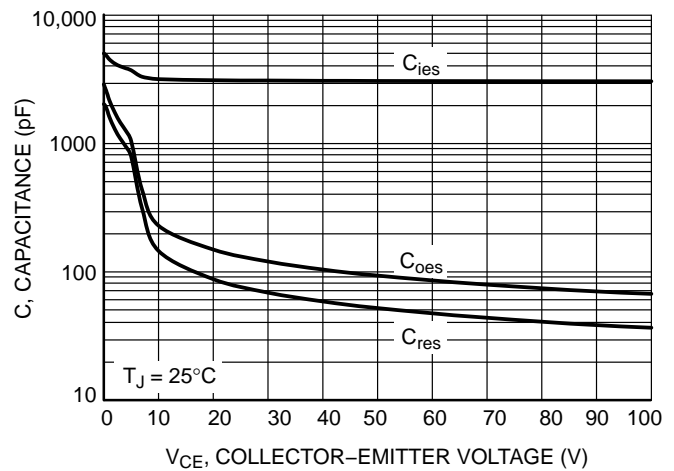


Figure 6. Typical Capacitance

NGTG35N65FL2WG

TYPICAL CHARACTERISTICS

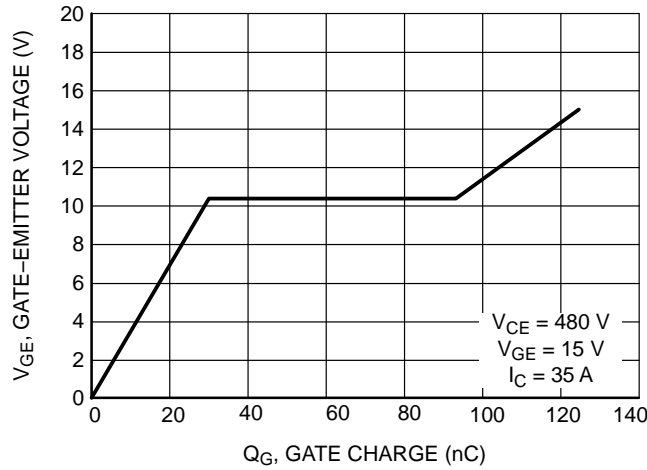


Figure 7. Typical Gate Charge

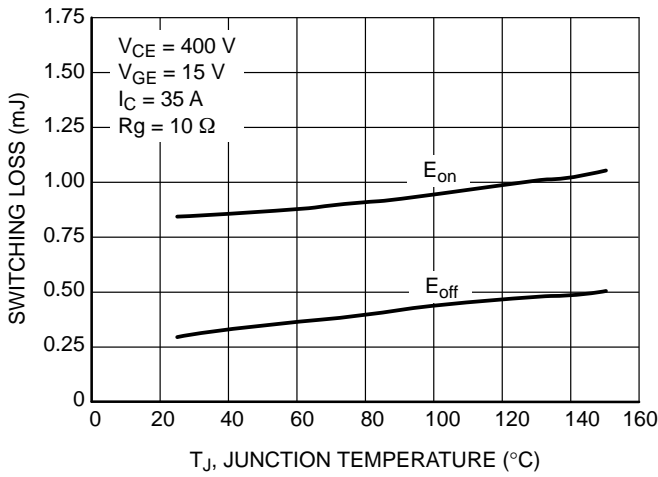


Figure 8. Switching Loss vs. Temperature

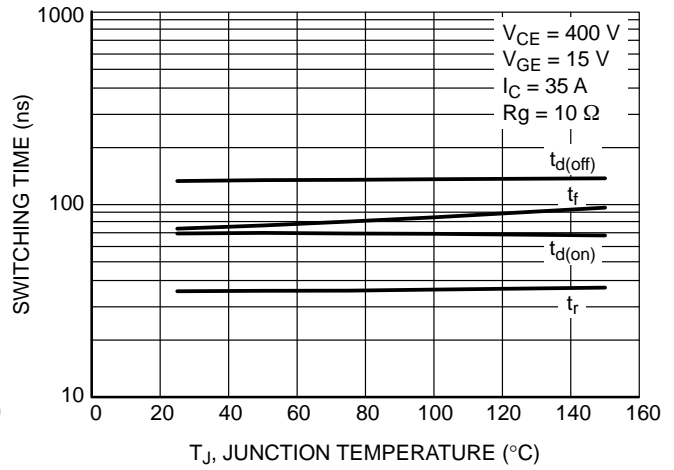


Figure 9. Switching Time vs. Temperature

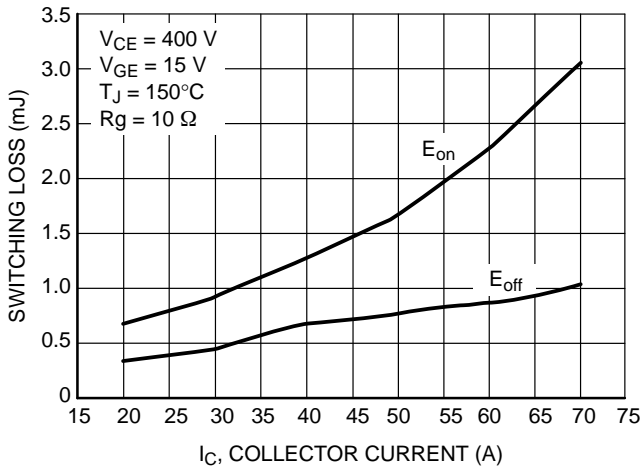


Figure 10. Switching Loss vs. I_C

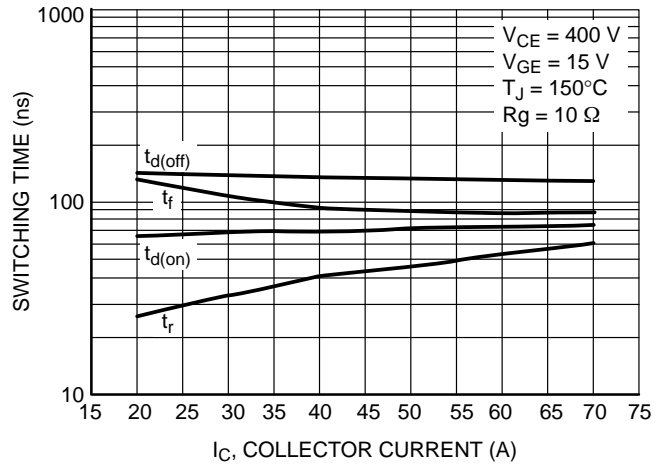


Figure 11. Switching Time vs. I_C

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TYPICAL CHARACTERISTICS

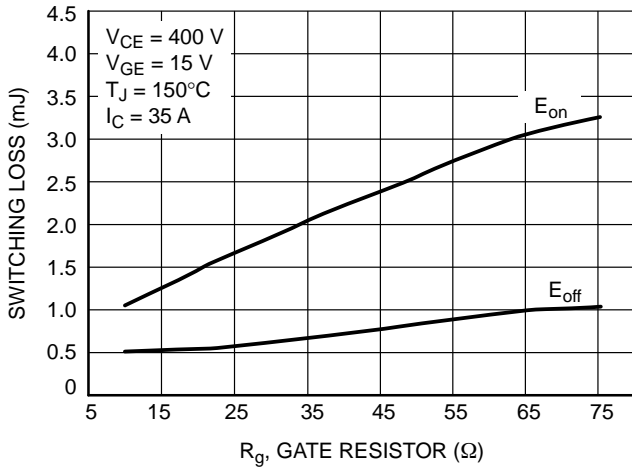


Figure 12. Switching Loss vs. R_g

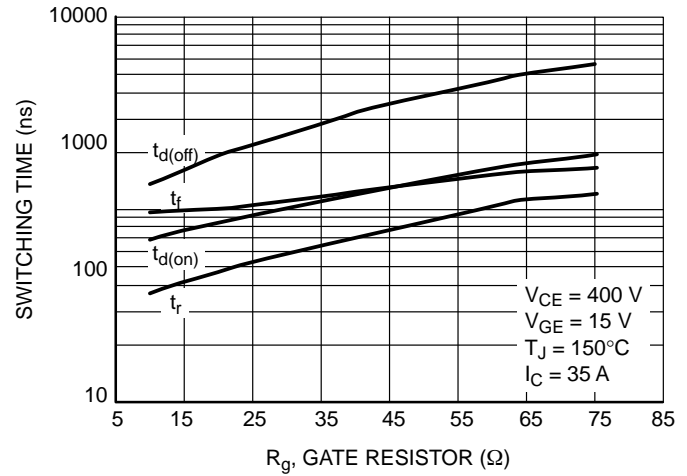


Figure 13. Switching Time vs. R_g

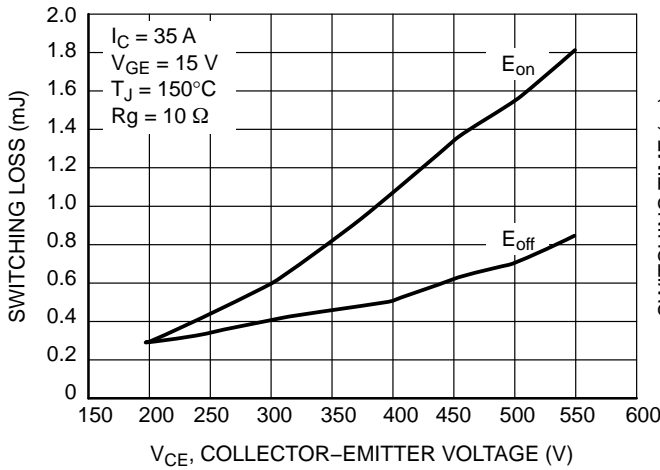


Figure 14. Switching Loss vs. V_{CE}

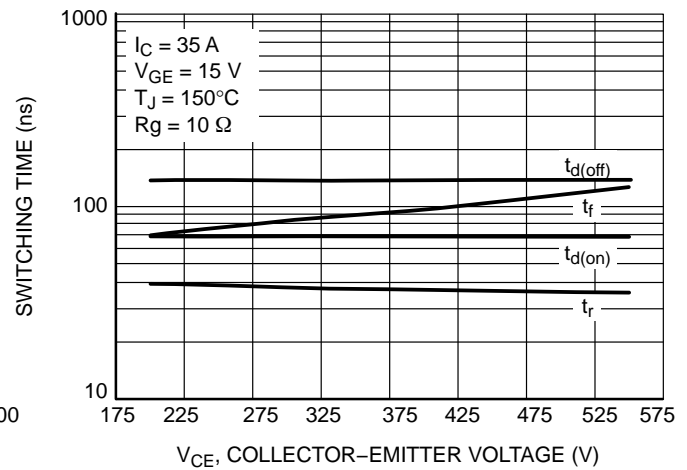


Figure 15. Switching Time vs. V_{CE}

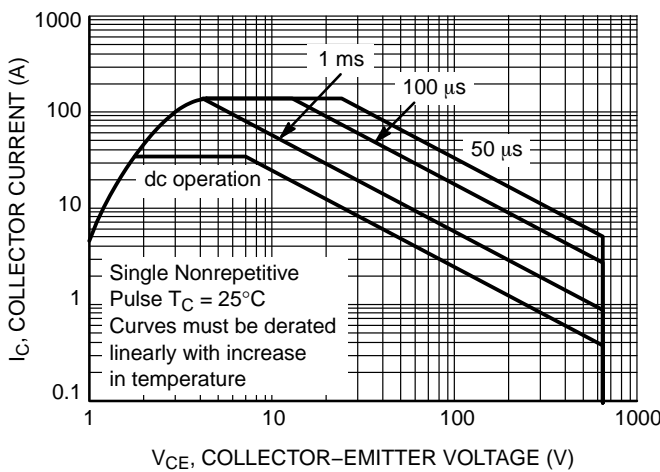


Figure 16. Safe Operating Area

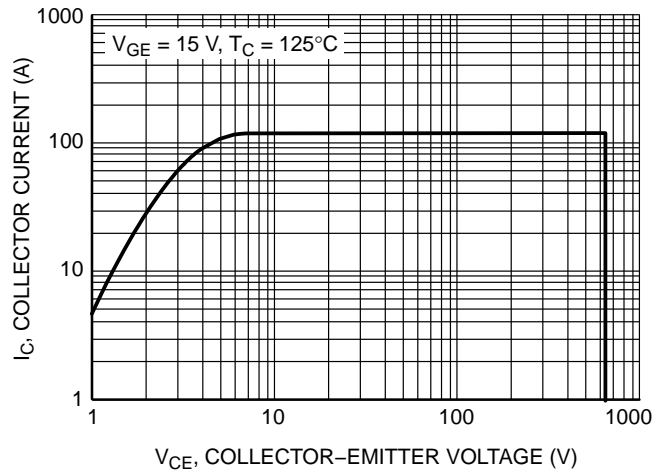


Figure 17. Reverse Bias Safe Operating Area

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TYPICAL CHARACTERISTICS

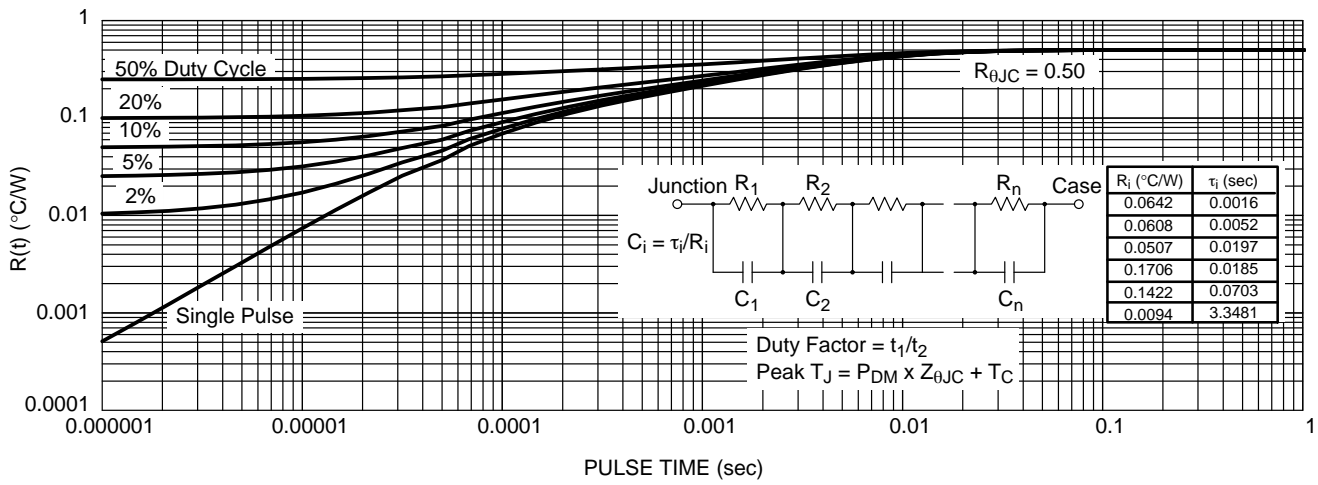


Figure 18. IGBT Transient Thermal Impedance

MECHANICAL CASE OUTLINE

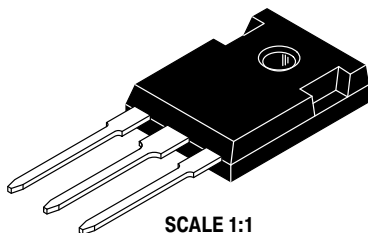
PACKAGE DIMENSIONS

ON Semiconductor®

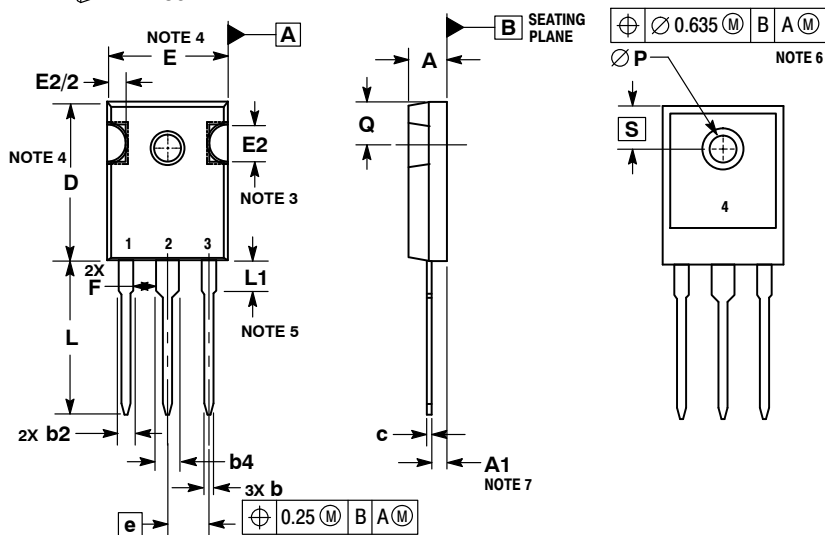


TO-247
CASE 340AL
ISSUE D

DATE 17 MAR 2017



SCALE 1:1

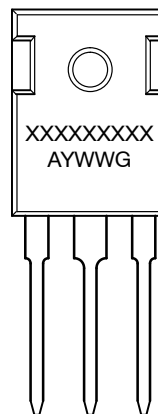


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. SLOT REQUIRED, NOTCH MAY BE ROUNDED.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
5. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.
6. ØP SHALL HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM DIAMETER OF 3.91.
7. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.

MILLIMETERS		
DIM	MIN	MAX
A	4.70	5.30
A1	2.20	2.60
b	1.07	1.33
b2	1.65	2.35
b4	2.60	3.40
c	0.45	0.68
D	20.80	21.34
E	15.50	16.25
E2	4.32	5.49
e	5.45 BSC	
F	2.655	---
L	19.80	20.80
L1	3.81	4.32
P	3.55	3.65
Q	5.40	6.20
S	6.15 BSC	

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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