User's Guide

SLVU404–September 2010

TLV7101828EVM-595

This user's guide describes the characteristics, operation, and use of the TLV7101828EVM-595 Evaluation Module (EVM) as a reference design for engineering demonstration and evaluation of the TLV710xxxx dual-channel, low-dropout (LDO) linear regulator. Included in this user's guide are setup instructions, a schematic diagram, layout and thermal guidelines, a bill of materials, and test results.

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1 Introduction

The Texas Instruments TLV7101828EVM-595 EVM helps designers evaluate the operation and performance of the TLV710xxxx family of linear regulators for possible use in their circuit applications. This particular integrated circuit (IC) configuration contains two separate linear regulators with separate thermal and current-limit shutdowns, and separate enable circuitry in an extremely small, 1.5-mm x 1.5-mm package. Each channel is simultaneously capable of delivering up to 200 mA of load current depending on thermal/layout considerations and input/output voltage drops across the part. The TLV710xxxx does not require an input capacitor, and the output capacitor only need be 0.1 µF (effective minimum) for stability; however, for conservative design practice accounting for widely varying noise environments and dynamic line/load conditions, a 1-µF capacitor has been employed at the input and both output ports.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TLV7101828EVM-595.

2.1 *Input/Output Connectors and Jumper Descriptions*

- **J1 (VIN) –** The positive input supply voltage connector. Twist the positive input lead and ground lead, and keep them as short as possible to minimize EMI transmission. Additional bulk capacitance must be added between J1 and J2 if the supply leads are greater than six inches. An additional 47-µF or greater capacitor improves the transient response of the TLV710xxxx and reduces ringing on the input due to long wire connections.
- **J2 (GND) –** Ground-return connection for the input power supply.
- **J3 (OUT 1) –** Channel 1, positive voltage, output connector.
- **J4 (GND) –** Channel 1, output ground-return connector.
- **J5 (OUT 2) –** Channel 2, positive voltage, output connector.
- **J6 (GND) –** Channel 2, output ground-return connector.
- **JP1 (EN1) –** Channel 1, output enable. To enable the channel 1 output, connect a jumper to short the VIN pin 1 to the EN1 center pin 2. To disable the channel 1 output, connect the jumper between the EN1 center pin 2 and GND pin 3.
- **JP2 (EN2) –** Channel 2, output enable. To enable the channel 2 output, connect a jumper to short the VIN pin 1 to the EN2 center pin 2. To disable the channel 1 output, connect the jumper between the EN2 center pin 2 and GND pin 3.

2.2 *Soldering Guidelines*

Any solder re-work to modify the EVM for the purpose of repair or other application reasons must be performed using a hot-air system to avoid damaging the integrated circuit IC especially.

2.3 *Equipment Interconnect*

- Turn off the input power supply after verifying that its output voltage is less than 5.5 V. Connect the positive voltage lead from input power supply to the JP1 connector of the EVM. Connect the ground lead from the input power supply to JP2 of the EVM.
- Connect a 0-mA to 200-mA load between the positive output of channel 1, OUT 1 – JP3, and the channel 1 ground connection, JP4.
- Connect a 0-mA to 200-mA load between the positive output of channel 2, OUT 2 – JP5, and the channel 2 ground connection, JP6.
- Disable OUT 1 by jumpering JP1 – EN1 to GND.
- Disable OUT 2 by jumpering JP2 – EN2 to GND.

3 Operation

- Turn on the input power supply. For initial operation, it is recommended that the input power supply, VIN – JP1, be set to 3.6 V.
- Enable OUT 1 and or OUT 2 as desired – reconnect the jumper on JP1 (and or JP2) from EN1 (EN2)

to VIN.

- Vary the respective loads and VIN voltages as necessary for test purposes.

4 Test Results

This section provides typical performance waveforms for the TLV7101828EVM-595 printed-circuit board.

4.1 Turnon Sequence

Figure 1 shows the turnon sequence for the case where the enable is connected to the VIN voltage. The VIN turnon voltage rises to 4 V followed by an approximate 50-µs delay preceding the simultaneous ramp up of the two output voltages. These two output voltages are completely independent, and the ramp rates are set by design. The output voltage startup ramp is not load dependant.

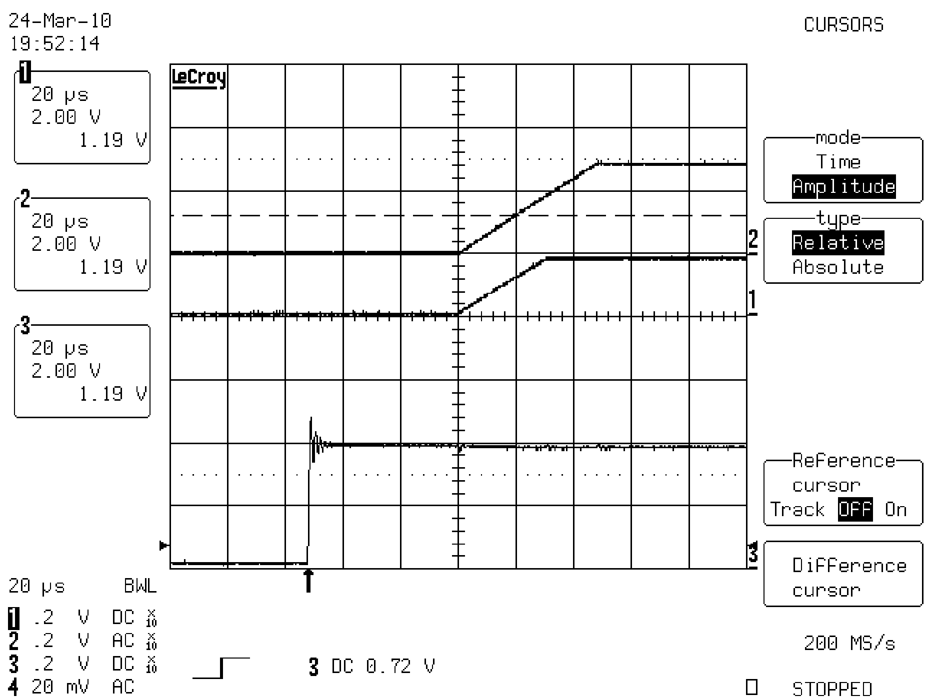


Figure 1. Turnon Sequence: Ch 3 VIN – Turnon to 4 V, Ch2 OUT 2 – 2.8-V Turnon Ramp, Ch1 OUT 1 – 1.8-V Turnon Ramp

4.2 OUT 1 Load Transient

Figure 2 shows the load transient response – oscilloscope channel 1 – for a 90-mA to 180-mA load transient applied to OUT 1 (1.8-V output). Oscilloscope channel 2 shows the crosstalk coupling from the LDO OUT 1 channel into OUT 2, where OUT 2 is loaded with 200 mAdc. Oscilloscope channel 4 shows the approximate load current transient.

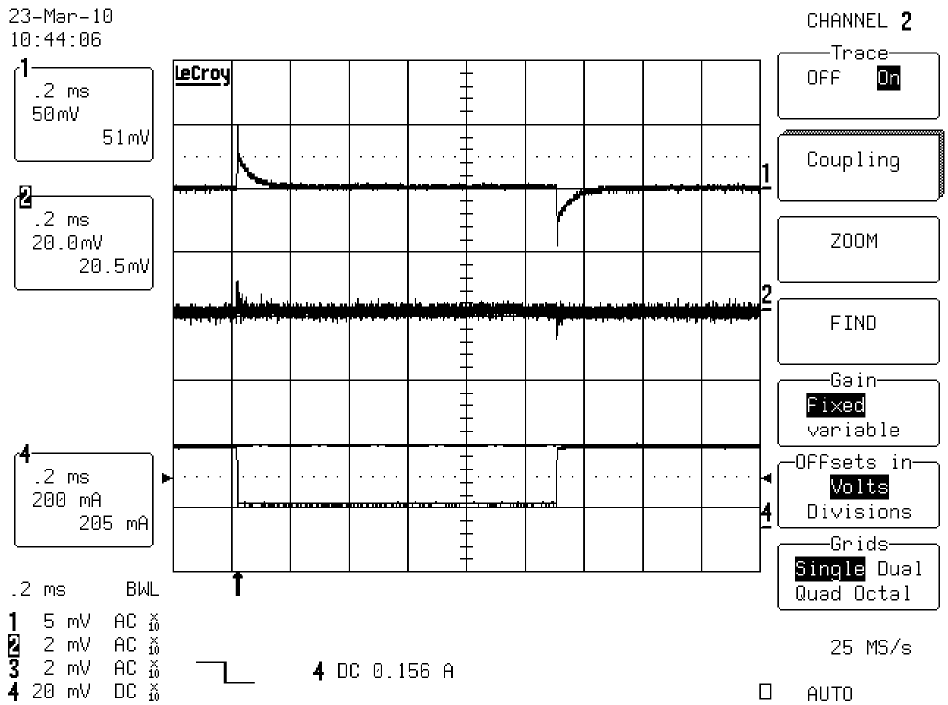


Figure 2. Ch 1 OUT 1 -1.8-V Load Transient Response for VIN at 3.3 V, Ch2 OUT 2 – 2.8-V Crosstalk Response, Ch 4 OUT 1 Load Current Transient

4.3 OUT 2 Load Transient

Figure 2 shows the load transient response – oscilloscope channel 1 – for a 90-mA to 180-mA load transient applied to OUT 1 (1.8-V output). Oscilloscope channel 2 shows the crosstalk coupling from the LDO OUT 1 channel into OUT 2, where OUT 2 is loaded with 200 mAdc. Oscilloscope channel 4 illustrates the approximate load current transient.

Figure 3 shows the load transient response – oscilloscope channel 2 – for a 90-mA to 180-mA load transient applied to OUT 2 (2.8-V output). Oscilloscope channel 1 shows the crosstalk coupling from the LDO OUT 2 channel into OUT 1, where OUT 1 is loaded with 200 mAdc. Oscilloscope channel 4 illustrates the approximate load current transient.

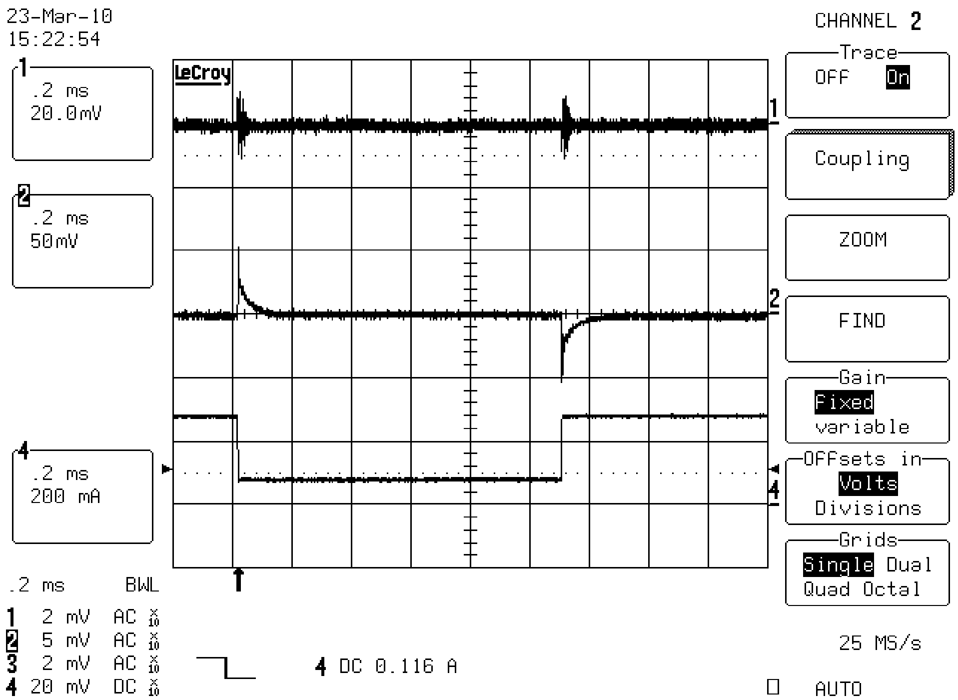


Figure 3. Ch 1 OUT 1 -1.8-V Crosstalk Response, Ch2 OUT 2 – 2.8-V Transient Response for VIN at 3.3-V, Ch 3 OUT 2 Load Current Transient

5 Thermal Guidelines

Thermal management is a key component of design of any power converter and is especially important when the power dissipation in the LDO is high. Use the following formula to approximate the maximum power dissipation for the particular ambient temperature:

$$T_j = T_a + Pd \times \theta_{ja}$$

where T_j is the junction temperature, T_a is the ambient temperature, P_d is the power dissipation in the device, and θ_{ja} is the thermal resistance from junction to ambient. All temperatures are in degrees Celsius. The maximum silicon junction temperature, T_j, must not be allowed to exceed 150°C. The layout design of the copper trace and plane areas must be used effectively as thermal sinks in order to avoid T_j from exceeding the absolute maximum rating under all temperature conditions and voltage conditions across the part.

Note that because the TLV710xxxx consists of two separate LDOs in the same package, the total dissipated power, P_d, is the sum of the power dissipated in each LDO channel separately calculated as follows:

$$P_d = (Vin - Vout_1) \times Iout_1 + (Vin - Vout_2) \times Iout_2$$

where Vin is the input supply voltage at the VIN connector, $Vout_1$ is the output voltage at OUT 1, $Iout_1$ is the output load current from OUT 1, $Vout_2$ is the output voltage at OUT_2, and $Iout_2$ is the output load current from OUT 2.

The thermal design of the PCB must be carefully considered in the layout. It is difficult to calculate the thermal resistance for a custom layout with a unique copper area attached to each pin of the IC. repeats information from the Dissipation Ratings Table of the TPS710xx data sheet for comparison with the thermal resistance, θ_{ja}, calculated for this EVM to show the wide variation in thermal resistances for given copper areas. The high-K value is determined using a standard JEDEC high-k (2s2p) board with dimensions of 3 inch x 30 inch with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

Table 1. Thermal Resistance, θ_ja , and Maximum Power Dissipation

Board	Package	θ_ja	Maximum Dissipation Without Derating (T_A = 25°C)	Maximum Dissipation Without Derating (T_A = 70d°C)
High-K	DSE	206°C/W	485 mW	269 mW
TPS710xxEVM-595	DSE	120°C/W	833 mW	458 mW

The thermal resistance for the TPS710xxEVM-595, θ_ja, is the measured value for this particular layout scheme. The maximum power dissipation is proportional to the volume of copper volume connected to the package.

6 Board Layout

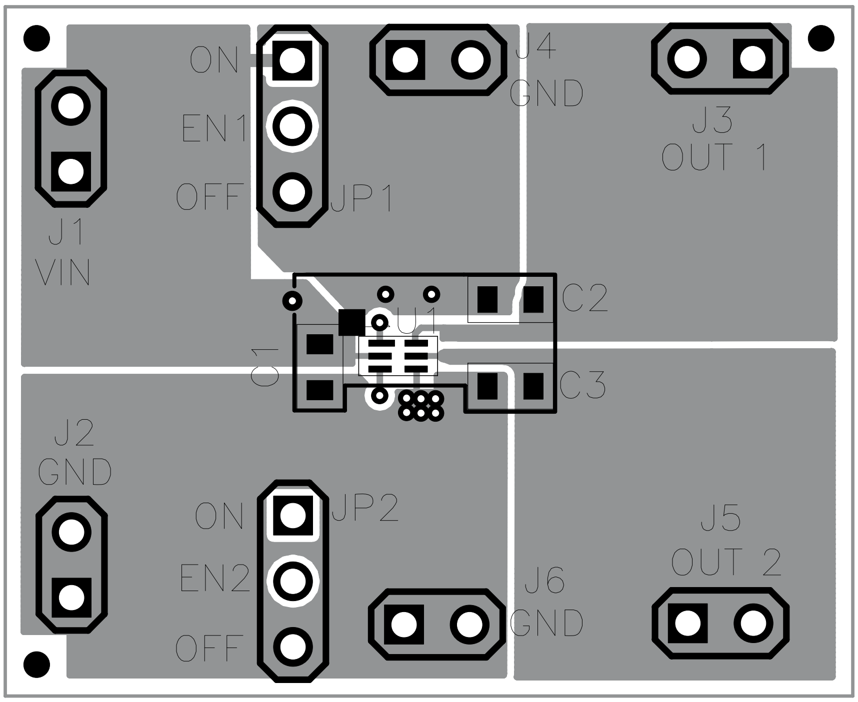


Figure 4. Assembly Layer

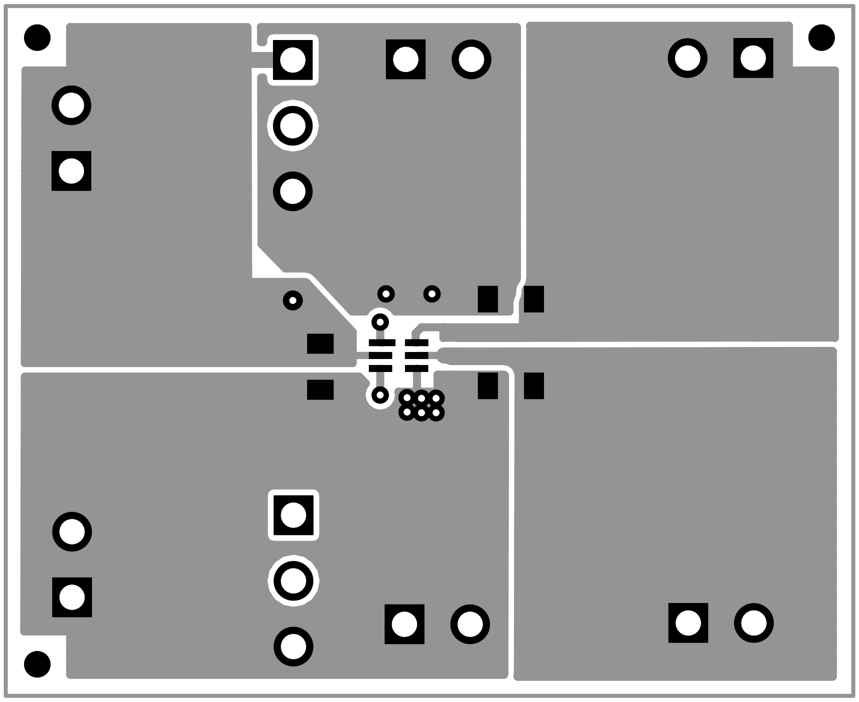


Figure 5. Layer One Routing

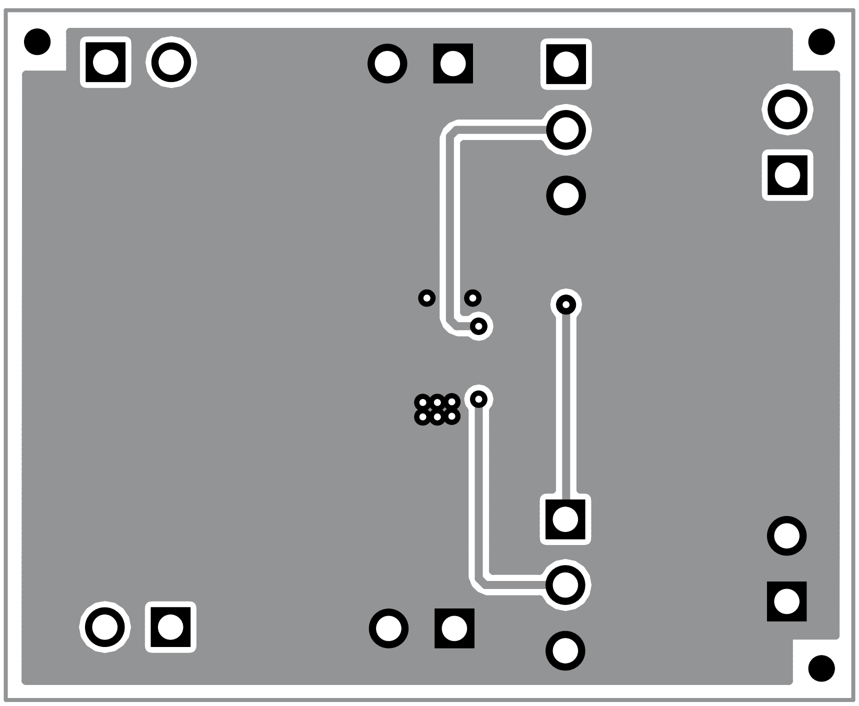


Figure 6. Layer Two Routing

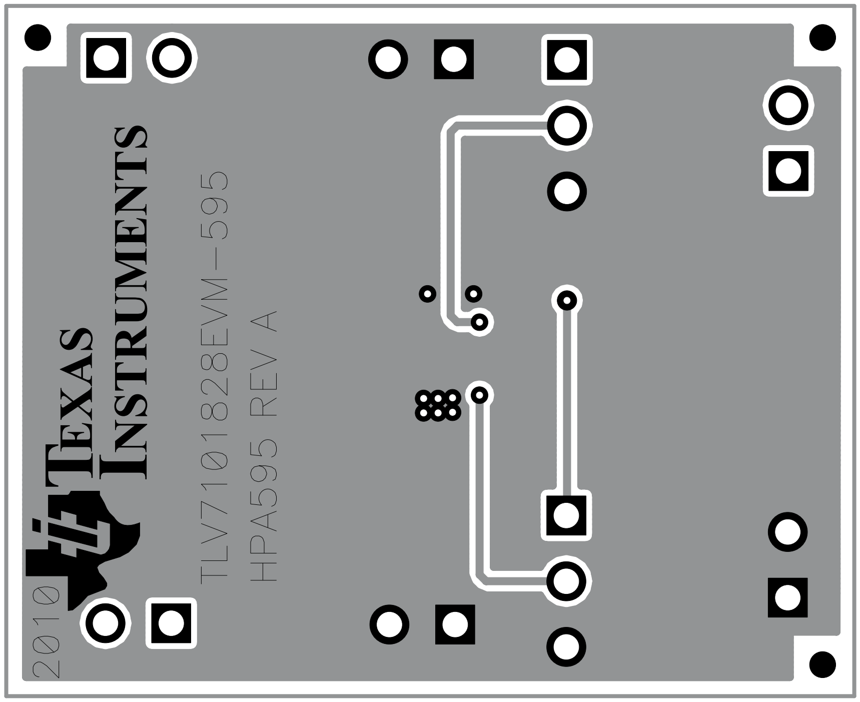
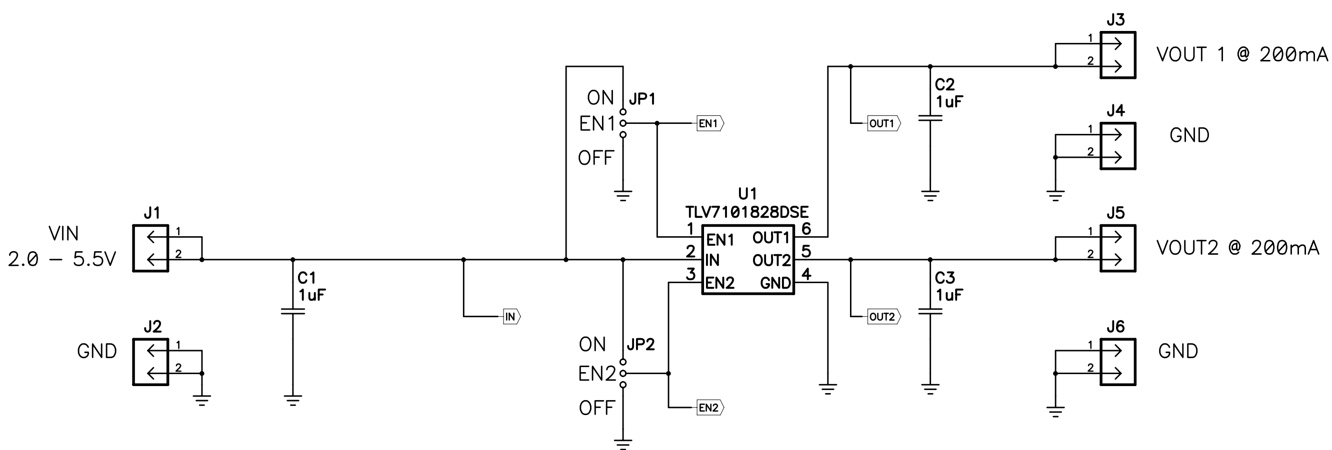


Figure 7. Bottom Layer Routing

7 Schematic and Bill of Materials

7.1 Schematic



ASSY	U1	VOUT1	VOUT2
–001	TLV7101828DSE	1.8V	2.8V

Figure 8. TLV7101828EVM-595 Schematic

7.2 Bill of Materials

Table 2. TLV7101828EVM-595 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
3	C1-C3	1 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	603	STD	STD
6	J1-J6	PEC02SAAN	Header, 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
2	JP1, JP2	PEC03SAAN	Header, 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	U1	TLV7101828DSE	IC, Dual 200mA, LDO Regulator	SON-6	TLV7101828DSE	TI
1	N/A		PCB, FR-4, 2-Layer, SMOBC,1.052 in. x 1.290 in. x 0.062 in.		HPA595	TI
2	N/A		Shunt, Open-top		151-8000	Kobiconn

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. 2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

5. Do not separate PCB

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2 V to 5.5 V and the output voltage range of 1.2 V to 4.8 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 130° C. The EVM is designed to operate properly with certain components above 130° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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