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Evaluating the ADIN1300 Robust, Industrial, Low Latency, and Low Power 10 Mbps, 100 Mbps, and 1 Gbps Ethernet PHY

FEATURES

- FMC connector for MII interface, MDIO signals, and status signals
- Accessible, surface-mount configuration resistors and dial switches
- Operates from a single, external 5 V supply

EVALUATION KIT CONTENTS

- EVAL-ADIN1300FMCZ evaluation board
- MDIO interface dongle

EQUIPMENT NEEDED

- Power supply (choose one of the following):
  - 5 V power supply rail to connect to the EXT_5V connector
  - 5 V barrel adaptor to connect to the P4 plug
- Ethernet cable
- USB cable
- PC running Windows 7 and upward

SOFTWARE NEEDED

- Ethernet PHY software and GUI (available to download on the ADIN1300 product page)

DOCUMENTS NEEDED

- ADIN1300 data sheet

GENERAL DESCRIPTION

The EVAL-ADIN1300FMCZ allows simplified evaluation of the key features of the ADIN1300 robust, industrial, low latency gigabit, 10 Mbps, 100 Mbps, and 1 Gbps, Ethernet physical layer (PHY). The EVAL-ADIN1300FMCZ is powered by a single, external, 5 V supply rail that can be supplied either via the EXT_5V connector or via the P4 plug.

All chip supplies are regulated from the 5 V rail providing supply rails required for AVDD3P3, VDD0P, and VDDIO.

The P3 field programmable gate array (FPGA) mezzanine connector (FMC) connector is provided for connection to a master FPGA system for the media access control (MAC) interface and management data input/output (MDIO) control. The P5 connector provides an alternative means for MDIO control. The EVAL-ADIN1300FMCZ is fitted with a 25 MHz crystal (Y1).

For complete specifications for the ADIN1300 device, see the ADIN1300 data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADIN1300FMCZ.

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REVISION HISTORY

10/2019—Revision 0: Initial Version

EVAL-ADIN1300FMCZ WITH OPTIONAL MDIO INTERFACE DONGLE CONNECTED

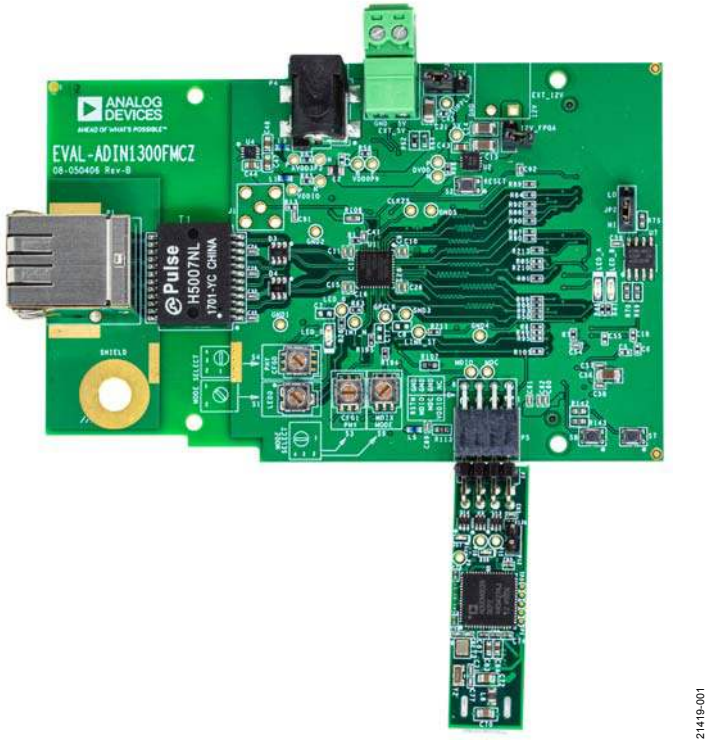

Figure 1.

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-ADIN1300FMCZ operates from a single, external, 5 V supply rail.

Apply 5 V either to the P4 plug or to the EXT_5V connector with the JP3 jumper configured for 5 V at Position A.

The rest of the EVAL-ADIN1300FMCZ power requirements are generated from the 5 V supply. Two on-board ADP223 devices generate the AVDD3P3, VDDIO, VDD0P9, and DVDD power rails. The default nominal voltages are listed in Table 1.

The VDDIO voltage rail defaults to 2.5 V with the installed components, and may be adjusted if other VDDIO voltages are required by changing the value of the R16 resistor accordingly, as shown in Table 1.

Table 1. Default Device Power Supply Configuration

Supply Rail	Nominal Voltage	Adjustment
AVDD3P3	3.3 V	Not applicable
VDDIO	2.5 V	1.8 V with R16 = 130 kΩ
		2.5 V with R16 = 200 kΩ
		3.3 V with R16 = 280 kΩ
VDD0P9	0.9 V	Not applicable
DVDD	3.3 V	Not applicable

Table 2 shows an overview of the EVAL-ADIN1300FMCZ current for various operating modes.

Table 2. EVAL-ADIN1300FMCZ Quiescent Current (EXT_5V = 5 V)

Board Status	Typical Quiescent Current
On Power-Up	30 mA initially
	6.5 mA in energy detect power down (EDPD) mode
In Hardware Power-Down (RESET_N Held Low)	6.5 mA
10BASE-Te	50 mA
100BASE-TX	60 mA
1000BASE-T	145 mA

POWER SEQUENCING

There is no particular power sequence required for the ADIN1300 device.

When using the EVAL-ADIN1300FMCZ with the MDIO interface dongle, there is a known sequence requirement for the MDIO interface dongle. The MDIO interface dongle should be powered from the USB cable prior to connection to the EVAL-ADIN1300FMCZ. Alternatively, if issues are observed, restart the GUI software to resolve any board connection issues.

EVALUATION BOARD USAGE OPTIONS

The EVAL-ADIN1300FMCZ can be used in two general modes. In standalone mode, the EVAL-ADIN1300FMCZ can be used to evaluate the ADIN1300 in IEEE 802.3 test modes, establish links with a link partner, and evaluate the performance of the chip. In standalone mode, power the EVAL-ADIN1300FMCZ with a 5 V supply at the EXT_5V connector.

Alternatively to standalone mode, the EVAL-ADIN1300FMCZ has an FMC low pin count (LPC) connector, which can be plugged into an FPGA development board. When used with an FPGA board, the media independent interfaces (MIIs), clocks, and light emitting diodes (LEDs) can be connected to the FPGA board where the MAC and upper layers can be implemented for evaluation of the ADIN1300 in a full system.

JUMPER OPTIONS

A number of jumpers on the EVAL-ADIN1300FMCZ must be set for the required operating setup before using the EVAL-ADIN1300FMCZ for evaluation. The default settings and functions of these jumper options are described in Table 3.

Table 3. Default Jumper Options and Descriptions

Link	Position	Function
JP1	Not inserted	Do not install (DNI).
JP2	B (high)	This jumper sets the write mode of U7.
		Position A (low): enable writing to the electrically erasable programmable read only memory (EEPROM).
		Position B (high): WP the EEPROM (default).
JP3	A (5V)	This jumper sets the 5 V supply source. Set to Position A.
		Position A (5V): either P4 or EXT_5V is the 5 V supply source (default).
		Position B (12V): This circuit is not installed. JP3 should always be set to Position A.

CLOCK OPTIONS

The EVAL-ADIN1300FMCZ provides the option to supply the ADIN1300 clock requirements from either an on-board crystal oscillator, or an external clock applied to the J1 connector.

The crystal oscillators on the EVAL-ADIN1300FMCZ and the MDIO interface dongle include the following:

- Y1 is a 25 MHz crystal connected across the XTAL_I pin and XTAL_O pin of the ADIN1300 on the EVAL-ADIN1300FMCZ.
- Y2 is a 32.768 kHz crystal used on the MDIO interface dongle for the on-board ADuCM3029.
- Y3 is a 26 MHz crystal used on the MDIO interface dongle for the on-board ADuCM3029.

When a 25 MHz external clock is applied to the J1 connector, the R120 resistor must be populated and the R15 and R119 resistors must be removed to disconnect the Y1 crystal. The 25 MHz clock must be a sine or square wave signal with an input range of 1.8 V to 2.5 V. See the ADIN1300 data sheet for more information.

The ADIN1300 can also be configured to provide a 25 MHz clock output on the CLK25_REF pin, which is available on the FMC connector. The source of this clock is the on-board Y1 crystal. Note that when a pin reset is applied to the ADIN1300, the clock disappears for the duration of the reset and must be reenabled via the Ethernet PHY software following the reset. This clock can be used to synchronously clock the FPGA logic. If a reset for ADIN1300 is required without CLK25_REF stopping, use a software reset instead. Alternatively, the GP_CLK pin is also available on the FMC connector and can be configured to output several different clocks from the ADIN1300. See the ADIN1300 data sheet for more information.

ON-BOARD EEPROM AND LEDS

The EVAL-ADIN1300FMCZ has two FPGA controllable LEDs and one unprogrammed, I²C EEPROM, U7.

U7 can be programmed with voltage settings to allow the FPGA board to provide the correct voltages on the supply rails. The write address of the EEPROM is 0b[10100 [GA1] [GA0] 0] and the read address is 0b[10100 [GA1] [GA0] 1].

ADIN1300 LED PIN

There is one LED pin (LED_0) on the ADIN1300. The LED_0 pin can be configured in various operating modes using the MDIO interface dongle (see the ADIN1300 data sheet). By default, the LED_0 pin LED illuminates when a link is established, and flashes when there is activity.

The LED_0 pin is a multifunction pin shared with the PHY_CFG0 pin configuration function. Therefore, it can be necessary for the voltage level on the LED_0 pin to be set at a certain value at power-on and reset to configure the ADIN1300 as required. See the ADIN1300 data sheet for more information on the multilevel strapping being used as part of the hardware configuration.

The LED_0 pin has a two-pole rotary switch, S1, to allow easy configuration for all modes of the PHY_CFG0 pin (as set by S4). Table 4 describes how S1 should be configured for the appropriate S4 PHY_CFG0 pin setting. The LED_0 pin is driven from the AVDD3P3 supply rail, see Figure 2.

Table 4. S1 Switch Positions

Jumper	S4, PHY_CFG0	S1 Position
JP1	Mode 3 and Mode 4	1
JP2	Mode 1 and Mode 2	2

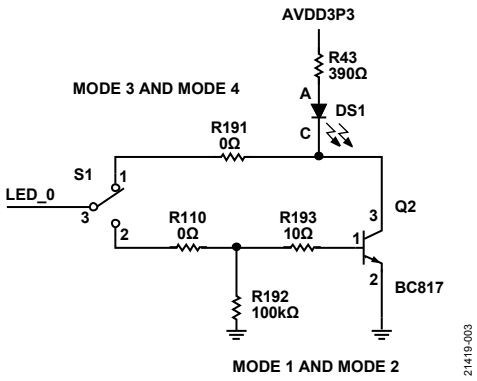

Figure 2. Hardware LED_0 Pin Configuration

MDIO INTERFACE

The MDIO interface of the ADIN1300 can be accessed directly through the P5 connector to connect the MDIO interface dongle to the PHY.

The MDIO interface dongle also allows interfacing with the EVAL-ADIN1300FMCZ via the Ethernet PHY software graphical user interface (GUI) running on the PC (see Figure 3).

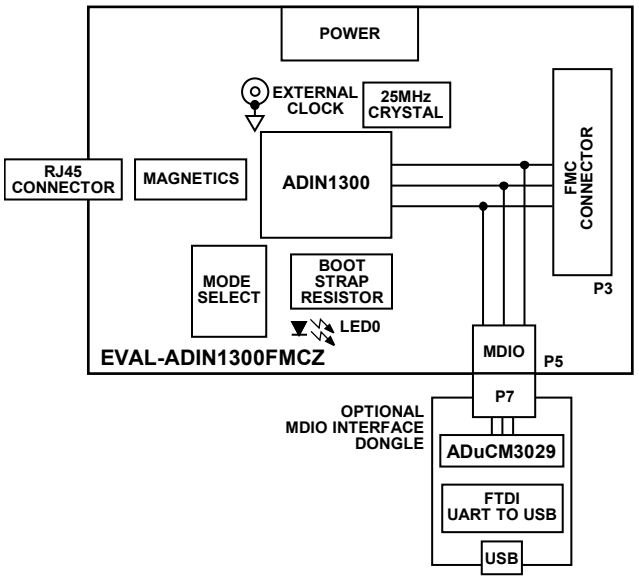

Figure 3. Simplified Overview of EVAL-ADIN1300FMCZ with MDIO Interface Dongle Connected

MDIO INTERFACE DONGLE

The MDIO interface dongle is a separate board included in the EVAL-ADIN1300FMCZ evaluation kit. The MDIO interface dongle has an on-board, ADuCM3029 microcontroller and an FDTI Chip FT232RQ, universal asynchronous receive transmitter (UART) to USB interface. The schematic for this hardware is shown in Figure 41. When using the MDIO interface dongle, connect the USB cable to the MDIO interface dongle first, then connect the MDIO interface dongle to the EVAL-ADIN1300FMCZ with the ADuCM3029 facing up (see Figure 4).

Using the MDIO interface dongle allows interaction with the ADIN1300 device via the Ethernet PHY software GUI running on the PC.

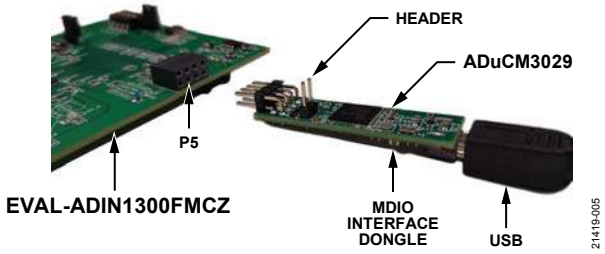

Figure 4. MDIO Interface Dongle Connection to the USB Cable and EVAL-ADIN1300FMCZ

There are two LEDs on the MDIO interface dongle, DS7 and DS8. When the powered USB cable is initially connected to the MDIO interface dongle, DS8 illuminates. When the Ethernet PHY software GUI establishes communication with the EVAL-ADIN1300FMCZ, DS7 and DS8 flash. The LEDs continue to flash while the GUI is active and the EVAL-ADIN1300FMCZ is selected as the local board within the GUI.

The MDIO interface dongle has two push-button switches on the underside of the board, S5 and S6, as shown in Figure 5. S5 is for download and reboot purposes. S6 is used to reset the on-board ADuCM3029.

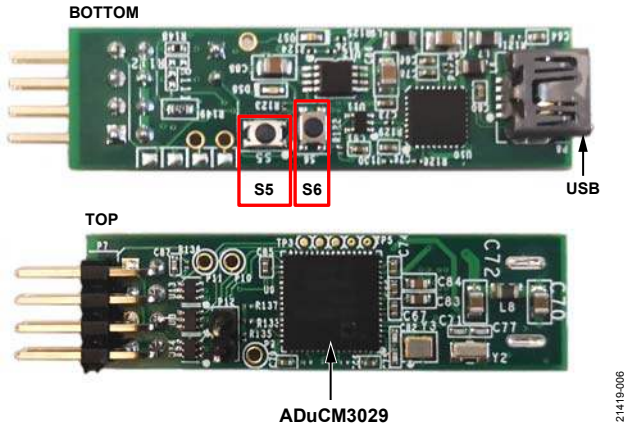

Figure 5. Overview of MDIO Interface Dongle

CONFIGURATION PINS SETUP

The EVAL-ADIN1300FMCZ default configuration and configuration options are detailed in Table 5. The ADIN1300 configuration settings can be changed by manipulating the resistors listed in the right column. See the ADIN1300 data sheet for more details on all available configuration options. Figure 6 shows the location of the resistors on the underside of the printed circuit board (PCB) of the EVAL-ADIN1300FMCZ. The speed configuration is configured via two rotary switches, S3 and S4, and the media defined interface configuration is controlled using the S9 switch. Table 5 lists the different switch configurations available.

Table 5. EVAL-ADIN1300FMCZ Configuration Settings

Configuration Option	Relevant Pins	Resistor and Switch Settings
PHY Address = 0b00000	RXD_3/PHYAD_3 RXD_2/PHYAD_2 RXD_1/PHYAD_1 RXD_0/PHYAD_0	R22, R29, R31, R37 = DNI. R23, R30, R32, R38 = DNI. Using internal pull-down resistors.
MDIX Mode Configuration	GP_CLK/RX_ER/MDIX_MODE	S9 Position1, Mode 1, manual MDI. S9 Position 2, Mode 2, manual MDIX. S9 Position 3, Mode 3, prefer MDIX. S9 Position 4, Mode 4, prefer MDI (default).

Configuration Option	Relevant Pins	Resistor and Switch Settings
PHY Configuration Downspeed, EDPD, Energy Efficient Ethernet (EEE), Software Power-Down, Forced Speed	LINK_ST/PHY_CFG1	Controlled by S1, S3, and S4 switches to provide the various configuration options (see the ADIN1300 data sheet).
	LED_0/COL/TX_ER/PHY_CFG0	Default configuration: PHY_CFG1/S3 = 1 or 2. Note that the EVAL-ADIN1300FMCZ boards are shipped in pairs with one board set to 1 and the other set to 2. PHY_CFG0 and S4 = 4, and LED_0 and S1 = 1.
MAC Interface Selection	RX_CTL/RX_DV/CRS_DV/MACIF_SEL1 RXC/RX_CLK/MACIF_SEL0	R8, R9 = DNI. R27, R28 = DNI. Using internal pull-down resistors results in MAC interface default selection being the reduced gigabit media independent interface (RGMII) MAC interface with 2 ns internal delay on the RXC pin and TXC pin.

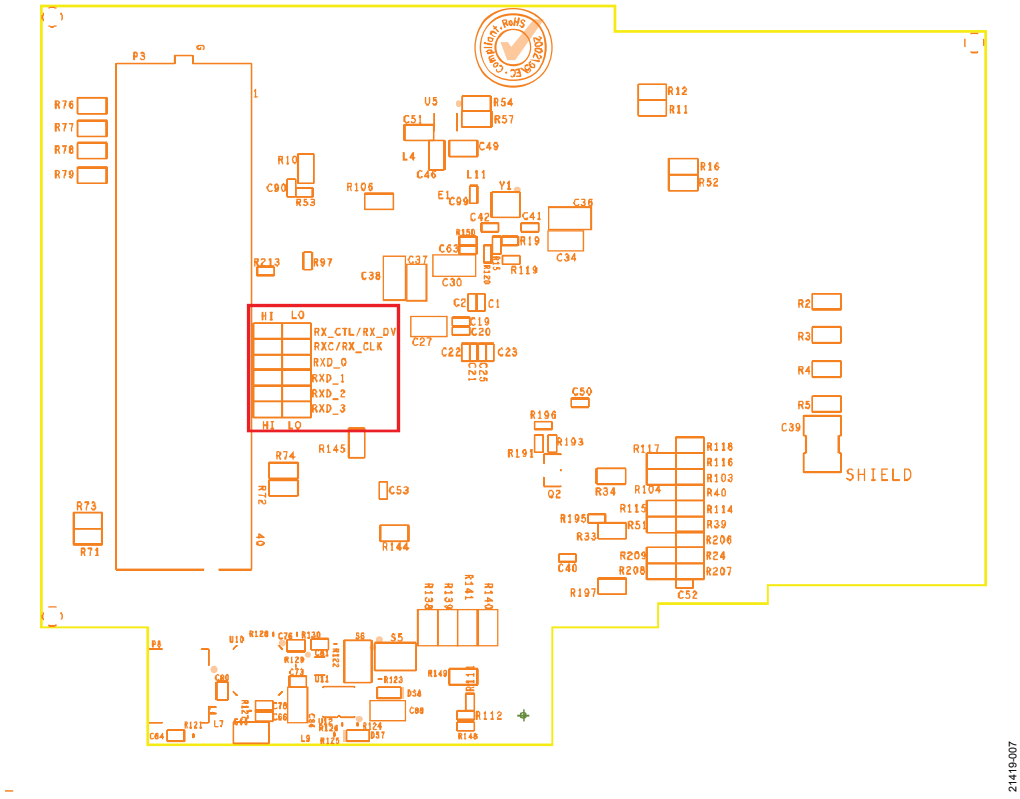

Figure 6. Configuration Resistor Placement, Underside of PCB

SOFTWARE OVERVIEW

INSTALLING THE ETHERNET PHY SOFTWARE

The Ethernet PHY software GUI requires the installation of the Ethernet PHY software and the installation of the USB communications drivers. Both installations must be complete before connecting the EVAL-ADIN1300FMCZ to the USB port of the PC to ensure that the evaluation system is properly recognized when connected to the PC.

First, install the Ethernet PHY software and the associated documentation (the ADIN1300 data sheet). The installation steps are listed in the following section. The default location for the Ethernet PHY software GUI installation is the **C:\Analog Devices** folder.

When the Ethernet PHY software installation is complete, install the USB communications drivers. The MDIO interface dongle uses the FT232RQ for UART to USB communication. The MDIO interface dongle requires the installation of drivers for the FTDI chip. Locate and install this driver separately. These drivers are available at: www.ftdichip.com/Drivers/CDM/CDM21228_Setup.zip.

Ethernet PHY Software GUI Installation

To install the Ethernet PHY software GUI, take the following steps:

1. Launch the installer file to begin the Ethernet PHY software installation.
2. If a window appears asking for permission to allow the program to make changes to the PC, click **Yes**.
3. The welcome window appears (see Figure 7). Click **Next.**

Figure 7. Welcome Window

4. The Ethernet PHY software launches. An overview of what is being installed and recommendations in terms of hardware power-up appears. Read the overview and click **Next** (see Figure 8).

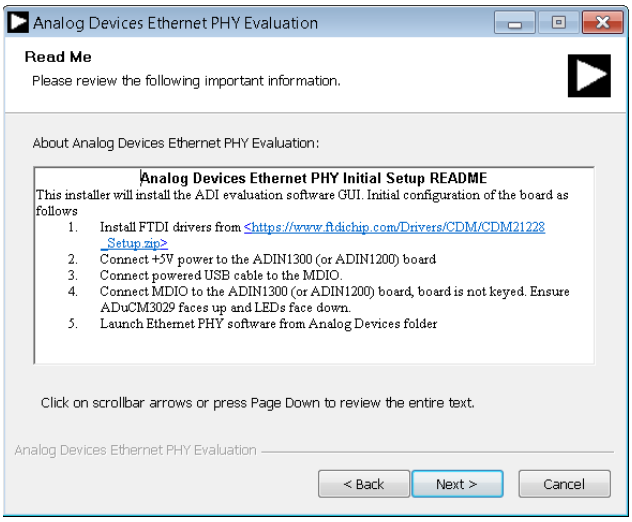

Figure 8. Installation Process Overview

5. A license agreement appears. Read the agreement and click **I Agree** to allow the installation to proceed (see Figure 9).

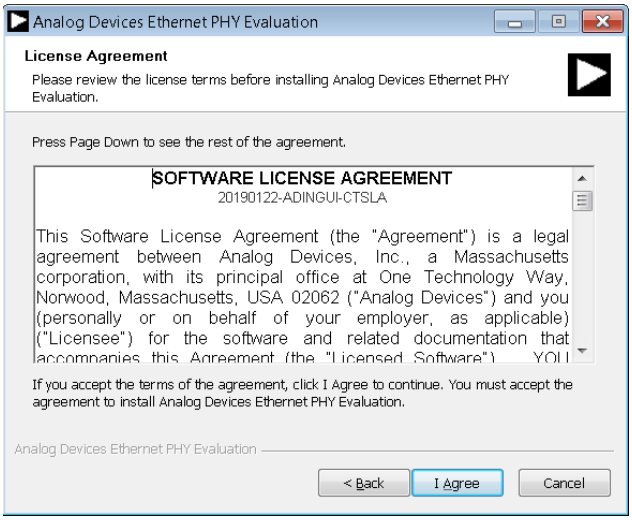

Figure 9. Accepting the License Agreement

6. Select a location to install the Ethernet PHY software and then click **Install** (see Figure 10).

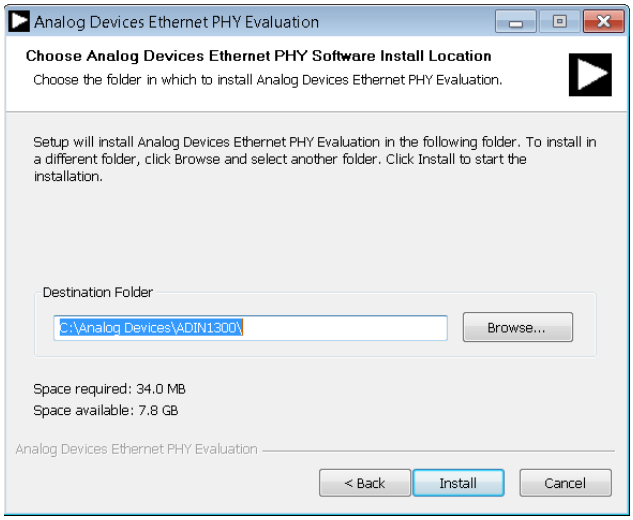

Figure 10. Installation Location

7. A window appears stating that the installation is complete. Click **Finish** to continue (see Figure 11).

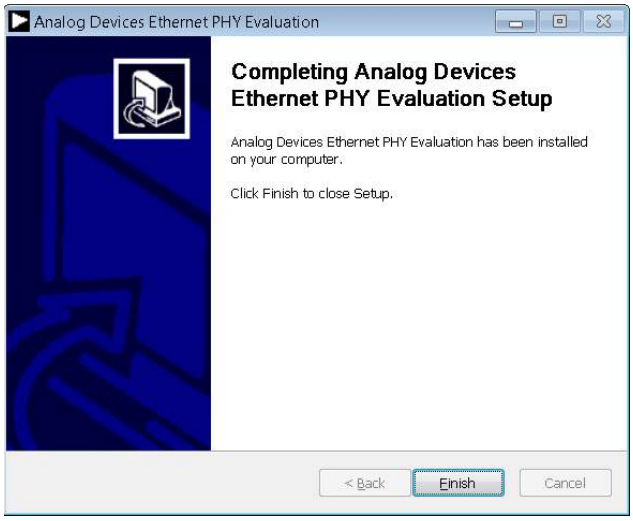

Figure 11. Installation Complete

8. The Ethernet PHY software is automatically installed in the **Analog Devices** folder on the PC. Access the Ethernet PHY software via Windows® explorer at **C:\Analog Devices\ADIN1300** or from the **Start** menu.

INITIAL SETUP

To set up the EVAL-ADIN1300FMCZ and use it with the Ethernet PHY software GUI, take the following steps:

1. Connect a 5 V power supply to the EVAL-ADIN1300FMCZ via the EXT_5V connector or the 5 V barrel connector.
2. Connect the USB cable to the MDIO interface dongle.
3. Connect the USB cable to the PC. When connecting the EVAL-ADIN1300FMCZ to the PC for the first time, the drivers are automatically installed. Wait until the driver installation is complete before proceeding to the next step.
4. Ensure that the ADuCM3029 microcontroller faces up (see Figure 4) and connect the MDIO interface dongle to the EVAL-ADIN1300FMCZ. The MDIO interface dongle is not keyed.
5. Launch the Ethernet PHY software from the **Analog Devices** folder in the **Start** menu.

USING THE EVALUATION SOFTWARE

When the Ethernet PHY software is launched, the GUI window shown in Figure 12 appears. Figure 12 shows the GUI features with labels, and Table 6 lists the GUI labels and the corresponding descriptions.

Table 6. GUI Label Descriptions

Label	Description
1	**Select Local** section. Shows connected evaluation hardware. The board name shown corresponds to the MDIO interface dongle that is connected to the EVAL-ADIN1300FMCZ.
2	User buttons.
3	**Link Properties** tab. Use this tab to change the PHY configuration.
4	**Register Access** tab. Allows the user read or write device registers.
5	**Clock Pin Control** tab. Controls which clock is applied to the GP_CLK pin and enables the CLK25_REF pin.
6	**Loopback** tab. Controls the various loopback modes.
7	**Test Modes** tab. Provides access to the various test modes on the device.
8	**Framechecker** tab. Configures and enables the frame generator and frame checker.
9	**Cable Diagnostics** tab. Provides easy access to the cable diagnostics features on the device.
10	Activity information window. This window provides an overview of the PHY activity, reads, and writes issued to the device.
11	**Activity Log** section. Section shows read, write, and status activity for the selected PHY.
12	Dropdown menus to load a script file. These two dropdown menus allow the user to load a script file with a sequence of write commands to load to the device.

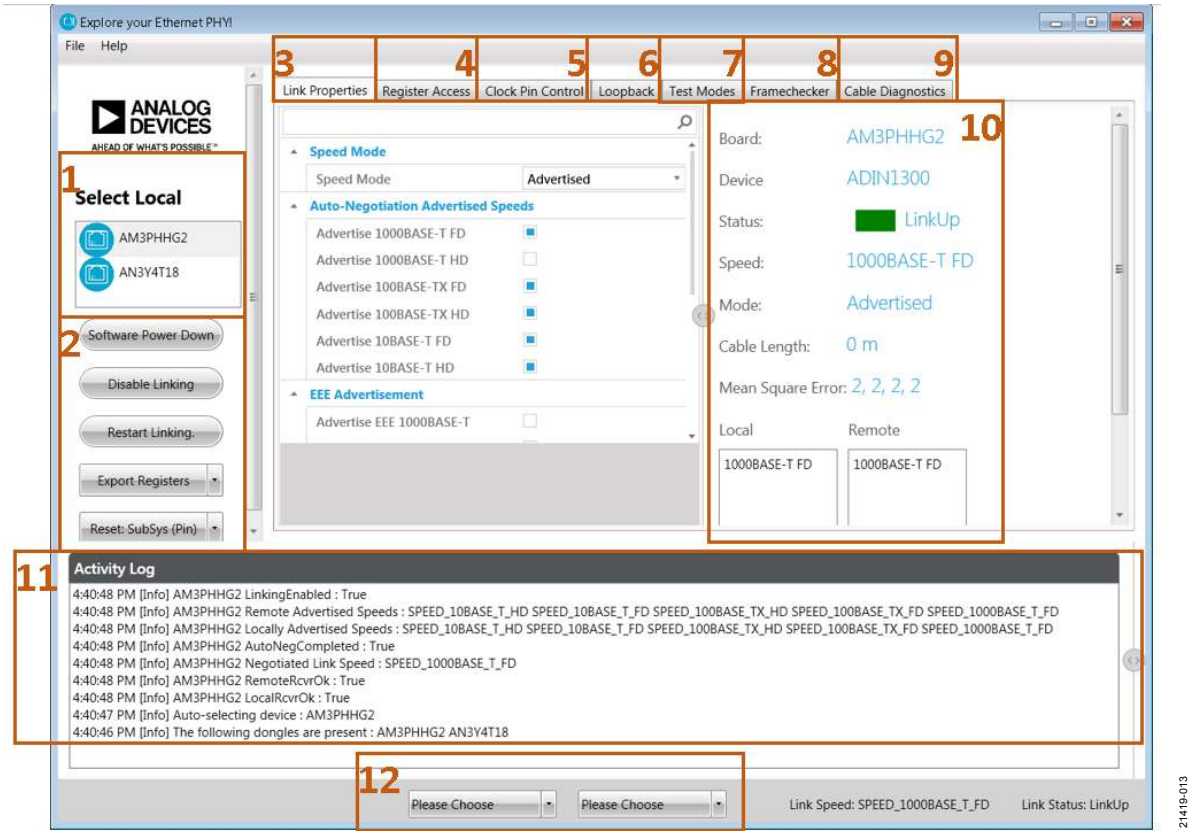

Figure 12. Main GUI Window

GUI DETAILED OVERVIEW

BOARD DISPLAY SHOWING CONNECTED EVAL-ADIN1300FMCZ HARDWARE

In the **Select Local** section (see Figure 12), a unique hardware identifier is shown for each MDIO interface dongle connected to the PC. In the example shown in Figure 13, there are two MDIO interface dongles connected to the same PC (the A62UK21O and AL2YSWGN).

The Ethernet PHY software GUI can only communicate with one MDIO interface dongle at a time. To choose which MDIO interface dongle is addressed as the local board in this section, click the appropriate device identifier to select and highlight it. All register controls, displayed link properties, and local board information in other sections of the GUI apply to the selected ADIN1300 device connected to the MDIO interface dongle.

Figure 13. MDIO Interface Dongle Selection

USER BUTTONS SECTION

Use the buttons in this section to control the basic operation of the GUI and the ADIN1300 device.

Figure 14. Basic User Buttons

Software Power-Down and Power-Up

Click **Software Power Down** to place the selected device into software power-down mode where the analog and digital circuits are placed into a low power state. Most clocks are gated off and no link is brought up. Click **Software Power Down** to enable a software power-down. The button color changes to orange and the button label changes to **Software Power Up**. Click **Software Power Up** to exit from the software power-down and restart linking. When the software power-down is asserted, the other buttons for the selected device are grey and disabled.

Disable or Enable Linking

Click **Disable Linking** to disable linking when a link is up. The button label changes from **Disable Linking** to **Enable Linking**. Click **Enable Linking** to enable linking.

Restart Linking

If the software configuration has been changed, click **Restart Linking** to restart the linking process with the new configuration. If the link has already been established, the link is first brought down and then restarted.

Export Registers

Click **Export Registers** to perform a data dump to the **Activity Log** section. The register dump can be saved to text format for offline review. Right click and click **Save as** to save the data to a log file.

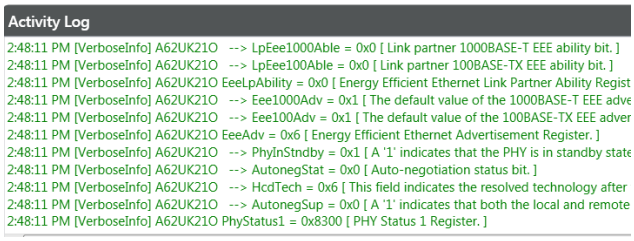

Figure 15. Activity Log with Export Registers Displayed

Reset

Click **Reset** to use the dropdown menu to initiate different resets. The reset options include the following:

Figure 16. Reset Options

- Subsystem Software Reset with Pin Configuration: click **Reset: SubSys (Pin)** to perform a reset of the subsystem with the subsystem requesting a new set of hardware configuration pin settings from the chip during the software reset sequence.
  The GeSftRst bit and the GESftRstCfgEn bit are set to 1.
- Subsystem Software Reset: click **Reset: SubSys** to perform a reset of the subsystem with the subsystem requesting previously stored hardware configuration pin settings to be reloaded during the software reset sequence.
  The GeSftRst bit and the GESftRstCfgEn bit are set to 0.
- PHY Core Software Reset: click **Reset: PHY** to perform a reset where the SftRst bit resets the PHY core registers.

LINK PROPERTIES TAB

The **Link Properties** tab provides user access to the main linking configurations within the device. This tab has a slider to access all controls. When a control is selected, the GUI provides a prompt describing the function at the bottom of the linking control box (see Figure 17).

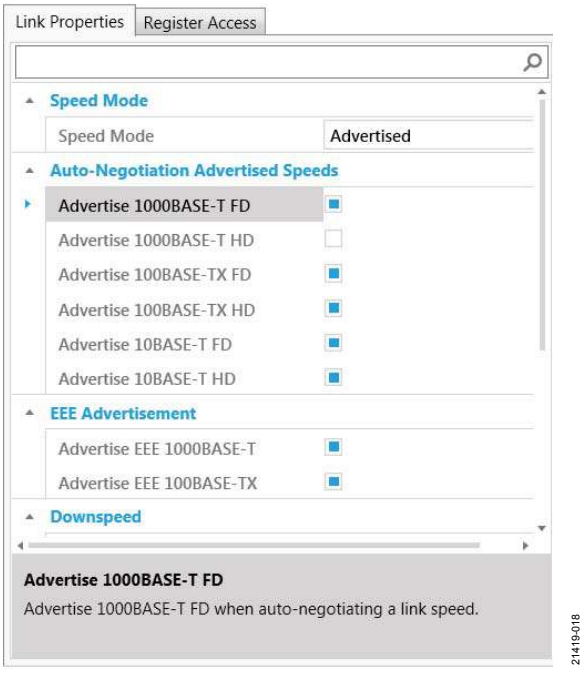

*Figure 17. **Link Properties** Tab*

Speed Mode

For the selected device, advertised speed or forced speed can be chosen. The speed selection prepopulates the remaining user controls for the **Link Properties** tab with the following:

- **Advertised**: subset of controls available in advertised mode. The controls include the following:
  - **Auto-Negotiated Advertised Speeds**: shows the checkbox availability of all autonegotiated advertised speeds available. Select and clear the checkboxes as required. All speed options are available in this section. The default advertised reflects the hardware configuration pins.
  - **EEE Advertisement**: use the checkboxes to advertise the EEE as a speed option for 1000BASE-T and 100BASE-TX.
  - **Downspeed**: use the checkbox to enable downspeed, which allows the PHY to change down to a lower speed after a number of attempts to bring up a link at the highest advertised speed.
  - **Downspeed Retries**: sets the number of times the PHY attempts to bring up a link. The default is four attempts.
  - **MDIX**: use dropdown menu to choose between **Auto MDIX**, **FixedMDI**, or **FixedMDIX.**
  - **Energy Detect PowerDown Mode**: use the dropdown menu to choose between **Disabled**, **Enabled**, or **EnabledWithPeriodicPulseTx.**
  - **Master/Slave**: use the dropdown menu to choose between **Master** and **Slave**. The default is **Slave**.
- **Forced**: subset of controls available in forced mode. The controls include the following:
  - **Forced Speeds**: use the dropdown menu to choose the required speed.
  - **MDIX**: use the dropdown menu to choose between **Auto, FixedMDI**, or **FixedMDIX**.
  - **Energy Detect Powerdown Mode**: use the dropdown menu to choose between **Disabled**, **Enabled**, or **EnabledWithPeriodicPulseTx**.
  - **Master/Slave**: use the dropdown menu to choose between **Master** and **Slave**. The default is **Slave**.

REGISTER ACCESS TAB

The **Browse** tab within the **Register Access** tab allows the user to review the bank of registers and edit the register fields or bit fields as required (see Figure 18).

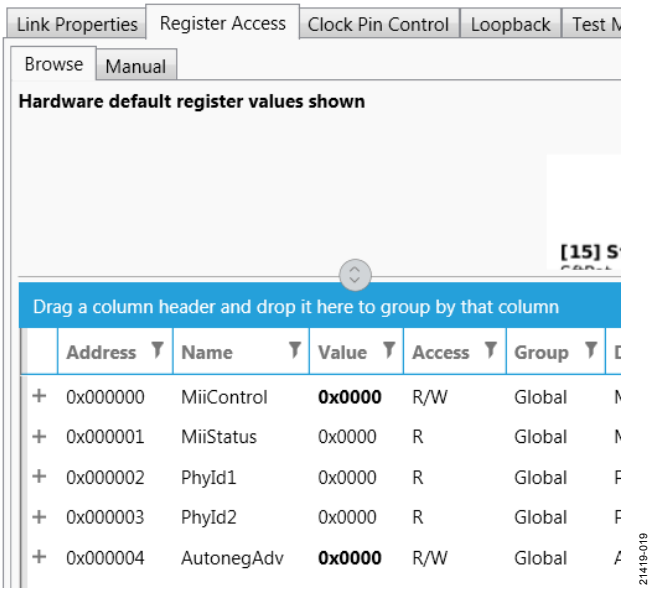

*Figure 18. **Register Access** Tab Full Register Map*

The **Manual** tab within the **Register Access** tab allows the user to perform basic reads from and writes to individual ADIN1300 registers (see Figure 19).

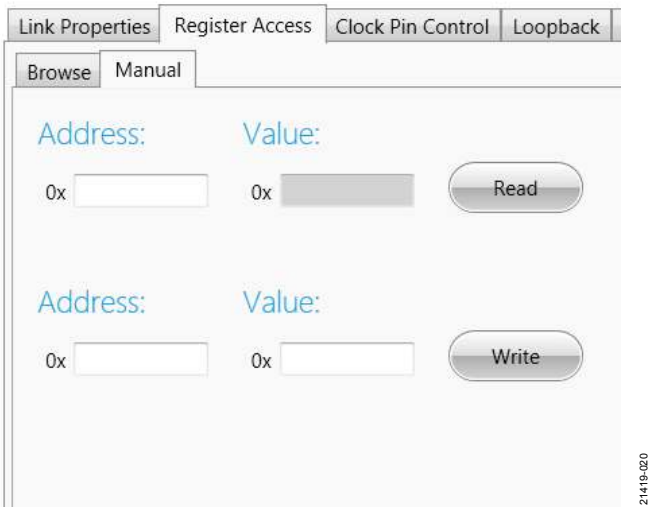

*Figure 19. **Register Access** Tab*

Access the direct register read/write function on the right side of the **Activity Log** section. To access this function, slide the arrow to the left to expose it (see Figure 20).

*Figure 20. **Activity Log** Section Register Access*

CLOCK PIN CONTROL TAB

Use this tab to control which clock is applied to the GP_CLK pin, and to enable the CLK25_REF pin (see Figure 21).

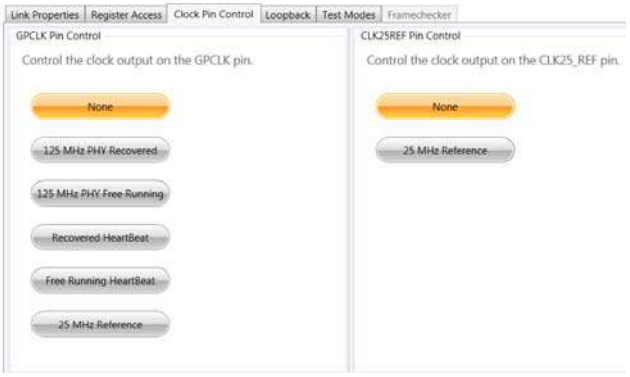

*Figure 21. **Clock Pin Control** Tab*

LOOPBACK TAB

The various loopback modes are available in this tab (see Figure 22). Consult the ADIN1300 data sheet for a full description of each loopback mode.

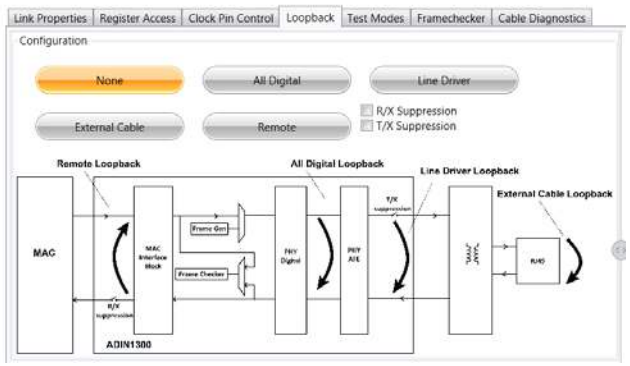

*Figure 22. **Loopback** Tab*

TESTMODES TAB

Use this tab to initiate the various test mode functions in the device. Select the appropriate test mode and click **Execute Test** (see Figure 23).

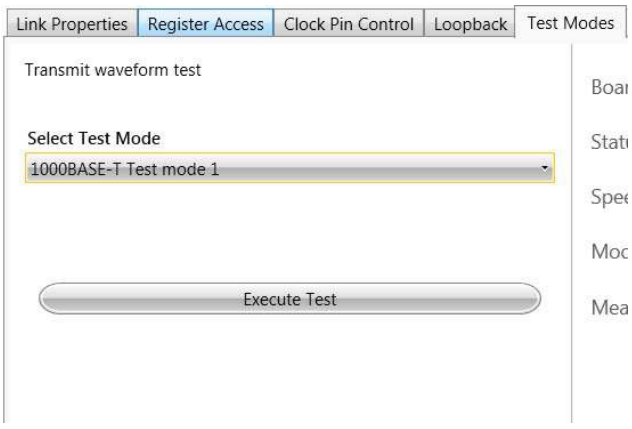

*Figure 23. **Test Modes** Tab*

FRAMECHECKER TAB

This tab provides access to the frame generator and frame checker features of the ADIN1300 (see Figure 24).

Control the number of frames generated by the generator, the frame length, and the content of the frame within this tab. Choose to have the frame generator to either run in burst mode or run continuously. To halt the frame generator when the frame generator is running continuously, use the **Terminate** button.

Use the **Loopback** button to enable the remote device to loop back the data to the local device. To ensure that the appropriate device is selected, choose which connected board is the local, configure that board to generate frames, then configure the other board in remote loopback.

The frame checker information displayed on the screen accumulates the number of frames sent and shows the number of errors observed (see Figure 25).

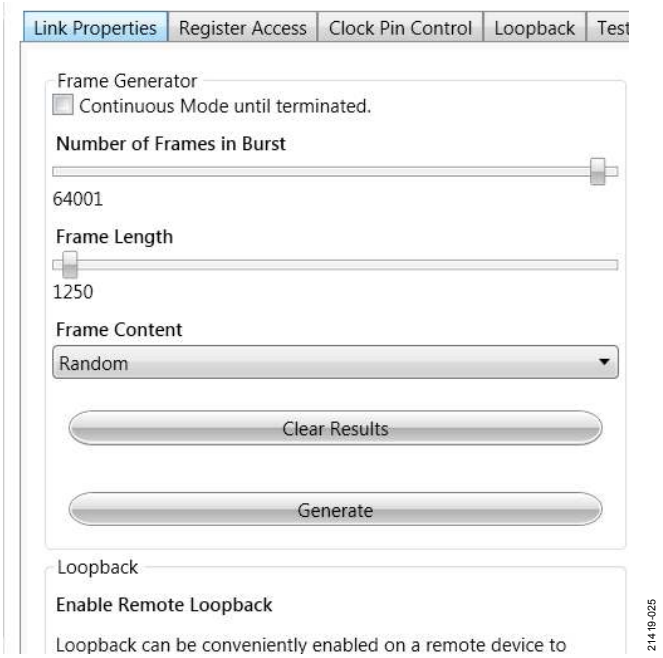

Figure 24. Overview of Frame Generator and Frame Checker

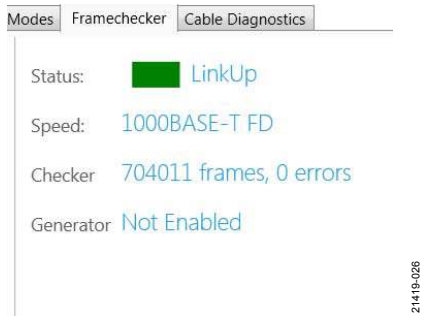

Figure 25. Frame Generator Status and Frame Checker Result

CABLE DIAGNOSTICS TAB

The cable diagnostic feature allows the user to diagnose issues with the link. Various features within the device are available when the link is up, which quantify the quality of the link by measuring features such as the mean squared error (MSE) level and estimated cable length. These measurements are displayed in the main **Link Properties** tab.

The features in the **Cable Diagnostics** tab (see Figure 26) are the features available to run when the link is disabled, such as checking for shorts, checking for opens, and identifying the distance to the first fault (see Figure 28). The LinkEn bit must be clear to run these checks.

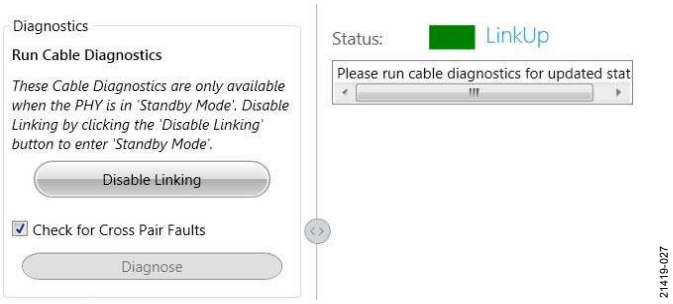

Figure 26. Cable Diagnostics Configuration with Link Up

Click the **Disable Linking** button to set the LinkEn bit to 0 to allow diagnostics to be run (see Figure 27 through Figure 29).

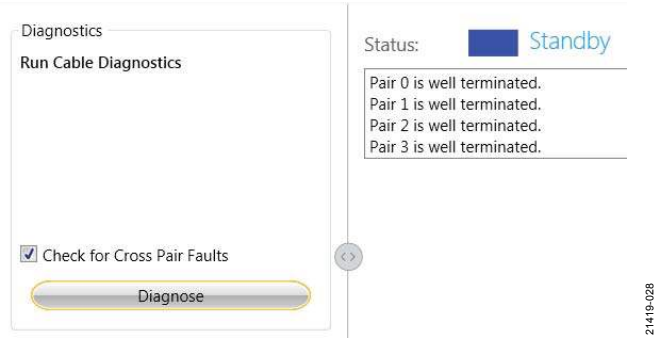

Figure 27. Cable Diagnostics Configuration when Link is Disabled with Cable Connected to Remote PHY

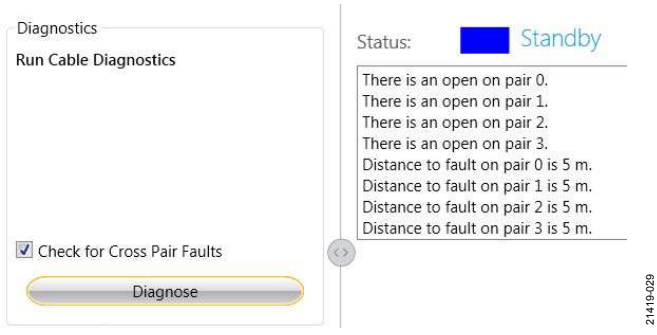

Figure 28. Cable Diagnostics Configuration with Cable Open

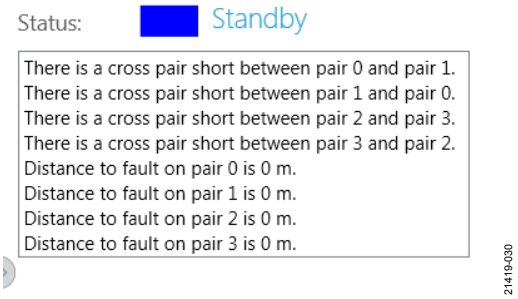

Figure 29. Cable Diagnostics Configuration with Cable Crossed

ACTIVITY WINDOW AND LINKING STATUS

This window displays the current status of the selected PHY chip (as determined in the **Select Local** section), including whether a link is established, the speed of the link, and the speed mode. The local and remote fields show the advertised speeds available in the local PHY device and also what the remote PHY is returning (see Figure 30).

If the user switches between two EVAL-ADIN1300FMCZ boards in the **Select Local** section, the information shown in these fields will be updated to reflect the information provided from the board defined as local.

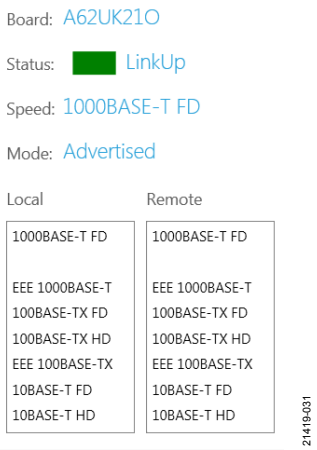

Figure 30. Board Status Information

The GUI displays a color code to show the status of the link depending on how the user has configured the device (see Figure 31).

Figure 31. GUI Link Status

ACTIVITY LOG INFORMATION SECTION

The activity log reports status information and register write issues to the selected EVAL-ADIN1300FMCZ board (see Figure 32). The activity log captures the activity in the GUI corresponding to the activity on the local PHY, which indicates the various reads, writes, and information on whether a link is established. When the frame generator is enabled, this window shows the frame generator activity. The board identification is recorded with each bit field change to clarify which device is being addressed.

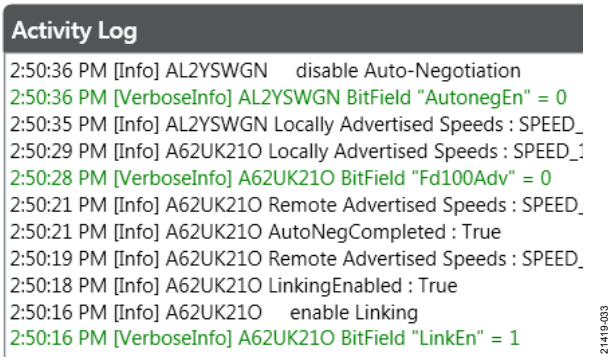

Figure 32. Activity Log Showing Device Status

To clear the activity log, right click and then click **Clear**. To export the contents of the activity log for offline review, right click and then click **Save as**. The file saved is a text file with a default location in the **Analog Devices** > **ADIN1300** folder.

LOADING A SCRIPT FILE

The GUI allows the user to load a sequence of register commands from a file. Within the GUI window, there are two dropdown menus under the **Activity Log** section where the user can select the script file and which section of the script to run. Click a dropdown menu, choose the script by name, and then click the dropdown menu again to load the selected script. The Activity log displays the register writes issued from the script.

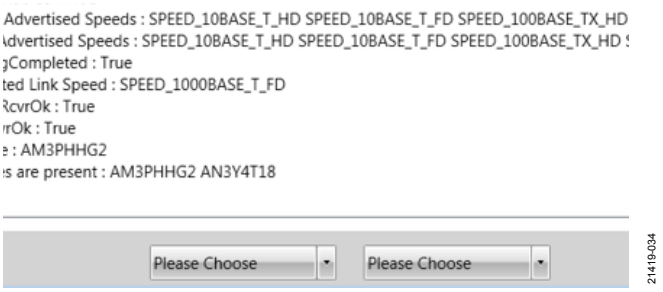

Figure 33. Script File Loading Dropdown Menus

The script file is located in the **ADIN1300** folder and is named **registers_scripts.json** (see Figure 34).

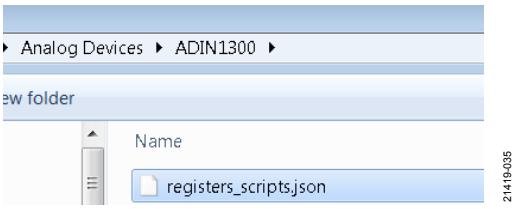

Figure 34. Script File Location

The register commands can be loaded with either the register name or the register address, as shown in the simple examples in the file. The commands are loaded sequentially. Create the sequence of write commands using a text editor. Ensure that the exact syntax is copied and match the register names with those in the data sheet to prevent errors reported in the activity log. Give the script a unique name. For when the **SftPd Down&Up** routine is selected, see the following example:

```
{
  Name: SftPd Down&Up,
  RegisterAccesses: [
    {
      MemoryMap : GEPhy,
      RegisterName: SftPd,
      Value: 1
    },
    {
      MemoryMap : GEPhy,
      RegisterName: SftPd,
      Value: 0
    },
  ]
},
```

TROUBLESHOOTING

SOFTWARE INSTALLATION TIPS

Ethernet PHY software installation tips follow:

- Always allow the software installation to be completed, and keep in mind that the Ethernet PHY software is a two-part installation including the ADI package installer (GUI and documentation) and the FTDI drivers which can be found at www.ftdichip.com/Drivers/CDM/CDM21228_Setup.zip. The installation may require a restart of the PC.
- When the MDIO interface dongle is first plugged in via the USB cable, allow the new found hardware wizard to run completely. This step is required prior to starting the Ethernet PHY software.
- If the EVAL-ADIN1300FMCZ does not appear in the GUI window, ensure that the following steps have been competed:
  - Power is applied to the EVAL-ADIN1300FMCZ.
  - The powered USB connector is connected to the MDIO interface dongle.
  - Both the EVAL-ADIN1300FMCZ and the MDIO interface dongle are connected together.
  - The Ethernet cable is connected.
  - The Ethernet PHY software is launched.

SOFTWARE TIPS

If the Ethernet PHY software does not read any data back, check for any messages in the **Activity Log** section. There is one known communication bug in the connection of the MDIO interface dongle and EVAL-ADIN1300FMCZ, as discussed in the following section.

MDIO Interface Dongle Communications, Known Issue

A known behavior when using the MDIO interface dongle with the EVAL-ADIN1300FMCZ is related to the sequence of how the boards are powered and connected together. If the GUI is open, and the user connects the MDIO interface dongle to the EVAL-ADIN1300FMCZ before connecting the USB power to the MDIO interface dongle, the GUI may not properly establish communications with the MDIO interface dongle.

The GUI polls for the MDIO interface dongle regularly, and if an error in the MDIO interface dongle communications is found, it is flagged in the **Activity Log** section and highlighted in red font, as shown in Figure 35. The message also includes a prompt explaining how to resolve the issue.

In the example shown in Figure 35, the user is advised to reset the MDIO interface dongle through Button S6. There are two buttons on the underside of the MDIO interface dongle. In this case, the user identifies S6 and reset. This action restarts the MDIO interface dongle. If the S6 restart does not resolve communications, exit the GUI and relaunch the Ethernet PHY software.

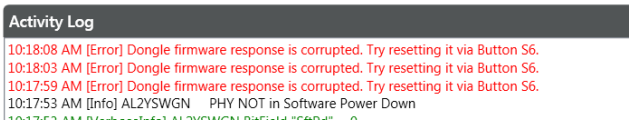

*Figure 35. Example **Activity Log** when MDIO Interface Dongle is Not Responding*

HARDWARE TIPS

Ensure that power is applied to the MDIO interface dongle and EVAL-ADIN1300FMCZ as previously discussed. Measure the voltage at various points on the EVAL-ADIN1300FMCZ using the DVDD, VDD0P9, 5V, AVDD3P3, and VDDIO test points. Crosscheck the voltages against the information in Table 1.

No Link Established

If no link is established, take the following steps to assist debug:

- Ensure that the Ethernet cable is connected properly to the RJ45 connector and between the EVAL-ADIN1300FMCZ boards or PHY pairs.
- When using two EVAL-ADIN1300FMCZ boards, ensure that both boards are powered.
- Ensure that the hardware configuration is appropriate for the required linking arrangement.

LED Not Illuminated, but Link Established Reported in GUI

By default, LED_0 illuminates when a link is established, and flashes when there is activity. The EVAL-ADIN1300FMCZ is configured for Mode 3 and Mode 4 by default, with S1 in Position 1. If PHY_CFG0 is to be used in Mode 1 or Model 2, change the position of S1 to Position 2, as described in Table 4.

LAYOUT GUIDELINES

BOARD STACKUP

The EVAL-ADIN1300FMCZ consists of a 4-layer PCB: the top layer, Layer 2, Layer 3, and the bottom layer. All layers have a copper pour, with an exception around sensitive traces for the MAC and MDI interfaces.

GROUND PLANES

The top and bottom layers of the EVAL-ADIN1300FMCZ mainly carry signal and routing signals from the ADIN1300. The two inner layers are used for ground planes. Layer 2 is a full ground plane. Layer 3 contains primarily of ground with area dedicated to the DVDD and VDDIO power planes. Although the ADIN1300 is a mixed signal device, it only has one type of ground return, GND.

ISOLATION GUIDELINES

Transformer Layout

No metal layers can be directly underneath the transformer to minimize any noise coupling across the transformer.

RJ45 Layout

For optimal electromagnetic computability (EMC) performance, use a metal shielded RJ45 connector with the shield connected to chassis ground. There must be an isolation gap between the chassis ground and the IC GND with consistent isolation across all layers.

POWER SUPPLY DECOUPLING

From a PCB layout point of view, it is important to locate the decoupling capacitors as close as possible to the power supply and GND pins to minimize the inductance.

MAC INTERFACE

When routing the MAC interface traces, ensure that the lengths of the pairs are matched. Avoid crossover of the signals where possible. Stubs should be avoided on all signal traces. It is recommended to route traces on the same layer.

MANAGEMENT INTERFACE

MDI interface

Traces running from the MDI_[x]_P/N pins of the ADIN1300 to the magnetics must be on the same side of the EVAL-ADIN1300FMCZ (no vias), kept as short as possible (less than 1 inch in length), and individual trace impedance of these tracks must be kept below 50 Ω with a differential impedance of 100 Ω for each pair. The same recommendations apply for traces running from the magnetics to the RJ45 connector. Impedance must be kept constant throughout. Any discontinuities can impact signal integrity.

Each pair must be routed together with trace widths the same throughout. Trace lengths must be kept equal where possible and any right angles on these traces must be avoided (use curves or 45° angles in the traces). Stubs must be avoided on all signal traces. It is recommended to route traces on the same layer.

PLACEMENT OF THE TVS DIODE

It is recommended to place the TVS diode close to the ADIN1300 device to ensure minimal track inductance between the external protection and internal protection within the device.

THERMAL CONSIDERATIONS

The ADIN1300 is packaged in an LFCSP package. This package is designed with an exposed paddle which must be soldered to the PCB for mechanical and thermal reasons. The exposed paddle acts to conduct heat away from the package and into the PCB. By incorporating an array of thermal vias in the PCB thermal paddle, heat is dissipated more effectively into the inner metal layers of the PCB. When designing the PCB layout for optimum thermal performance, use a 4 mm × 4 mm array of vias under the paddle.

This LFCSP device includes two exposed power bars adjacent to the exposed pad at the top and bottom, highlighted in red in Figure 36. These bars are connected to internal power rails and the area around them is a keep out zone. Keep these areas clear of traces or vias.

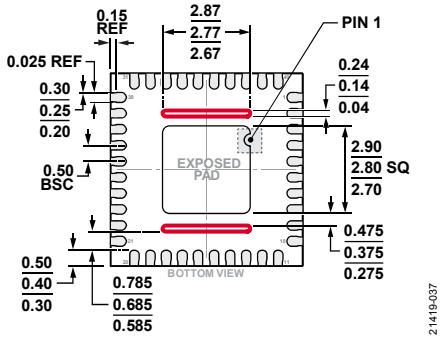

Figure 36. LFCSP Simplified Package Drawing with Keep Out Area for Power Bars Highlighted (Underside)

EVALUATION BOARD SCHEMATICS AND ARTWORK

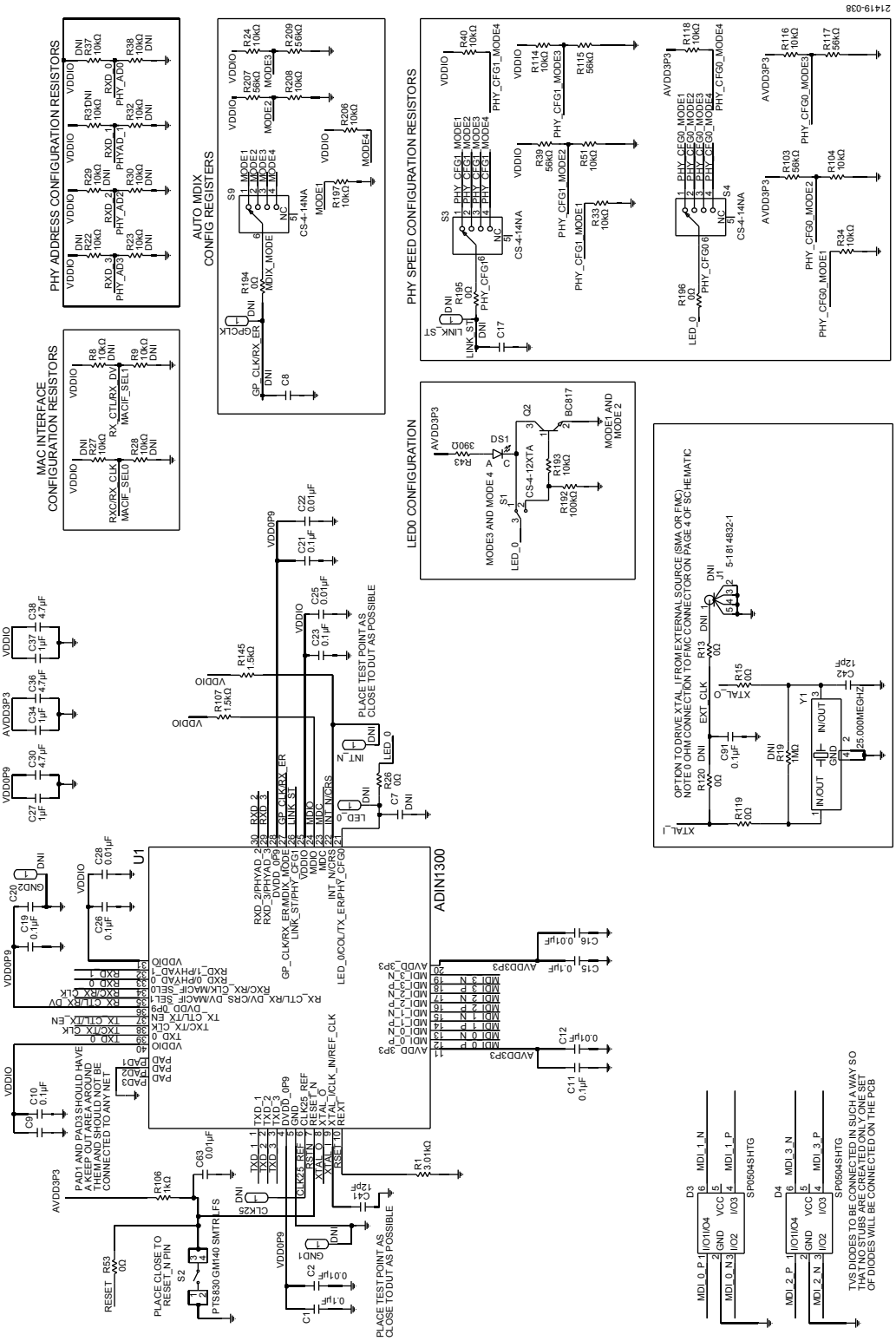

Figure 37. PHY Schematic

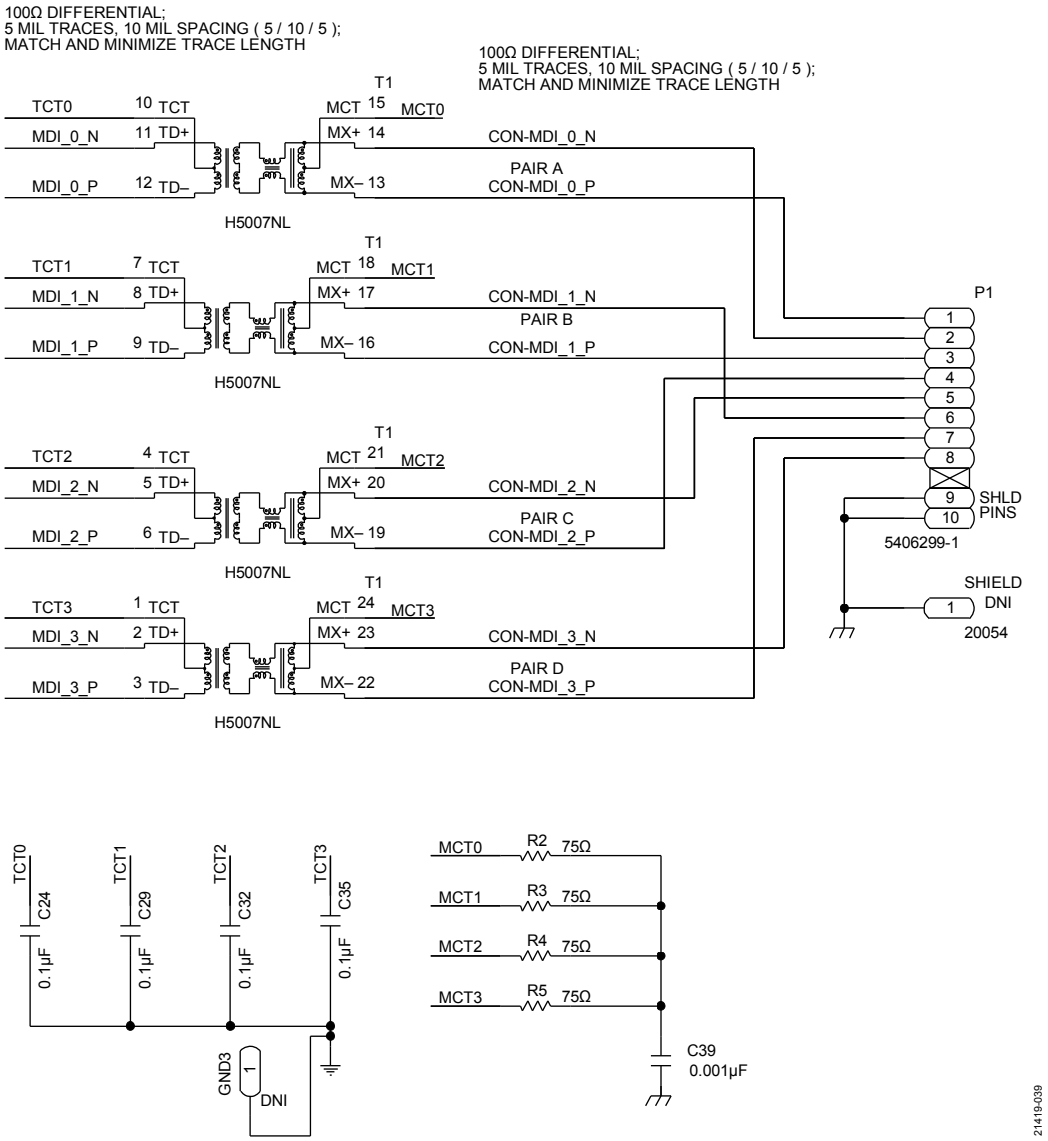

Figure 38. Magnetics

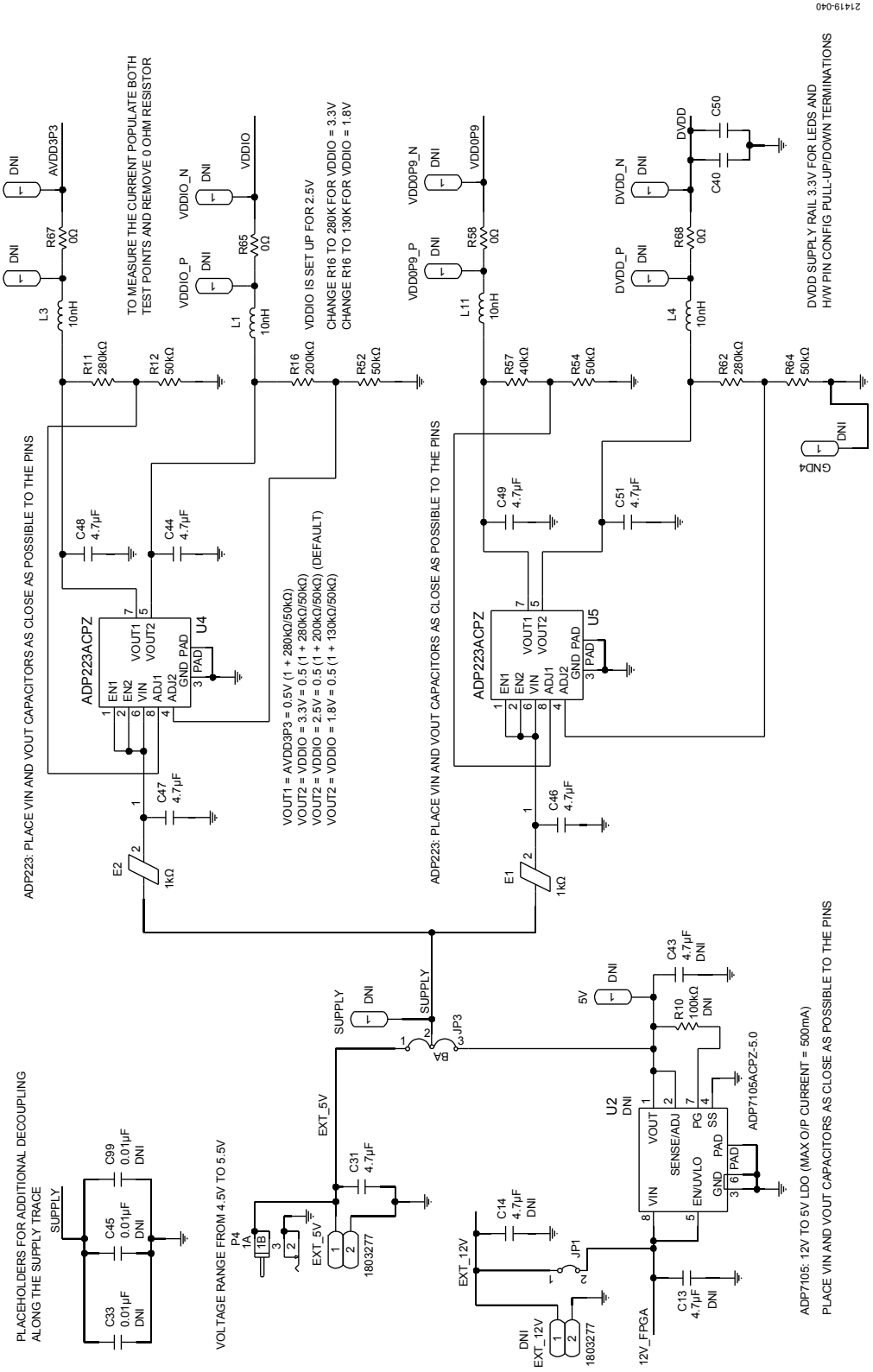

Figure 39. Power Supplies

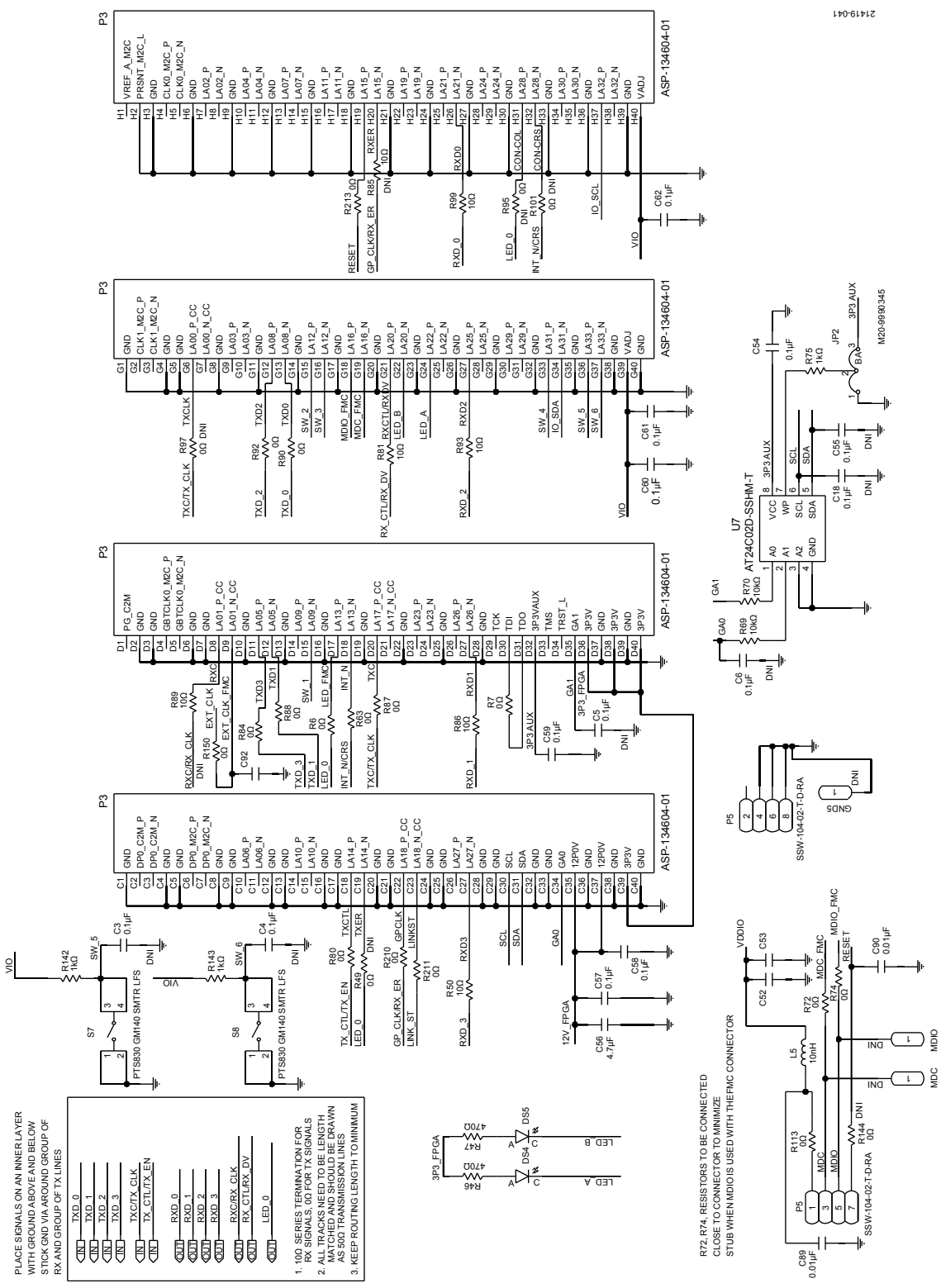

Figure 40. FMC Connector

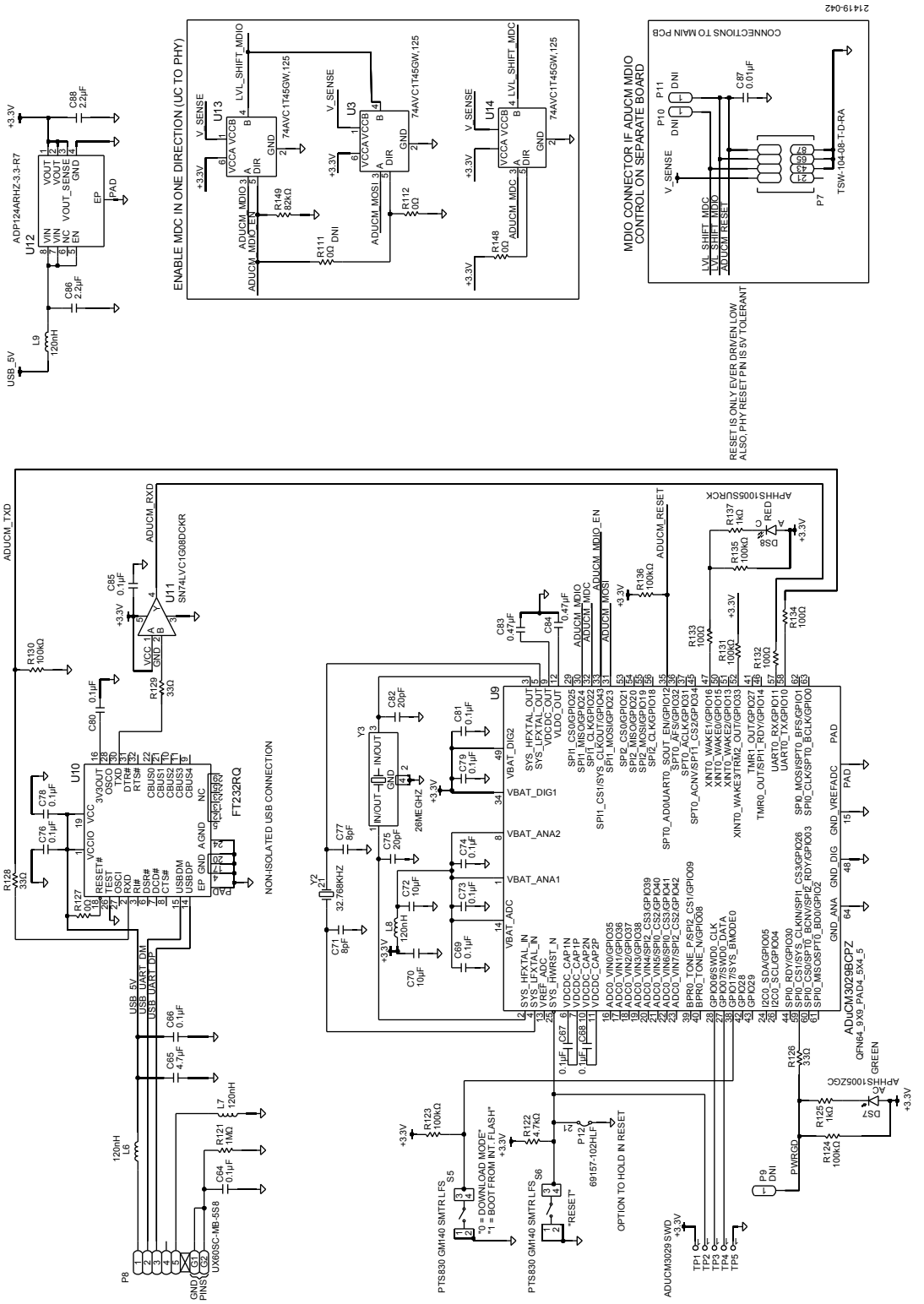

Figure 41. MDIO Interface Dongle

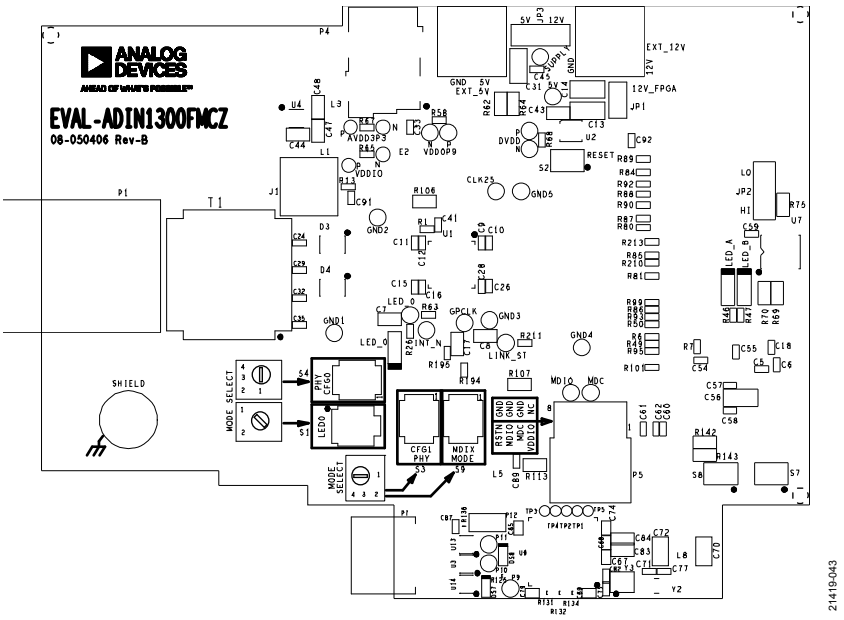

Figure 42. Schematic Silkscreen, Top

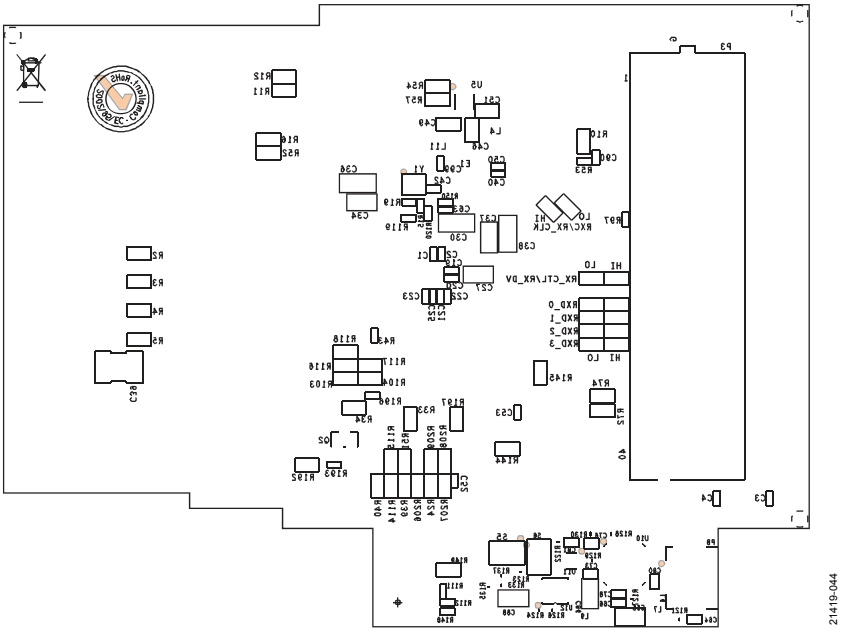

Figure 43. Schematic Silkscreen, Bottom

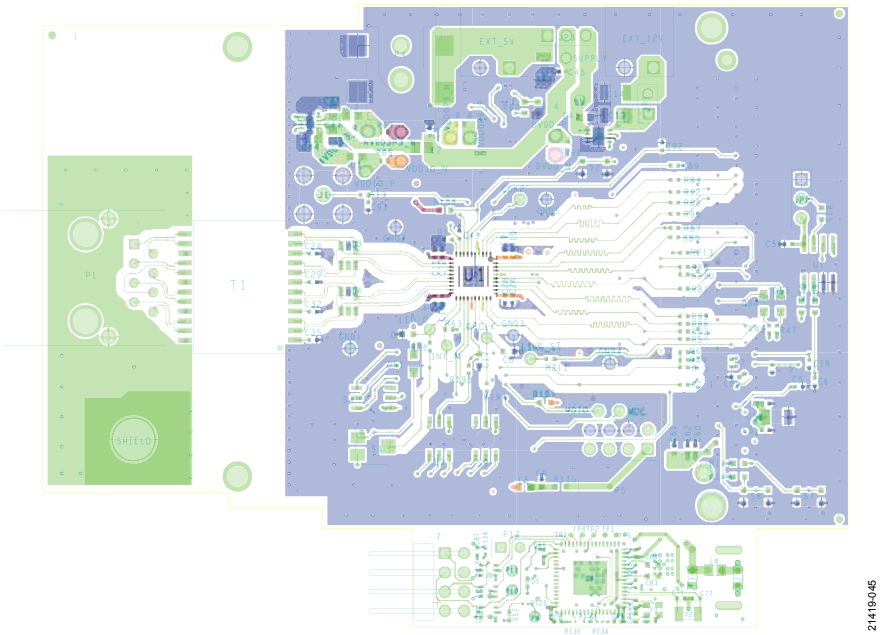

Figure 44. Top Layer

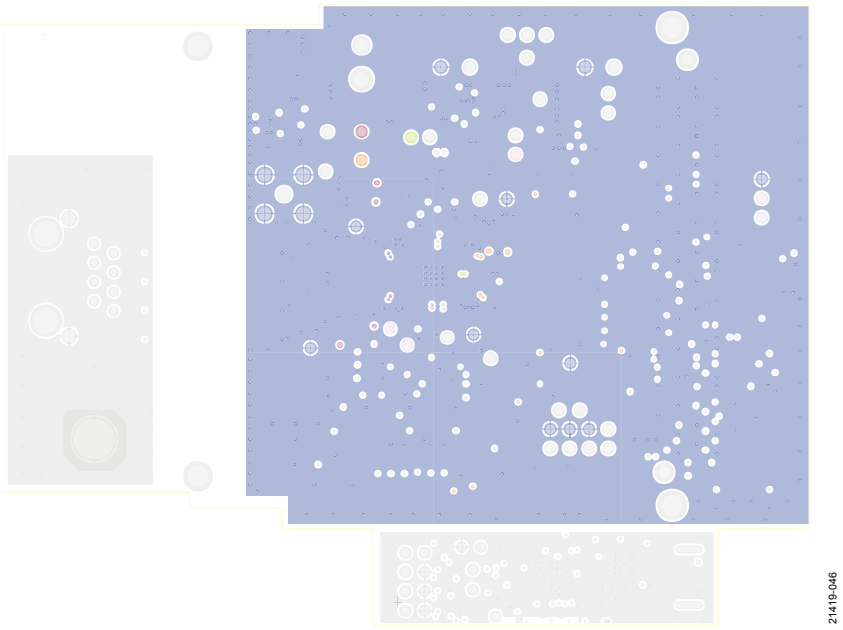

Figure 45. Layer 2, Ground Layer

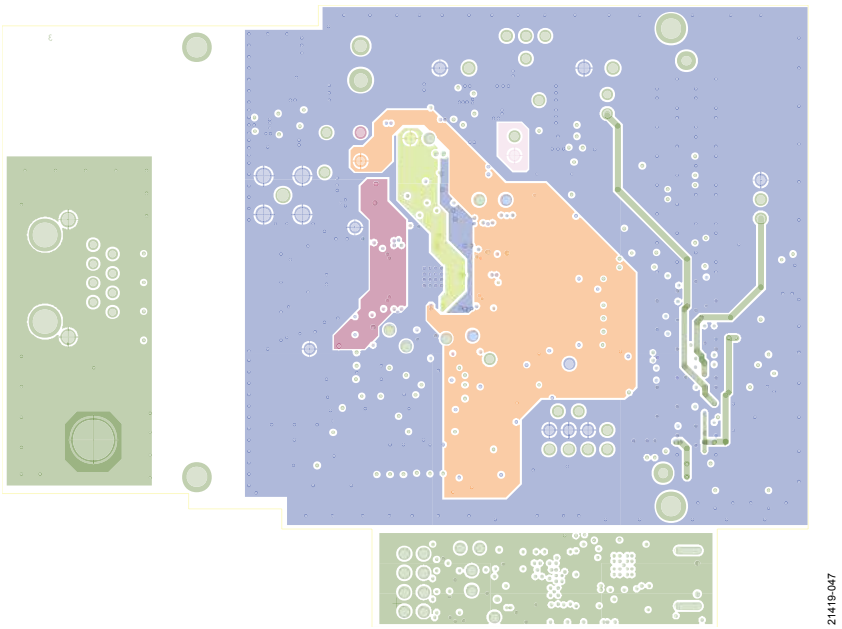

Figure 46. Layer 3, Power and Ground Layer

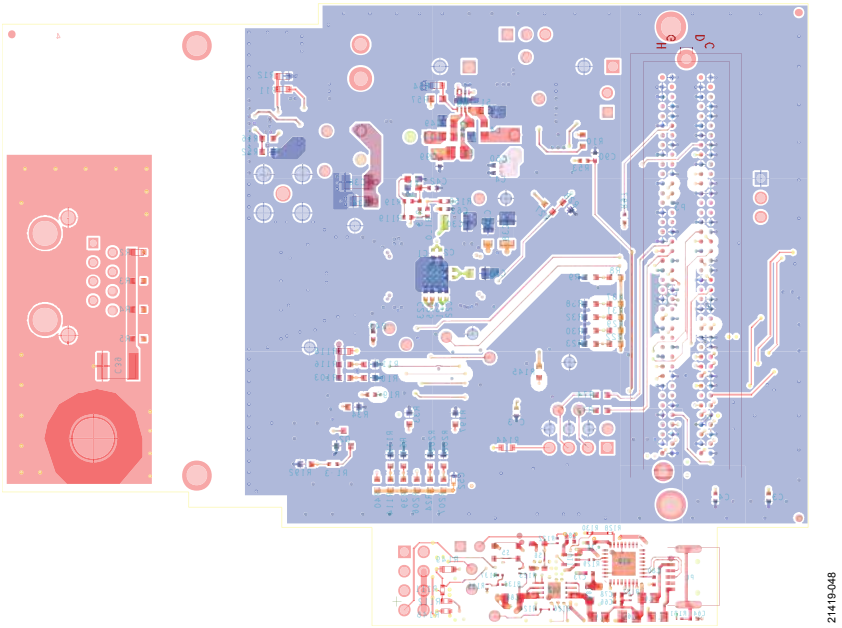

Figure 47. Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 7.

Qty	Reference Designator	Description	Manufacturer	Part Number
16	C1, C10, C11, C15, C19, C21, C23, C26, C54, C55, C57 to C62	Ceramic capacitors, 0.1 µF, 16 V, 10%, 0402, X7R	American Technical Ceramics	530L104KT16T
16	C2, C9, C12, C16, C20, C22, C25, C28, C40, C50, C52, C53, C63, C87, C89, C90	Ceramic capacitors, 0.01 µF, 25 V, 10%, 0402, X7R	TDK	C1005X7R1E103K050EB
5	C13, C14, C30, C31, C36, C38, C56	Ceramic capacitors, 4.7 µF, 25 V, 10%, 1206, X7R	KEMET	C1206C475K3RACTU
4	C24, C29, C32, C35	Ceramic capacitors, 0.1 µF, 50 V, 10%, 0402, X7R	TDK	C1005X7R1H104K050BE
3	C27, C34, C37	Ceramic capacitors, 1 µF, 100 V, 10%, 0805, X7S	TDK	C2012X7S2A105K
1	C39	Ceramic capacitor, 0.001 µF, 3000 V, 10%, 1812, X7R	KEMET	C1812C102KHRACTU
2	C41, C42	Ceramic capacitors, 12 pF, 50 V, 1%, 0402, NP0(C0G)	Murata	GJM1555C1H120FB01D
6	C44, C46 to C49, C51	Ceramic capacitors, 4.7 µF, 10 V, 10%, 0603, X6S	Murata	GRM185C81A475KE11D
13	C64, C66 to C69, C73, C74, C76, C78 to C81, C85	Ceramic capacitors, 0.1 µF, 50 V, 10%, 0402, X7R	TDK	CGA2B3X7R1H104K050BB
1	C65	Ceramic capacitor, 4.7 µF, 50 V, 10%, 0805, X7R	Murata	GRM21BZ71H475KE15L
2	C70, C72	Ceramic capacitors, 10 µF, 25 V, 10%, 0805, X5R	TDK	C2012X5R1E106K085AC
2	C71, C77	Ceramic capacitors, 8 pF, 16 V, 0.5 pF, 0402, C0G	AVX Corporation	0402YA8R0DAT2A
2	C75, C82	Ceramic capacitors, 20 pF, 16 V, 5%, 0402, C0G	AVX Corporation	0402YA200JAT2A
2	C83, C84	Ceramic capacitors, 0.47 µF, 35 V, 10%, 0603, X7R	Taiyo Yuden	GMK107B7474KAHT
2	C86, C88	Ceramic capacitors,2.2 µF, 50 V, 10%, 0805, X7R	Taiyo Yuden	UMK212BB7225KG-T
2	D3, D4	6 V, SOT23_6, TVS diode arrays, low capacitor ESD protection	Littelfuse, Inc.	SP0504SHTG
3	DS1, DS4, DS5	1.7 V, 0805, LEDs, red, clear, 660 nm	Lumex Inc.	SML-LX0805SRC-TR
1	DS7	2.1 V, 0402, LED, orange, 610 nm	Kingbright Electronic	APHHS1005SECK
1	DS8	0402, LED, red	Kingbright Electronic	APHHS1005SURCK
2	E1, E2	1 kΩ at 100MHz, L0805, ferrite bead, 0805	Taiyo Yuden	BK2125HS102-T
1	EXT_5V	PCB connector header, CNHDRRA1X2H285, 3.81 mm	Phoenix Contact	1803277
2	JP2, JP3	PCB connectors, 3-position, male, header, unshrouded, single-row, 2.54 mm pitch	Harwin	M20-9990345
5	L1, L3, L4, L5, L11	10 nH, 2%, 0603, inductors, high frequency wirewound	Murata Manufacturing	LQW18AN10NG10D
4	L6 to L9	120 nH, 25%, 0805, inductors	Murata Manufacturing	BLM21BB750SN1B
1	P1	PCB connector, modular jack assembly, single-port, shielded, RJ45	TE Connectivity	5406299-1

Qty	Reference Designator	Description	Manufacturer	Part Number
1	P12	PCB connector, straight, male, 2-pin header	Amphenol FCI	69157-102HLF
1	P3	PCB connector, single-ended array, male, 160-position, FMC	Samtec	ASP-134604-01
1	P4	PCB connector, CNCUI-PJ-002A_A, power jack	CUI	PJ-002AH-SMT-TR
1	P5	PCB connector, 8-position, socket strip, double-row, right angled, 2.54 mm pitch	Samtec	SSW-104-02-T-D-RA
1	P7	PCB connector, right angled, male header	Samtec	TSW-104-08-T-D-RA
1	P8	PCB connector, female, mini USB 2.0	Hirose Electric	UX60SC-MB-5S8
1	Q2	45 V, SOT23-M3, NPN transistor	NXP Semiconductors	BC817
1	R1	Resistor, 3.01 kΩ, 1%, R0402	Panasonic	ERJ-2RKF3011X
1	R10	Resistor, 100 kΩ, 1%, 0603,	Bourns	CR0603-FX-1003ELF
6	R39, R103, 115, R117, R207, R209	Resistors, 56 kΩ, 1%, 0603	Multicomp (SPC)	MC 0.063W 0603 1% 56K.
16	R24, R33, R34, R40, R51, R69, R70, R71, R73, R104, R114, R116, R118, R197, R206, R208	Resistors, 10 kΩ, 1%, 0603	Multicomp (SPC)	MC0063W0603110K
8	R75 to R79, R106, R142, R143	Resistors, 1 kΩ, 1%, 0603	Multicomp (SPC)	MC0063W060311K
2	R107, R145	Resistors, 1.5 kΩ, 50 V, 1%, 0603,	Multicomp (SPC)	MC 0.063W 0603 1% 1K5
2	R11, R62	Resistors, 280 kΩ, 0.1%, 0603	Panasonic	ERA-3AEB2803V
27	R6, R15, R26, R53, R58, R63, R65, R67, R68, R80, R84, R87, R88, R90, R92, R112, R119, R148, R150, R191, R194, R195, R196, R210 to R213	Resistors, 0 Ω, 50 V, 1%, 0402	Multicomp (SPC)	MC00625W040210R
4	R72, R74, R113, R144	Resistors, 0 Ω, 1%, 0603	Multicomp (SPC)	MC0603WG00000T5E-TC
4	R12, R52, R54, R64	Resistors, 50 kΩ, 0.1%, 0603	Vishay	PNM0603E5002BST5
1	R121	Resistor, 1 MΩ, 1%, 0201	Panasonic	ERJ-1GNF1004C
1	R122	Resistor, 4.7 kΩ, 25 V, 1%, 0201	Multicomp (SPC)	MC0201L6F4701SE
6	R123, R124, R130, R131, R135, R136	Resistors, 100 kΩ, 1%, 0201	Panasonic	ERJ-1GNF1003C
2	R125, R137	Resistors, 1 kΩ, 1%, 0201	Panasonic	ERJ-1GNF1001C
3	R126, R128, R129	Resistors, 33 Ω, 1%, 0201	Panasonic	ERJ-1GNF33R0C
1	R127	Resistor, 0 Ω, 5%, 0201	Bourns	CR0201-J/-000GLF
3	R132 to R134	Resistors, 100 Ω, 1%, 0201	Panasonic	ERJ-1GNF1000C
1	R149	Resistor, 82 kΩ, 1%, 0603,	Multicomp (SPC)	MC 0.063W 0603 1% 82K.
1	R16	Resistor, 200 kΩ, 1%, 0603	Panasonic	ERJ-3EKF2003V
1	R192	Resistor, 100 kΩ, 1%, 0603	Yageo	RC0603JR-07100KL
1	R193	Resistor, 10 kΩ, 1%, 0402	Panasonic	ERJ-2RKF1002X
4	R2 to R5	Resistors, 75 Ω, 1%, 0603	Panasonic	ERJ-3EKF75R0V
1	R43	Resistor, 390 Ω, 5%, 0402	Panasonic	ERJ-2GEJ391X
2	R46, R47	Resistors, 470 Ω, 1%, 0402	Yageo	RC0402FR-07470RL
1	R48	Resistor, 0 Ω, 500 V, 2512	Vishay	CRCW25120000Z0EG
6	R50, R81, R86, R89, R93, R99	Resistors, 10 Ω, 1%, 0402	Multicomp (SPC)	MC00625W0402110R
1	R57	Resistor, 40 K, 0.1%, 0603	Vishay	PAT0603E4002BST1
1	S1	Switch, 4-position, surface mount, SM_DIP8-2	CTS	219-4MST
5	S2, S5 to S8	Switches, tactile, microminiature top actuated, single-pole, single throw, normally open (SPST-NO)	C&K	PTS830 GM140 SMTR LFS

Qty	Reference Designator	Description	Manufacturer	Part Number
3	S3, S4, S9	16 V, single-pole, 4 throw, rotary switches, SP4T	NIDEC COPAL Electronics	CS-4-14NA
1	T1	Transformer 1000BASE-T magnetic modules	Pulse Electronics	H5007NL
1	U1	IC robust, low latency gigabit Ethernet PHY	Analog Devices	ADIN1300
1	U10	IC USB serial UART	FTDI CHIP	FT232RQ
1	U11	IC-TTL single-positive and gate, SC70-5	Texas Instruments	SN74LVC1G08DCKR
1	U12	3.3 V complementary metal-oxide semiconductor (CMOS) linear regulator with low quiescent current	Analog Devices	ADP124ARHZ-3.3-R7
3	U3, U13, U14	IC-TTL dual supply transceivers, 3-state	NXP Semiconductors	74AVC1T45GW,125
2	U4, U5	Dual 300mA adjustable output, low noise, high power supply rejection ratio (PSRR) voltage regulators	Analog Devices	ADP223ACPZ-R7
1	U7	I^2C compatible serial EEPROM 2-kBit	ATMEL	AT24C02D-SSHM-T
1	U8	CMOS I^2C serial EEPROM, 32-kBit.	ONSEMI	CAT24C32WI-GT3
1	U9	Ultralow power ARM® Cortex®-M3 Micro-controller with integrated power management and 256 kB of embedded flash memory	Analog Devices	ADUCM3029BCPZ
1	Y1	25 MHz, 10 ppm, crystal, 10 pF load capacitor	Seiko Epson	FA-128_25.000000MHZ_10.0_+10-10
1	Y2	32.768 kHz, 20 ppm, crystal, 6 pF load capacitor	Abracon Corp.	ABS07-120-32.768KHZ-T
1	Y3	26 MHz, 30 ppm, crystal, 10 pF load capacitor	ECS, INC.	ECS-260-10-36Q-ES-TR

Table 8. Not Populated

Qty	Reference Designator	Description	Supplier	Part Number
26	5V, AVDD3P3_N, AVDD3P3_P, CLK25, DVDD_N, DVDD_P, GND1, GND2, GND3, GND4, GND5, GPCLK, INT_N, LED_0, LINK_ST, MDC, MDIO, P9, P10, P11, SUPPLY, VDD0P9_N, VDD0P9_P, VDDIO_N, VDDIO_P, XTAL_I	Test point, DNI	Keystone Electronics	1405-2
3	C33, C45, C99	Ceramic capacitors, 0.01 µF, 25 V, 10%, 0402, X7R	TDK	C1005X7R1E103K050EB
1	EXT_12V	PCB connector header, 3.81 mm	Phoenix Contact	1803277
1	J1	PCB connector, straight SMA	TE Connectivity LTD	5-1814832-1
7	R49, R95, R97, R101, R110, R111, R120	Resistors, 0 Ω, 50 V, 1%, 0402	Multicomp (SPC)	MC00625W040210R
4	R138 to R141	Resistors, 0 Ω, R0805	Multicomp (SPC)	MC 0.1W 0805 0R
1	R19	Resistor, 1 MΩ, 1%, 0402	Panasonic	ERJ-2RKF1004X
12	R8, R9, R22, R23, R27 to R32, R37, R38	Resistors, 10 kΩ, 1%, 0603	Multicomp (SPC)	MC0063W0603110K
1	R85	Resistor 10 Ω, 1%, R0402	Multicomp (SPC)	MC00625W0402110R

Qty	Reference Designator	Description	Supplier	Part Number
1	U2	500 mA, low noise low dropout (LDO) regulator with soft start	Analog Devices	ADP7105ACPZ-5.0-R7
1	C43	Ceramic capacitors, 4.7 µF, 10 V, 10%, 0603, X6S	Murata	GRM185C81A475KE11D
2	C13, C14	Ceramic capacitors, 4.7 µF, 25 V, 10 %, 1206, X7R	KEMET	C1206C475K3RACTU
1	JP1	PCB connector, jumper, straight, male, 2-pin, 2.54 mm pitch	Amphenol FCI	69157-102HLF
1	SHIELD	PCB connector, 4 mm socket	Rapid	20054

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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