



# 16-Channel Buffered CMOS Logic-Level Translators

## General Description

The MAX13101E/MAX13102E/MAX13103E/MAX13108E 16-bit bidirectional CMOS logic-level translators provide the level shifting necessary to allow data transfer in multivoltage systems. These devices are inherently bidirectional due to their design and do not require the use of a direction input. Externally applied voltages,  $V_{CC}$  and  $V_L$ , set the logic levels on either side of the devices. Logic signals present on the  $V_L$  side of the device appear as a higher voltage logic signal on the  $V_{CC}$  side of the device, and vice-versa.

The MAX13101E/MAX13102E/MAX13103E feature an enable input (EN) that, when low, reduces the  $V_{CC}$  and  $V_L$  supply currents to less than  $2\mu A$ . The MAX13108E features a multiplexing input (MULT) that selects one byte between the two, thus allowing multiplexing of the signals. The MAX13101E/MAX13102E/MAX13103E/MAX13108E have  $\pm 15kV$  ESD protection on the I/O  $V_{CC}$  side for greater protection in applications that route signals externally. Three different output configurations are available during shutdown, allowing the I/O on the  $V_{CC}$  side or the  $V_L$  side to be put in a high-impedance state or pulled to ground through an internal  $6k\Omega$  resistor.

The MAX13101E/MAX13102E/MAX13103E/MAX13108E accept  $V_{CC}$  voltages from +1.65V to +5.5V and  $V_L$  voltages from +1.2V to  $V_{CC}$ , making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. The MAX13101E/MAX13102E/MAX13103E/MAX13108E are available in 36-bump UCSP™ and 40-pin TQFN packages, and operate over the extended  $-40^\circ C$  to  $+85^\circ C$  temperature range.

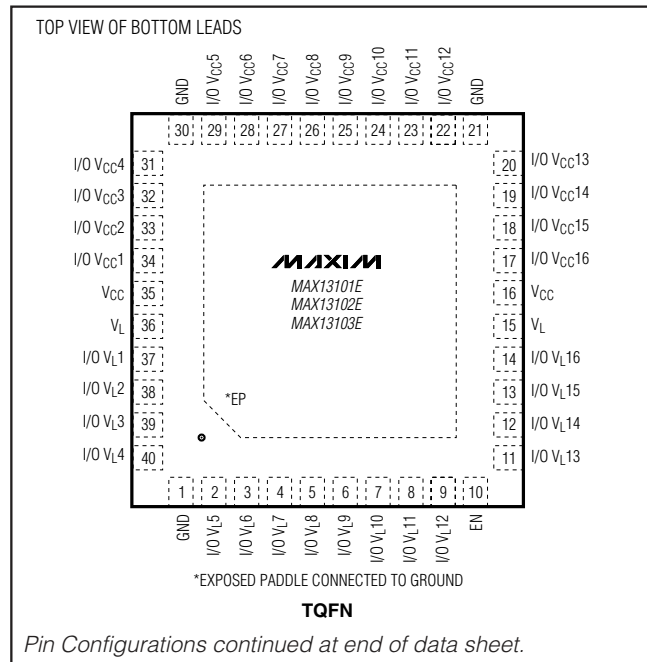
## Applications

CMOS Logic-Level Translation	PDA's
Portable Equipment	Digital Still Cameras
Cell Phones	Smart Phones

## Features

- ◆ Wide Supply Voltage Range  
 $V_{CC}$  Range of 1.65V to 5.5V  
 $V_L$  Range of 1.2V to  $V_{CC}$
- ◆ ESD Protection on I/O  $V_{CC}$  Lines  
 $\pm 15kV$  Human Body Model
- ◆ Up to 20Mbps Throughput
- ◆ Low  $0.03\mu A$  Typical Quiescent Current
- ◆ UCSP and TQFN Packages

## Pin Configurations



## Ordering Information/Selector Guide

PART	PIN-PACKAGE	DATA RATE (Mbps)	I/O $V_L$ STATE DURING SHUTDOWN	I/O $V_{CC}$ STATE DURING SHUTDOWN	MULTIPLEXER FEATURE	PKG CODE
MAX13101EEBX*	36 UCSP** 3.06mm x 3.06mm	20	High impedance	$6k\Omega$ to GND	No	B36-1
MAX13101EETL	40 TQFN 5mm x 5mm x 0.8mm	20	High impedance	$6k\Omega$ to GND	No	T4055-1

**Note:** All devices operate over the  $-40^\circ C$  to  $+85^\circ C$  operating temperature range.

\*Future product—contact factory for availability.

\*\*UCSP bumps are in a 6 x 6 array.

Ordering Information/Selector Guide continued at end of data sheet.

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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).

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## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V <sub>CC</sub> .....	-0.3V to +6V
V <sub>L</sub> .....	-0.3V to +6V
I/O V <sub>CC</sub> .....	-0.3V to (V <sub>CC</sub> + 0.3V)
I/O V <sub>L</sub> .....	-0.3V to (V <sub>L</sub> + 0.3V)
EN, MULT .....	-0.3V to +6V
Short-Circuit Duration I/O V <sub>L</sub> , I/O V <sub>CC</sub> to GND .....	Continuous
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
36-Bump UCSP (derate 17.0mW/°C above +70°C) ..	1361mW
40-Pin TQFN (derate 35.7mW/°C above +70°C) .....	2857mW

Operating Temperature Range .....	-40°C to +85°C
Maximum Junction Temperature .....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (soldering, 10s) .....	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +1.65V to +5.5V, V<sub>L</sub> = +1.2V to V<sub>CC</sub>, EN = V<sub>L</sub> (MAX13101E/MAX13102E/MAX13103E), MULT = V<sub>L</sub> or GND (MAX13108E), T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V<sub>CC</sub> = +1.65V, V<sub>L</sub> = +1.2V, T<sub>A</sub> = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLIES</b>						
V <sub>L</sub> Supply Range	V <sub>L</sub>		1.2		V <sub>CC</sub>	V
V <sub>CC</sub> Supply Range	V <sub>CC</sub>		1.65		5.50	V
Supply Current from V <sub>CC</sub>	I <sub>QVCC</sub>	I/O V <sub>CC</sub> = GND, I/O V <sub>L</sub> = GND or I/O V <sub>CC</sub> = V <sub>CC</sub> , I/O V <sub>L</sub> = V <sub>L</sub> , EN = V <sub>L</sub> , MULT = GND or V <sub>L</sub>		0.03	10	μA
Supply Current from V <sub>L</sub>	I <sub>QVL</sub>	I/O V <sub>CC</sub> = GND, I/O V <sub>L</sub> = GND or I/O V <sub>CC</sub> = V <sub>CC</sub> , I/O V <sub>L</sub> = V <sub>L</sub> , EN = V <sub>L</sub> , MULT = GND or V <sub>L</sub>		0.03	20	μA
V <sub>CC</sub> Shutdown Supply Current	I <sub>SHDN-VCC</sub>	T <sub>A</sub> = +25°C, EN = GND, I/O V <sub>CC</sub> = GND, I/O V <sub>L</sub> = GND, MAX13101E/MAX13102E/MAX13103E		0.03	1	μA
V <sub>L</sub> Shutdown Supply Current	I <sub>SHDN-VL</sub>	T <sub>A</sub> = +25°C, EN = GND, I/O V <sub>CC</sub> = GND, I/O V <sub>L</sub> = GND, MAX13101E/MAX13102E/MAX13103E		0.03	2	μA
I/O V <sub>CC</sub> Tri-State Output Leakage Current		T <sub>A</sub> = +25°C, EN = GND, MAX13102E/MAX13103E		0.02	1	μA
		T <sub>A</sub> = +25°C, MULT = GND (I/O V <sub>CC</sub> 1 - I/O V <sub>CC</sub> 8) or MULT = V <sub>L</sub> (I/O V <sub>CC</sub> 9 - I/O V <sub>CC</sub> 16) MAX13108E		0.02	1	
I/O V <sub>L</sub> Tri-State Output Leakage Current		T <sub>A</sub> = +25°C, EN = GND, MAX13101E/ MAX13103E		0.02	1	μA
		T <sub>A</sub> = +25°C, MULT = GND (I/O V <sub>L</sub> 1 - I/O V <sub>L</sub> 8) or MULT = V <sub>L</sub> (I/O V <sub>L</sub> 9 - I/O V <sub>L</sub> 16) MAX13108E		0.02	1	
I/O V <sub>L</sub> Pull-down Resistance During Shutdown		EN = GND, MAX13102E	4		10	kΩ

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +1.65V$  to  $+5.5V$ ,  $V_L = +1.2V$  to  $V_{CC}$ ,  $EN = V_L$  (MAX13101E/MAX13102E/MAX13103E),  $MULT = V_L$  or  $GND$  (MAX13108E),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = +1.65V$ ,  $V_L = +1.2V$ ,  $T_A = +25^\circ C$ .) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Pulldown Resistance During Shutdown		$EN = GND$ , MAX13101E	4		10	$k\Omega$
EN or MULT Input Leakage Current		$T_A = +25^\circ C$			1	$\mu A$
<b>LOGIC-LEVEL THRESHOLDS</b>						
I/O $V_L\_ $ Input-Voltage High Threshold	$V_{IHL}$				$2/3 \times V_L$	V
I/O $V_L\_ $ Input-Voltage Low Threshold	$V_{ILL}$		$1/3 \times V_L$			V
I/O $V_{CC\_}$ Input-Voltage High Threshold	$V_{IHC}$				$2/3 \times V_{CC}$	V
I/O $V_{CC\_}$ Input-Voltage Low Threshold	$V_{ILC}$		$1/3 \times V_{CC}$			V
EN, MULT Input-Voltage High Threshold	$V_{IH-SHDN}$				$V_L - 0.4$	V
EN, MULT Input-Voltage Low Threshold	$V_{IL-SHDN}$		0.4			V
I/O $V_L\_ $ Output-Voltage High	$V_{OHL}$	I/O $V_L\_ $ source current = $20\mu A$ , I/O $V_{CC\_} \geq V_{IHC}$	$V_L - 0.4$			V
I/O $V_L\_ $ Output-Voltage Low	$V_{OLL}$	I/O $V_L\_ $ sink current = $20\mu A$ , I/O $V_{CC\_} \leq V_{ILC}$			0.4	V
I/O $V_{CC\_}$ Output-Voltage High	$V_{OHC}$	I/O $V_{CC\_}$ source current = $20\mu A$ , I/O $V_L\_ \geq V_{IHL}$	$V_{CC} - 0.4$			V
I/O $V_{CC\_}$ Output-Voltage Low	$V_{OLC}$	I/O $V_{CC\_}$ sink current = $20\mu A$ , I/O $V_L\_ \leq V_{ILL}$			0.4	V
<b>RISE/FALL-TIME ACCELERATOR STAGE</b>						
Transition-Detect Threshold		I/O $V_{CC}$ side			$V_{CC} / 2$	V
		I/O $V_L$ side			$V_L / 2$	
Accelerator Pulse Duration		$V_L = 1.2V$ , $V_{CC} = 1.65V$		20		ns
I/O $V_L\_ $ Output-Accelerator Sink Impedance		$V_L = 1.2V$ , $V_{CC} = 1.65V$		60		$\Omega$
		$V_L = 5V$ , $V_{CC} = 5V$		5		
I/O $V_{CC\_}$ Output-Accelerator Sink Impedance		$V_L = 1.2V$ , $V_{CC} = 1.65V$		15		$\Omega$
		$V_L = 5V$ , $V_{CC} = 5V$		5		
I/O $V_L\_ $ Output-Accelerator Source Impedance		$V_L = 1.2V$ , $V_{CC} = 1.65V$		30		$\Omega$
		$V_L = 5V$ , $V_{CC} = 5V$		5		
I/O $V_{CC\_}$ Output-Accelerator Source Impedance		$V_L = 1.2V$ , $V_{CC} = 1.65V$		20		$\Omega$
		$V_L = 5V$ , $V_{CC} = 5V$		7		
<b>ESD PROTECTION</b>						
I/O $V_{CC\_}$		Human Body Model		$\pm 15$		kV

MAX13101E/MAX13102E/MAX13103E/MAX13108E

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## TIMING CHARACTERISTICS

( $V_{CC} = +1.65V$  to  $+5.5V$ ,  $V_L = +1.2V$  to  $V_{CC}$ ,  $EN = V_L$  (MAX13101E/MAX13102E/MAX13103E),  $MULT = V_L$  or  $GND$  (MAX13108E),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = +1.65V$ ,  $V_L = +1.2V$ ,  $T_A = +25^\circ C$ .) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_L$ _ Rise Time	$t_{RVL}$	$R_S = 50\Omega$ , $C_{I/OVL\_} = 15pF$ , $t_{RISE} \leq 3ns$ , (Figures 2a, 2b)			15	ns
I/O $V_L$ _ Fall Time	$t_{FVL}$	$R_S = 50\Omega$ , $C_{I/OVL\_} = 15pF$ , $t_{FALL} \leq 3ns$ , (Figures 2a, 2b)			15	ns
I/O $V_{CC}$ _ Rise Time	$t_{RVCC}$	$R_S = 50\Omega$ , $C_{I/OVCC\_} = 50pF$ , $t_{RISE} \leq 3ns$ , (Figures 1a, 1b)			15	ns
I/O $V_{CC}$ _ Fall Time	$t_{FVCC}$	$R_S = 50\Omega$ , $C_{I/OVCC\_} = 50pF$ , $t_{FALL} \leq 3ns$ , (Figures 1a, 1b)			15	ns
Propagation Delay (Driving I/O $V_L$ _)	$t_{PVL-VCC}$	$R_S = 50\Omega$ , $C_{I/OVCC\_} = 50pF$ , $t_{RISE} \leq 3ns$ , (Figures 1a, 1b)			20	ns
Propagation Delay (Driving I/O $V_{CC}$ _)	$t_{PVCC-VL}$	$R_S = 50\Omega$ , $C_{I/OVL\_} = 15pF$ , $t_{RISE} \leq 3ns$ , (Figures 2a, 2b)			20	ns
Channel-to-Channel Skew	$t_{SKEW}$	$R_S = 50\Omega$ , $C_{I/OVCC\_} = 50pF$ , $C_{I/OVL\_} = 15pF$ , $t_{RISE} \leq 3ns$			5	ns
Part-to-Part Skew	$t_{PPSKEW}$	$R_S = 50\Omega$ , $C_{I/OVCC\_} = 50pF$ , $C_{I/OVL\_} = 15pF$ , $t_{RISE} \leq 3ns$ , $\Delta T_A = +20^\circ C$ (Notes 3, 4)			10	ns
Propagation Delay from I/O $V_L$ _ to I/O $V_{CC}$ _ After EN	$t_{EN-VCC}$	$C_{I/OVCC\_} = 50pF$ (Figure 3)			1	$\mu s$
Propagation Delay from I/O $V_{CC}$ _ to I/O $V_L$ _ After EN	$t_{EN-VL}$	$C_{I/OVL\_} = 15pF$ (Figure 4)			1	$\mu s$
Maximum Data Rate		$R_{SOURCE} = 50\Omega$ , $C_{I/OVCC\_} = 50pF$ , $C_{I/OVL\_} = 15pF$ , $t_{RISE} \leq 3ns$	20			Mbps

**Note 1:** All units are 100% production tested at  $T_A = +25^\circ C$ . Limits over the operating temperature range are guaranteed by design and not production tested.

**Note 2:** For normal operation, ensure that  $V_L < (V_{CC} + 0.3V)$ . During power-up,  $V_L > (V_{CC} + 0.3V)$  does not damage the device.

**Note 3:**  $V_{CC}$  from device 1 must equal  $V_{CC}$  of device 2.  $V_L$  from device 1 must equal  $V_L$  of device 2.

**Note 4:** Guaranteed by design, not production tested.

# 16-Channel Buffered CMOS Logic-Level Translators

## Test Circuits/Timing Diagrams

MAX13101E/MAX13102E/MAX13103E/MAX13108E

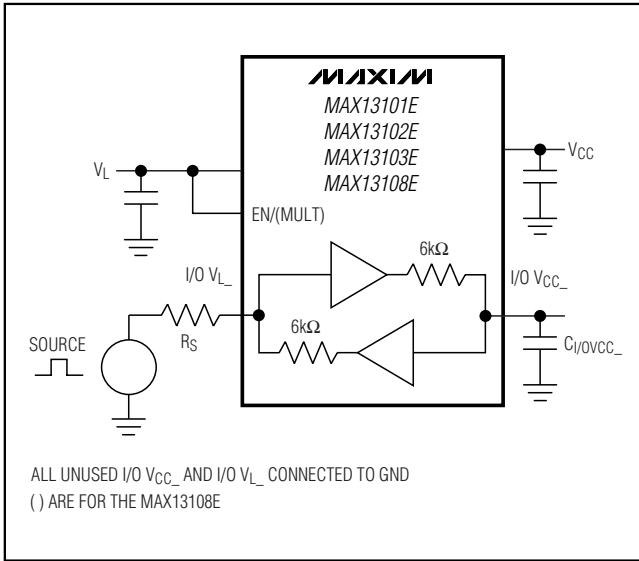


Figure 1a. Driving I/O VL\_

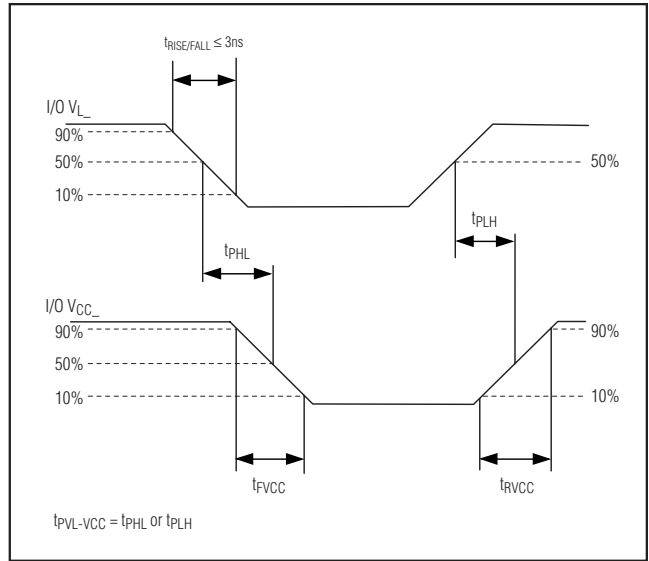


Figure 1b. Timing for Driving I/O VL\_

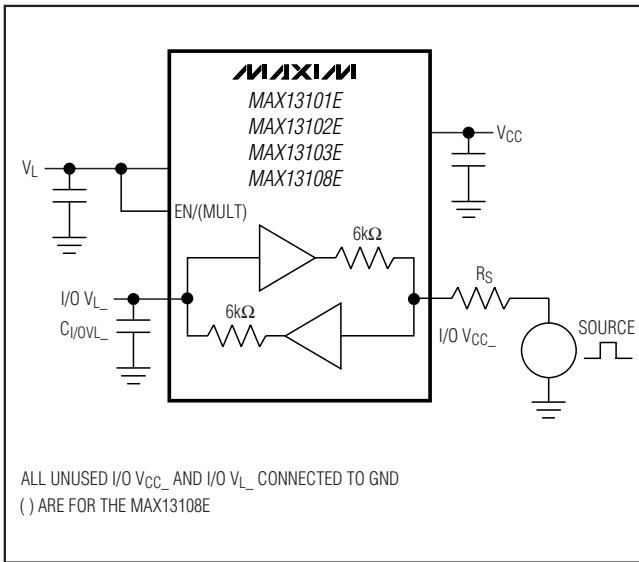


Figure 2a. Driving I/O VCC\_

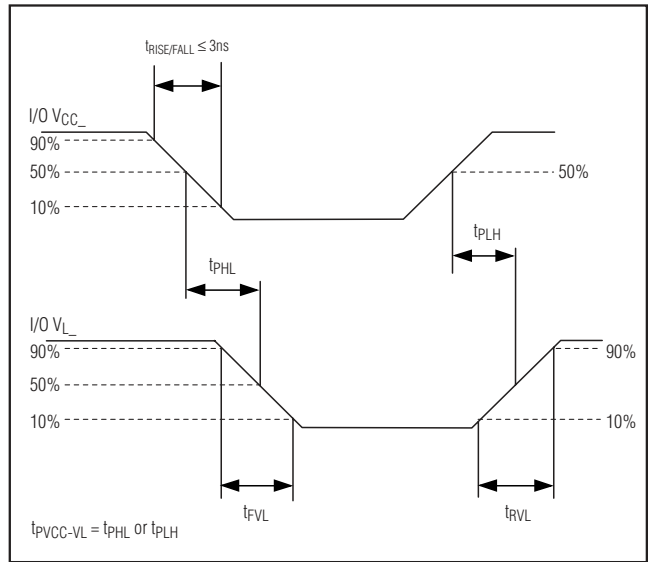


Figure 2b. Timing for Driving I/O VCC\_

# 16-Channel Buffered CMOS Logic-Level Translators

## Test Circuits/Timing Diagrams (continued)

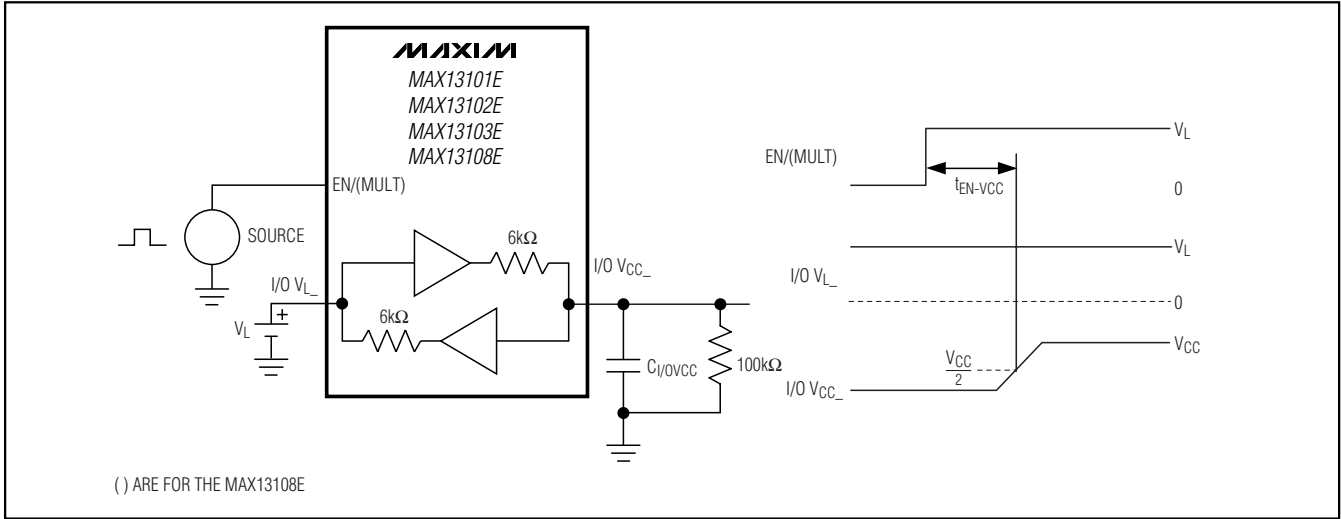


Figure 3. Propagation Delay from I/O VL\_ to I/O VCC\_ After EN

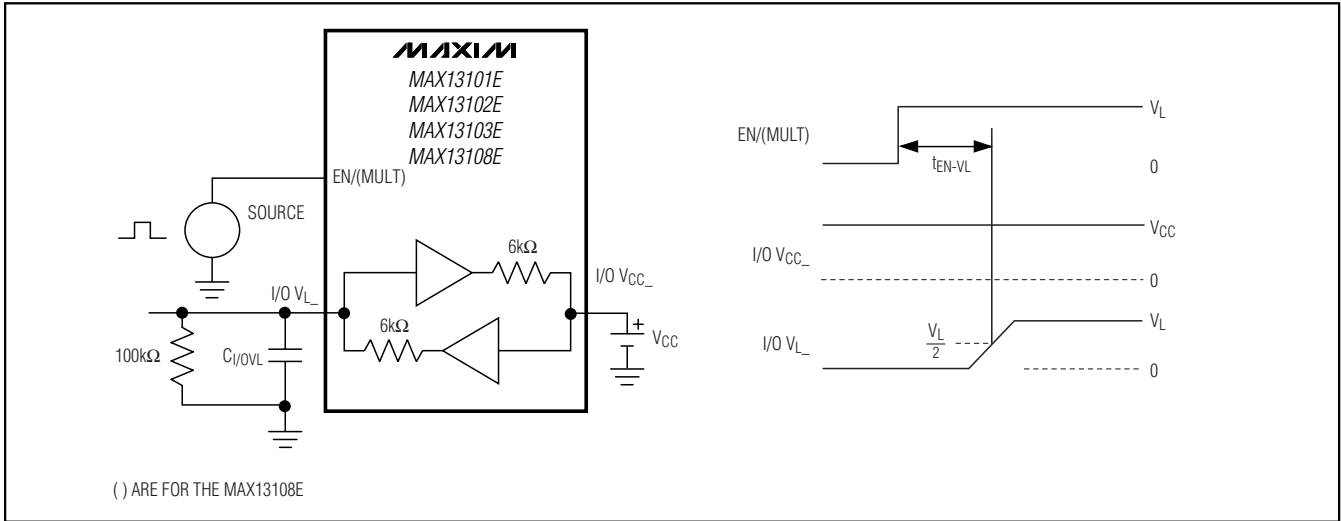


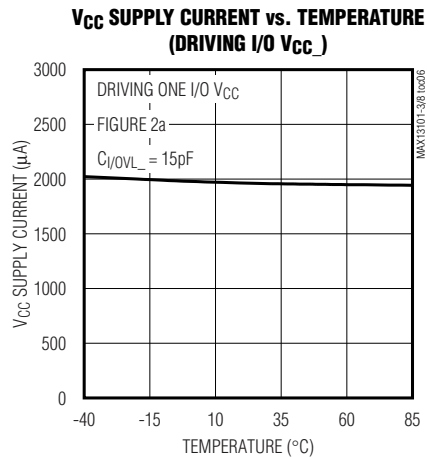
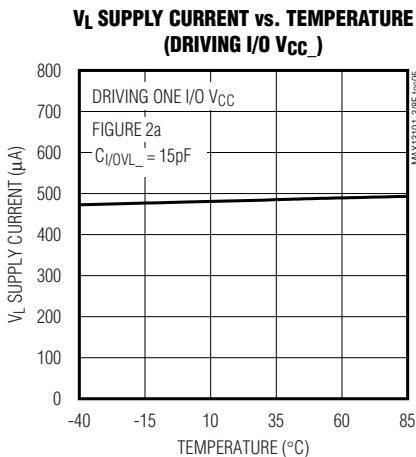
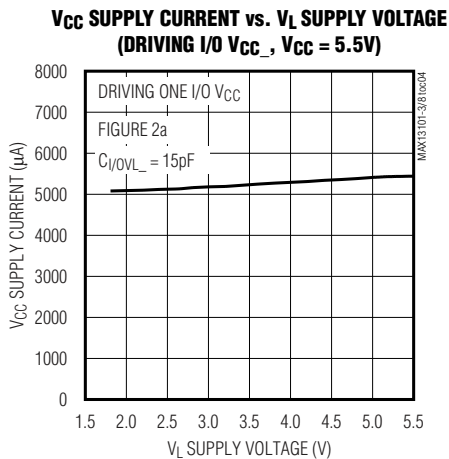
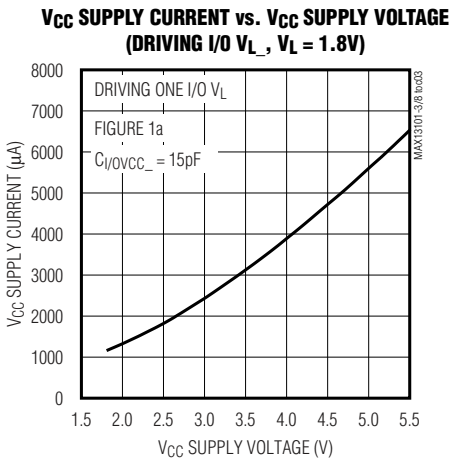
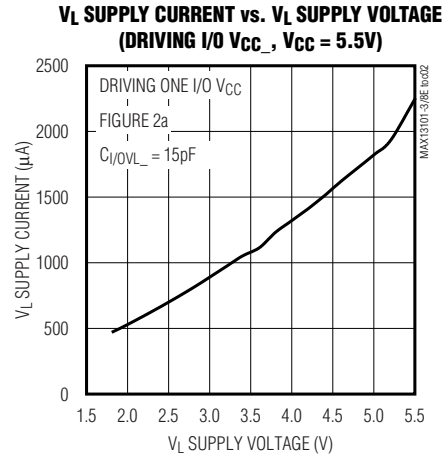
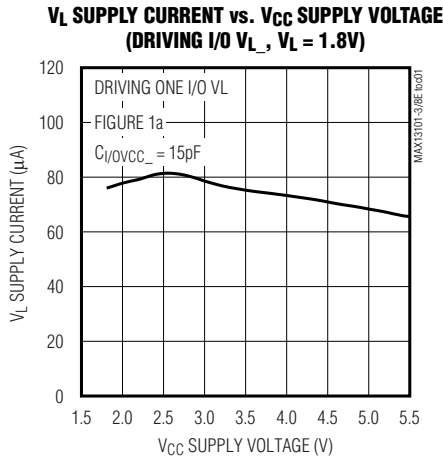
Figure 4. Propagation Delay from I/O VCC\_ to I/O VL\_ After EN

# 16-Channel Buffered CMOS Logic-Level Translators

## Typical Operating Characteristics

( $V_{CC} = 3.3V$ ,  $V_L = 1.8V$ , data rate = 20Mbps,  $T_A = +25^\circ C$ , unless otherwise noted.)

MAX13101E/MAX13102E/MAX13103E/MAX13108E

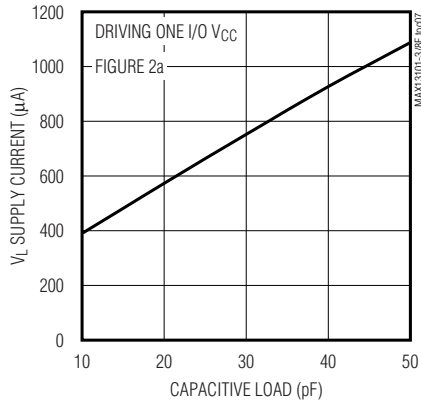


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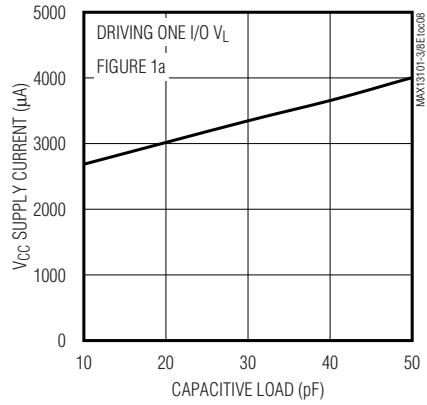
## Typical Operating Characteristics (continued)

( $V_{CC} = 3.3V$ ,  $V_L = 1.8V$ , data rate = 20Mbps,  $T_A = +25^\circ C$ , unless otherwise noted.)

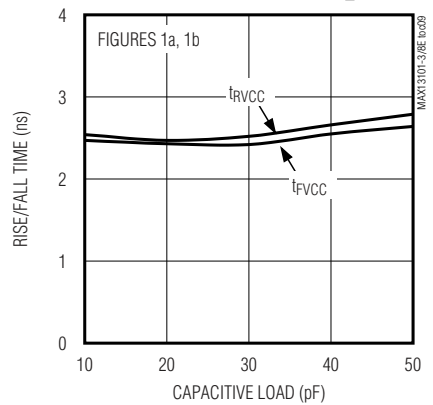
**$V_L$  SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O  $V_L$  (DRIVING I/O  $V_{CC}$ )**



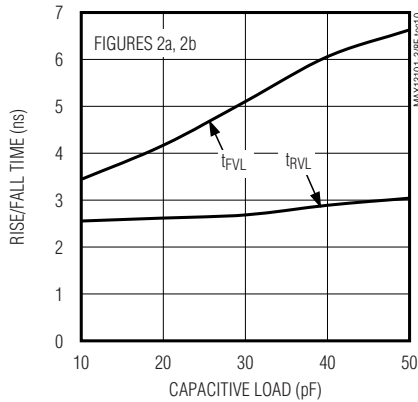
**$V_{CC}$  SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O  $V_{CC}$  (DRIVING I/O  $V_L$ )**



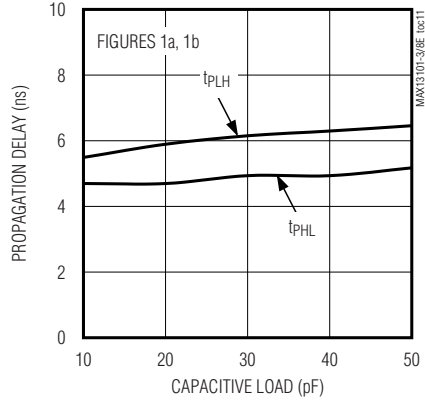
**RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O  $V_{CC}$  (DRIVING I/O  $V_L$ )**



**RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O  $V_L$  (DRIVING I/O  $V_{CC}$ )**



**PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O  $V_{CC}$  (DRIVING I/O  $V_L$ )**

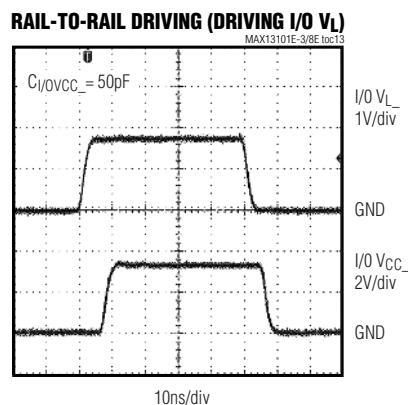
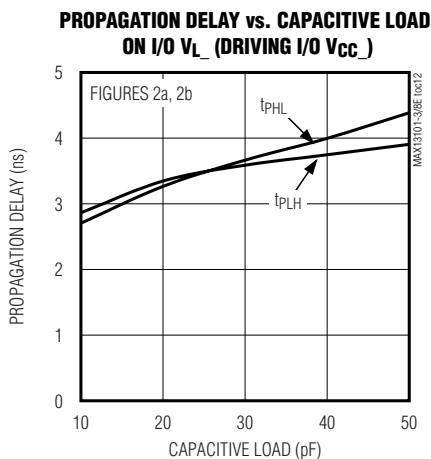




# 16-Channel Buffered CMOS Logic-Level Translators

## Typical Operating Characteristics (continued)

( $V_{CC} = 3.3V$ ,  $V_L = 1.8V$ , data rate = 20Mbps,  $T_A = +25^\circ C$ , unless otherwise noted.)



## Pin Description—MAX13101E/MAX13102E/MAX13103E

PIN		NAME	FUNCTION
TQFN	UCSP		
1, 21, 30	D6	GND	Ground
2	C2	I/O $V_L5$	Input/Output 5. Referenced to $V_L$ .
3	A3	I/O $V_L6$	Input/Output 6. Referenced to $V_L$ .
4	B3	I/O $V_L7$	Input/Output 7. Referenced to $V_L$ .
5	C3	I/O $V_L8$	Input/Output 8. Referenced to $V_L$ .
6	A4	I/O $V_L9$	Input/Output 9. Referenced to $V_L$ .
7	B4	I/O $V_L10$	Input/Output 10. Referenced to $V_L$ .
8	C4	I/O $V_L11$	Input/Output 11. Referenced to $V_L$ .
9	A5	I/O $V_L12$	Input/Output 12. Referenced to $V_L$ .
10	C6	EN	Global Enable Input. Pull EN low for shutdown. Drive EN to $V_{CC}$ or $V_L$ for normal operation.
11	B5	I/O $V_L13$	Input/Output 13. Referenced to $V_L$ .
12	C5	I/O $V_L14$	Input/Output 14. Referenced to $V_L$ .
13	A6	I/O $V_L15$	Input/Output 15. Referenced to $V_L$ .
14	B6	I/O $V_L16$	Input/Output 16. Referenced to $V_L$ .
15, 36	A1	$V_L$	Logic Supply Voltage, $+1.2V \leq V_L \leq V_{CC}$ . Bypass $V_L$ to GND with a $0.1\mu F$ capacitor.
16, 35	F1	$V_{CC}$	$V_{CC}$ Supply Voltage, $+1.65V \leq V_{CC} \leq +5.5V$ . Bypass $V_{CC}$ to GND with a $0.1\mu F$ capacitor. For full ESD protection, connect a $1.0\mu F$ capacitor from $V_{CC}$ to GND, located as close to the $V_{CC}$ input as possible.
17	E6	I/O $V_{CC}16$	Input/Output 16. Referenced to $V_{CC}$ .
18	F6	I/O $V_{CC}15$	Input/Output 15. Referenced to $V_{CC}$ .

# 16-Channel Buffered CMOS Logic-Level Translators

## Pin Description—MAX13101E/MAX13102E/MAX13103E (continued)

PIN		NAME	FUNCTION
TQFN	UCSP		
19	D5	I/O V <sub>CC14</sub>	Input/Output 14. Referenced to V <sub>CC</sub> .
20	E5	I/O V <sub>CC13</sub>	Input/Output 13. Referenced to V <sub>CC</sub> .
22	F5	I/O V <sub>CC12</sub>	Input/Output 12. Referenced to V <sub>CC</sub> .
23	D4	I/O V <sub>CC11</sub>	Input/Output 11. Referenced to V <sub>CC</sub> .
24	E4	I/O V <sub>CC10</sub>	Input/Output 10. Referenced to V <sub>CC</sub> .
25	F4	I/O V <sub>CC9</sub>	Input/Output 9. Referenced to V <sub>CC</sub> .
26	D3	I/O V <sub>CC8</sub>	Input/Output 8. Referenced to V <sub>CC</sub> .
27	E3	I/O V <sub>CC7</sub>	Input/Output 7. Referenced to V <sub>CC</sub> .
28	F3	I/O V <sub>CC6</sub>	Input/Output 6. Referenced to V <sub>CC</sub> .
29	D2	I/O V <sub>CC5</sub>	Input/Output 5. Referenced to V <sub>CC</sub> .
31	E2	I/O V <sub>CC4</sub>	Input/Output 4. Referenced to V <sub>CC</sub> .
32	F2	I/O V <sub>CC3</sub>	Input/Output 3. Referenced to V <sub>CC</sub> .
33	D1	I/O V <sub>CC2</sub>	Input/Output 2. Referenced to V <sub>CC</sub> .
34	E1	I/O V <sub>CC1</sub>	Input/Output 1. Referenced to V <sub>CC</sub> .
37	B1	I/O V <sub>L1</sub>	Input/Output 1. Referenced to V <sub>L</sub> .
38	C1	I/O V <sub>L2</sub>	Input/Output 2. Referenced to V <sub>L</sub> .
39	A2	I/O V <sub>L3</sub>	Input/Output 3. Referenced to V <sub>L</sub> .
40	B2	I/O V <sub>L4</sub>	Input/Output 4. Referenced to V <sub>L</sub> .
EP	—	EP	Exposed Paddle. Connect EP to GND.

## Pin Description—MAX13108E

PIN		NAME	FUNCTION
TQFN	UCSP		
1, 21, 30	D6	GND	Ground
2	C2	I/O V <sub>L5</sub>	Input/Output 5. Referenced to V <sub>L</sub> .
3	A3	I/O V <sub>L6</sub>	Input/Output 6. Referenced to V <sub>L</sub> .
4	B3	I/O V <sub>L7</sub>	Input/Output 7. Referenced to V <sub>L</sub> .
5	C3	I/O V <sub>L8</sub>	Input/Output 8. Referenced to V <sub>L</sub> .
6	A4	I/O V <sub>L9</sub>	Input/Output 9. Referenced to V <sub>L</sub> .
7	B4	I/O V <sub>L10</sub>	Input/Output 10. Referenced to V <sub>L</sub> .
8	C4	I/O V <sub>L11</sub>	Input/Output 11. Referenced to V <sub>L</sub> .
9	A5	I/O V <sub>L12</sub>	Input/Output 12. Referenced to V <sub>L</sub> .

# 16-Channel Buffered CMOS Logic-Level Translators

## Pin Description—MAX13108E (continued)

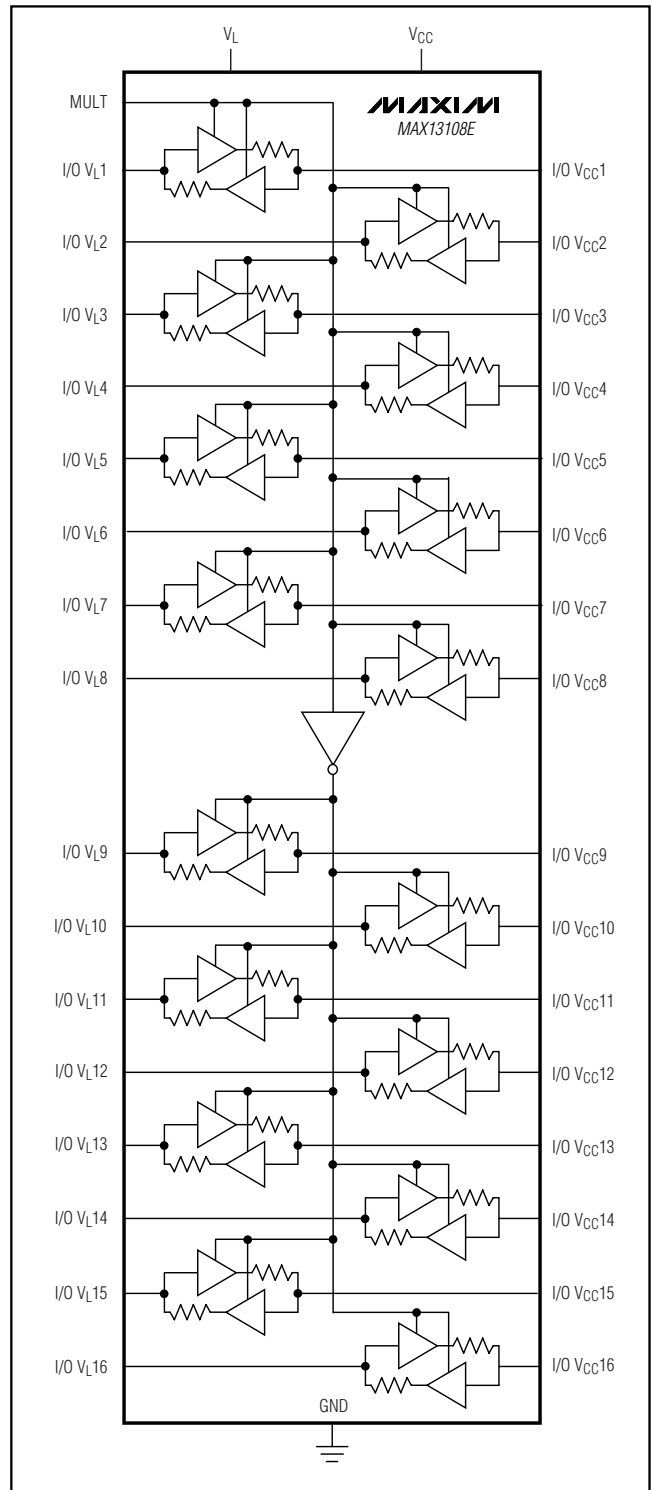
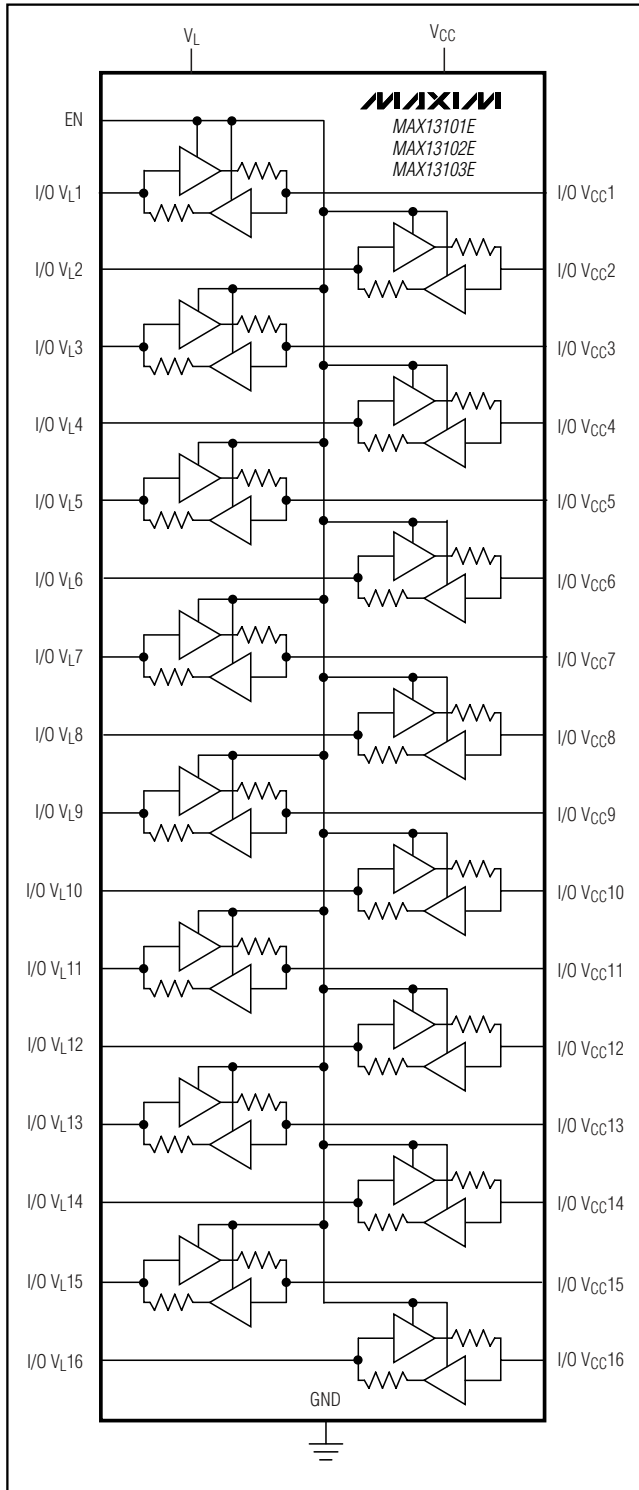
PIN		NAME	FUNCTION
TQFN	UCSP		
10	C6	MULT	Multiplexing Input. Drive MULT low to enable channels 9 to 16. Driving MULT low puts channels 1 to 8 into tri-state. Drive MULT to V <sub>CC</sub> or V <sub>L</sub> to enable channels 1 to 8. Driving MULT to V <sub>CC</sub> or V <sub>L</sub> puts channels 9 to 16 into tri-state.
11	B5	I/O V <sub>L</sub> 13	Input/Output 13. Referenced to V <sub>L</sub> .
12	C5	I/O V <sub>L</sub> 14	Input/Output 14. Referenced to V <sub>L</sub> .
13	A6	I/O V <sub>L</sub> 15	Input/Output 15. Referenced to V <sub>L</sub> .
14	B6	I/O V <sub>L</sub> 16	Input/Output 16. Referenced to V <sub>L</sub> .
15, 36	A1	V <sub>L</sub>	Logic Supply Voltage, +1.2V ≤ V <sub>L</sub> ≤ V <sub>CC</sub> . Bypass V <sub>L</sub> to GND with a 0.1μF capacitor.
16, 35	F1	V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage, +1.65V ≤ V <sub>CC</sub> ≤ +5.5V. Bypass V <sub>CC</sub> to GND with a 0.1μF capacitor. For full ESD protection, connect a 1.0μF capacitor from V <sub>CC</sub> to GND, located as close to the V <sub>CC</sub> input as possible.
17	E6	I/O V <sub>CC</sub> 16	Input/Output 16. Referenced to V <sub>CC</sub> .
18	F6	I/O V <sub>CC</sub> 15	Input/Output 15. Referenced to V <sub>CC</sub> .
19	D5	I/O V <sub>CC</sub> 14	Input/Output 14. Referenced to V <sub>CC</sub> .
20	E5	I/O V <sub>CC</sub> 13	Input/Output 13. Referenced to V <sub>CC</sub> .
22	F5	I/O V <sub>CC</sub> 12	Input/Output 12. Referenced to V <sub>CC</sub> .
23	D4	I/O V <sub>CC</sub> 11	Input/Output 11. Referenced to V <sub>CC</sub> .
24	E4	I/O V <sub>CC</sub> 10	Input/Output 10. Referenced to V <sub>CC</sub> .
25	F4	I/O V <sub>CC</sub> 9	Input/Output 9. Referenced to V <sub>CC</sub> .
26	D3	I/O V <sub>CC</sub> 8	Input/Output 8. Referenced to V <sub>CC</sub> .
27	E3	I/O V <sub>CC</sub> 7	Input/Output 7. Referenced to V <sub>CC</sub> .
28	F3	I/O V <sub>CC</sub> 6	Input/Output 6. Referenced to V <sub>CC</sub> .
29	D2	I/O V <sub>CC</sub> 5	Input/Output 5. Referenced to V <sub>CC</sub> .
31	E2	I/O V <sub>CC</sub> 4	Input/Output 4. Referenced to V <sub>CC</sub> .
32	F2	I/O V <sub>CC</sub> 3	Input/Output 3. Referenced to V <sub>CC</sub> .
33	D1	I/O V <sub>CC</sub> 2	Input/Output 2. Referenced to V <sub>CC</sub> .
34	E1	I/O V <sub>CC</sub> 1	Input/Output 1. Referenced to V <sub>CC</sub> .
37	B1	I/O V <sub>L</sub> 1	Input/Output 1. Referenced to V <sub>L</sub> .
38	C1	I/O V <sub>L</sub> 2	Input/Output 2. Referenced to V <sub>L</sub> .
39	A2	I/O V <sub>L</sub> 3	Input/Output 3. Referenced to V <sub>L</sub> .
40	B2	I/O V <sub>L</sub> 4	Input/Output 4. Referenced to V <sub>L</sub> .
EP	—	EP	Exposed Paddle. Connect EP to GND.

MAX13101E/MAX13102E/MAX13103E/MAX13108E

# 16-Channel Buffered CMOS Logic-Level Translators

**MAX13101E/MAX13102E/MAX13103E/MAX13108E**

## Functional Diagrams



# 16-Channel Buffered CMOS Logic-Level Translators

## Detailed Description

The MAX13101E/MAX13102E/MAX13103E/MAX13108E logic-level translators provide the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages,  $V_{CC}$  and  $V_L$ , set the logic levels on either side of the device. Logic signals present on the  $V_L$  side of the device appear as a higher voltage logic signal on the  $V_{CC}$  side of the device, and vice-versa. The MAX13101E/MAX13102E/MAX13103E/MAX13108E are bidirectional level translators allowing data translation in either direction ( $V_L \leftrightarrow V_{CC}$ ) on any single data line. The MAX13101E/MAX13102E/MAX13103E/MAX13108E accept  $V_L$  from +1.2V to  $V_{CC}$ . All devices have a  $V_{CC}$  range from +1.65V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX13101E/MAX13102E/MAX13103E feature an output enable mode that reduces  $V_{CC}$  supply current to less than  $1\mu\text{A}$ , and  $V_L$  supply current to less than  $2\mu\text{A}$  when in shutdown. The MAX13108E features a multiplexing input that selects one byte between the two, thus allowing multiplexing of the signals. The MAX13101E/MAX13102E/MAX13103E/MAX13108E have  $\pm 15\text{kV}$  ESD protection on the I/O  $V_{CC}$  side for greater protection in applications that route signals externally. The MAX13101E/MAX13102E/MAX13103E/MAX13108E operate at a guaranteed data rate of 20Mbps. The maximum data rate depends heavily on the load capacitance (see the *Typical Operating Characteristics*) and the output impedance of the external driver.

## Power-Supply Sequencing

For proper operation, ensure that  $+1.65\text{V} \leq V_{CC} \leq +5.5\text{V}$ ,  $+1.2\text{V} \leq V_L \leq +5.5\text{V}$ , and  $V_L \leq V_{CC}$ . During power-up sequencing,  $V_L \geq V_{CC}$  does not damage the device. When  $V_{CC}$  is disconnected and  $V_L$  is powering up, up to 10mA of current can be sourced to each load on the  $V_L$  side, yet the device does not latch up. To guarantee that no excess leakage current flows and that the device does not interfere with the I/O on the  $V_L$  side,  $V_{CC}$  should be connected to GND with a max  $50\Omega$  resistor when the  $V_{CC}$  supply is not present (Figure 5).

## Input Driver Requirements

The MAX13101E/MAX13102E/MAX13103E/MAX13108E architecture is based on a one-shot accelerator output stage (Figure 6). Accelerator output stages are always in tri-state except when there is a transition on any of the translators on the input side, either I/O  $V_{L\_}$  or I/O  $V_{CC\_}$ . Then a short pulse is generated, during which the accelerator output stages become active and charge/discharge the capacitances at the I/Os. Due to

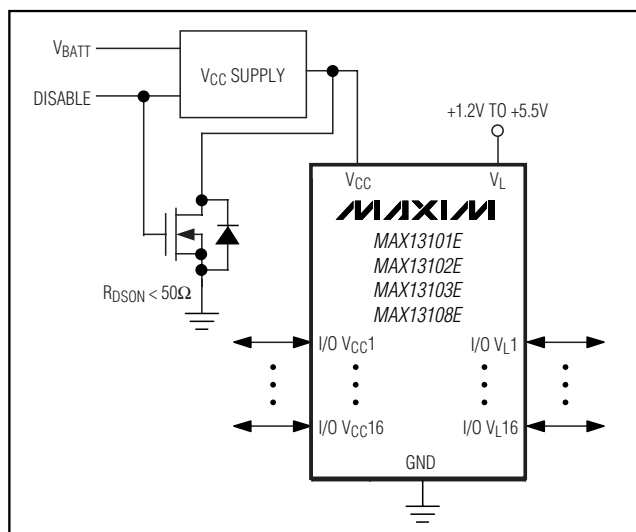


Figure 5. Recommended Circuit for Powering Down  $V_{CC}$

the bidirectional nature, both input stages become active during the one-shot pulse. This can lead to some current feeding into the external source that is driving the translator. However, this behavior helps to speed up the transition on the driven side.

For proper full-speed operation, the output current of a device that drives the inputs of the MAX13101E/MAX13102E/MAX13103E/MAX13108E should meet the following requirement:

$$i > 10^8 \times V \times (C + 10\text{pF})$$

where,  $i$  is the driver output current,  $V$  is the logic-supply voltage (i.e.,  $V_L$  or  $V_{CC}$ ) and  $C$  is the parasitic capacitance of the signal line.

## Enable Output Mode (EN)

The MAX13101E/MAX13102E/MAX13103E feature an enable input (EN) that, when driven low, places the device into shutdown mode. During shutdown, the MAX13101E I/O  $V_{CC\_}$  ports are pulled down to ground with internal  $6\text{k}\Omega$  resistors and the I/O  $V_{L\_}$  ports enter tri-state. MAX13102E I/O  $V_{CC\_}$  lines enter tri-state and the I/O  $V_{L\_}$  lines are pulled down to ground with internal  $6\text{k}\Omega$  resistors. All I/O  $V_{CC\_}$  and I/O  $V_{L\_}$  lines on the MAX13103E enter tri-state while the device is in shutdown mode. During shutdown, the  $V_{CC}$  supply current reduces to less than  $1\mu\text{A}$ , and the  $V_L$  supply current reduces to less than  $2\mu\text{A}$ . To guarantee minimum shutdown supply current, all I/O  $V_{L\_}$  need to be driven to GND or  $V_L$ , or pulled to GND or  $V_L$  through  $100\text{k}\Omega$  resistors. All I/O  $V_{CC\_}$  need to be driven to GND or  $V_{CC}$ , or pulled to GND or  $V_{CC}$  through  $100\text{k}\Omega$  resistors. Drive EN to logic-high ( $V_L$  or  $V_{CC}$ ) for normal operation.

MAX13101E/MAX13102E/MAX13103E/MAX13108E

# 16-Channel Buffered CMOS Logic-Level Translators

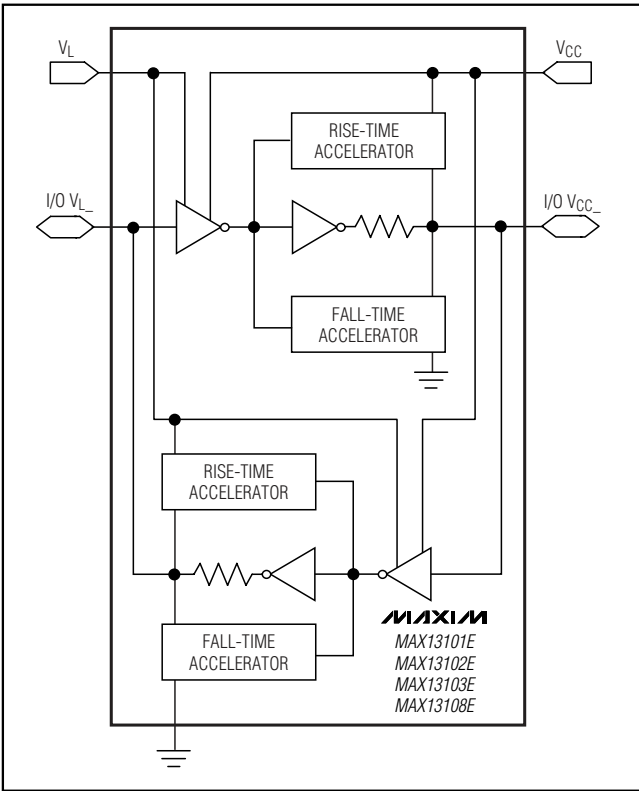


Figure 6. Simplified Diagram (1 I/O Line)

### Multiplexing Input (MULT)

The MAX13108E features a multiplexing input (MULT) that enables 8 of the 16 channels and places the remaining 8 into tri-state. Figure 7 depicts a typical multiplexing configuration using the MAX13108E. Drive MULT high to enable I/O V<sub>CC</sub>1 through I/O V<sub>CC</sub>8 and I/O V<sub>L</sub>1 through I/O V<sub>L</sub>8. Driving MULT high sets I/O V<sub>CC</sub>9 through I/O V<sub>CC</sub>16 and I/O V<sub>L</sub>9 through I/O V<sub>L</sub>16 into tri-state. Drive MULT low to enable I/O V<sub>CC</sub>9 through I/O V<sub>CC</sub>16 and I/O V<sub>L</sub>9 through I/O V<sub>L</sub>16. Driving MULT low sets I/O V<sub>CC</sub>1 through I/O V<sub>CC</sub>8 and I/O V<sub>L</sub>1 through I/O V<sub>L</sub>8 into tri-state.

### ±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The I/O V<sub>CC</sub>\_ lines have extra protection against static discharge. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, tri-state output mode, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing products can latch and must be powered down to remove the latchup condition.

ESD protection can be tested in various ways. The I/O V<sub>CC</sub>\_ lines of the MAX13101E/ MAX13102E/ MAX13103E/MAX13108E are characterized for protection to ±15kV using the Human Body Model.

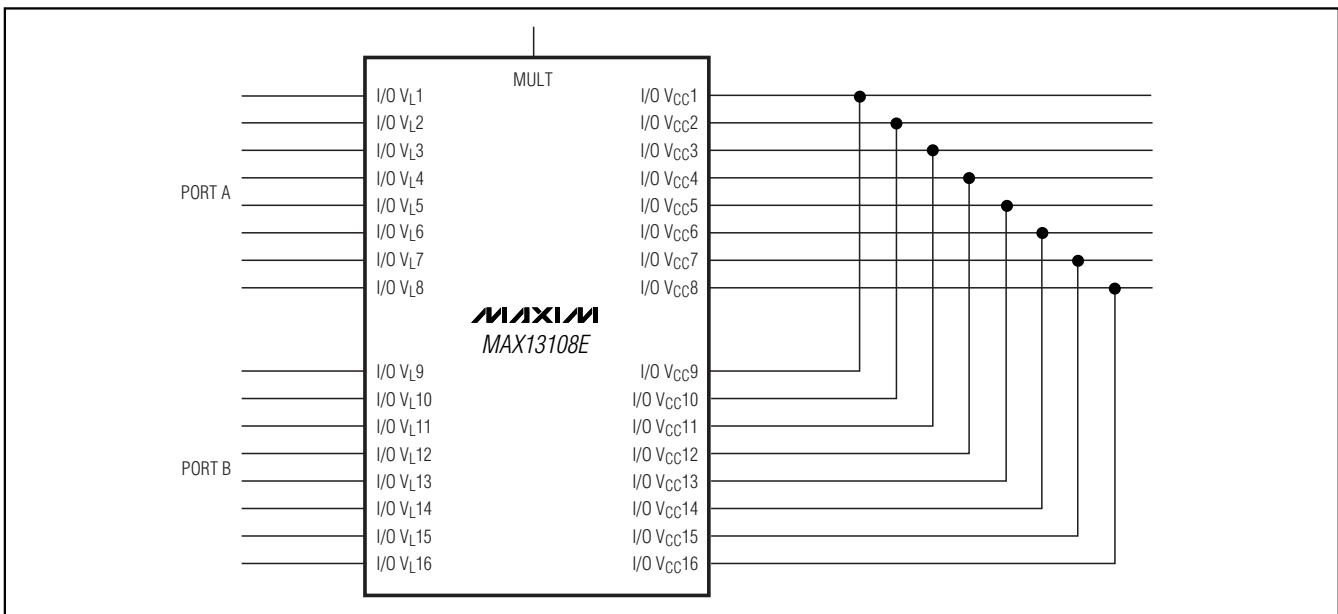


Figure 7. MAX13108E Multiplexing Configuration

# 16-Channel Buffered CMOS Logic-Level Translators

MAX13101E/MAX13102E/MAX13103E/MAX13108E

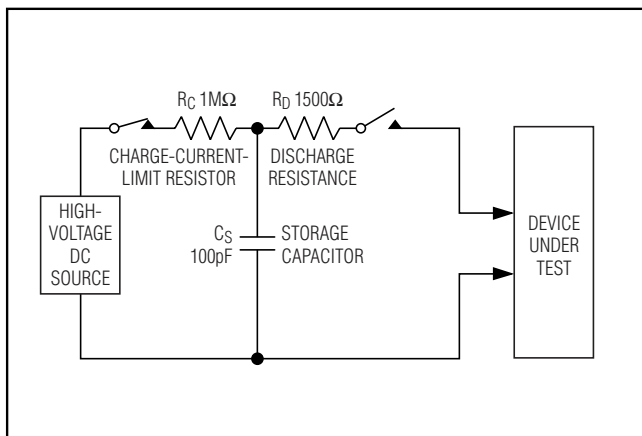


Figure 8a. Human Body ESD Test Model

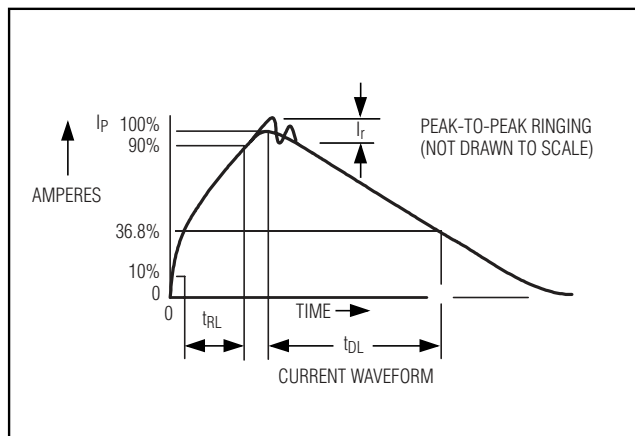


Figure 8b. Human Body Model Current Waveform

## ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

## Human Body Model

Figure 8a shows the Human Body Model and Figure 8b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

## Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. All pins require this protection during manufacturing, not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

## Applications Information

### Power-Supply Decoupling

To reduce ripple and the chance of transmitting incorrect data, bypass  $V_L$  and  $V_{CC}$  to ground with 0.1μF capacitors. To ensure full ±15kV ESD protection, bypass  $V_{CC}$  to ground with a 1μF ceramic capacitor. Place all capacitors as close to the power-supply inputs as possible.

### Capacitive Loading

Capacitive loading on the I/O lines impacts the rise time (and fall time) of the MAX13101E/MAX13102E/MAX13103E/MAX13108E when driving the signal lines. The actual rise time is a function of the parasitic capacitance, the supply voltage, and the drive impedance of the MAX13101E/MAX13102E/MAX13103E/MAX13108E. For proper operation, the signal must reach the  $V_{OH}$  as required before the rise-time accelerators turn off.

# 16-Channel Buffered CMOS Logic-Level Translators

## Ordering Information/Selector Guide (continued)

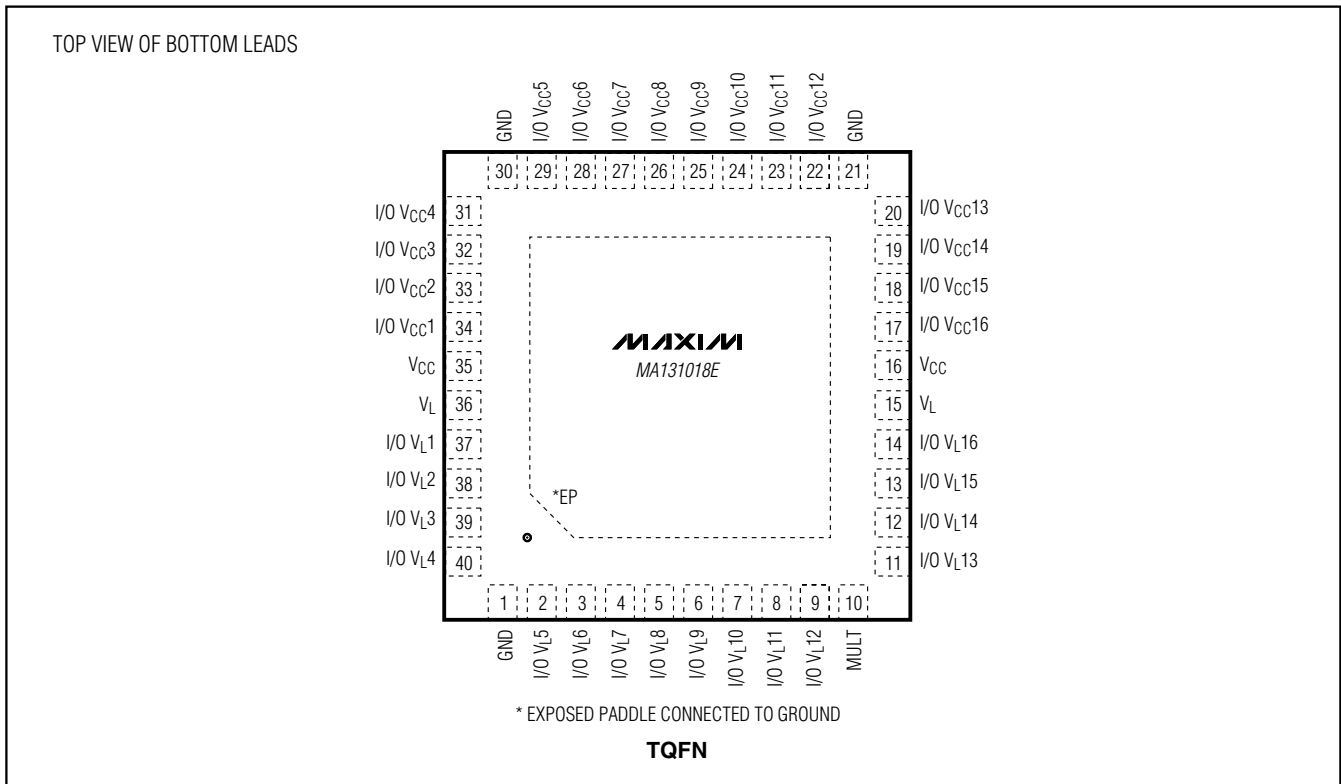
PART	PIN-PACKAGE	DATA RATE (Mbps)	I/O V <sub>L</sub> STATE DURING SHUTDOWN	I/O V <sub>CC</sub> STATE DURING SHUTDOWN	MULTIPLEXER FEATURE	PKG CODE
MAX13102EEBX*	36 UCSP** 3.06mm x 3.06mm	20	6kΩ to GND	High impedance	No	B36-1
MAX13102EETL	40 TQFN 5mm x 5mm x 0.8mm	20	6kΩ to GND	High impedance	No	T4055-1
MAX13103EEBX*	36 UCSP** 3.06mm x 3.06mm	20	High impedance	High impedance	No	B36-1
MAX13103EETL	40 TQFN 5mm x 5mm x 0.8mm	20	High impedance	High impedance	No	T4055-1
MAX13108EEBX*	36 UCSP** 3.06mm x 3.06mm	20	High impedance	High impedance	Yes	B36-1
MAX13108EETL	40 TQFN 5mm x 5mm x 0.8mm	20	High impedance	High impedance	Yes	T4055-1

**Note:** All devices operate over the -40°C to +85°C operating temperature range.

\*Future Product—contact factory for availability.

\*\*UCSP bumps are in a 6 x 6 array.

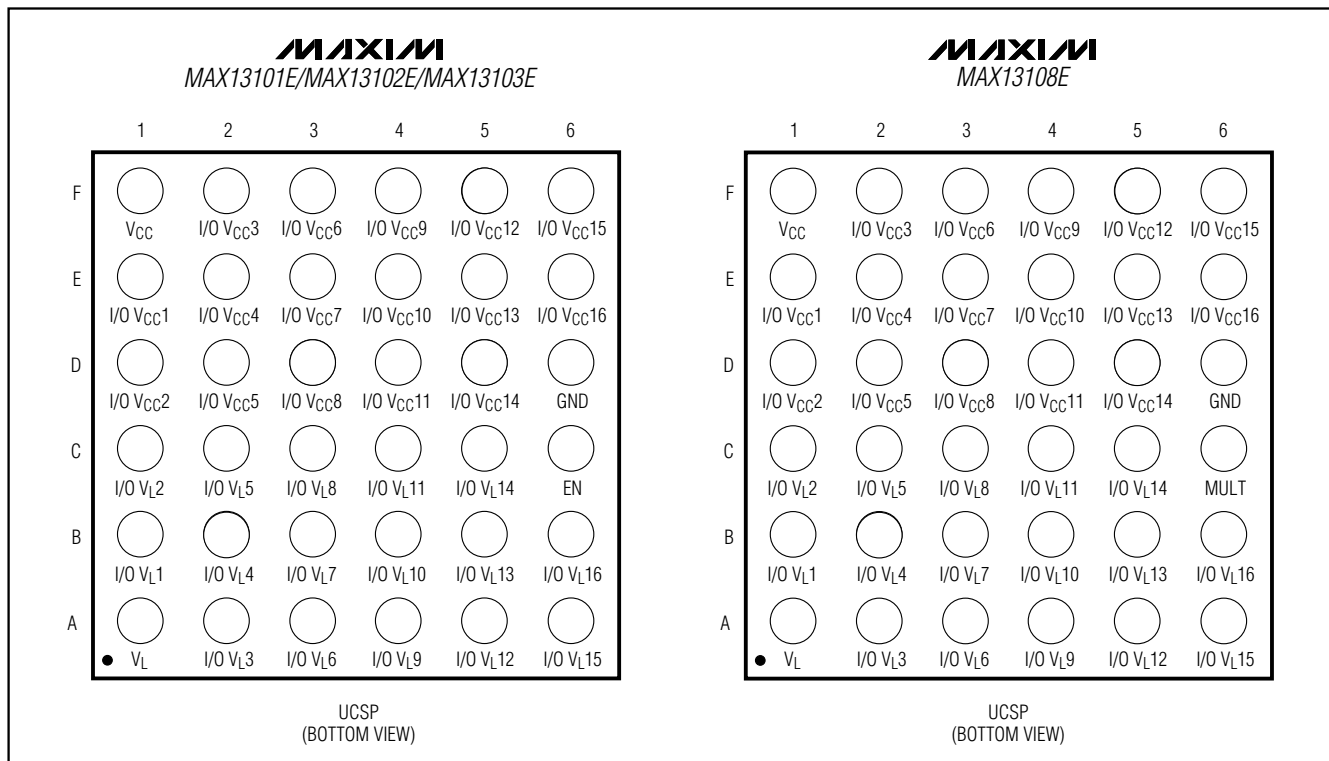
## Pin Configurations (continued)





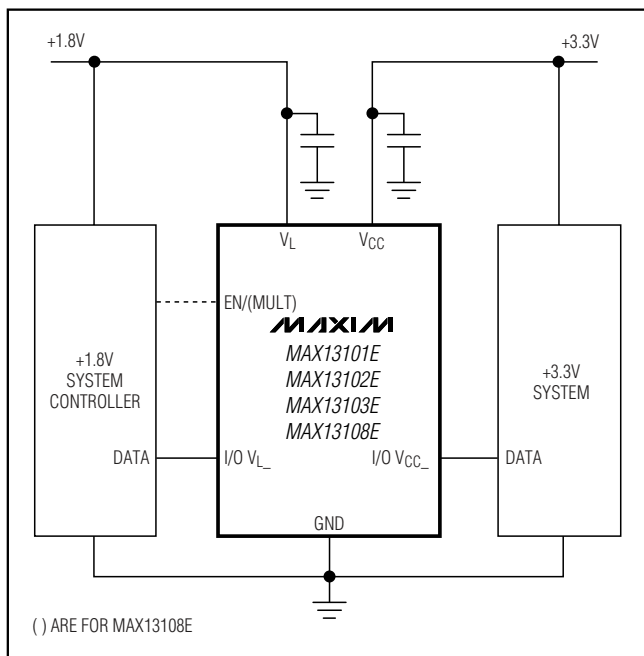
# 16-Channel Buffered CMOS Logic-Level Translators

## Pin Configurations (continued)



### Typical Operating Circuit

### Chip Information



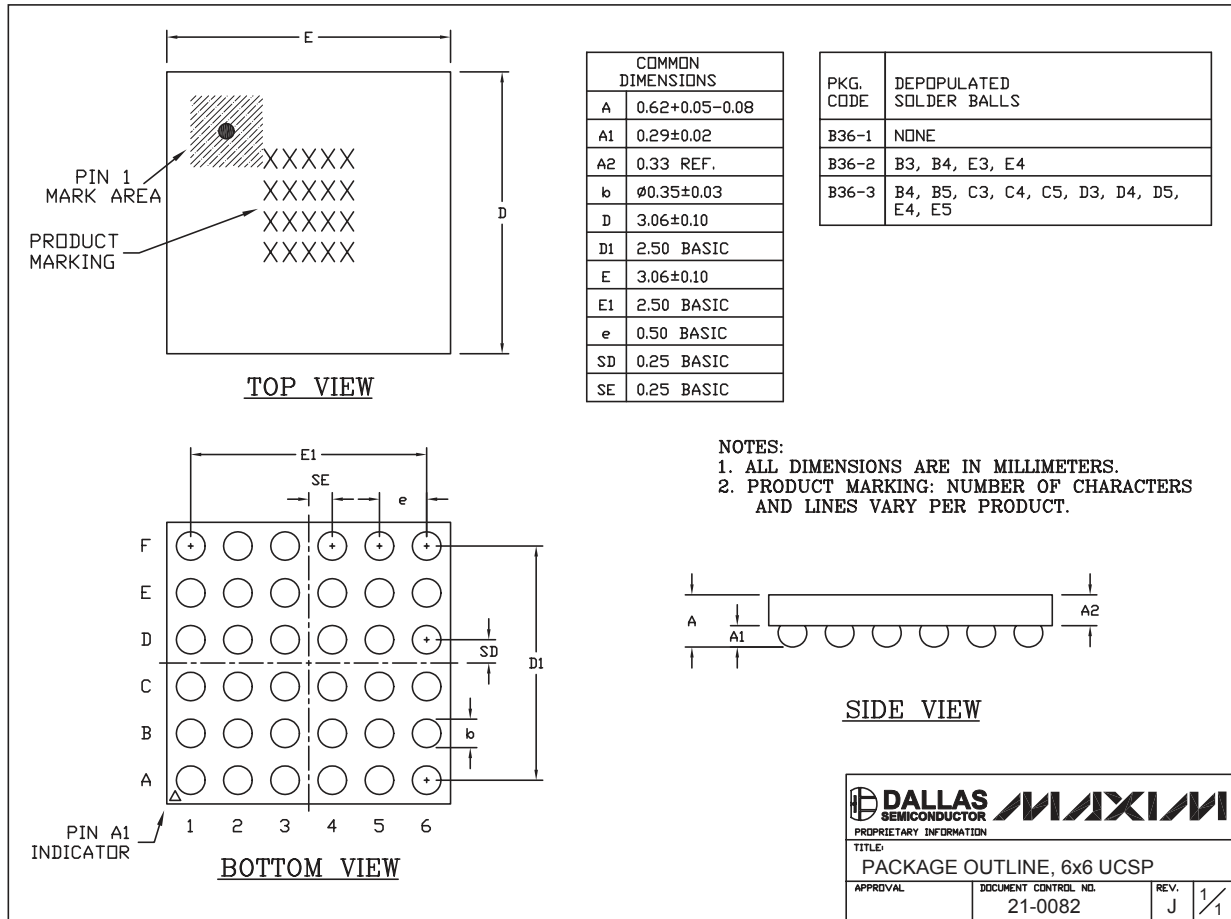
PROCESS: BICMOS

MAX13101E/MAX13102E/MAX13103E/MAX13108E

# 16-Channel Buffered CMOS Logic-Level Translators

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



36L UCSP.EPS

**DALLAS SEMICONDUCTOR** **MAXIM**

PROPRIETARY INFORMATION

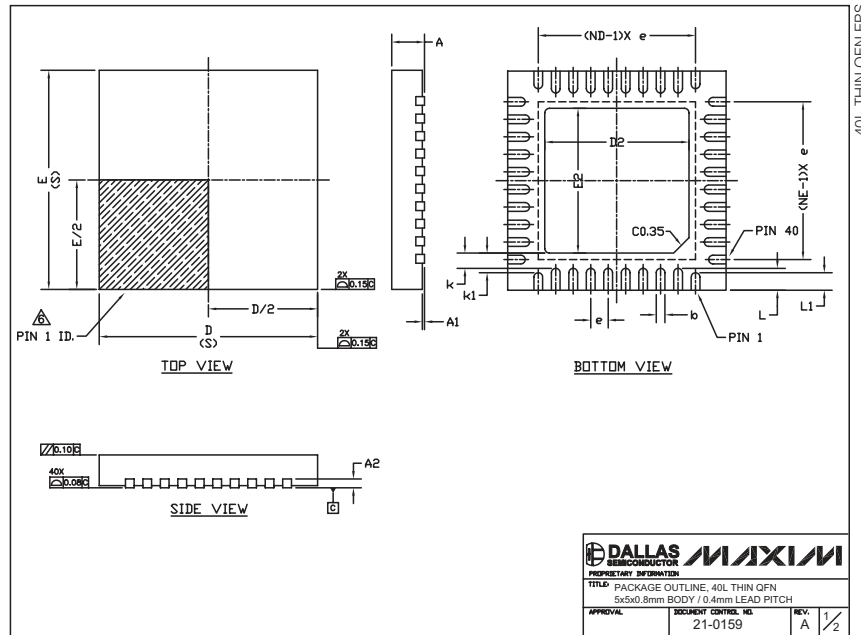
TITLE:  
 PACKAGE OUTLINE, 6x6 UCSP

APPROVAL	DOCUMENT CONTROL NO. 21-0082	REV. J	1/1
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# 16-Channel Buffered CMOS Logic-Level Translators

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



**NOTES:**

- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
- WARPAGE SHALL NOT EXCEED 0.10mm.
- PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTICS. (S)
- REFER TO JEDEC MO-220.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

SYMBOLS	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.700	0.750	0.800
A1	0.000	--	0.050
A2	0.200 REF.		
b	0.150	0.200	0.250
D	4.900	5.000	5.100
e	0.400 TYP.		
E	4.900	5.000	5.100
k	0.250	0.350	0.450
k1	0.350	0.450	0.550
L	0.400	0.500	0.600
L1	0.300	0.400	0.500
N	40		
ND	10		
NE	10		

PKG. CODE	EXPOSED PAD VARIATIONS					
	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40

**DALLAS SEMICONDUCTOR MAXIM**  
 PROPRIETARY INFORMATION  
 TITLE: PACKAGE OUTLINE, 40L THIN QFN  
 5x5x0.8mm BODY / 0.4mm LEAD PITCH  
 APPROVAL: DOCUMENT CONTROL NO. 21-0159 REV. A 1/2

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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**MAX13101E/MAX13102E/MAX13103E/MAX13108E**

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## Ordering Information

Notes:

1. Other options and links for purchasing parts are listed at: <http://www.maxim-ic.com/sales>.
2. [Didn't Find What You Need?](#) Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
3. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See [Full Data Sheet](#) or [Part Naming Conventions](#).
4. \* Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

### Devices: 1-14 of 14

MAX13101E	Free Sample	Buy	Package: TYPE PINS FOOTPRINT DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
MAX13101EETL+T			THIN QFN;40 pin;26 mm Dwg: <a href="#">21-0140L</a> (PDF) Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: <a href="#">Lead Free Materials Analysis</a>
MAX13101EETL+			THIN QFN;40 pin;26 mm Dwg: <a href="#">21-0140L</a> (PDF) Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: <a href="#">Lead Free Materials Analysis</a>
MAX13101EETL			THIN QFN;40 pin;26 mm Dwg: <a href="#">21-0140L</a> (PDF) Use pkgcode/variation: T4055-1*	-40C to +85C	RoHS/Lead-Free: <a href="#">No Materials Analysis</a>
MAX13101EETL-T			THIN QFN;40 pin;26 mm Dwg: <a href="#">21-0140L</a> (PDF) Use pkgcode/variation: T4055-1*	-40C to +85C	RoHS/Lead-Free: <a href="#">No Materials Analysis</a>
MAX13102E	Free Sample	Buy	Package: TYPE PINS FOOTPRINT DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
MAX13102EETL+T			THIN QFN;40 pin;26 mm Dwg: <a href="#">21-0140L</a> (PDF) Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: <a href="#">Lead Free Materials Analysis</a>
MAX13102EETL+			THIN QFN;40 pin;26 mm Dwg: <a href="#">21-0140L</a> (PDF) Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: <a href="#">Lead Free Materials Analysis</a>
MAX13103E	Free Sample	Buy	Package: TYPE PINS FOOTPRINT DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
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MAX13108EETL+T			THIN QFN;40 pin;26 mm Dwg: <a href="#">21-0140L (PDF)</a> Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: <a href="#">Lead Free Materials Analysis</a>
MAX13108EETL-T			THIN QFN;40 pin;26 mm Dwg: <a href="#">21-0140L (PDF)</a> Use pkgcode/variation: T4055-1*	-40C to +85C	RoHS/Lead-Free: <a href="#">No Materials Analysis</a>
MAX13108EETL			THIN QFN;40 pin;26 mm Dwg: <a href="#">21-0140L (PDF)</a> Use pkgcode/variation: T4055-1*	-40C to +85C	RoHS/Lead-Free: <a href="#">No Materials Analysis</a>

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